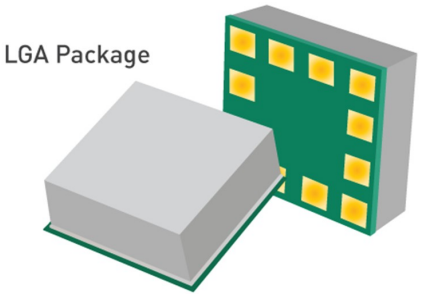
mEZDPD3603AS-84DE

mEZ20A-24Vin-3.3Vout-3A

DESCRIPTION

This device is a fully integrated power module that offers ultra-low EMI, in an LGA (15mmx15mmx6mm) metal can. This device meets EN55022 Class-B emissions standards, and integrates internal high-side and low-side power MOSFETs along with an integrated inductor. This device offers a compact solution with minimal external components needed.



SPECIFICATION OVERVIEW

I_{OUT}	3A
V_{OUT}	3.3V
Typical V_{IN}	24V
V_{IN} Min	20V
V_{IN} Max	28V

FEATURES

- Power Good and Enable
- Over Temperature Protection (OTP), Short-Circuit Protection
- High Efficiency
- Available in a LGA (15mmx15mmx6mm) Package

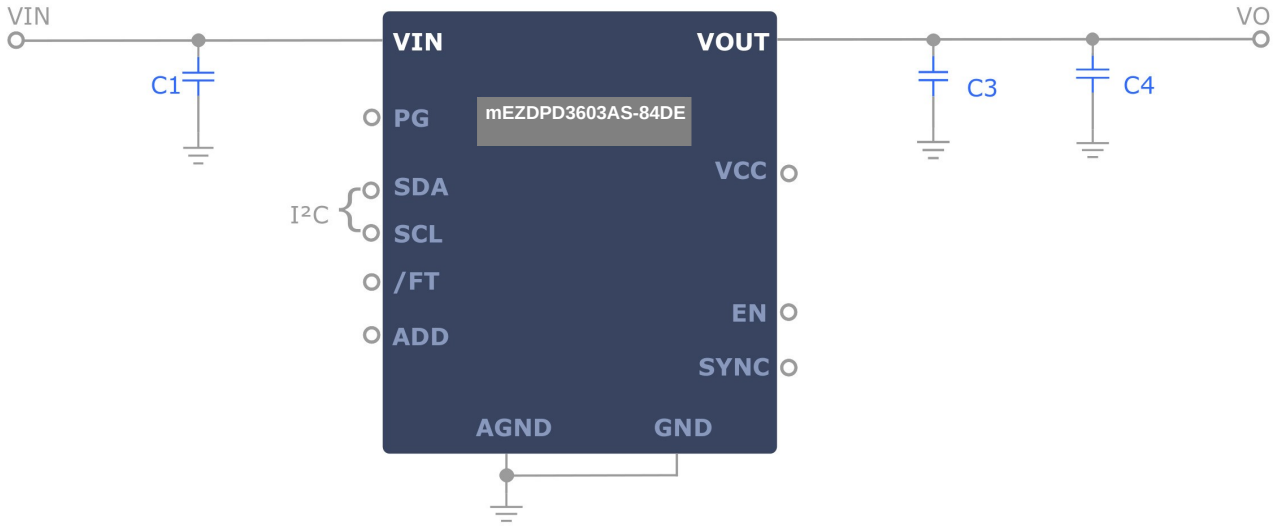
EFFICIENCY



Vin = 24V, Vout = 3.3V, Iout = 3A

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
©2019 MPS. All Rights Reserved.

TYPICAL APPLICATION



BOM

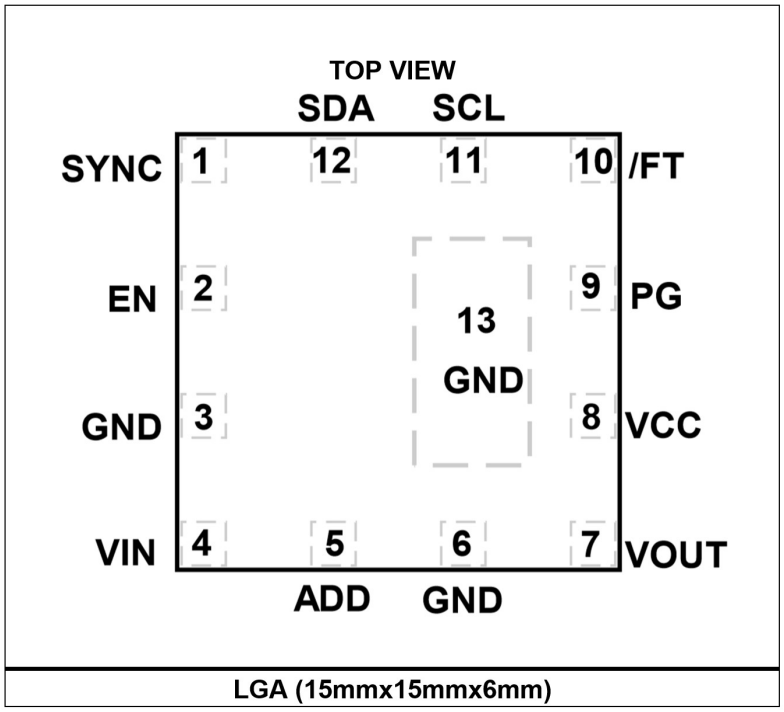
Reference	Quantity	Value	Description	Package	Manufacturer	Part Number
C1		NS	NS			
C3	2	10uF	Cap,Ceramic,10V,X5R(material)	'1206'	MuRata	GRM31CR61A106K
C4		NS	NS			
U1	1	-	Programmable 36V DC/DC Power module supply up to 3A	'LGA (15x15x6mm)'	MPS	mEZDPD3603AS

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
©2019 MPS. All Rights Reserved.

ORDERING INFORMATION

Part Number	Finalize Design to Order
mEZDPD3603AS-84DE	https://www.monolithicpower.com/mezdpd3603as.html

PACKAGE REFERENCE



LGA (15mmx15mmx6mm)

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
©2019 MPS. All Rights Reserved.

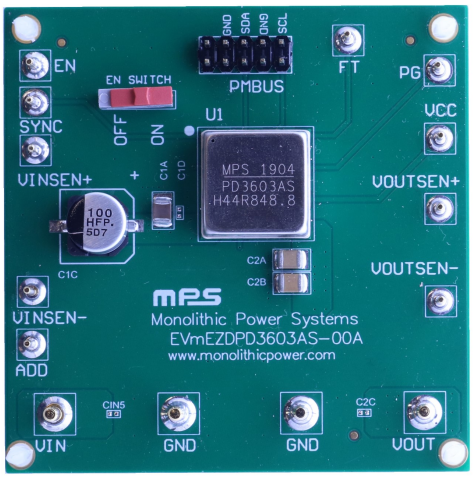
OTHER ORDERING OPTIONS

Evaluation Board for Surface Mount Device

The evaluation board is designed to demonstrate the capabilities of your custom MPS mEZDPD3603AS-84DE.

The EVB device is programmed with custom configuration.

Part Number
EVmEZDPD3603AS-00A

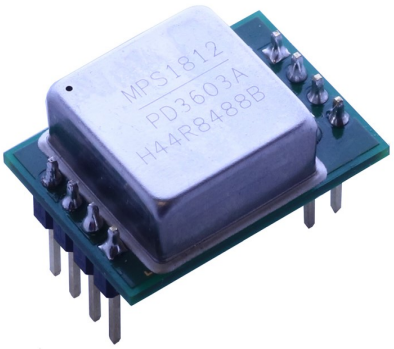


DIP Mount (Pin Out Version)

The mEZDPD3603AS-84DE is your custom device on a DIP mount for an easy-to-use, plug-and-play form factor.

The pin out module device is programmed with custom configuration.

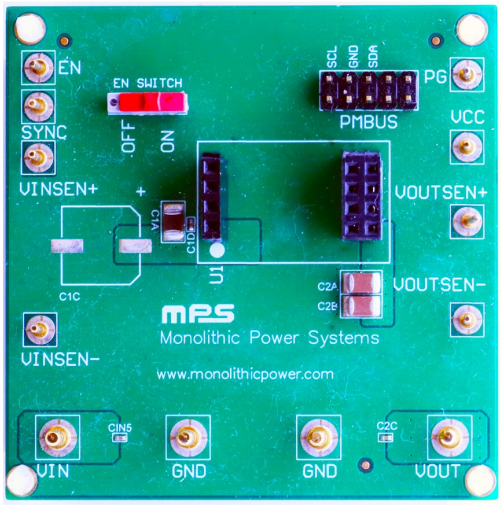
Part Number
mEZDPD3603A



Socket Evaluation Board for DIP Mount

DIP Mount Socket Only. For easy evaluation of pin out module.

Part Number
EVmEZDPD3603A-00A



All EVB schematic and layout files can be found at:
https://www.monolithicpower.com/mezdpd3603as.html

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
©2019 MPS. All Rights Reserved.

PIN FUNCTIONS

Pin #	Name	Description
1	SYNC	**Synchronize.** Input, clock synchronization.
2	EN	**Enable.** Input, drive EN high to turn on the device.
3	GND	**Power ground.** Power ground.
4	VIN	**Input voltage.** Input, supply voltage.
5	ADD	**Address setting.** Address setting for I²C.
6	GND	**Power ground.** Power ground.
7	VOUT	**Output voltage.** Sense input of output voltage.
8	VCC	**Internal LDO output.** Output, internal 5V LDO regulator output.
9	PG	**Power good.** Output, power good indicator.
10	/FT	**Fault indicator.** Output, fault indicator.
11	SCL	**I²C serial clock.** Communication bus, I²C serial clock.
12	SDA	**I²C serial data.** Communication bus, I²C serial data.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
©2019 MPS. All Rights Reserved.

ABSOLUTE MAXIMUM RATINGS (1)

V_{IN} ..... -0.3V to +48V
V_{SW}.....-0.3V to V_{IN}+0.3V
V_{EN} ..... -0.3V to +48V
All other pins ..... -0.3V to +5.5V
Continuous power dissipation (T_A = 25°C) (2)
Junction temperature ..... 150°C
Lead temperature..... 260°C
Storage temperature .....-65°C to +150°C

Recommended Operating Conditions

Operating junction temp (T_J) ....-40°C to +125°C

Thermal Resistance (3)	***θ_{JA}***	***θ_{JC}***
LGA (15mmx15mmx4mm)	TBD	TBD °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) Measured on JESD51-7, 4-layer PCB.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
©2019 MPS. All Rights Reserved.

PROGRAMMABLE ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Condition	Min	Typ	Max	Units
AAM peak current threshold		Programmed value		530		mA
Compensation, R_{COMP}	R_{COMP}	Programmed value		800		kΩ
Compensation, R_T	R_T	Programmed value		0		kΩ
Compensation, C_{COMP1}	C_{COMP1}	Programmed value		45		pF
Slope compensation	Vpp	Programmed value		0.3		V
V_{OUT} set	V_{OUT}	Programmed value		3.3		V
Switching frequency	f_{SW}	Programmed value		800		kHz
Switching slew rate (rising) (5)		Programmed value		4		V/ns
Switching slew rate (falling) (5)		Programmed value		4		V/ns
Frequency dithering cycle		Programmed value		150		μs
Frequency dithering amplitude		Programmed value, as proportion of f_{SW}		3/28		
V_{IN} UVLO rising threshold	$INUV_{Vth}$	Programmed value		3.3		V
V_{IN} UVLO hysteresis	$INUV_{HYS}$	Programmed value		4		mV
EN rising threshold	V_{EN}	Programmed value		1.2		V
EN rising hysteresis	V_{EN_HYS}	Programmed value		200		mV
Soft-start time	t_{SS}	Programmed value		1		ms
PG upper rising threshold		Programmed value, as % of V_{OUT} set		110		%
PG upper hysteresis		Programmed value, as % of V_{OUT} set		5		%
PG lower rising threshold		Programmed value, as % of V_{OUT} set		90		%
PG lower hysteresis		Programmed value, as % of V_{OUT} set		5		%
Valley current limit threshold	I_{VALLEY_LIMIT}	Programmed value		4		A
Peak current limit threshold	I_{PEAK_LIMIT}	Programmed value		5		A
SCP triggered FB voltage		Programmed value, as % of V_{OUT} set		50		%
SCP detecting time		Programmed value, as proportion of t_{SW}		128		
Hiccup duty (on time)		Programmed value		10		%
Output OVP rising threshold	$V_{OUT_OVP_TH}$	Programmed value, as % of V_{OUT} set		120		%
Output OVP hysteresis	$V_{OUT_OVP_HYS}$	Programmed value, as % of V_{OUT} set		5		%
Thermal shutdown (5)	T_{SD}	Programmed value. Over-temperature protection threshold		175		°C
Thermal shutdown hysteresis (5)	T_{SD_SYS}	Programmed value. Over-temperature protection hysteresis		25		°C
Input OVP rising threshold	$V_{IN_OVP_TH}$	Programmed value		No		V
Input OVP hysteresis	$V_{IN_OVP_HYS}$	Programmed value, as % of input OVP threshold set		5		%

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
©2019 MPS. All Rights Reserved.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, V_{EN} = 2V, T_A= -40°C to +125°C, typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
V_{IN} quiescent current	I_Q	V_{OUT} = 5V V_{FB}>V_{REF} with BIAS power, no load		600	1000	μA
	I_Q	V_{OUT} = 5V V_{FB}>V_{REF} with BIAS power, no load (6)		11		μA
V_{IN} shutdown current	I_{SD}	V_{EN} = 0V, T_J =25°C			1	μA
Sync frequency range	f_{SYNC}	Sync clock set range	250		2500	kHz
Sync voltage high threshold	V_{SYNC_HIGH}			1.4	2	V
Sync voltage low threshold	V_{SYNC_LOW}		0.4	1.1		V
Minimum on time (5)	t_{ON_MIN}	With peak current mode		80		ns
Minimum off time (5)	t_{OFF_MIN}			380		ns
HS switch on resistance	R_{DSON_H}	V_{BST} - V_{SW} = 5V		95	180	mΩ
LS switch on resistance	R_{DSON_L}			50	100	mΩ
Integrated inductor inductance	L_1			10		μH
Inductor DC resistance	L_{1_DCR}			61.5	70	mΩ
PG output voltage low	V_{PG_SINK}	I_{SINK} = 1mA		0.1	0.3	V
PG deglitch timer	T_{PG_DELAY}			30		μs
VCC regulator	V_{CC}	I_{CC} = 0mA, with V_{CC} LDO powered by V_{IN}	4.8	5	5.2	V
Input OVP threshold accuracy		I^2C set 36V	32	34	36	V

Note:

5) Not tested in production. Guaranteed by design and characterization.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
©2019 MPS. All Rights Reserved.

PROGRAMMABLE OPERATION SETTINGS

Parameter	Selected	Description	Note
Light Load Mode			
AAM/forced CCM	0	0: AAM 1: Forced CCM	
Switching			
Frequency dithering enable	0	0: Disable 1: Enable	
Protection			
SCP mode	0	0: Hiccup 1: Latch 2: Switching and Non-hiccup	
Output OVP mode	1	0: Discharge 1: Stop switching 2: Latch	
FT setting	1	Fault flag 0: Latch 1: Auto-reset	

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
©2019 MPS. All Rights Reserved.

I²C PORT SIGNAL CHARACTERISTICS

V_{IN} = 12V, V_{EN} = 2V, T_A = -40°C to +125°C, typical values tested at T_J = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
I²C Interface Specifications						
Input logic low	V_{IL}		0		0.4	V
Input logic high	V_{IH}		1.3			V
Output logic low	V_{OL}	I_{LOAD} = 3mA			0.4	V
SCL clock frequency	f_{SCL}				400	kHz
SCL high time	t_{HIGH}		0.6			µs
SCL low time	t_{LOW}		1.3			µs
Data set-up time	$t_{SU,DAT}$		100			ns
Data hold time	$t_{HD,DAT}$		0		0.9	µs
Set-up time for repeated start	$t_{SU,STA}$		0.6			µs
Hold time for start	$t_{HD,STA}$		0.6			µs
Bus free time between a start and a stop condition	t_{BUF}		1.3			µs
Set-up time for stop condition	$t_{SU,STO}$		0.6			µs
Rise time of SCL and SDA	t_R		20 + 0.1 × C_B		120	ns
Fall time of SCL and SDA	t_F		20 + 0.1 × C_B		120	ns
Pulse width of suppressed spike	t_{SP}		0		50	ns
Capacitance bus for each bus line	C_B				400	pF

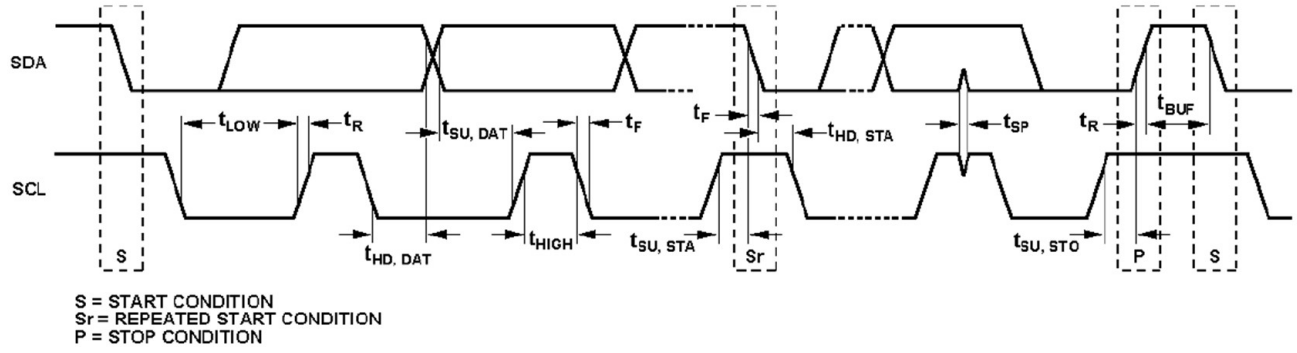


Figure 1: I²C-Compatible Interface Timing Diagram

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
©2019 MPS. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS

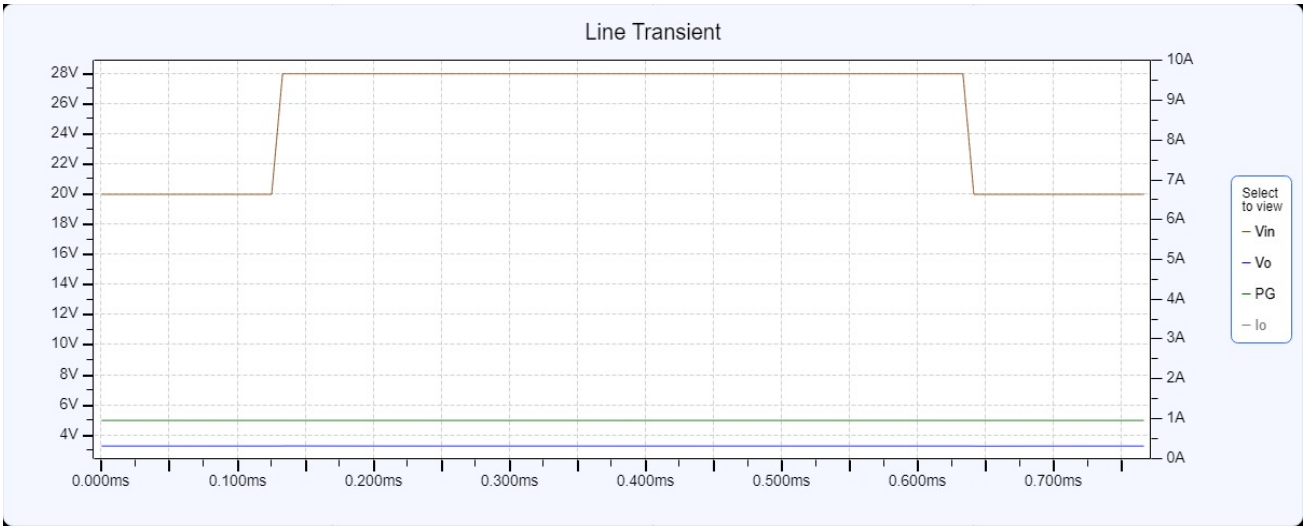
All waveforms simulated.

EFFICIENCY



Vin = 24V, Vout = 3.3V, Iout = 3A

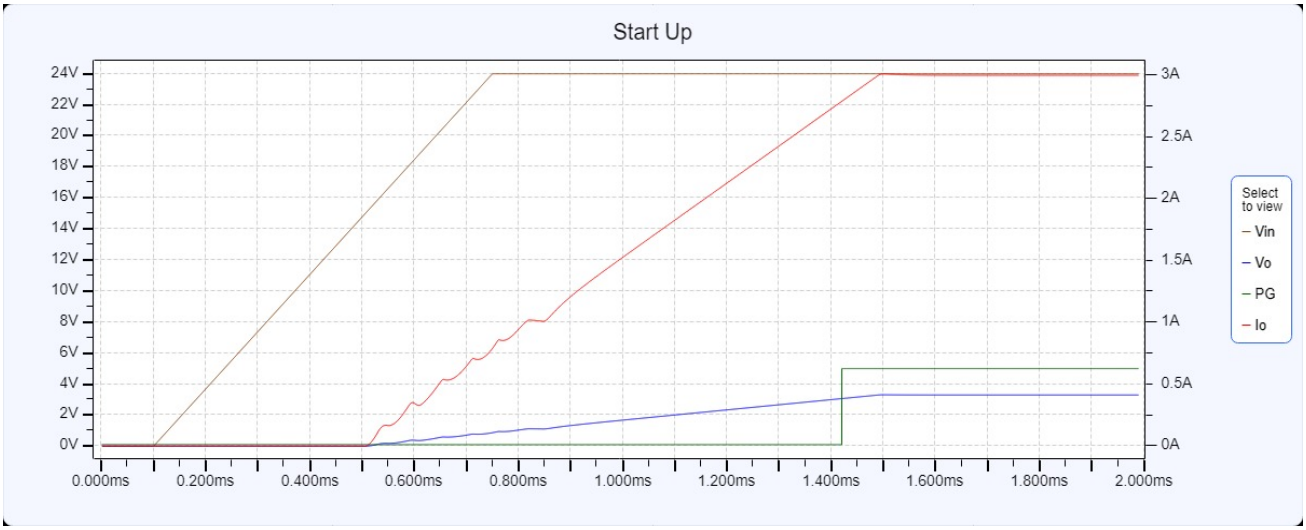
LINE TRANSIENT



Vlow= 20A, Vhigh= 28A, Iout= 3A, Slew rate= 1V/µs

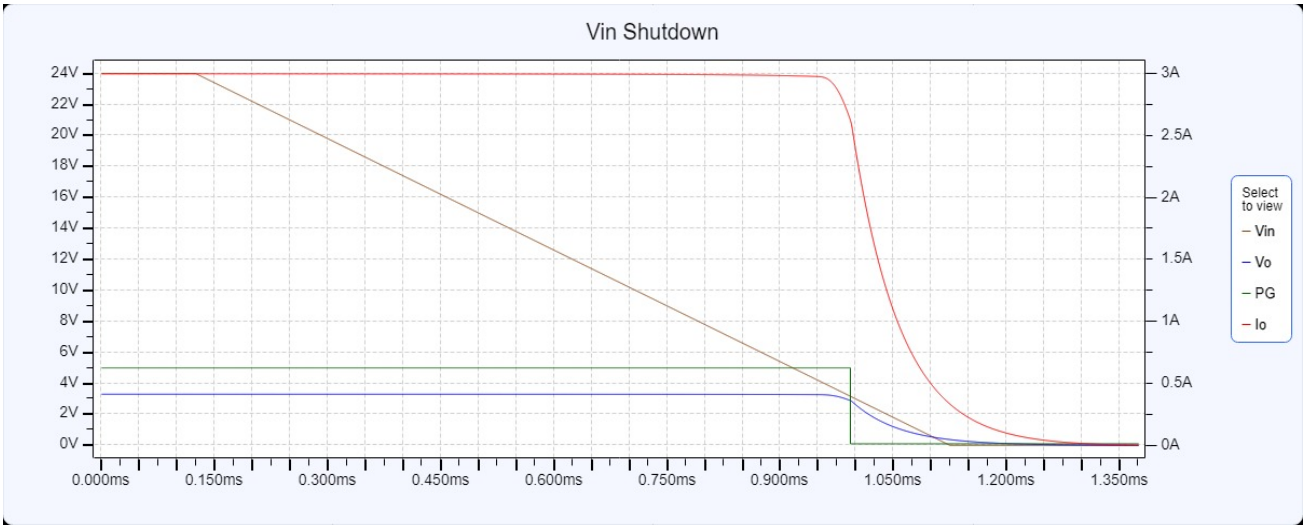
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
©2019 MPS. All Rights Reserved.

START UP



Vin = 24V, Iout = 3A

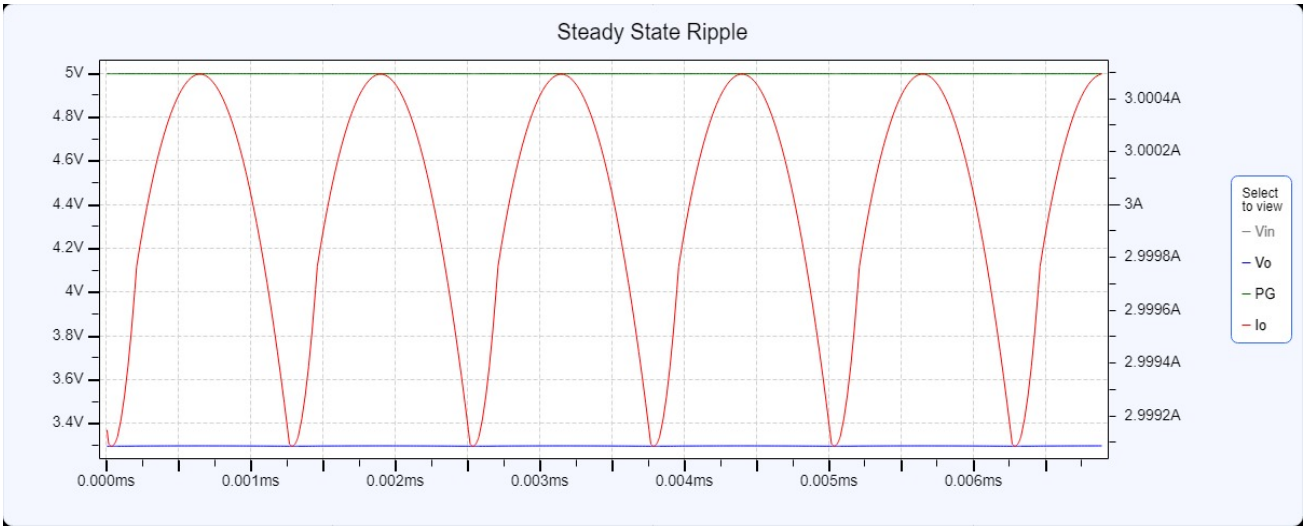
VIN SHUTDOWN



Vin = 24V, Iout = 3A

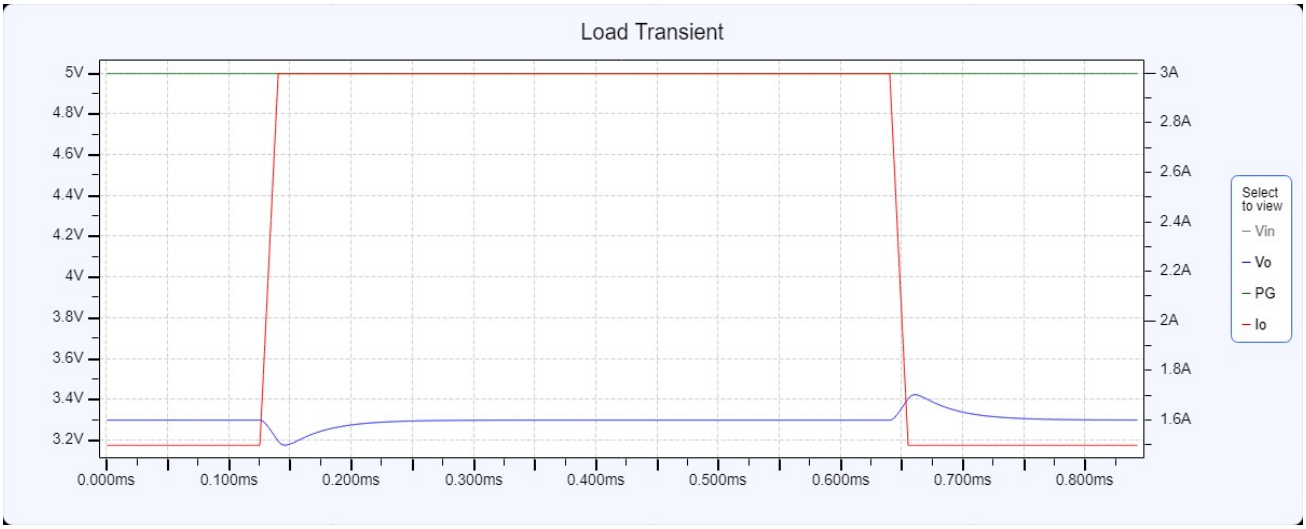
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
©2019 MPS. All Rights Reserved.

STEADY STATE RIPPLE



Vin = 24V, Iout = 3A

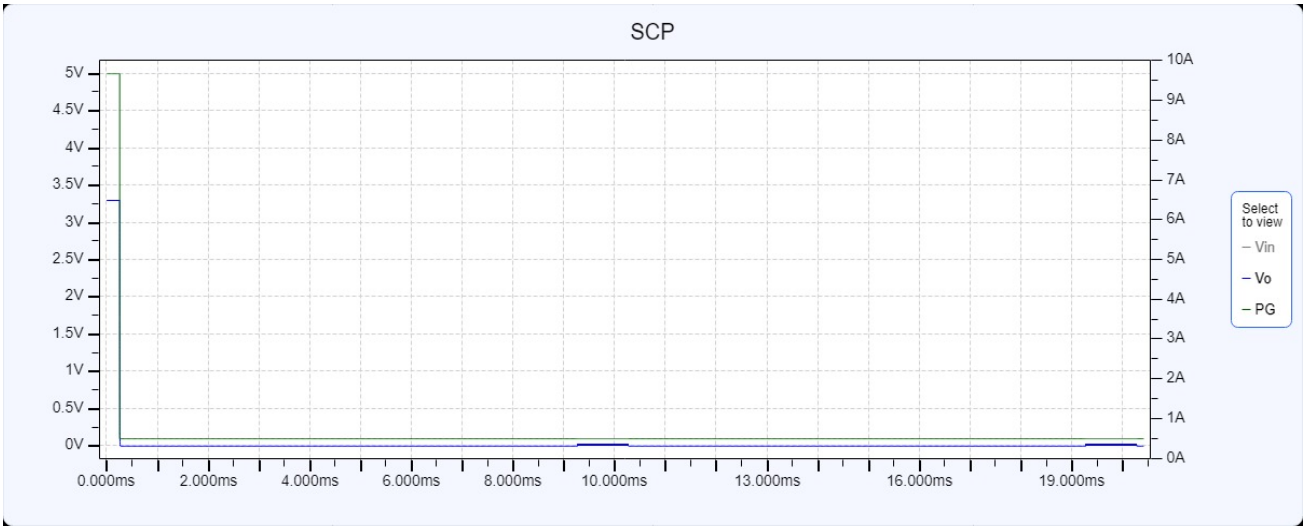
LOAD TRANSIENT



Vin = 24V, Ihigh = 3A, Ilow =1.5A, Slew rate = 0.1A/µs

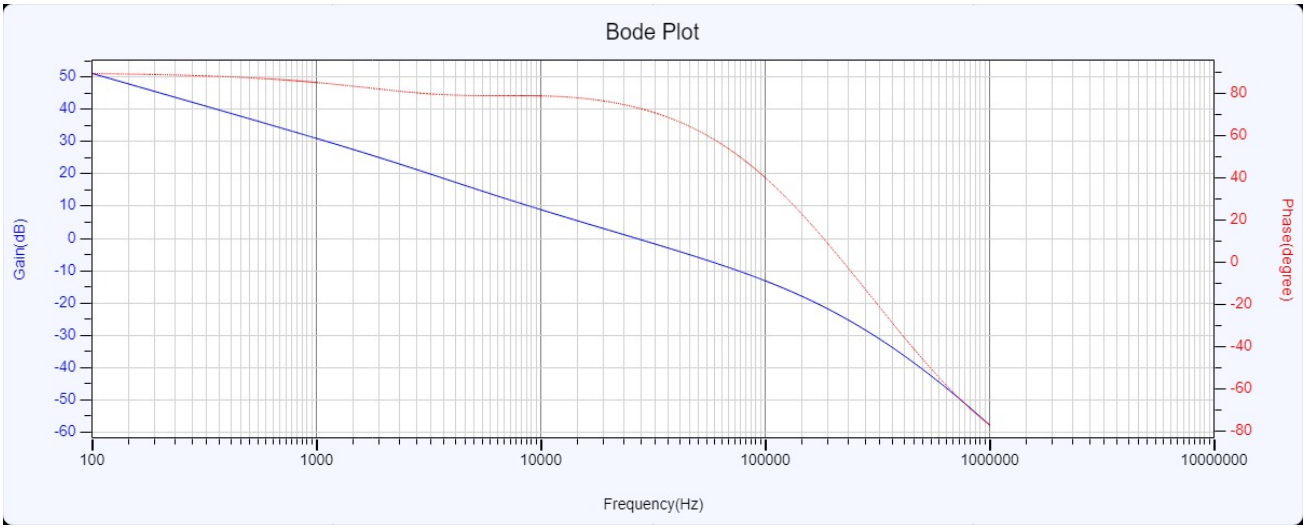
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
©2019 MPS. All Rights Reserved.

SCP



Vin = 24V

BODE PLOT



Bandwidth = 27kHz, Phase Margin = 73.22degree, Gain Margin = -24.16dB

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
©2019 MPS. All Rights Reserved.

FUNCTIONAL BLOCK DIAGRAM

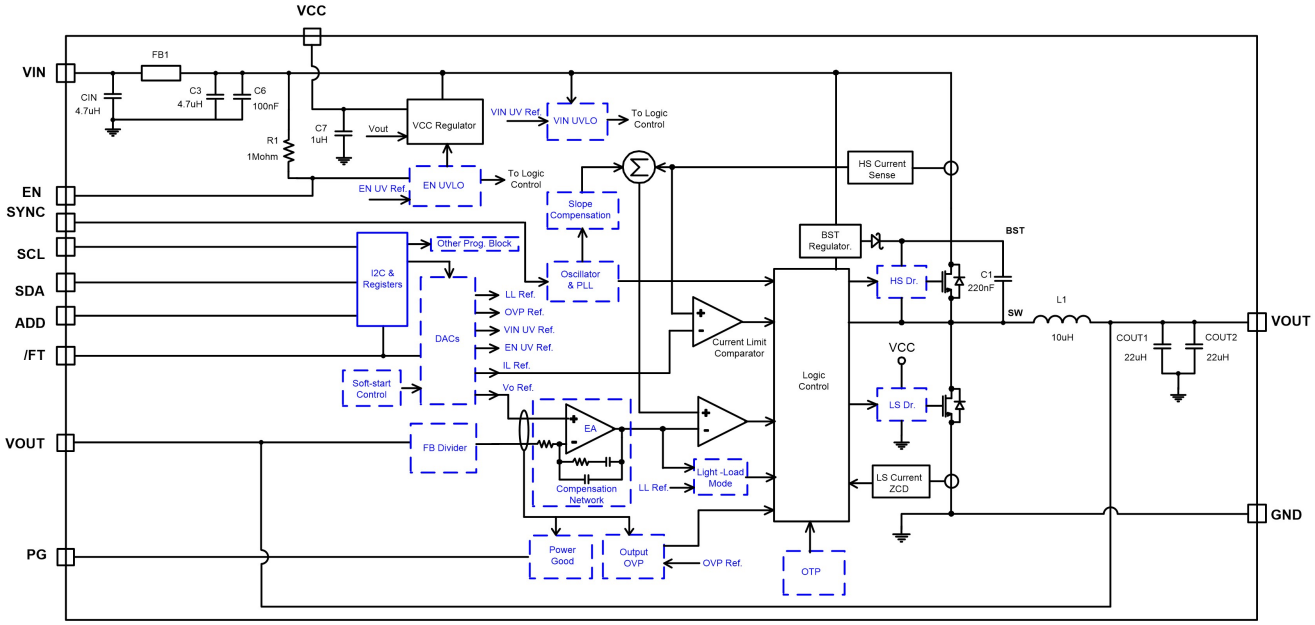


Figure 2: Functional Block Diagram

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
©2019 MPS. All Rights Reserved.

OPERATION

This device is a high-frequency, synchronous, step-down power supply. It is available with a wide 4.5V to 36V input supply range and can achieve up to 3A continuous output current with excellent load and line regulation over an ambient temperature range of -40°C to +125°C.

PWM Control

At moderate to high output currents, this device operates in a fixed-frequency, peak current control mode to regulate the output voltage. An internal clock initiates a PWM cycle. Then the rising edge of the clock the high-side switch (HS-FET) turns on and the inductor current rises linearly to provide energy to the load. The HS-FET remains on until its current reaches the COMP voltage, which is the output of the internal error amplifier. The output voltage of error amplifier depends on the difference of output feedback voltage and the internal high-precision reference. It determines how much energy should be transferred to the load. The higher the load current, the higher the COMP voltage will be. Both the feedback divider ratio and reference can be adjusted by the I^2C, which makes it easy to adjust for different output voltages.

When the HS-FET is off, the low-side switch (LS-FET) turns on immediately and remains on until the next clock starts. During this time, the inductor current flows through the LS-FET. In order to avoid shoot-through, dead time is inserted to avoid the HS-FET and LS-FET turning on at the same time.

If in one PWM period, the current in the HS-FET does not reach the COMP set current value, the HS-FET remains on, saving a turn-off operation.

Mode Selection (AAM and Forced CCM)

This device can operate in light load AAM or forced CCM mode. AAM (advanced asynchronous modulation) mode is employed to optimize the efficiency during light-load or no-load conditions. Forced CCM can maintain a constant switching frequency and smaller output ripple, but it has low efficiency at light load.

If AAM mode is enabled with load decreasing, the device enters discontinuous conduction operation (DCM) with fixed-frequency as long as the inductor current approaches zero. If the load is further decreased or there is no load that makes the inductor peak current below AAM peak current threshold set by the I^2C, the device enters sleep mode. In sleep mode, it consumes very low quiescent current to further improve light-load efficiency. The internal clock is also blocked, and the device skips some pulses. The feedback voltage is less than the reference, so V_{COMP} ramps up until the inductor peak current exceeds the AAM threshold. Then the internal clock is reset, and the crossover time is taken as the benchmark of the next clock. This control scheme helps achieve high efficiency by scaling down the frequency to reduce switching and gate driver losses.

As the output current increases from light load, V_{COMP} and the switching frequency increase. If the output current exceeds the critical level set by V_{COMP}, the device resumes fixed-frequency PWM control.

When forced CCM is enabled, the device operates in fixed-frequency peak current control mode to regulate the output voltage, regardless of the output current.

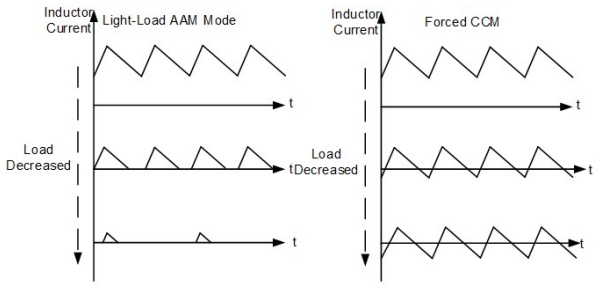


Figure 3: AAM and Forced CCM

Internal Regulator

A 5V internal regulator powers most of the internal circuitries. This regulator takes V_{IN} and operates in the full V_{IN} range. When V_{IN} exceeds 5.0V, the output of the regulator is in full regulation. Lower V_{IN} values result in lower output voltages. The regulator is enabled when V_{IN} exceeds its UVLO threshold and EN is high. In EN shutdown mode, the internal VCC regulator is disabled to reduce power dissipation.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
©2019 MPS. All Rights Reserved.

For better thermal performance, BIAS mode can be chosen via the I²C if V_{OUT} is greater than 5V. VCC and the internal circuit are then powered by V_{OUT}.

Enable Control

EN is a digital control pin that turns the regulator, including I²C block on and off. Drive EN high to turn on the regulator; drive it low to turn the regulator off. The EN threshold can be programmed by the I²C. An internal 5MΩ resistor from EN to GND allows EN to be floated to shut down the chip.

Oscillator Frequency

The default frequency of this device is 500kHz, and it can be programmed from 250kHz to 2.5MHz by the I²C. The frequency can also be set by a logic level synchronal signal.

SYNC IN and SYNC OUT

The SYNC pin can be programmed by the I²C to SYNC IN or SYNC OUT. When operating as SYNC IN, the internal oscillator frequency can be synchronized by an external clock via this pin. At start-up, the device first operates at the internal set frequency, and quickly synchronizes to the external clock once soft start is ready. Ensure the high amplitude of the SYNC clock is above 1.8V and the low amplitude is below 0.4V to drive the internal logic. The recommended external SYNC frequency is between 250kHz and 2.5MHz.

The device operates in forced CCM mode with a fixed frequency when there is a SYNC clock, regardless of the output current. A pulse longer than 200ns is recommended in application.

When the SYNC pin is set to SYNC OUT, the device can output the internal clock with a 0° or 180° phase shift. By this function, two devices can operate in same frequency but 180° out of phase to reduce the total input current ripple so that a smaller input bypass capacitor can be used.

Under-Voltage Lockout (UVLO)

The device has input under-voltage lockout protection (UVLO) to ensure reliable output power. Assuming EN is active, the device is powered on when the input voltage exceeds the UVLO rising threshold, and is powered off when the input voltage drops below the UVLO falling threshold. The UVLO threshold can be set between 3.3V and 7.5V the I²C. This function prevents the device from operating at an insufficient voltage. It is a non-latch protection.

Soft-Start

The device has built-in soft start (SS), which ramps up the output voltage in a controlled slew rate when the EN pin goes high, avoiding overshoot during start-up. When the chip starts, the internal circuitry generates a soft-start voltage that ramps up slowly. When the SS voltage (V_{SS}) is below the internal reference (V_{REF}), V_{SS} overrides V_{REF} as the error amplifier reference. When V_{SS} exceeds V_{REF}, V_{REF} acts as the reference. At this point, soft start finishes and the device enters steady state.

The SS time is internally set to default 1ms, and can also be set to 0.5ms, 2ms, or 4ms by the I²C. When the output voltage is shorted to GND, the feedback voltage is pulled low and V_{SS} is discharged. The part soft starts again when it returns to its normal state.

Pre-Bias Start-Up

For this device, at start-up, if the output feedback voltage is greater than V_{SS}, which means the output has pre-bias voltage, neither the HS-FET nor LS-FET turn on until V_{SS} exceeds the feedback voltage.

Power Good Indicator

This device has power good (PG) indication. The PG pin is the open drain of a MOSFET. It should be connected to a voltage source through a resistor (e.g. 100kΩ). In the presence of an input voltage, the MOSFET turns on so that the PG pin is pulled to GND before soft start is ready. When the output voltage is within default ±10% window of the rated voltage, the PG pin is pulled high after a delay (typically 30μs).

If V_{OUT} moves outside the default ±10% range with a hysteresis, the device pulls PG low to indicate a failure output status. Both the PG threshold and hysteresis can be programmed by the I²C.

FAULT Indicator

The /FT pin is also an open drain of a MOSFET. It should be connected to a voltage source through a resistor (e.g. 100kΩ). The /FT pin is

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
©2019 MPS. All Rights Reserved.

pulled high in normal operation, and any fault or warning pulls this pin low to indicate a fault status, including input OVP, output OVP, SCP, and thermal shutdown.

Over-Current Protection (OCP)

This device has cycle-by-cycle over-current limit control. The inductor current is monitored during the HS-FET on state. Once the inductor peak current exceeds the set current limit threshold, the HS-FET immediately turns off. Then the LS-FET turns on to discharge the energy, and the inductor current decreases. The HS-FET does not turn on again until the inductor current is below a certain current threshold, called the valley current limit. This prevents the inductor current from running away and possibly damaging the components. Both the peak current and valley current threshold can be programmed by the I²C.

When the peak current limit is triggered, the OCP timer starts immediately. The OCP timer can be set to 32, 64, 128, or 256 cycles by the I²C. Reaching the current limit during each cycle during this OCP timer triggers SCP operation (hiccup as default), which is introduced in the following section.

Short-Circuit Protection (SCP)

When a short circuit occurs, this device immediately reaches its current limit. Meanwhile, the output voltage quickly drops to its under-voltage threshold (default is 50% of the setting output). The device considers this an output dead short and directly triggers SCP operation. Three modes can be selected by the I²C for SCP operation: hiccup as default, switching with non-hiccup, and latch-off.

In default hiccup mode, this device disables its output power stage and resets the soft-start voltage, then initiates a soft start. The off time is determined by the soft-start time and hiccup duty, which can both be set by the I²C. If the short-circuit condition still remains after soft start ends, the device repeats this operation until the short circuit disappears and the output returns to the regulation level. This protection mode greatly reduces the average short-circuit current by periodically restarting the part to alleviate thermal issues and protect the regulator.

Output Over-Voltage Protection (V_{OUT} OVP)

This device monitors the output voltage through the VOUT pin to detect output over-voltage conditions. When the output voltage exceeds OVP threshold (the default is 120% of the setting voltage), OVP mode is triggered. Three modes can be selected by the I²C for OVP operation: disable as default, discharge, and latch-off.

Input Over-Voltage Protection (V_{IN} OVP)

This device also has optional input OVP. The threshold can be set to 28V, 34V, or 40V. If V_{IN} exceeds the threshold, the device stops switching. This is a non-latch protection, and there is a hysteresis of either 2.5% or 5% of the input OVP threshold voltage. The device resumes normal operation when the input OVP is removed. Both the input OVP threshold and hysteresis can be set by the I²C interface.

Thermal Shutdown

This device has over-temperature protection (OTP) by monitoring the IC temperature internally. This function prevents the chip from operating at exceedingly high temperatures. If the junction temperature exceeds the threshold (default 175°C), it shuts down the whole chip. This is a non-latch protection, and there is a default 25°C hysteresis. Once the junction temperature drops to about 150°C, the device resumes operation by initiating a soft start. Both the OTP threshold and hysteresis can be set by the I²C interface.

Floating Driver and Bootstrap Charging

An external bootstrap capacitor powers the floating power MOSFET driver. The floating driver has its own UVLO protection, with a rising threshold of 2.5V and hysteresis of 200mV.

The bootstrap capacitor voltage is charged to about 5V from VCC through a PMOS pass transistor when the LS-FET is on.

In high duty cycle operation or sleep mode, the bootstrap charging time period is shorter, so the bootstrap capacitor may not be charged sufficiently. In case the external circuit does not have sufficient voltage and time to charge the bootstrap capacitor, extra external circuitry can be used to ensure the bootstrap voltage is in the normal operation range.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
©2019 MPS. All Rights Reserved.

Low-Dropout Operation (BST Refresh)

To improve dropout, the device is designed to operate at close to 100% duty cycle as long as the BST to SW pin voltage is greater than 2.5V. When the voltage from BST to SW drops below 2.5V, the high-side MOSFET turns off using a UVLO circuit that allows the low-side MOSFET to conduct and refresh the charge on the BST capacitor.

In cases where the input voltage drops, the HS-FET remains on and close to 100% duty cycle to maintain output regulation, until the BST to SW voltage falls below 2.5V. Since the supply current sourced from the BST capacitor is low, the high-side MOSFET can remain on for more switching cycles than are required to refresh the capacitor. Therefore, the effective duty cycle of the switching regulator is high.

The effective duty cycle during dropout of the regulator is mainly influenced by the voltage drops across the power MOSFET, inductor resistance, low-side diode, and PCB resistance.

I²C Control and Default Output Voltage

When the device is enabled (which means EN = high and V_{IN} > UVLO), the chip starts up to a default 5V output voltage. After that, the I²C bus can communicate with master. Once the I²C receives a valid output voltage set instruction, the output voltage is determined by the I²C control.

The output voltage is set by adjusting the internal reference voltage and output feedback divider ratio. After this device receives a valid data byte of output voltage setting, it searches the corresponding value from the truth table and then sends the command of adjusting reference and divider ratio. Finally, it outputs the correct voltage.

Frequency Dithering for Low EMI

Frequency dithering is a technique used in the power industry to reduce EMI, especially for EMI-sensitive applications. This spread-spectrum modulation technique spreads the frequency spectrum of converter, which in turn spreads the energy of the switching harmonics over a wider band while reducing their amplitudes, helping to meet stringent EMI goals.

The programmable frequency dithering feature of this device allows either 3/48 or 3/28 variation range in the switching frequency, with a 120μs or 150μs dithering cycle. Both the frequency dithering range and cycle can be set by the I²C interface.

Multi-Page One-Time-Programmable Memory

The device features three pages of one-time-programmable memory to store desired settings permanently.

Differential one-time-programmable cells, rather than single-ended, are used for long-term reliability. Data is stored on two floating gate avalanche injection metal oxide semiconductor (FAMOS), and output comparators are used for differential reading.

The first page of the multi-page one-time-programmable memory has been programmed with manufacturer default values.

Once the device is enabled, the default values on the first page are used to set the control parameters in the registers. If there is data on other pages of the one-time-programmable memory, the newest setting is identified by an internal indicator to write registers. See the Register Map and Register Description sections for details.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
©2019 MPS. All Rights Reserved.

I²C INTERFACE

I²C Serial Interface Description

I²C is a two-wire, bidirectional serial interface, consisting of a data line (SDA) and a clock line (SCL). The lines are externally pulled to a bus voltage when they are idle. Connecting to the line, a master device generates the SCL signal and device address, then arranges the communication sequence. The device's interface is an I²C slave, which supports both fast mode (400kHz) and typically high-speed mode (3.4MHz), adding flexibility to the power supply solution. The output voltage, transition slew rate, or other interesting parameters can be instantaneously controlled by the I²C interface.

Data Validity

One clock pulse is generated for each data bit transferred. The data on the SDA line must be stable during the high period of the clock. The high or low state of the data line can only change when the clock signal on the SCL line is low (see Figure 4).

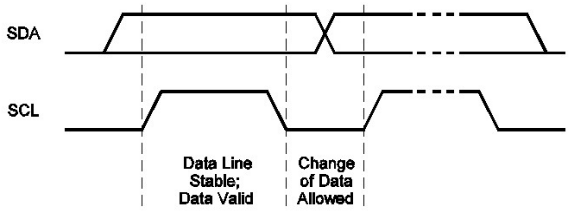


Figure 4: Bit Transfer on the I²C Bus

Start and Stop Conditions

Start and stop conditions are signaled by the master device, which signifies the beginning and the end of the I²C transfer. A start condition (S) is defined as the SDA signal transitioning from high to low while the SCL is high. A stop condition (P) is defined as the SDA signal transitioning from low to high while the SCL is high (see Figure 4).

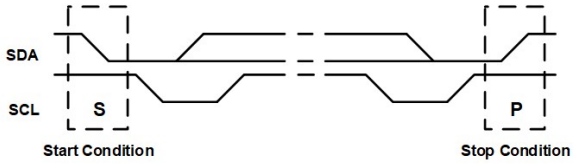


Figure 5: Start and Stop Conditions

Start and stop conditions are always generated by the master. The bus is considered busy after the start condition. The bus is considered free again after a minimum of 4.7μs after the stop condition. The bus stays busy if a repeated start (Sr) is generated instead of a stop condition. The start and repeated start conditions are functionally identical.

Transfer Data

Every byte put on the SDA line must be 8 bits long. Each byte must be followed by an acknowledge (ACK) bit. The acknowledge-related clock pulse is generated by the master. The transmitter releases the SDA line (high) during the acknowledge clock pulse. The receiver must pull down the SDA line during the acknowledge clock pulse, so that it remains stable low during the high period of the clock pulse.

Figure 6 shows the format that data transfers follow. After the start condition, a slave address is sent. This address is 7 bits long, followed by an 8th data direction bit (R/W). A 0 indicates a transmission (write), and a 1 indicates a request for data (read). A data transfer is always terminated by a stop condition, generated by the master. However, if a master still wishes to communicate on the bus, it can generate a repeated start condition and address another slave without first generating a stop condition.

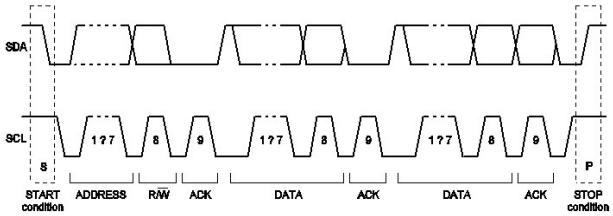


Figure 6: A Complete Data Transfer

I²C Update Sequence

This device requires a start condition, a valid I²C address, a register address byte, and a data byte for a single data update. After receipt of each byte, the device acknowledges by pulling the SDA line low during the high period of a single clock pulse. A valid I²C address selects the device. The device performs an update on the falling edge of the LSB byte.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
©2019 MPS. All Rights Reserved.

I²C Chip Address

The ADD pin can be used to program the I²C address. This device supports 8 addresses for up to 8 voltage rails through configuring the resistor value that connecting between the ADD pin and ground. When the master sends the address as an 8-bit value, the 7-bit address should be followed by “0/1” to indicate write/read operation

Table 1 shows the resistor values for different I²C addresses.

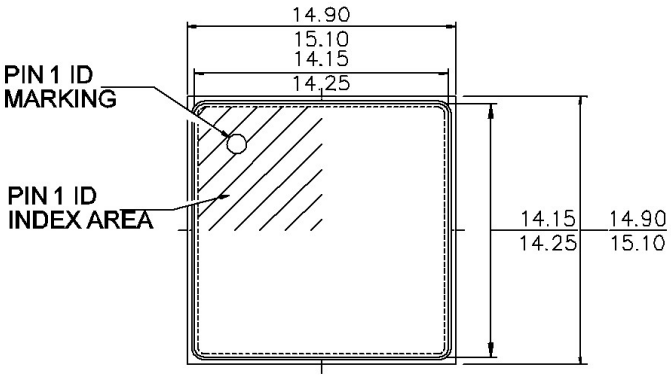
Table 1: I²C Address

Resistor (kΩ) 1%	Address
0 to 21.5	21h
22 to 47	22h
47.5 to 71.5	23h
73.5 to 97.3	24h
100 to 124	25h
127 to 147	26h
150 to 174	27h
>178	28h

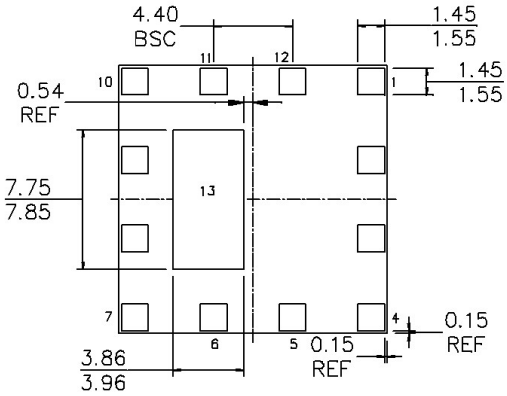
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
©2019 MPS. All Rights Reserved.

PACKAGE INFORMATION

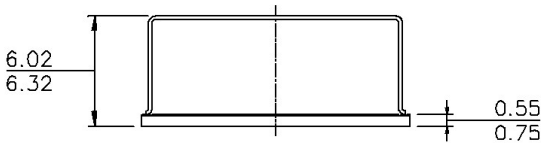
LGA (15mmx15mmx6mm)



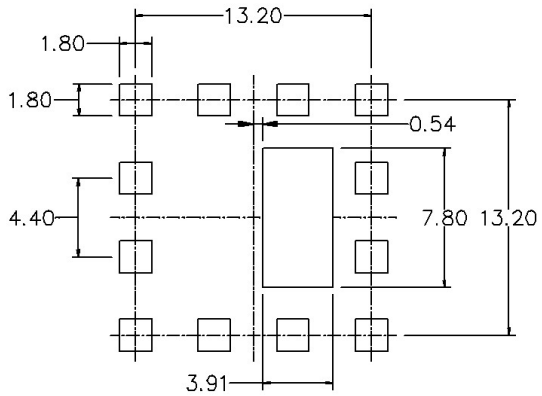
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE :

1) ALL DIMENSIONS ARE IN MILLIMETERS
2) DRAWING IS NOT TO SCALE

NOTICE: The information in this document is subject to change without notice. Please contact MPS for current specifications. Users should warrant and guarantee that third-party Intellectual Property rights are not infringed upon when integrating MPS products into any application. MPS will not assume any legal responsibility for any said applications.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
©2019 MPS. All Rights Reserved.