

# **Customer Information Notification**

Issue Date: 18-Mar-2020 Effective Date: 19-Mar-2020

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# 2020010011



Change Category				
[] Wafer Fab Process	[] Assembly	[] Product Marking	[] Test	[] Design
	Process		Location	
[] Wafer Fab Materials	[] Assembly	[] Mechanical Specification	n[]Test	[X] Errata
	Materials		Process	
[] Wafer Fab Location	[] Assembly	[]	[] Test	[] Electrical
	Location	Packing/Shipping/Labeling	Equipment	spec./Test
				coverage
[] Firmware	[X] Other - Data Sheet Update for correction and clarification			

i.MXRT1060 Data Sheet Rev 0.2 and Errata Rev 1.1 Updates

# **Description**

NXP Semiconductors announces errata update to revision 1.1 and data sheet update to revision 0.2 for i.MXRT1060. The revision history included in the updated documents provides a detailed description of the changes. Changes are summarized below.

## For RT1060 Chip Errata:

Added following errata:

\* ERR050235 CCM: Incorrect clock setting for CAN affects UART clock gating

## For RT1060 Consumer DS, Data Sheet Changes:

- 1. Updated the SPI NAND Flash in the Section 1.1, Features
- 2. Updated the features of RT1062 in the Table 1, Ordering information
- 3. Updated the Table 81, Boot through UART1 and removed the Table, Boot through UART2
- 4. Updated the figure and table numbers in the Section 6.2, 12 x 12 mm package information
- 5. Updated the Figure 53, "10 x 10 mm BGA, case x package top, bottom, and side Views" and Figure 54, "12 x 12 mm BGA, case x package top, bottom, and side Views"

# For RT1060 Industrial DS, Data Sheet Changes:

- 1. Updated the SPI NAND Flash in the Section 1.1, Features
- 2. Updated the Table 81, Boot through UART1 and removed the Table, Boot through UART2
- 3. Updated the figure and table numbers in the Section 6.2, 12 x 12 mm package information
- 4. Updated the Figure 53, "10 x 10 mm BGA, case x package top, bottom, and side Views" and Figure 54, "12 x 12 mm BGA, case x package top, bottom, and side Views"

The i.MXRT1060 errata revision 1.1 is attached to this notice, and can be found at:

https://www.nxp.com/products/processors-and-microcontrollers/arm-microcontrollers/i.mx-rt-series/i.mx-rt1060-crossover-processor-with-arm-cortex-m7-core:i.MX-RT1060?tab=Documentation Tab&linkline=Errata

The i.MXRT1060 data sheet revision 0.2 is attached to this notice, and can be found at:

https://www.nxp.com/products/processors-and-microcontrollers/arm-microcontrollers/i.mx-rt-series/i.mx-rt1060-crossover-processor-with-arm-cortex-m7-core:i.MX-RT1060?tab=Documentation\_Tab&linkline=Data-Sheet

#### Reason

The errata was added for additional technical clarification on some device features.

The data sheets have been updated to correct errors and / or provide additional technical clarification on some device features.

#### **Identification of Affected Products**

Product identification does not change

# Anticipated Impact on Form, Fit, Function, Reliability or Quality

No impact on form, fit, function, reliability or quality.

#### **Data Sheet Revision**

A new datasheet will be issued

## **Contact and Support**

For all inquiries regarding the ePCN tool application or access issues, please contact NXP "Global Quality Support Team".

For all Quality Notification content inquiries, please contact your local NXP Sales Support team.

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NXP Quality Management Team.

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# **Affected Part Numbers**

MIMXRT1062CVL5A

MIMXRT1062DVL6A

MIMXRT1061CVJ5A

MIMXRT106LDVL6A

MIMXRT1062DVJ6A

MIMXRT106ADVL6A

MIMXRT106FDVL6A

MIMXRT1062CVJ5A