Customer Information Notification | 201912006I

Issue Date: 10-Jan-2020
Effective Date: 11-Jan-2020

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Change Category

[ ] Wafer Fab Process	[ ] Assembly Process	[ ] Product Marking	[ ] Test Location	[ ] Design
[ ] Wafer Fab Materials	[ ] Assembly Materials	[ ] Mechanical Specification	[ ]Test Process	[X] Errata
[ ] Wafer Fab Location	[ ] Assembly Location	[ ] Packing/Shipping/Labeling	[ ] Test Equipment	[X] Electrical spec./Test coverage
[ ] Firmware	[ ] Other			

i.MXRT1064 Data Sheet Rev 1 and Errata Rev 1.1 Updates

Description

NXP Semiconductors announces errata update to revision 1.1 and data sheet update to revision 1 for i.MXRT1064. The revision history included in the updated documents provides a detailed description of the changes. Changes are summarized below.

For RT1064 Chip Errata:
Added following errata:
* ERR050235 CCM: Incorrect clock setting for CAN affects UART clock gating

For RT1064 Consumer DS, Data Sheet Changes:
1. Updated ADC and SPI NAND Flash in the Section 1.1, Features; removed DAC from Section 1.1,Features
2. Updated ADC and RAM in the Figure 2, "i.MX RT1064 system block diagram"
3. Updated the RT website link in the Section 1.2, Ordering information
4. Updated FlexSPI and SNVS in the Table 1, Ordering information; added KPP, SPI, XBAR/AOI, CSU, and second package information in the Table 1, Ordering information
5. Removed tamper detection from the Table 2, i.MX RT1064 modules list
6. Updated the on-chip termination values of JTAG_TCK and JTAG_MOD in the Table 4, JTAG Controller

interface summary
7. Updated the Section 4.1.2, Thermal resistance
8. Changed 528 MHz PLL to System PLL in the Table 16, System PLL's electrical parameters
9. Changed 480 MHz PLL to USB PLL in the Table 18, USB PLL's electrical parameters
10.Updated the VDD name of supply voltage conditions column in the Table 54, 12-bit ADC operating conditions
11.Updated the Section 4.9.1, LPSPI timing parameters
12.Updated the Table 82, Boot through UART1 and removed the Table, Boot through UART2
13.Updated the Figure 53, "10 x 10 mm BGA, case x package top, bottom, and side Views"
14.Added the Section 7.2, 12 x 12 mm package information

For RT1064 Industrial DS, Data Sheet Changes:
1. Updated SPI NAND Flash in the Section 1.1, Features
2. Updated FlexSPI, LCD/CSI/PXP, and SNVS in the Table 1, Ordering information; added KPP, SPI, XBAR/AOI, and CSU in the Table 1, Ordering information
3. Updated RAM in the Figure 2, "i.MX RT1064 system block diagram"
4. Updated the Section 4.1.2, Thermal resistance
5. Updated the Table 82, Boot through UART1 and removed the Table, Boot through UART2
6. Updated the Figure 53, "10 x 10 mm BGA, case x package top, bottom, and side Views" and Figure 54, "12 x 12 mm BGA, case x package top, bottom, and side Views"

The i.MXRT1064 errata revision 1.1 is attached to this notice, and can be found at:
https://www.nxp.com/products/processors-and-microcontrollers/arm-microcontrollers/i.mx-rt-series/i.mx-rt1064-crossover-processor-with-arm-cortex-m7-core:i.MX-RT1064?tab=Documentation_Tab&linkline=Errata

The i.MXRT1064 data sheet revision 1 is attached to this notice, and can be found at:
https://www.nxp.com/products/processors-and-microcontrollers/arm-microcontrollers/i.mx-rt-series/i.mx-rt1064-crossover-processor-with-arm-cortex-m7-core:i.MX-RT1064?tab=Documentation_Tab&linkline=Data-Sheet

Reason

The errata was added for additional technical clarification on some device features.
The data sheets have been updated to correct errors and / or provide additional technical clarification on some device features.

Identification of Affected Products

Product identification does not change

Anticipated Impact on Form, Fit, Function, Reliability or Quality

No impact on form, fit, function, reliability or quality.

Data Sheet Revision

A new datasheet will be issued

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Affected Part Numbers

MIMXRT1064DVL6A

MIMXRT1064CVL5A