Customer Information Notification | 201907005I

Issue Date: 08-Aug-2019
Effective Date: 09-Aug-2019

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Change Category

[ ] Wafer Fab Process	[ ] Assembly Process	[ ] Product Marking	[ ] Test Location	[ ] Design
[ ] Wafer Fab Materials	[ ] Assembly Materials	[ ] Mechanical Specification	[ ]Test Process	[X] Errata
[ ] Wafer Fab Location	[ ] Assembly Location	[ ] Packing/Shipping/Labeling	[ ] Test Equipment	[X] Electrical spec./Test coverage
[ ] Firmware	[ ] Other			

i.MXRT1015&1020 Errata and Data Sheet Update to Rev.1

Description

NXP Semiconductors announces errata and data sheet update for both i.MXRT1015&RT1020 to revision 1. The revision history included in the updated documents provides a detailed description of the changes. Changes are summarized below.

For RT1015&RT1020 both Industrial and Consumer Chip Errata:
Added following 5 errata:
* ERR011572
* ERR050130
* ERR050144
* ERR050101
* ERR050194

For RT1015 both Industrial and Consumer DS, Data Sheet Changes:
1. Updated the SNVS descriptions in the Table 2, i.MX RT1015 modules list
2. Updated the Section 4.8.1, LPSPI timing parameters

For RT1020 both Industrial and Consumer DS, Data Sheet Changes:
1. Added analog descriptions in the Section 1.1, Features
2. Added ADC channel number in the Table 1, The comparison between 100 LQFP and 144 LQFP package
3. Updated the RT website link in the Section 1.2, Ordering information
4. Updated the ADC descriptions in the Figure 2, "i.MX RT1020 system block diagram
5. Updated the RAM size, SNVS descriptions, and USB descriptions in the Table 3, i.MX RT1020 modules list
6. Updated the on-chip termination values of JTAG_TCK and JTAG_MOD in the Table 5, JTAG controller interface summary
7. Removed the USB_OTG2_VBUS from the Table 8, Absolute maximum ratings, Table 11, Operating ranges, and Section 4.2.1.1, Power-up sequence
8. Changed 528 MHz PLL to System PLL in the Table 17, System PLLs electrical parameters
9. Changed 480 MHz PLL to USB PLL in the Table 19, USB PLLs electrical parameters
10. Updated the Section 4.8.1, LPSPI timing parameters
11. Added the Figure 32, "Minimum Sample Time Vs Ras (Cas = 2pF)", Figure 33, "Minimum Sample Time Vs Ras (Cas = 5 pF)", and Figure 34, "Minimum Sample Time Vs Ras (Cas = 10 pF)" in the Section 4.7.2, A/D converter

The i.MXRT1015 errata revision 1 is attached to this notice, and can be found at:
https://www.nxp.com/docs/en/errata/IMXRT1015CE.pdf

The i.MXRT1020 errata revision 1 is attached to this notice, and can be found at:
https://www.nxp.com/docs/en/errata/IMXRT1020CE.pdf

The i.MXRT1015 data sheet revision 1 is attached to this notice, and can be found at:
https://www.nxp.com/products/processors-and-microcontrollers/arm-based-processors-and-mcus/i.mx-applications-processors/i.mx-rt-series/i.mx-rt1015-crossover-processor-with-arm-cortex-m7-core:i.MX-RT1015?&tab=Documentation_Tab&linkline=Data-Sheet

The i.MXRT1020 data sheet revision 1 is attached to this notice, and can be found at:
https://www.nxp.com/products/processors-and-microcontrollers/arm-based-processors-and-mcus/i.mx-applications-processors/i.mx-rt-series/i.mx-rt1020-crossover-processor-with-arm-cortex-m7-core:i.MX-RT1020?&tab=Documentation_Tab&linkline=Data-Sheet

Reason

The errata were added for additional technical clarification on some device features.
The data sheets have been updated to correct errors and / or provide additional technical clarification on some device features.

Identification of Affected Products

Product identification does not change

Anticipated Impact on Form, Fit, Function, Reliability or Quality

No impact on form, fit, function, reliability or quality.

Data Sheet Revision

A new datasheet will be issued

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Affected Part Numbers	Affected 12NC
MIMXRT1021CAF4A	935360317557
MIMXRT1021CAG4A	935360318557
MIMXRT1015DAF5A	935380893557
MIMXRT1021DAG5A	935360321557
MIMXRT1015CAF4A	935380892557
MIMXRT1021DAF5A	935360319557