



Customer Information Notification

201904013I

Issue Date: 15-May-2019

Effective Date: 16-May-2019

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QUALITY

Change Category

- | | | | | |
|--|---|--|---|--|
| <input type="checkbox"/> Wafer Fab Process | <input type="checkbox"/> Assembly Process | <input type="checkbox"/> Product Marking | <input type="checkbox"/> Test Location | <input type="checkbox"/> Design |
| <input type="checkbox"/> Wafer Fab Materials | <input type="checkbox"/> Assembly Materials | <input type="checkbox"/> Mechanical Specification | <input type="checkbox"/> Test Process | <input type="checkbox"/> Errata |
| <input type="checkbox"/> Wafer Fab Location | <input type="checkbox"/> Assembly Location | <input type="checkbox"/> Packing/Shipping/Labeling | <input type="checkbox"/> Test Equipment | <input checked="" type="checkbox"/> Electrical spec./Test coverage |
| <input type="checkbox"/> Firmware | <input type="checkbox"/> Other | | | |

i.MXRT1060 Data
Sheet Rev 0.1
Updates

Description

NXP Semiconductors announces a data sheet update for the i.MXRT1060 to revision 0.1. The revision history included in the updated documents provides a detailed description of the changes. Changes are summarized below.

Data Sheet Changes:

1. Updated ADC information and removed DAC from Section 1.1, Features and Figure 2, "i.MX RT1060 system block diagram"
2. Added a new part number in the Table 1, Ordering information (For consumer part only)
3. Updated the RT website link in the Section 1.2, Ordering information
4. Removed tamper detection from the Table 2, i.MX RT1060 modules list
5. Updated the on-chip termination values of JTAG_TCK and JTAG_MOD in the Table 4, JTAG Controller interface summary
6. Updated the maximum value of VDD_SOC_IN in the Table 7, Absolute maximum ratings
7. Changed 528 MHz PLL to System PLL in the Table 16, System PLL's electrical parameters
8. Changed 480 MHz PLL to USB PLL in the Table 18, USB PLL's electrical parameters
9. Updated the VDD name of supply voltage conditions column in the Table 54, 12-bit ADC operating

conditions

10. Added the Figure 36, "Minimum Sample Time Vs Ras (Cas = 2pF)", Figure 37, "Minimum Sample Time Vs Ras (Cas = 5 pF)", and Figure 38, "Minimum Sample Time Vs Ras (Cas = 10 pF)" in the Section 4.8.2, A/D converter

11. Updated the Section 4.9.1, LPSPI timing parameters

The i.MXRT1060 data sheet revision 0.1 is attached to this notice, and can be found at:

https://www.nxp.com/products/processors-and-microcontrollers/arm-based-processors-and-mcus/i.mx-applications-processors/i.mx-rt-series/i.mx-rt1060-crossover-processor-with-arm-cortex-m7-core:i.MX-RT1060?tab=Documentation_Tab&linkline=Data-Sheet

Reason

The data sheet has been updated to correct errors and / or provide additional technical clarification on some device features.

Identification of Affected Products

Product identification does not change

Anticipated Impact on Form, Fit, Function, Reliability or Quality

No impact on form, fit, function, reliability or quality.

Data Sheet Revision

A new datasheet will be issued

Contact and Support

For all inquiries regarding the ePCN tool application or access issues, please contact NXP "Global Quality Support Team".

For all Quality Notification content inquiries, please contact your local NXP Sales Support team.

For specific questions on this notice or the products affected please contact our specialist directly:

Name Daniel Cheng

Position Product Engineer

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Customer Focus, Passion to Win.

NXP Quality Management Team.

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NXP Semiconductors

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Changed Orderable Part#	Changed Part 12NC	Changed Part Number	Changed Part Description	Package Outline	Package Name	Status	Product Line
MIMXRT1062CVJ5A	935379987557	MIMXRT1062CVJ5A	i.MXRT1060	SOT1968-1	LFBGA196	RFS	MCUs
MIMXRT1062CVL5A	935373203557	MIMXRT1062CVL5A	i.MXRT1060	SOT1546-2	LFBGA196	RFS	MCUs
MIMXRT1062DVJ6A	935379988557	MIMXRT1062DVJ6A	i.MXRT1060	SOT1968-1	LFBGA196	RFS	MCUs
MIMXRT1061CVJ5A	935379986557	MIMXRT1061CVJ5A	i.MXRT1060	SOT1968-1	LFBGA196	RFS	MCUs
MIMXRT1062DVL6A	935373204557	MIMXRT1062DVL6A	i.MXRT1060	SOT1546-2	LFBGA196	RFS	MCUs