

Customer Information Notification

Issue Date: 19-May-2014 Effective Date: 17-Jun-2014

UPDATE

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QUALITY

201405009IU01

Management Summary

The change defines the I2C-bus address by metal mask to fixed logic levels. Before one bit in the OTP memory selected upon power-on.

Change Category

| • · · · · · · · · · · · · · · · · · · · | | | |
|---|----------------------|--------------------------|-----------------------------|
| [] Wafer Fab process | [] Assembly Process | [] Product Marking | [X] Design |
| [] Wafer Fab | [] Assembly | [] Electrical spec./Test | [] Mechanical Specification |
| materials | Materials | coverage | |
| [] Wafer Fab location | [] Assembly Location | [] Test Location | [] |
| | | | Packing/Shipping/Labeling |

PCF8523T fix in I2C address definition

Information Notification

- When addressing the circuit before the internal power-on-reset was completed it was possible that the RTC was not reacting correctly.
- In the existing version the I2C-bus address is fetched at power up from the OTP memory. This change fixes now the I2C-bus address by metal mask to static logic levels.
- Defining the address to a fix value: D0, guarantees that the I2C-bus address D0 is recognized as soon as internal supply voltage reaches VDDmin.

Why do we issue this Information Notification

To ensure correct I2C address in all cases.

Identification of Affected Products

Product identification does not change

Update Information

Address information A2 was wrong in the first version of thei CIN. Changed to D0.

Impact

It is a correction of a possible error in power-up. Correct functionality is better ensured.

Data Sheet Revision

No impact to existing datasheet

Contact and Support

For all inquiries regarding the ePCN tool application or access issues, please <u>contact NXP "Global Quality Support Team"</u>.

For all Quality Notification content inquiries, please contact your local NXP Sales Support team.

For specific questions on this notice or the products affected please contact our specialist directly:

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NXP Quality Management Team.

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