

Product Change Notification - SYST-18CTLL797

Date:

19 Feb 2019

Product Category:

32-bit Microcontrollers

Affected CPNs:**Notification subject:**

Data Sheet - SAM L10/L11 Family Data Sheet

Notification text:

SYST-18CTLL797

Microchip has released a new DeviceDoc for the SAM L10/L11 Family Data Sheet of devices. If you are using one of these devices please read the document located at [SAM L10/L11 Family Data Sheet](#).

Notification Status: Final**Description of Change:**

- 1) Configuration Summary - Updated SAML10/L11 Family Features
- 2) Oscillators Pinout - Updated XOSC32 Jitter Minimization
- 3) Memories
 - Updated NVM Software Calibration Bitfields Definition
 - Updated SAM L11 BOCOR Bitfields Definition
 - Updated SAM L11 BOCOR Mapping
- 4) 13.1 Features
 - Updated Features
 - Updated CRYA APIs Addresses with a note
- 5) Boot ROM
 - Updated Secure Boot Options
 - Updated Accessible Memory Range by Read Auxiliary Row Command, and added a note
- 6) Device Service Unit (DSU) - Updated STATUSB Register
- 7) Power Manager (PM) - Updated PLCFG Register
- 8) Oscillators Controller (OSCCTRL)
 - Corrected missing Block Diagram
 - Updated the reset value for the STATUS Register
- 9) 32KHz Oscillators Controller (OSC32KCTRL) - Updated the ULP32KSW bit in the OSCULP32K Register
- 10) Supply Controller (SUPC) - Corrected erroneous text and added a note to Low Power VREF in Active Mode
- 11) Real Time Counter (RTC)
 - Updated RTC Block Diagram (Tamper Detection Use Case)
 - Updated Active Layer Protection
 - Updated TAMPCTRL Register with new notes for the DEBNC and TAMLVL bits
 - Updated TAMPCTRLB Register with a note for the ALSI bits
- 12) Direct Memory Access Controller (DMAC)
 - Updated the text for the DMAC Clocks section
 - Updated the LVLEN bits for the CTRL Register
 - Updated the LVLEX bits for the ACTIVE Register
- 13) External Interrupt Controller (EIC)
 - Updated the NMIFLAG Register
 - Updated the CONFIG Register to reflect changes to the FILTEN and SENSE bits
- 14) Nonvolatile Memory Controller (NVMCTRL)
 - Corrected erroneous text in Cache
 - Corrected table entries in Memory Regions AHB Access Limitations and an updated a note.
 - Updated Data Flash Scrambling

15) TrustRAM (TRAM)

- Corrected Erroneous text in Overview
- Updated Features

16) I/O Pin Controller (PORT) - Updated the PORTEI, EVACT, and PID bits in the EVCTRL Register

17) Event System (EVSYS) - Corrected text in Initialization

18) SERCOM USART

- Updated the BAUD Register
- Updated the equation in the RXPL Register

19) SERCOM I2C

- Updated Signal Description
- Updated the property for the slave DATA Register
- Updated the master DATA Register

20) Timer/Counter (TC)

- Updated the MCEO bits in the EVCTRL Register for 8-bit, 16-bit and 32-bit Modes
- Updated The MC Bits in the INTENCLR, INTENSET, and INTFLAG Registers for 8-bit, 16-bit and 32-bit Modes

- Updated the CCBUFV bit in the STATUS Register for 8-bit, 16-bit and 32-bit Modes

- Updated the INVEN Bit in the DRVCTRL Register for 8-bit, 16-bit and 32-bit Modes

21) Configurable Custom Logic (CCL)

- Updated text in Overview
- Updated the Block Diagram
- Updated the table in Signal Description
- Updated Linked LUT
- Updated Analog Comparator Inputs
- Removed erroneous TCC text
- Updated the INSEL bits in the LUTCTRL0 Register
- Updated the INSEL bits in the LUTCTRL1 Register

22) Analog-to-Digital Converter (ADC)

- Updated Features
- Updated the Block Diagram
- Updated the text in ADC Resolution
- Added a note in Oversampling and Decimation
- Updated the CTRLC Register

23) Analog Comparators (AC)

- Updated the text in VDD Scaler
- Updated the START bits in the CTRLB Register
- Updated the COMPEO, COMPEI, and INVEI bits in the EVCTRL Register
- Updated the COMP bits in the INTENCLR, INTENSET, and INTFLAG Registers
- Updated the STATE bits in the STATUSA Register
- Updated the READY bits in the STATUSB Register
- Updated the COMPCTRL bits in the SYNCBUSY Register

24) Digital-to-Analog Converter (DAC)

- Updated Features
- Updated Dithering Mode

25) Operational Amplifier Controller (OPAMP)

- Updated the diagram in 44.6.11.3 Offset Compensation
- Updated the READY bits of the STATUS Register

26) Electrical Characteristics

- Updated the note in Absolute Maximum Ratings
- Removed erroneous data from the External Components Requirements in Switching Mode Table
- Updated the Operating Conditions Table
- Updated Active Current Consumption
- Updated Digital frequency Locked Loop Characteristics

27) Electrical Characteristics at 125°C

- Updated Operating Conditions Table



- Updated Active Current Consumption
- 28) Schematic Checklist - Updated External Analog Reference Schematic With One Reference
- 29) Appendix A - New Section for Migrating From SAM L21 to SAM L10/L11 (32-pin Package)
- 30) Appendix B - New Section for Migrating From SAM D20/D21 to SAM L10/L11 (32-pin Package)

Impacts to Data Sheet: None

Reason for Change: To Improve Manufacturability

Change Implementation Status: Complete

Date Document Changes Effective: 19 Feb 2019

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A

Attachment(s):

[SAM L10/L11 Family Data Sheet](#)

Please contact your local [Microchip sales office](#) with questions or concerns regarding this notification.

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Affected Catalog Part Numbers (CPN)

ATSAML10D14A-MF
ATSAML10D14A-MFT
ATSAML10D14A-MU
ATSAML10D14A-MUT
ATSAML10D14A-YF
ATSAML10D14A-YFT
ATSAML10D14A-YU
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