PCN Number:	20180226000	PCN Date:	March 2, 2018
Title:	Datasheet for DS90UB953-Q1		
Customer Contact:	PCN Manager	Dept:	Quality Services

Change Type:		
☐ Assembly Site	☐ Design	☐ Wafer Bump Site
☐ Assembly Process	☒ Data Sheet	☐ Wafer Bump Material
☐ Assembly Materials	☐ Part number change	☐ Wafer Bump Process
☐ Mechanical Specification	☐ Test Site	☐ Wafer Fab Site
☐ Packing/Shipping/Labeling	☐ Test Process	☐ Wafer Fab Materials
		☐ Wafer Fab Process

Notification Details

Description of Change:

Texas Instruments Incorporated is announcing an information only notification.
The product datasheet(s) is being updated as summarized below.
The following change history provides further details.

TEXAS INSTRUMENTS

DS90UB953-Q1

SNLS552A – SEPTEMBER 2017 – REVISED FEBRUARY 2018

Changes from Original (September 2017) to Revision A **Page**

- Changed RES1 pin description from "Leave OPEN" to "Do not connect" 4
- Added "Internal 1-MΩ pulldown" text to PDB pin description 4
- Expanded MODE pin description 5
- Changed "Requires" to "Typically connected to" in the Power and Ground pin descriptions 5
- Changed "and should not be connected to an external supply" to "Do not connect to an external supply rail" in the Power and Ground pin descriptions 5
- Changed the CSI_ERR_COUNT (0x5C) text to CSI_ERR_CNT (0x5C) 17
- Changed DS90UBUB954-Q1 to DS90UB954-Q1 18
- Changed the GPIO_INPUT_CTL text to GPIO_INPUT_CTRL in the *GPIO Input Control* and *GPIO Output Control* sections 20
- Changed CLK_IN lower limit with CLKIN_DIV =1 from 46 MHz to 25 MHz and CLK_IN lower limit from 92 MHz to 50 MHz. 21
- Corrected typo in MODE description saying the number of modes is 3 to the correct value of 2 23
- Changed I2C START description to "A START occurs when SDA transitions Low while SCLK is High" 25
- Changed internal reference clock in I2C timing section from 26.25 MHz to 25 MHz 25
- Added registers tables for reserved registers 0x04, 0x0F-0x12, 0x16, 0x1F, 0x25-0x30, 0x34, 0x36, 0x38, 0x4A-0x4F, 0x5B, 0x65-0xAF, and 0xB3-0xEF. 29
- Changed bit 6 and bit 7 in the MODE_SEL register to RESERVED 30
- Changed the SENSE_VO_HI and SENSE_VO_LO registers to SENSE_V0_HI and SENSE_V0_LO to match the title in Table 33 35
- Changed the SENSE_V0_HI and SENSE_V0_LO bit descriptions 35
- Changed the SENSOR_V0_THRESH bit description 36
- Changed the SENSE_T_HI and SENSE_T_LO bit descriptions 36
- Combined the CSI_EN_HSRX register bits 6–0 into one row 38
- Combined the CSI_EN_LPRX register bits 6–0 into one row 38

- Combined the CSI_EN_RXTERM register bits 7–4 into one row 38
- Changed serializer to deserializer in SLAVE_ID_ALIAS_x bit descriptions 44
- Changed Slave 0 to Slave 1 in the SLAVE_AUTO_ACK_1 bit description 44
- Changed Slave 0 to Slave 2 in the SLAVE_AUTO_ACK_2 bit description 45
- Changed Slave 0 to Slave 3 in the SLAVE_AUTO_ACK_3 bit description 45
- Changed Slave 0 to Slave 4 in the SLAVE_AUTO_ACK_4 bit description 45
- Changed Slave 0 to Slave 5 in the SLAVE_AUTO_ACK_5 bit description 46
- Changed Slave 0 to Slave 6 in the SLAVE_AUTO_ACK_6 bit description 46
- Changed Slave 0 to Slave 7 in the SLAVE_AUTO_ACK_7 bit description 46
- Changed CRC_ERR bit description in GENERAL_STATUS to match CRC_ERR_CLR register name 47
- Changed the CNTRL_ERR_HSRQST_2 bit description 50
- Changed Figure 17 caption 68
- Added PIN(S) column to Table 175 69
- Changed large bulk capacitor typical range lower limit from 50 µF to 47 µF, removed mentions of dedicated power plane and tantalum capacitors, and changed recommended power rating for capacitors in layout guidelines 72
- Changed recommended CSI-2 guidelines on matching trace lengths and routing to help trace impedance 73
- Changed routing guidelines for the DOUT+ and DOUT– pins 74
- Added new links to the *Related Documentation* section 76

The datasheet number will be changing.

Device Family	Change From:	Change To:
DS90UB953-Q1	SNLS552	SNLS552A

These changes may be reviewed at the datasheet links provided.

http://www.ti.com/product/DS90UB953-Q1

Reason for Change:

To accurately reflect device characteristics.

Anticipated impact on Fit, Form, Function, Quality or Reliability (positive / negative):

No anticipated impact. This is a specification change announcement only. There are no changes to the actual device.

Changes to product identification resulting from this PCN:

None.

Product Affected:

DS90UB953TRHBRQ1	DS90UB953TRHBTQ1		

For questions regarding this notice, e-mails can be sent to the regional contacts shown below or your local Field Sales Representative.

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