CHANGE NOTIFICATION

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408) 432-1900

March 31, 2014

Dear Sir/Madam: PCN# 033114

Subject: Notification of Change to LT1910 Datasheet

Please be advised that Linear Technology Corporation has made a minor change to the LT1910 product datasheet to facilitate improvement in our manufacturing yield. The change is shown on the attached page of the marked up datasheet. There was no change made to the die. The product shipped after May 30, 2014 will be tested to the new limits.

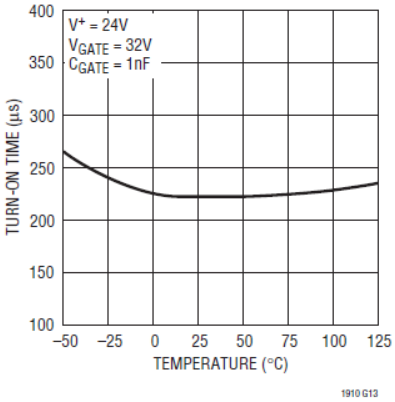
Should you have any further questions, please feel free to contact me at 408-432-1900 ext. 2077, or by e-mail at JASON.HU@linear.com. If I do not hear from you by May 30, 2014, we will consider this change approved by your company.

Sincerely,

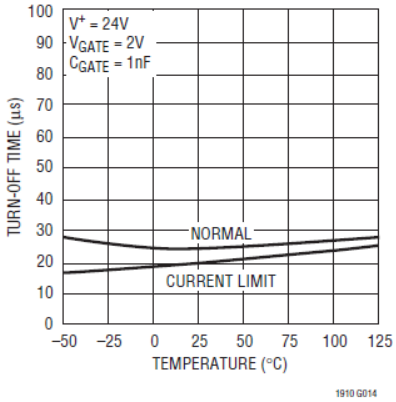
Jason Hu
Quality Assurance Engineer

TYPICAL PERFORMANCE CHARACTERISTICS

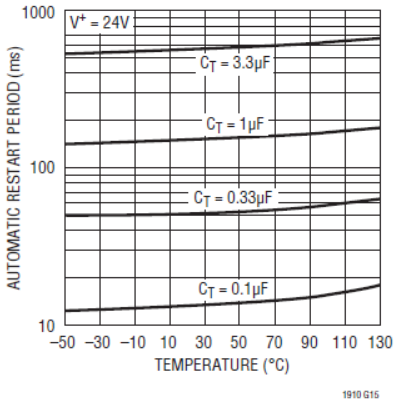
Turn-On Time vs Temperature



Turn-Off Time vs Temperature



Automatic Restart Period vs Temperature



PIN FUNCTIONS

GND (Pin 1): Common Ground.

TIMER (Pin 2): A timing capacitor, C_T, from the TIMER pin to ground sets the restart time following overcurrent detection. Upon detection of an overcurrent condition, C_T is rapidly discharged to less than 1V and then recharged by a 14µA nominal current source back to the 2.9V timer threshold, whereupon the restart is attempted. Whenever TIMER pulls below 2.9V, the GATE pin pulls low to turn off the external switch. This cycle repeats until the overcurrent condition goes away and the switch restarts successfully. During normal operation the pin clamps at 3.5V nominal.

maximum of

$\overline{\text{FAULT}}$ (Pin 3): The $\overline{\text{FAULT}}$ pin monitors the TIMER pin voltage and indicates the overcurrent condition. Whenever the TIMER pin is pulled below 3.3V at the onset of a current limit condition, the $\overline{\text{FAULT}}$ pin pulls active LOW. The $\overline{\text{FAULT}}$ pin resets HIGH immediately when the TIMER pin ramps above 3.4V during autorestart. The $\overline{\text{FAULT}}$ pin is an open-collector output, thus requiring an external pull-up resistor and is intended for logic interface. The resistor should be selected with a ~~typical~~ 1mA pull-up at low status ~~and less than 2mA under worst-case conditions~~.

IN (Pin 4): The IN pin threshold is TTL/CMOS compatible and has approximately 200mV of hysteresis. When the IN pin is pulled active HIGH above 2V, an internal charge pump is activated to pull up the GATE pin. The IN pin can be pulled as high as 15V regardless of whether the supply is on or off. If the IN pin is left open, an internal 75k pull-down resistor pulls the pin below 0.8V to ensure that the GATE pin is inactive LOW.

GATE (Pin 5): The GATE pin drives the power MOSFET gate. When the IN pin is greater than 2V, the GATE pin is pumped approximately 12V above the supply. It has relatively high impedance (the equivalence of a few hundred kΩ) when pumped above the rail. Care should be taken to minimize any loading by parasitic resistance to ground or supply. The GATE pin pulls LOW when the TIMER pin falls below 2.9V.

SENSE (Pin 6): The SENSE pin connects to the input of a supply-referenced comparator with a 65mV nominal offset. When the SENSE pin is taken more than 65mV below supply, the MOSFET gate is driven LOW and the timing capacitor is discharged. The SENSE pin threshold has a 0.33%/°C temperature coefficient (TC), which closely matches the TC of the drain-sense resistor formed from the copper trace of the PCB.

For loads requiring high inrush current, an RC timing delay can be added between the drain-sense resistor and the SENSE pin to ensure that the current-sense comparator does not false trigger during start-up (see Applications