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PRODUCT BULLETIN

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ISSUE DATE:	24-May-2016
NOTIFICATION:	16950
TITLE:	Updating T4240/T4160/T4080 Hardware Spec from Rev0 to Rev1
EFFECTIVE DATE:	25-May-2016

DEVICE(S)

MPN
T4080NSE7PQB
T4080NSE7QTB
T4080NSN7PQB
T4080NSN7QTB
T4080NXE7PQB
T4080NXN7PQB
T4081NSE7PQB
T4081NSE7QTB
T4081NSE7TTB
T4081NSN7PQB
T4081NSN7QTB
T4081NSN7TTB
T4081NXE7PQB
T4081NXE7QTB
T4081NXE7TTB
T4081NXN7PQB
T4081NXN7QTB
T4081NXN7TTB
T4160NSE7PQB
T4160NSE7QTB
T4160NSE7TTB
T4160NSN7PQB
T4160NSN7QTB
T4160NSN7TTB
T4160NXE7PQB

T4160NXN7PQB
T4161NSE7PQB
T4161NSE7QTB
T4161NSE7TTB
T4161NSN7PQB
T4161NSN7QTB
T4161NSN7TTB
T4161NXE7PQB
T4161NXE7QTB
T4161NXE7TTB
T4161NXN7PQB
T4161NXN7QTB
T4161NXN7TTB
T4240NSE7PQB
T4240NSE7QTB
T4240NSE7TTB
T4240NSN7PQB
T4240NSN7QTB
T4240NSN7TTB
T4240NXE7PQB
T4240NXN7PQB
T4241NSE7PQB
T4241NSE7QTB
T4241NSE7TTB
T4241NSN7PQB
T4241NSN7QTB
T4241NSN7TTB
T4241NXE7PQB
T4241NXE7QTB
T4241NXE7TTB
T4241NXN7PQB
T4241NXN7QTB
T4241NXN7TTB

AFFECTED CHANGE CATEGORIES

- DATASHEET

DESCRIPTION OF CHANGE

The following are corrections to the T4240/4160 H/W Spec Rev 0 document. All changes below are captured in the T4 Rev 1 of the H/W spec.

• Updated the document title to conform with new naming requirements.

• Rebranded to NXP company name within the body of the document.

• Removed all references" to/ and" sections for 10.3215G Interlaken.

• Updated the speed units throughout the document.

• In the pinout list table:
1- Modified notes 6, 8, 23, and 24.
2- Added note 29.
3- Added note 28 to the D3_MDMn pins.
4- Changed the note reference on IFC_AD16 to 29.
5- Updated note 29 so the pull down resistance is 4.7 K instead of 10 to 50 kΩ.

• In Table 2 [Absolute maximum ratings]:
1- Changed format to group "Supply Voltage Levels," "Storage Temperature Conditions," and "Signal Voltage Levels."
2- Reduced Maximum VDD, SnVDD supply voltage level from 1.1 V to 1.08 V.
3- Reduced the max GnVDD I/O voltage levels from 1.65 to 1.58 (DDR3) and from 1.45 to 1.42 (DDR3L).
4- Increased the storage temperature range max value from 150 to 155.
5- Added "Min_DCV V_input," "Max_DCV V_input," and "Max Overshoot Voltage" columns for Signal Voltage level signals.
6- In the SerDes signals, added additional rows for "No internal termination selected" and "50 ohm internal termination selected".
7- Added the LP Trust signal LP_TMP_DETECT_B.
8- Renamed "USBn_VIN_3P3" and "USBn_VIN_1P8" in note 5 and stressed the max slew rate of Dn_MVREF to 25 kv/s.
9- Updated note 9 to include "See also note 6 in Table 3".
10- Updated note 10 to include required biasing.
11- Added notes 11, 12, and 13.

• In Table 3, [Recommended operating conditions],added table note 11 and added the LP Trust signal.

• Updated Figure 7, [Overshoot/Undershoot voltage for SB_OVIN/USB_HVIN/LVIN/OVIN/MVIN/SVIN/DVIN].

• In Power sequencing, added a paragraph for VDD_LP special power sequencing.

• In Table 6 ,[T4240 Power dissipation for rev 2 silicon with Altivec power-gated off]:
1- dded 1.8 GHz power numbers.
2- Updated note 9.

• In Table 8, [T4240 Power dissipation for rev 2 silicon with Altivec enabled] :
1- Added 1.8 GHz power numbers.
2- Changed the 1667 MHz freq DDR data rate from 1867 to 1866.
3- Updated note 9.

• Added Table 7 and Table 9 for the T4241 low-power device.

• In Table 10, [T4240/T4160/T4080 rev 2 single core, single cluster low power mode power savings, 1.0 V] :
1- Added the 1.8 GHz frequency.
2- Added the T4240/T4160 and T4080 LPM20 data.
3- Updated power numbers so they are relevant to 65°C.
4- Added a note saying that these numbers are good for the T4241 device.

• In Table 11, [T4240/T4241 I/O power dissipation] :
1- Reduced the 1600 MT/s GVDD typical and max values from 3150 to 3100 and 4920 to 4900, respectively.
2- Improved the PLL_SerDes typical value from 40 to 60.
3- Added a formula for XVDD and SVDD typical power estimation rather than have multiple rows showing different SerDes configuration power.
4- Removed the note: "Maximum DDR power numbers are based on one 2-rank DIMM with 100% utilization," (previously note 5) and renumbered the notes.
5- Updated note 6 and added example.
6- Added low power devices to the table title.

• In Table 13, [SYSCLK and RTC DC electrical characteristics],included RTC clock DC specifications and updated the input capacitance data for both SYSCLK and RTC clock pins.

• In Table 14, [SYSCLK AC timing specifications], changed the maximum SYSCLK AC swing value from "TBD" to "1 x OVDD" and updated note 6.

• In "SYSCLK and RTC AC timing specifications," added Table 15, "RTC AC timing specification."

• In Real-time clock (RTC) timing, removed the 50% duty cycle requirement from the RTC period minimum.

• In Table 19, [DDRCLK DC electrical characteristics] ,changed the DDRCLK input pin capacitance typical value from 7 to 11 and removed the max value.

• In Table 20, [DDRCLK AC timing specifications] :
1- Changed the minimum DDRCLK cycle time from 5 ns to 7.5 ns.
2- Changed the maximum DDRCLK AC swing value from "TBD" to "1 x OVDD".
3- Updated note 6.

• In Table 21, [RESET Initialization timing specifications], relaxed HRESET_B signal rise/fall time to 4 SYSCLK cycles.

• In Table 29, [eSPI AC timing specifications], updated the SPI_MOSI hold time min and SPI_MOSI delay max formulas.

• Updated the tMDKHDX delay equation presentation in Table 38 and Table 39. (When MDIO_CFG[NEG] = 0 then Y = 0.5 and tMDKHDX is Y x TMDC_ClK ± 3 ns.)

• In Table 42, [IEEE 1588 AC timing specifications] :
1- Updated the TSEC_1588_CLK_IN clock period min value and removed the max value.
2- Updated the TSEC_1588_CLK_OUT clock period min value.
3- Added "hold time" to TSEC_1588_ALARM_OUT1/2.
4- Changed the TSEC_1588_TRIG_IN1/2 pulse width min value.
5- Removed notes 4 and 5 and updated notes 1 and 2.
6- Updated all note references.

• In Table 46, [Integrated flash controller DC electrical characteristics (1.8 V)]. changed VOH/VOL min and max from (0.8 x OVDD, 0.4) to (1.6 V, 0.32 V).

• In Table 55, [I2C DC electrical characteristics (DVDD = 1.8V)], changed IOL at 1.8 V from 1 mA to 3 mA.

• In "GPIO DC electrical characteristics," added Table 59, "LP_TMP_DETECT_B pin DC electrical characteristics."

• In Table 76, Table 84, and Table 111, removed the absolute output voltage limits (min -0.4 V, max 2.30 V).

• In Table 105, [SGMII transmit AC timing specifications], changed the figure reference in note 2 from Figure 43 to Figure 42.

• In Table 122, [10GBase-KR receiver AC timing specifications], added note 2 and 3 and updated all note references.

• In Table 127, [Processor, platform, and memory clocking specifications], added the 1800 MHz data columns and added note 8 to describe why FMAN might have two different minimum frequencies.

• In Table 133, [DDR data Rate to DDRCLK ratios], , changed the 133.333 MHz DDRCLK frequency example value to 1866.667.

• In Table 137, [SYSCLK and core cluster frequency options], added the 1800 MHz Core cluster: SYSCLK Ratio options.

• In Minimum platform frequency requirements for high-speed interfaces, removed the SRIO equation that shows minimum platform frequency.

• In Table 147, [Fuse Status Register (DCFG_CCSR_FUSESR)], changed the VDD voltage note for "All other values". After the table, added paragraph for if DA_ALT_V is not all zeroes.

• In PLL power supply filtering, updated the second NOTE.

• Updated Figure 53,[PLL power supply filter circuit], and Figure 54, [SerDes PLL power supply filter circuit].

• In Connection recommendations, added the expected temperature error to the non-ideality factor temperature range.

• Updated Mechanical dimensions of the FC-PBGA to include package parameters.

• In Table 149, [Part numbering nomenclature], added 16 and 08 cores to column nn and added symbol T = 1800 MHz to column C.

• In Orderable part numbers addressed by this document, added two new orderable 1.8 G parts and added T4241 part numbers.

• Updated Part marking to include low power numbers.

REASON FOR CHANGE

Notify customers with hardware spec updates.

ANTICIPATED IMPACT OF PRODUCT CHANGE(FORM, FIT, FUNCTION, OR RELIABILITY)

No impact to product form, fit, function or reliability.

NOTE:
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QUALIFICATION STATUS: N/A

QUALIFICATION PLAN:

N/A

RELIABILITY DATA SUMMARY:

N/A

ELECTRICAL CHARACTERISTIC SUMMARY:

N/A

CHANGED PART IDENTIFICATION:

N/A

ATTACHMENT(S):
External attachment(s) FOR this notification can be viewed AT:
16950_Revision_History1.pdf
