MP5416

2.8V-5.5V, Power Management IC with Four 2A/2.5A/4A/4.5A Buck Converters, 5 LDOs, And Flexible System Settings via I2C and OTP

The Future of Analog IC Technology

DESCRIPTION

The MP5416 is a complete power management solution that integrates four high-efficiency, step-down, DC/DC converters, five low-dropout regulators, and a flexible logic interface.

A constant-on-time (COT) control DC/DC converter provides fast transient response. The 1.5MHz default fixed switching frequency during continuous conduction mode (CCM) reduces the external inductor and capacitor values greatly. Full protection features include under-voltage lockout (UVLO), over-current protection (OCP), and thermal shutdown.

The output voltage is adjustable through the I^2C bus or pre-set by the one-time programmable (OTP) function. In order to determine the most optimal output voltage configurations supported by this device, refer to application note AN139. The power on/off sequence is also programmable by the OTP or can be controlled through the I^2C bus online.

The MP5416 requires a minimal number of external components and is available in a space-saving, 28-pin QFN (4mmx4mm) package.

By using I2C or OTP, users can use the MP5416 to program the buck and LDO output voltages, MODE, current limit of buck1 and buck 3, and the enable function of all the bucks and LDO (ENBUCK/LDO).

When using just I2C and no OTP, the MP5416 allows users to program current limit of buck 2 and 4, slew rate (DVS Slew rate), Discharge (DISCHG), system enable (SYSEN), and software reset (SFRST). Status and ID2 registers can also be read via I2C.

Some other features, such as AUTOON, Frequency, PWR on delay, RST delay, pushbutton time, LDORTC output voltage, OTP version, and I2C slave address can only be programmed via OTP.

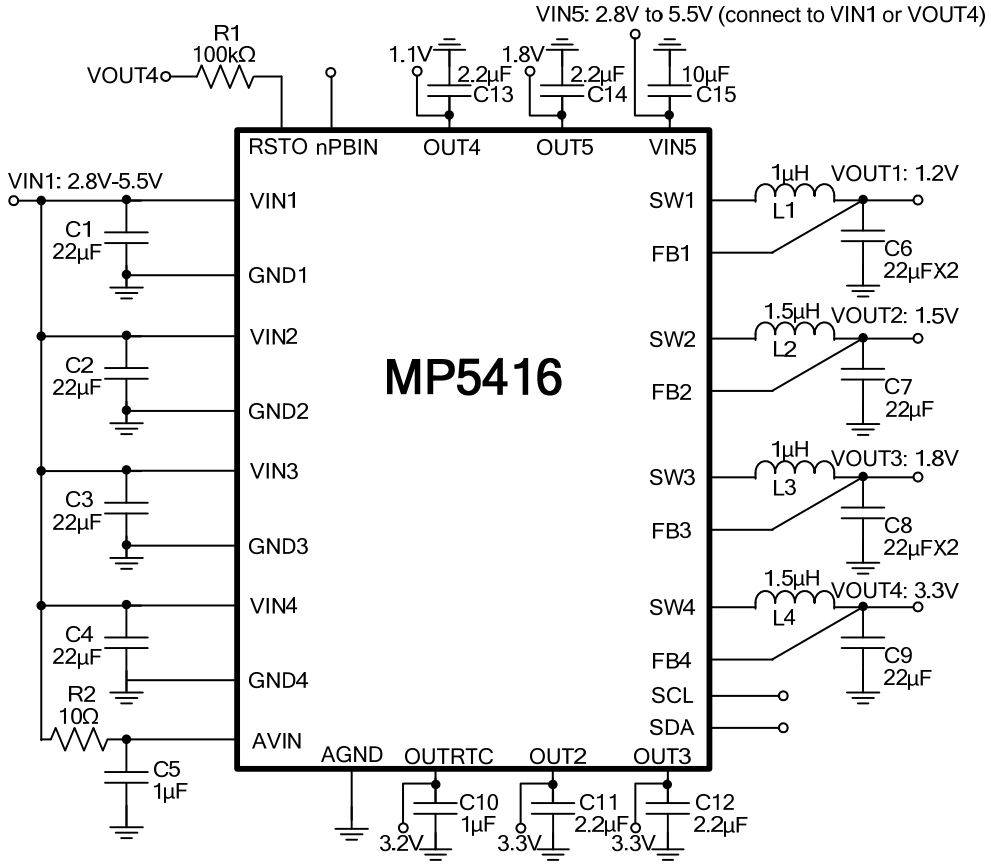
FEATURES

- Four High-Efficiency Step-Down Converters
  - Buck1: 4.5ADC/DC Converter
  - Buck2: 2.5A DC/DC Converter
  - Buck3: 4A DC/DC Converter
  - Buck4: 2A DC/DC Converter
  - 2.8V to 5.5V Operating Input Range
  - Adjustable Switching Frequency
  - Programmable Forced PWM, Auto PFM/PWM Mode
  - Hiccup Over-Current Protection (OCP)
- Five Low-Dropout Regulators
  - One RTC Dedicate LDO
  - Four Low Noise LDOs
  - Two Separate Input Power Supplies
  - 100mV Dropout at 300mA Load
- System
  - I^2C Bus and OTP
  - Power-On/-Off Button
  - Power-On Reset Output
  - Flexible Power-On/-Off Sequence via OTP
  - Flexible DC/DC, LDO On/Off via OTP
  - ±4kVHBM and ±2kV CDM ESD Rating For All Pins

APPLICATIONS

- Cable Modems, Set-Top Boxes
- Televisions
- MID, Tablets
- POS Machines
- SSD
- IP Cameras

TYPICAL APPLICATION



OTP-EFUSE SELECTED TABLE BY DEFAULT (MP5416-0000)

OTP Items	Buck1	Buck2	Buck3	Buck4	LDORTC	LDO2	LDO3	LDO4	LDO5
Output Voltage	1.2V	1.5V	1.8V	3.3V	3.2V	3.3V	3.3V	1.1V	1.8V
Initial On/Off	On	On	On	On	On	On	Off	On	On
Mode	FPWM	PFM	FPWM	FPWM	N/A				
Power-On Delay/Time Slot #	2ms/1	4ms/2	4ms/2	0ms/0	Always on	4ms/2	6ms/3	2ms/1	4ms/2
Automatic Turn-On	Yes								
Switching Frequency	1.5MHz								
Push-Button Timer	2 seconds								
RSTO Delay	10ms								
Buck 1 Peak Current Limit	6.8A								
Buck 3 Peak Current Limit	5.6A								
I^2C Slave Address	0x69								
OTP Version	0000								

ORDERING INFORMATION

Part Number*	Package	Top Marking
MP5416GR-xxxx**	QFN-28 (4mmx4mm)	*See Below*
MP5416GR-0000	QFN-28 (4mmx4mm)	*See Below*
EVKT-5416	Evaluation Kit	

* For Tape & Reel, add suffix –Z (e.g. MP5416GR-XXXX–Z)
** "xxxx" is the configuration code identifier for the register setting stored in the OTP.

The default number is "0000". Each "x" can be a hexadecimal value between 0 and F. Please work with an MPS FAE to create this unique number, even if ordering the "0000" code. MP5416GR-0000 is the default version.

TOP MARKING

MPSYWW
MP5416
LLLLLL

MPS: MPS prefix
Y: Year code
WW: Week code
MP5416: Product code
LLLLLL: Lot number

EVALUATION KIT EVKT-5416

EVKT-5416 Kit contents: (Items below can be ordered separately).

#	Part Number	Item	Quantity
1	EV5416-R-00D	MP5416GR-CCCC evaluation board	1
2	EVKT-USBI2C-02	Includes one USB to I2C dongle, one USB cable, and one ribbon cable	1
3	MP5416GR-CCCC	MP5416 IC which can be used for OTP programming	2
4	Tdrive-5416	USB flash drive that stores the GUI installation file and supplemental documents	1

Order direct from MonolithicPower.com or our distributors.

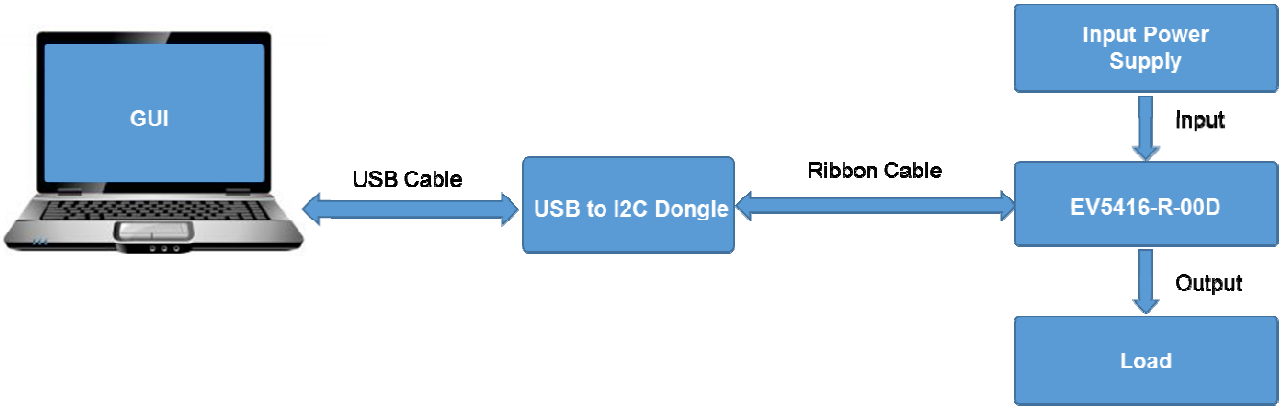
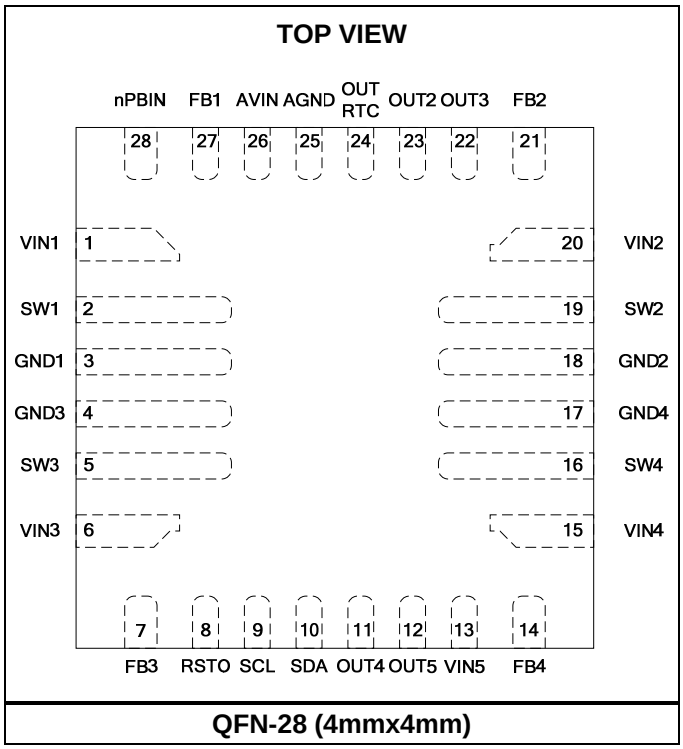


Figure 1: EVKT-5416 Evaluation Kit Set-Up

PACKAGE REFERENCE



QFN-28 (4mmx4mm)

ABSOLUTE MAXIMUM RATINGS (1)

VIN1, VIN2, VIN3, VIN4, VIN5, AVIN..... .....0.3V to 6.25V
V_{SWx}.....-0.6V (-5V for <10ns) to VIN+0.3V (7V for <10ns)
All other pins .....-0.3V to 6.25V
Continuous power dissipation (T_A = +25°C) **(2)** 2.84W
Junction temperature .....150°C
Lead temperature .....260°C
Storage temperature..... -65°C to 150°C

Recommended Operating Conditions (3)

Step-down regulator (VIN) .....2.8V to 5.5V
Step-down regulator ($V_{OUT1/3}$).....0.6V to 2.18V
Step-down regulator ($V_{OUT2/4}$).....0.8V to 3.9V
LDO regulator (V_{OUTL}) .....0.8V to 3.9V
Operating junction temp. (T_J) .. -40°C to +125°C

Thermal Resistance(4) θ_{JA} θ_{JC}

	θ_{JA}	θ_{JC}	
QFN-28 (4mmx4mm)	44	9	°C/W

NOTES:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

VIN1 = VIN2 = VIN3 = VIN4 =VIN5 =AVIN =5V, T_J = -40°C to 125°C(5), unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply current (no switching)	I_{IN}	No switching, feedback is highT_J=+25°C		350	480	μA
Default oscillation frequency	f_{SW}		1.2	1.5	1.8	MHz
Thermal shutdown entry threshold (6)	T_{OTP_R}		145	153	162	°C
Thermal shutdown recovery threshold (6)	T_{Hys}		121	130	139	°C
Step-Down Regulator						
AVIN UVLO rising	$V_{AIN1\ R}$		2.4	2.55	2.7	V
AVIN UVLO hysteresis	$V_{AIN1\ HYS}$			300		mV
VIN1 UVLO rising	$V_{IN1\ R}$		2.3	2.45	2.6	V
VIN1 UVLO hysteresis	$V_{IN1\ HYS}$			300		mV
VIN2 UVLO rising(7)	$V_{IN2\ R}$		2.3	2.45	2.6	V
VIN2 UVLO hysteresis(7)	$V_{IN2\ HYS}$			300		mV
VIN3 UVLO rising	$V_{IN3\ R}$		2.3	2.45	2.6	V
VIN3 UVLO hysteresis	$V_{IN3\ HYS}$			300		mV
VIN5 UVLO rising	$V_{IN5\ R}$		2.3	2.45	2.6	V
VIN5 UVLO hysteresis	$V_{IN5\ HYS}$			300		mV
Feedback voltage accuracy	V_{FB1}	Default output of Buck1	1.1820	1.2	1.2180	V
	V_{FB2}	Default output of Buck2	1.4775	1.5	1.5225	V
	V_{FB3}	Default output of Buck3	1.7730	1.8	1.8270	V
	V_{FB4}	Default output of Buck4	3.2505	3.3	3.3495	V
Maximum duty cycle	D_{max}	CH2 and CH4 only		100		%
Buck1, Buck3 (4.5A/4A)						
HS switch on resistance	$HS_{RDS-ON1}$	500mA, T_J=+25°C	20	30	40	mΩ
	$HS_{RDS-ON3}$					
	$HS_{RDS-ON1}$	500mA, T_J = -40°C to 125°C	10	30	50	mΩ
	$HS_{RDS-ON3}$					
LS switch on resistance	$LS_{RDS-ON1}$	500mA, T_J=+25°C		12	16	mΩ
	$LS_{RDS-ON3}$					
	$LS_{RDS-ON1}$	500mA, T_J = -40°C to 125°C		12	20	mΩ
	$LS_{RDS-ON3}$					
Switch leakage1	HSW_{ILK1}	EN=0V, VIN=5.5V, SW=0V or 5.5V, T_J=+25°C		0	1	μA
	HSW_{ILK3}					
Switch leakage2	LSW_{ILK1}	EN=0V, VIN=5.5V, SW=0V or 5.5V, T_J=+25°C		0	1	μA
	LSW_{ILK3}					
High-side current limit	I_{LIMIT1}	Under 20% duty cycle, T_J=+25°C	5.5	6.8	8.3	A
	I_{LIMIT3}		4.5	5.6	7	A

ELECTRICAL CHARACTERISTICS *(continued)*

VIN1 = VIN2 = VIN3 = VIN4 =VIN5 =AVIN =5V, T_J = -40°C to 125°C[5], unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Minimum on time[8]	t_{ON_MIN1}			40		ns
	t_{ON_MIN3}			33		ns
Minimum off time[8]	t_{OFF_MIN1}			120		ns
	t_{OFF_MIN3}			120		ns
Output discharge resistance	R_{O_DIS1}			7		Ω
Soft-start time	t_{SS_B1}	V_{OUT}=10% to 90%		450		µs
	t_{SS_B3}	V_{OUT}=10% to 90%		450		µs
Buck2, Buck4 (2.5A/2A)						
HS switchon resistance	$HS_{RDS-ON2}$	500mA, T_J=+25°C	35	50	65	mΩ
	$HS_{RDS-ON4}$					
	$HS_{RDS-ON2}$	500mA, T_J = -40°C to 125°C	20	50	80	mΩ
	$HS_{RDS-ON4}$					
LS switchon resistance	$LS_{RDS-ON2}$	500mA, T_J=+25°C		65	80	mΩ
	$LS_{RDS-ON4}$					
	$LS_{RDS-ON2}$	500mA, T_J = -40°C to 125°C		65	105	mΩ
	$LS_{RDS-ON4}$					
Switch leakage3	HSW_{ILK2}	Shutdown, VIN=5.5V, SW=0V or 5.5V, T_A=+25°C		0	1	µA
	HSW_{ILK4}					
Switch leakage 4	LSW_{ILK2}	Shutdown, VIN=5.5V, SW=0V or 5.5V, T_A=+25°C		0	1	µA
	LSW_{ILK4}					
High-side current limit	I_{LIMIT2}	Under 20% duty cycle, T_J=+25°C	3	4.2	5.4	A
	I_{LIMIT4}					
Minimum on time[8]	t_{ON_MIN2}			32		ns
	t_{ON_MIN4}			32		ns
Minimum off time[8]	t_{OFF_MIN2}			100		ns
	t_{OFF_MIN4}			100		ns
Output discharge resistance	R_{O_DIS2}			7		Ω
Soft-start time	t_{SS_B2}	V_{OUT}=10 to 90%		450		µs
	t_{SS_B4}	V_{OUT}=10 to 90%		450		µs
10mA RTC LDO						
Default output voltage	V_{RTC_LDO}	I_{OUT}=10mA, power on state	3.104	3.2	3.296	V
Ground current	I_{Q_RTC}	No load		6.5		µA
Dropout voltage[8]	V_{DROP1}	V_{OUT}=3V, I_{OUT}=10mA		100		mV
Current limit	I_{LIM_RTC}	VIN=3.3V, V_{OUT} drops 33%, T_J=+25°C	25	55	85	mA
Soft-start slew rate	τ_{SS_RTC}	V_{OUT}=10% to 90%, C_{OUT}=1µF		35		mV/µs

ELECTRICAL CHARACTERISTICS *(continued)*

VIN1 = VIN2 = VIN3 = VIN4 =VIN5 =AVIN =5V, T_J = -40°C to 125°C[5], unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Low Dropout (LDO) Regulator: LDO2 to LDO5						
Output voltage	V_{LDO2}		3.2340	3.30	3.3660	V
	V_{LDO3}		3.2634	3.33	3.3966	V
	V_{LDO4}		1.0780	1.10	1.1220	V
	V_{LDO5}		1.7730	1.80	1.8270	V
PSRR[8]	$PSRR_{1k}$	F=1kHz, 100mA, V_{OUT}=1.8V		47		dB
	$PSRR_{10k}$	F=10kHz, 100mA, V_{OUT}=1.8V		51		dB
Dropout voltage	V_{DROP1}	V_{OUT}=3V, I_{OUT}=300mA		100		mV
Current limit	$I_{LIMIT\ LDO}$	VIN=3.3V, V_{OUT} drops 33%	320	430	640	mA
Output discharge resistance	$R_{O\ DIS2}$			7		Ω
Soft-start time	t_{SS_B2}	V_{OUT}=10% to 90%, C_{OUT}=2.2μF		70		μs
Line regulation		VIN2=VIN5=2.8V to 5.5V		0.3		%/V
Load regulation		VIN2=VIN5=3.3V, $I_{OUT}$from 10mA to 100mA		0.5		%
Logic Pins						
nPBIN pull-up current	I_{PBIN}	Internal pull-up to AVIN	5	9	13	μA
Push-button detect threshold	V_{PB}		500	700	900	mV
Manual reset threshold	V_{MS}	Npbin pulls low, T_J=+25°C			50	mV
RSTO rising threshold	$V_{RSTO\ R}$	Monitor Buck4's output		90%		V_{FB4}
RSTO falling threshold	$V_{RSTO\ F}$			80%		V_{FB4}
RSTO rising delay	T_{RSTO}	Adjustable through I^2C/OTP		10		ms
I^2C Interface Specifications[9]						
Input logic high	V_{IH}		1.4			V
Input logic low	V_{IL}				0.4	V
Output voltage logic low	$V_{OUT\ L}$	RSTO pin sink 4mA			0.4	V
SCL clock frequency	f_{SCL}				3.4	MHz
SCL high time	t_{HIGH}		60			ns
SCL low time	t_{LOW}		160			ns
Data setup time	$t_{SU.DAT}$		10			ns
Data hold time	$t_{HD.DAT}$			70		ns
Setup time for repeated start	$t_{SU.STA}$		160			ns
Hold time for repeated start	$t_{HD.STA}$		160			ns
Bus free time between a start and a stop condition	t_{BUF}		160			ns
Setup time for stop condition	$T_{SU.STO}$		160			ns
Rise time of SCL and SDA	t_R		10		300	ns

ELECTRICAL CHARACTERISTICS *(continued)*

VIN1 = VIN2 = VIN3 = VIN4 =VIN5 =AVIN =5V, T_J = -40°C to 125°C(5), unless otherwise noted.

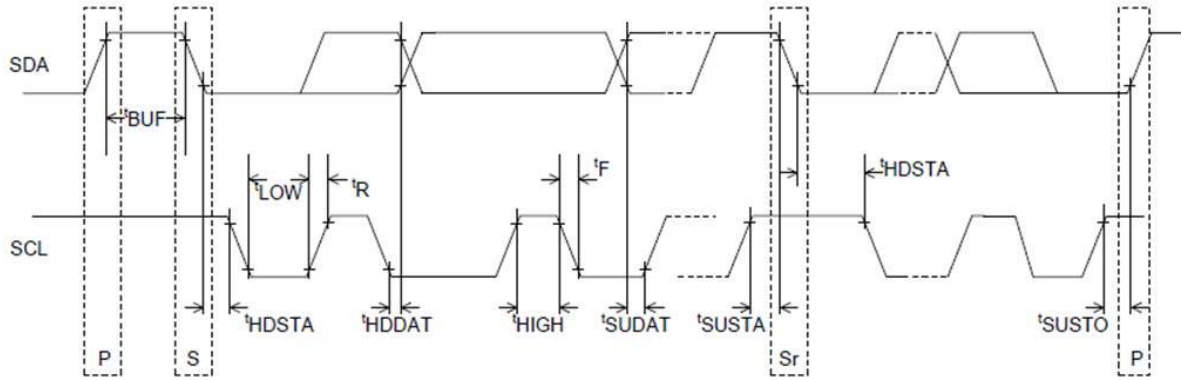
Parameter	Symbol	Condition	Min	Typ	Max	Units
Fall time of SCL and SDA	t_F		10		300	ns
Pulse width of suppressed spike	t_{SP}		0		50	ns
Capacitance bus for each bus line	C_B				400	pF
SCL low time	t_{LOW}		160			ns

NOTES:

5) Not tested in production, guaranteed by over-temperature correlation.
6) Guaranteed by design.
7) VIN2 and VIN4 share the same UVLO. It is recommended to connect VIN2 and VIN4 together in practical application.
8) Guaranteed by engineering sample characterization.
9) Refer to below I^2C timing chart when reading the I^2C interface specifications.

It is recommended to begin operating the I^2C function after the power-on sequence is finished or RSTO switches high.

TIMING DIAGRAM

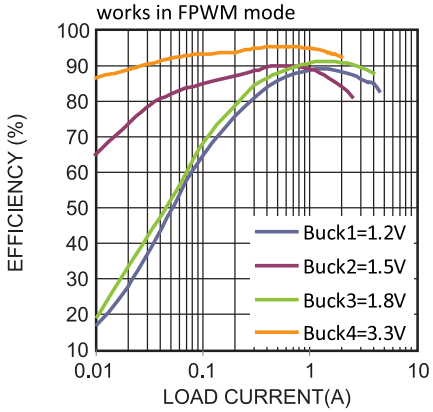


TYPICAL CHARACTERISTICS

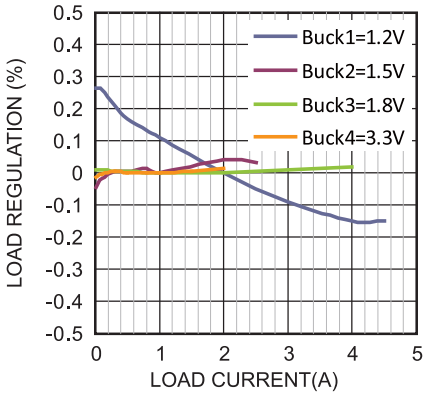
Performance waveforms are tested on the evaluation board.
VIN = 5V, T_A = 25°C, test using default spec parts, unless otherwise noted.

Efficiency

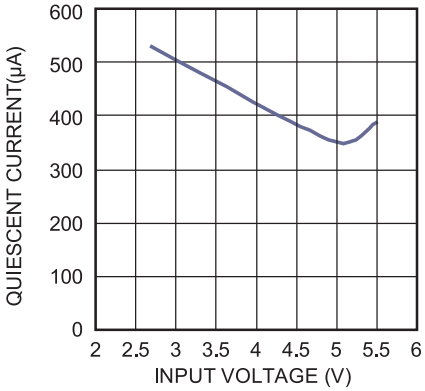
Buck1 and Buck3
works in FPWM mode



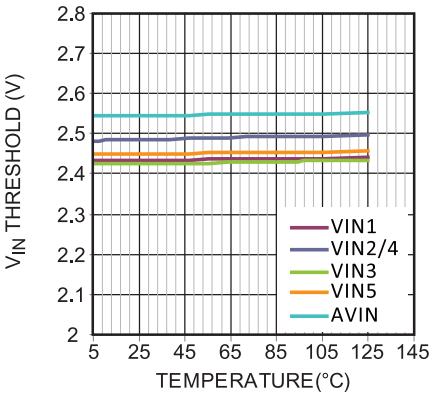
Load Regulation



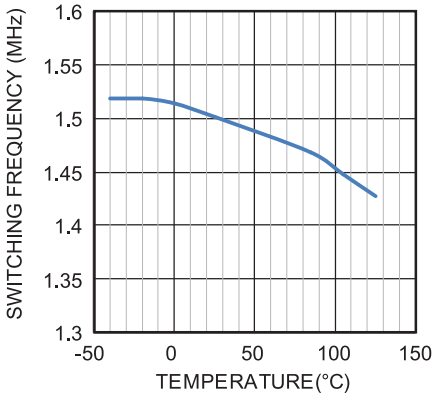
Quiescent Current vs. Input Voltage



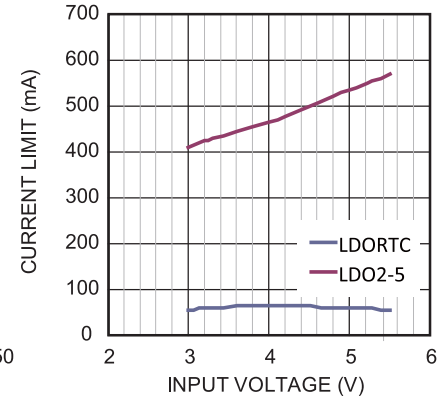
V_{IN} Threshold vs. Temperature



Switching Frequency vs. Temperature

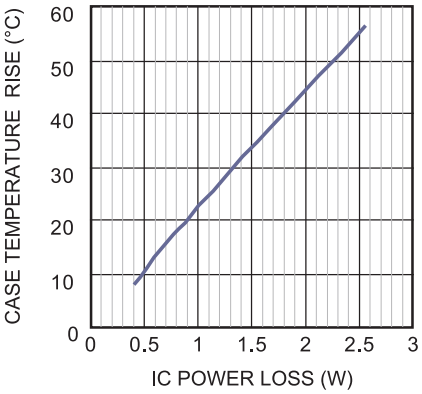


Current Limit vs. Input Voltage



IC Power Dissipation vs. Case Temperature Rise

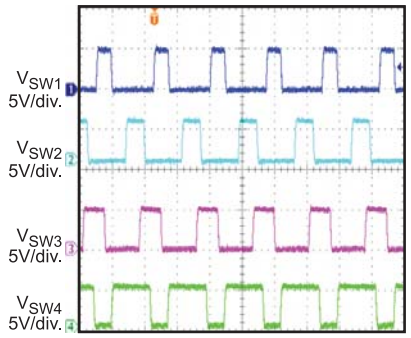
Tested on four layer PCB (9.3cm×8.5cm)



TYPICAL PERFORMANCE CHARACTERISTICS

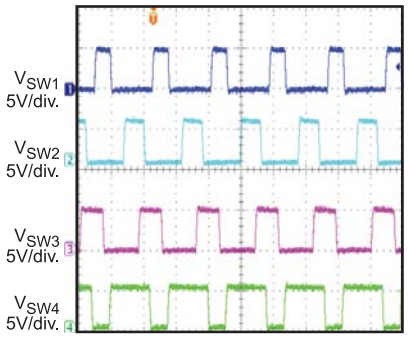
Performance waveforms are tested on the evaluation board.
VIN = 5V, T_A = 25°C, test using default spec parts, unless otherwise noted.

Steady State
Each Channel Buck with Half Load



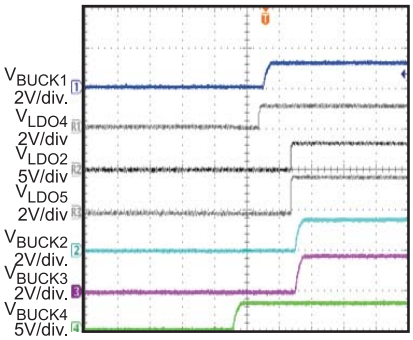
400ns/div.

Steady State
Each Channel Buck with Full Load



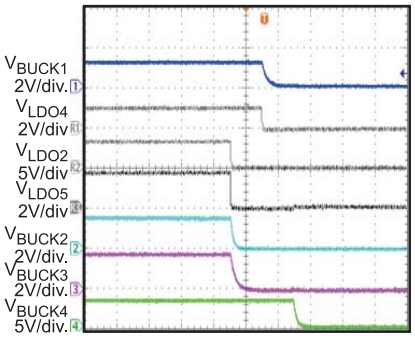
400ns/div.

nPBIN Power On
Each Channel Buck without Load



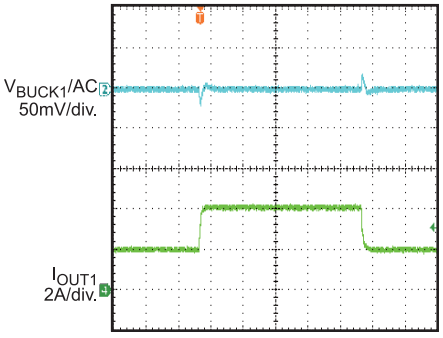
2ms/div.

nPBIN Power off
Each Channel Buck without Load



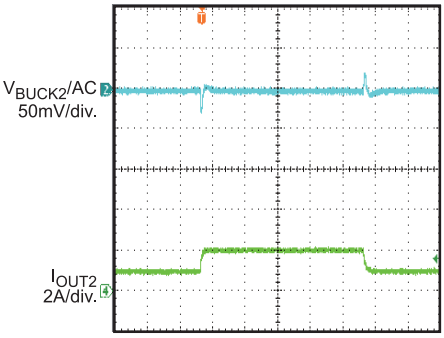
2ms/div.

Load Transient Response
I_{OUT} Transient from 2A to 4A,
Slew Rate=0.8A/μs.



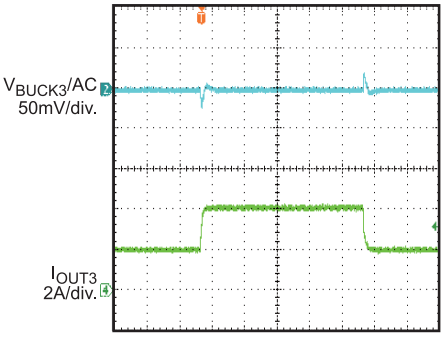
100μs/div

Load Transient Response
I_{OUT} Transient from 1A to 2A,
Slew Rate=0.8A/μs.



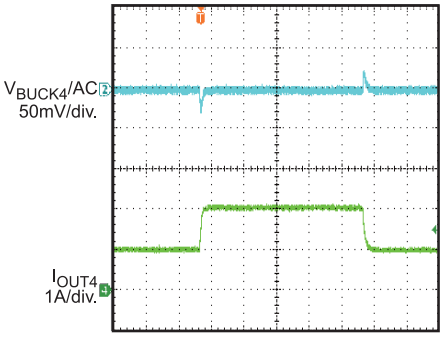
100μs/div

Load Transient Response
I_{OUT} Transient from 2A to 4A,
Slew Rate=0.8A/μs.



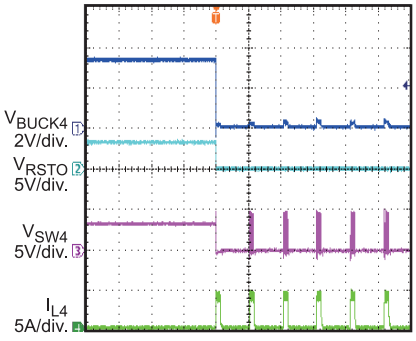
100μs/div

Load Transient Response
I_{OUT} Transient from 1A to 2A,
Slew Rate=0.8A/μs.



100μs/div

SCP Entry
Buck-4 Output 3.3V

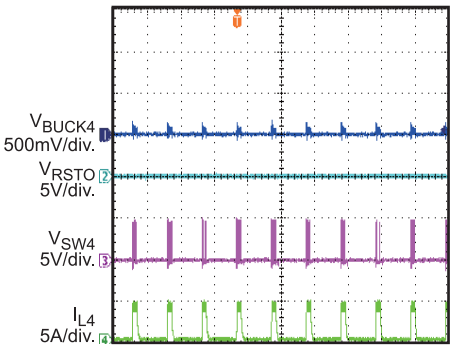


1ms/div

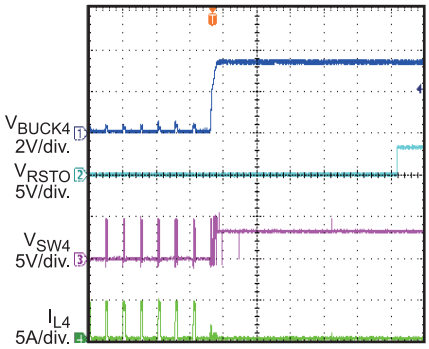
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board.
VIN = 5V,T_A= 25°C,test using default spec parts, unless otherwise noted.

SCP Steady State
Buck-4 Output 3.3V



SCP Recovery
Buck-4 Output 3.3V



PIN FUNCTIONS

Package Pin #	Name	Description
1	VIN1	**Supply voltage input of Buck1.** The MP5416 operates from a 2.8Vto5.5V input rail. A ceramic capacitor is required to decouple the input rail. Connect VIN1 using a wide PCB trace. VIN1, VIN2, VIN3, VIN4, and AVIN must be connected to the same bus voltage.
2	SW1	**Buck 1 switch output.** Connect SW1 using a wide PCB trace.
3	GND1	**Power ground of Buck1.**GND1 requires special consideration during PCB layout. Connect GND1 to GND with copper traces and vias.
4	GND3	**Power ground of Buck3.**GND3 requires special consideration during PCB layout. Connect GND3 to GND with copper traces and vias.
5	SW3	**Buck 3 switch output.** Connect SW3 using a wide PCB trace.
6	VIN3	**Supply voltage input of Buck3.** The MP5416 operates from a 2.8Vto5.5V input rail. A ceramic capacitor is required to decouple the input rail. Connect VIN3 using a wide PCB trace.
7	FB3	**Feedback of Buck3.**Connect the output of Buck3 to FB3 directly.
8	RSTO	**Reset output from the PMIC to the CPU.** The 3.3V (Buck4) output is ready after the RSTODELAY timer on RSTO goes high. RSTO is an open-drain output and needs an external pull-up resistor.
9	SCL	**I^2C clock signal input.** SCL needs an external resistor pulled up to AVIN if the I^2C function is unused.
10	SDA	**I^2C data.**SDA needs an external resistor pulled up to AVIN if the I^2C function is unused.
11	OUT4	**LDO4 output.** LDO4is powered by VIN5.
12	OUT5	**LDO5 output.** LDO5is powered by VIN5.
13	VIN5	**Power input of LDO4 and LDO5.**
14	FB4	**Feedback of Buck4.**Connect the output of Buck 4to FB4 directly.
15	VIN4	**Supply voltage input of Buck4.** The MP5416 operates from a 2.8Vto5.5V input rail. A ceramic capacitor is required to decouple the input rail. Connect VIN4 using a wide PCB trace.
16	SW4	**Buck 4 switch output.** Connect SW4 using a wide PCB trace.
17	GND4	**Power ground of Buck4.**GND4 requires special consideration during PCB layout. Connect GND4 to GND with copper traces and vias.
18	GND2	**Power ground of Buck2.**GND2 requires special consideration during PCB layout. Connect GND2 to GND with copper traces and vias.
19	SW2	**Buck 2 switch output.** Connect SW2 using a wide PCB trace.
20	VIN2	**Supply voltage input of Buck2, LDORTC, LDO2, and LDO3.**The MP5416 operates from a 2.8Vto5.5V input rail. A ceramic capacitor is required to decouple the input rail. Connect VIN2 using a wide PCB trace.
21	FB2	**Feedback of Buck2.**Connect the output of Buck 2 to FB2 directly.
22	OUT3	**LDO3 output.** LDO3is powered by VIN2.
23	OUT2	**LDO2 output.** LDO2is powered by VIN2.
24	OUTRTC	**RTC LDO output.** This LDO is powered by VIN2. Set a high enough output voltage to achieve a lower voltage gap between VIN2 to OUTRTC.
25	AGND	**Analog ground.** Connect AGND to power ground.

PIN FUNCTIONS*(continued)*

Package Pin #	Name	Description
26	AVIN	**Power supply input for logic circuitry.** Bypass AVIN with a 0.1μF-1μF ceramic capacitor to AGND. Connect AVIN to the system input.
27	FB1	**Feedback of Buck1.**Connect the output of Buck 1 to FB1 directly.
28	nPBIN	**Push-button input.** nPBIN is a logic input pin to start up or shut down the device. A logic low over a pre-set deglitch time must be applied to nPBIN. nPBIN has a weak internal pull-up current.

BLOCK DIAGRAM

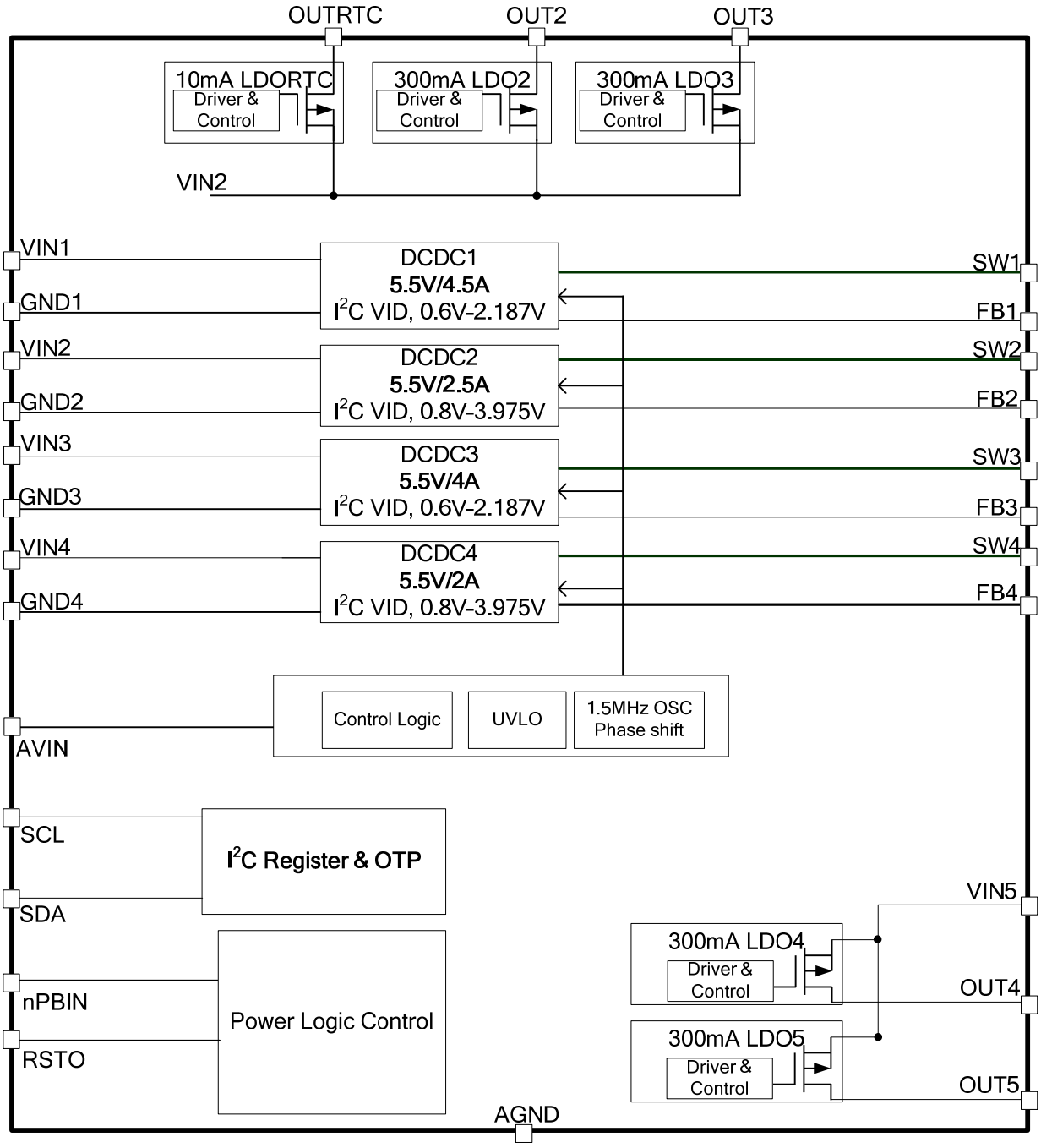


Figure 1: Functional Block Diagram

OPERATION

The MP5416 provides a complete power management solution for many 5V systems, such as televisions, SSD, STB, and so on. The MP5416integrates 4-channel, high-frequency, synchronous, rectified, step-down, switch-mode converters and 5-channel, low-dropout regulators. The MP5416reduces component count and PC board space greatly. The MP5416can manage the power system either for a 1-cell Li+ or a 5V regulated input voltage, allowing for greater flexibility of the system design.

The I^2C and one-time programmable (OTP) interface provide adjustable default output voltage and dynamic voltage scaling. In order to determine the most optimal output voltage configurations supported by this device, refer to application note AN139. The I^2C also provides powerful logic functions. See the Register Map on page 28for more detail.

1. Power Control

1.1 State Machine Diagram

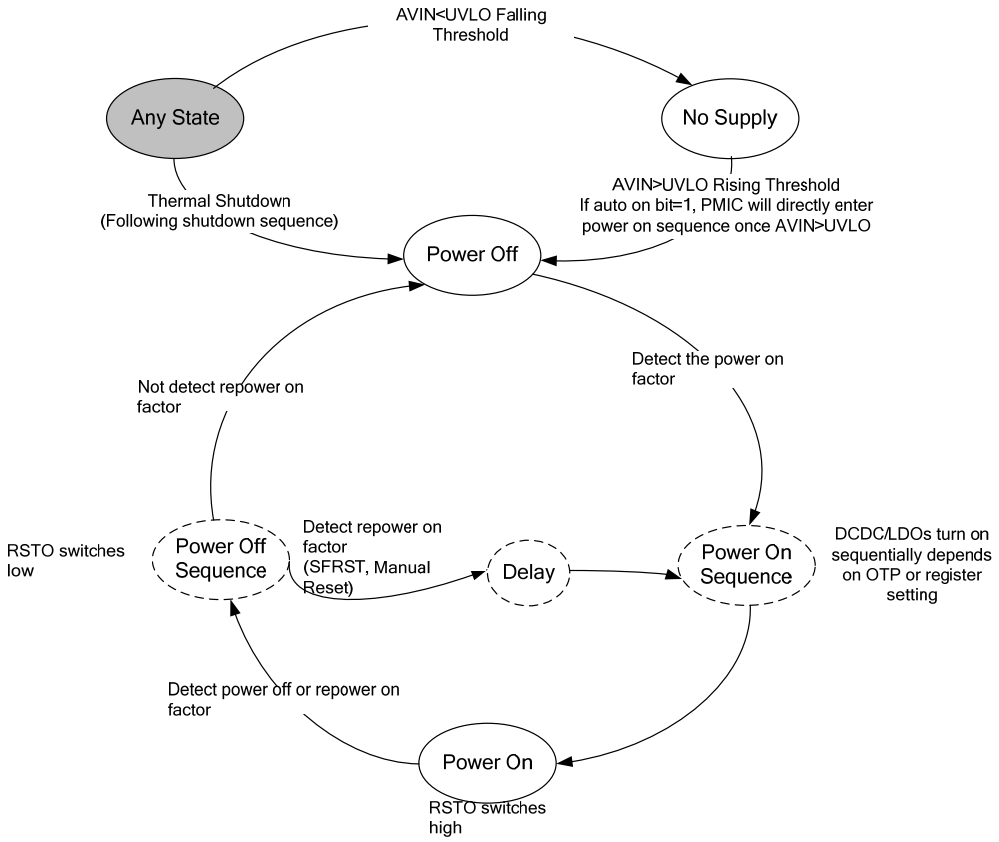


Figure 2: Power Control State Machine Diagram

State Machine Description

The state machine (shown in Figure 2) has the following features.

No Supply

The PMIC's input pin has an under-voltage lockout (UVLO) detection circuit. If the input voltage (AVIN) is lower than the UVLO rising threshold, the PMIC's functions are disabled.

Power Off

If the AUTOON bit=0, when AVIN is higher than its rising UVLO threshold, PMIC first enters a power-off state. In this state, the PMIC is always monitoring the power-on factor. Once

the power-on factor is detected, it changes to the power-on sequence state.

Power-On Sequence

DC/DC converters and LDO regulators turn on sequentially according to the pre-programmed order by the OTP eFuse.

Power-On

DC/DC converters and LDO regulators are turned on. The RSTO output switches high. In this state, the PMIC always monitors the power-off or repower-on factors.

Power-Off Sequence

The PMIC enters the power-off sequence when it detects the power-off or repower-on factors in the power-on state. RSTO is first switched low, and then the DC/DC converters and LDO regulators turn off sequentially in the reverse order of the power-on sequence. For repower-on condition(software control), after the power-off sequence is completed, the PMIC enters the power-on sequence automatically after a delay timer.

Shutdown Event

If the PMIC detects that the input voltage is lower than the UVLO falling threshold (enter no supply state) or over-temperature protection is triggered (enter power off state), the PMIC switches to no supply state or power-off state, regardless of the current state.

NOTE: If PMIC enters power-off state due to over-temperature protection triggering, LDORTC is off.

1.2 Power-On Factor

The PMIC has following power-on factors.

SYSEN

SYSEN is one data bit in the I^2C register. If the SYSEN bit is set to 1, the system changes from a power-off state to a power-on sequence. SYSEN can be set from 0 to 1by two different methods: first by setting the AUTOON bit to1 by the OTP, and the system auto-loads the AUTOON bit into SYSEN when the input voltage crosses the UVLO threshold, and second by the push button initiating a power on.

nPBIN_ON

nPBIN_ON includes two kinds of push button events. If nPBIN is pulled to logic low (but is not pulled to ground) and asserts low for longer than two seconds, the PMIC treats this as a power-on factor. In the power-off state, if nPBIN is pulled to ground (below the manual reset threshold) and asserts more than 30ms of max debounce time, the PMIC also treats this as a power-on factor. The SYSEN bit is set high when any of above nPBIN-initiated power-on events are detected.

Thermal Recovery

If the MP5416is in a power-off state due to the die temperature exceeding the thermal protection threshold, the PMIC enters a power-on sequence when the die's temperature decreases.

1.3 Power-On Sequence

There are eight slots of power-on sequence timing (see Figure 3). All the DC/DC converters and LDO regulators (except RTCLDO) can be programmed to time slots 0 to 7 by the OTP eFuse. The delay time between each time slot is related with the default switching frequency of MP5416 (see Table 1).

Table1: Slot Time Interval vs. Default Switching Frequency

Default Switching Frequency	Time Delay between Each Slot
1.0MHz	3ms
1.5MHz	2ms
2.0MHz	1.5ms
2.5MHz	1.2ms

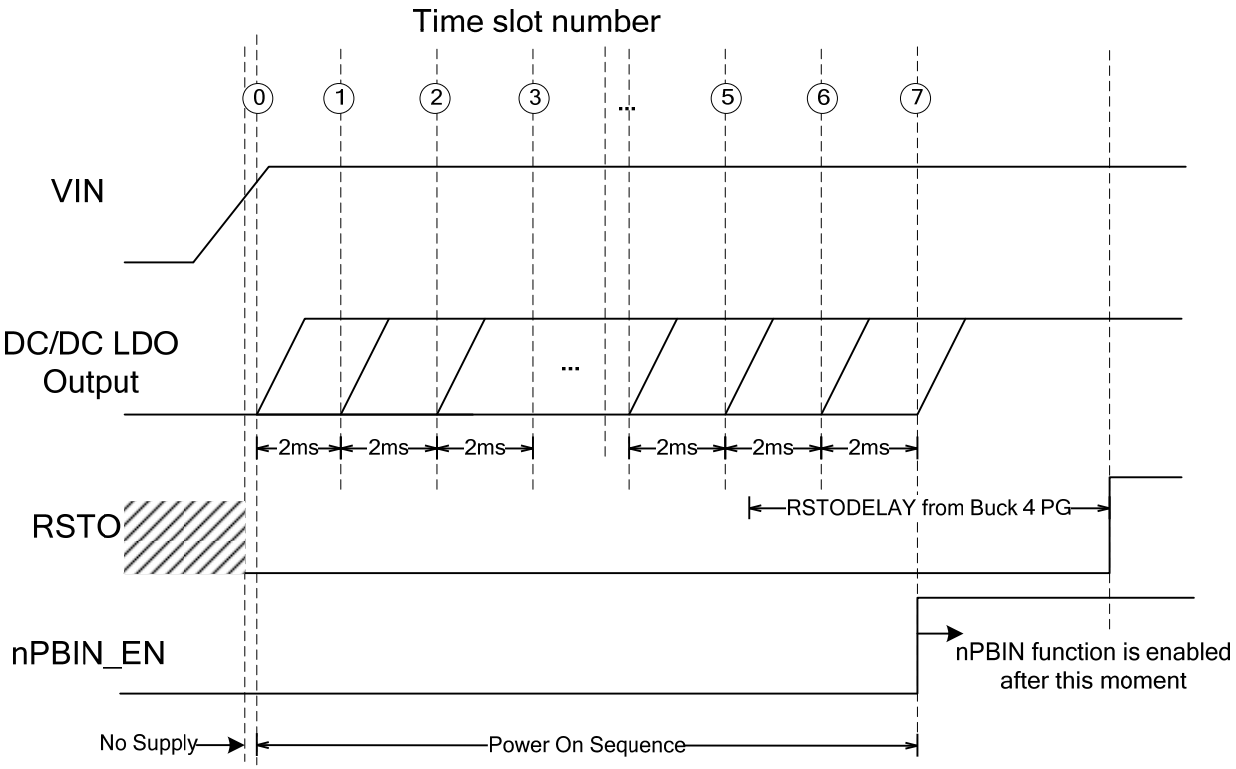


Figure 3: Power-On Sequence(Auto-On Bit Is Setto 1)

1.3.1 OUTRTC ON

OUTRTC LDO is always on if both VIN2 and AVIN are higher than their respective UVLO rising thresholds, regardless of any other pin's status. OUTRTC turns off if either VIN2 or AVIN falls below their respective UVLO falling thresholds or thermal shutdown is triggered.

1.3.2 Other Buck Regulators and LDOs On

The MP5416 provides a programmable power-on sequence. Once the power-on sequence is fixed, the power-off sequence is reversed. The OTP configuration table on page 25 shows the bits to set the time slot number for each channel.

1.4 Power-Off Factor

nPBIN_Long_Press

If nPBIN is pulled to logic low (but not pulled to ground) and asserts longer than eight seconds, the PMIC enters the power-off sequence.

nPBIN_Short_Press

If nPBINis pulled to GND(below the manual reset threshold) and lasts longer than 30ms of maximum debounce time, the PMIC enters the power-off sequence after 8msof delay time (see Figure 6).

SYSEN(Software-Initiated Power-Off)

The MP5416 supports a software-controlled power-off through the I^2C interface. SYSEN is one data bit in the I^2C register. If the SYSEN bit is set to 0, the system enters a power-off sequence. The nPBIN function or toggle input power supply method are needed to make the PMIC restart again.

1.4.1 Power-Off Sequence

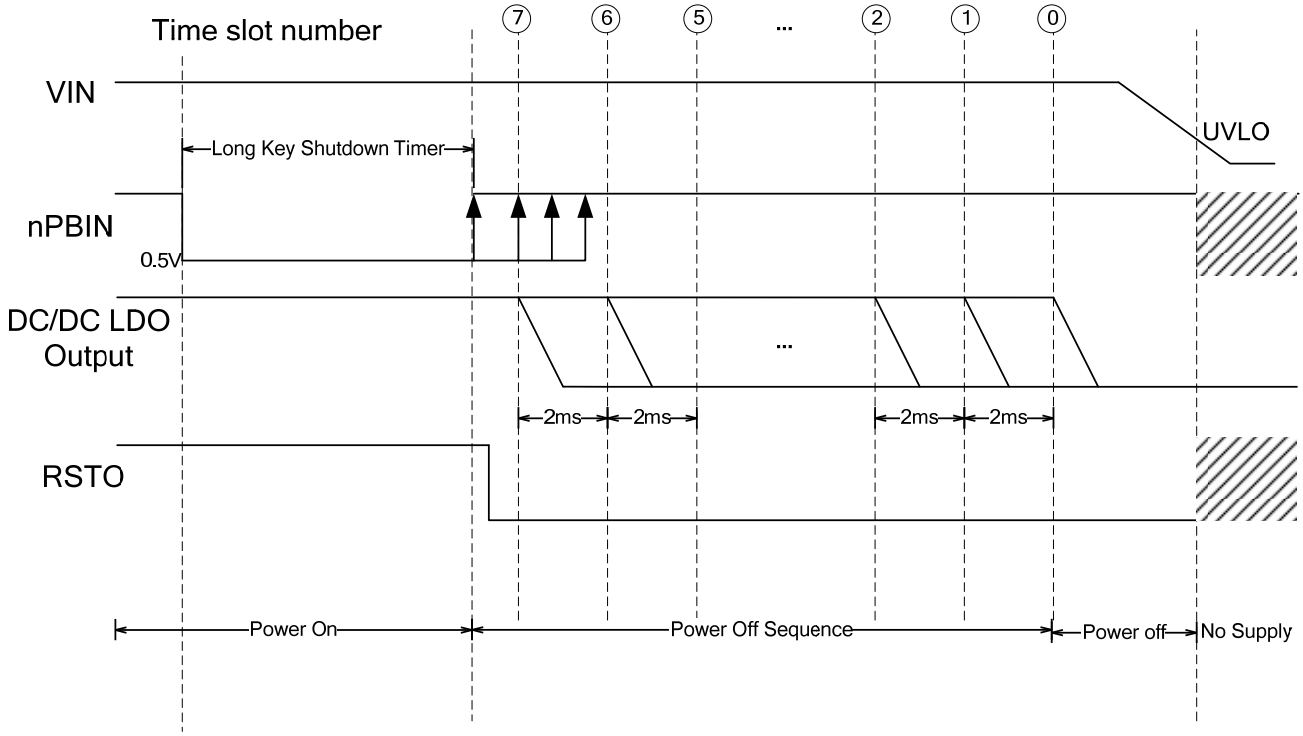


Figure 4: Power off Sequence by nPBIN Key Press

RSTO is pulled low before the DC/DC converter or LDO regulator turns off (see Figure 4). The DC/DC converter and LDO regulator power-off sequence is in the reverse order of the power-on sequence.

1.5 Repower-On Factor

Manual_Reset

nPBIN is pulled to ground (below the Manual Reset Threshold) for longer than 30ms of maximum debounce time and is released after a while (see Figure 6).

SFRST

Software reset. If the SFRST bit is set to1 through the I^2C interface, the system detects this as a repower-on factor.

1.6 Repower-On Sequence (Software-Initiated Power Cycle)

The MP5416 supports a software-controlled power reset through the I^2C interface or a manual reset push button.

When using the software-controlled method, the SFRST bit is set high. TheMP5416 waits for 8ms and powers off the system, and powers on the all the power rails again after a 60ms delay. The SFRST bit is reset to 0automatically by the RSTO rising edge. After the SFRST bit is reset to 0, the software can control power cycle again. There power-on factor detection is blocked during the repower-on period (t1 to t2) (see Figure 5).

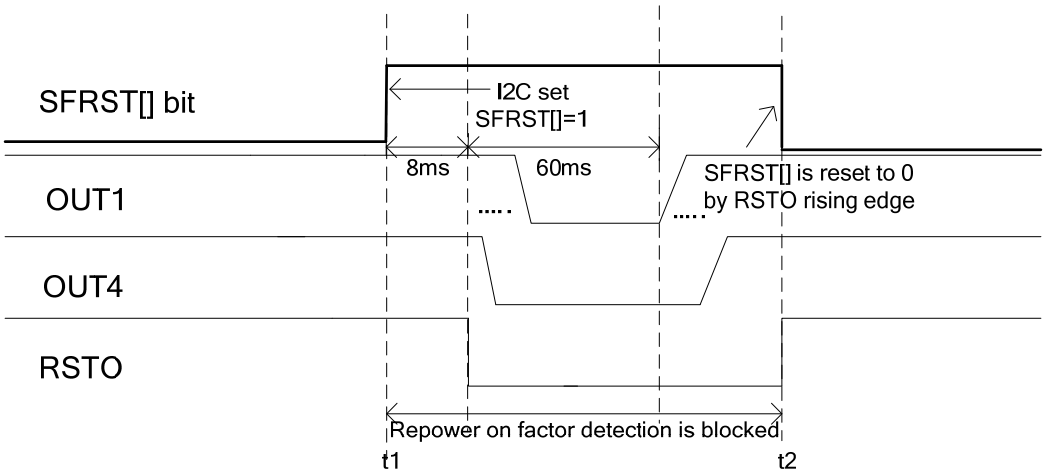


Figure 5:Repower-On Sequence(Software Control)

When using the manual reset control method, if the PMIC is working in a power-on state, once the manual reset button is pressed down, the PMIC enters a power-off sequence after 30ms of maximum debounce time and 8ms of delay, and remains in the power-off state until the manual reset button is released. After 30ms of debounce time, the PMIC enters the power-on sequence again, and the manual reset function is also completed (see Figure 6).

1.7 Shutdown Sequence

When the input voltage is lower than the UVLO falling threshold or the IC is over-temperature, the PMIC enters the shutdown sequence directly. All DC/DC converters and LDO regulators turn off at the same time (see Figure 7).

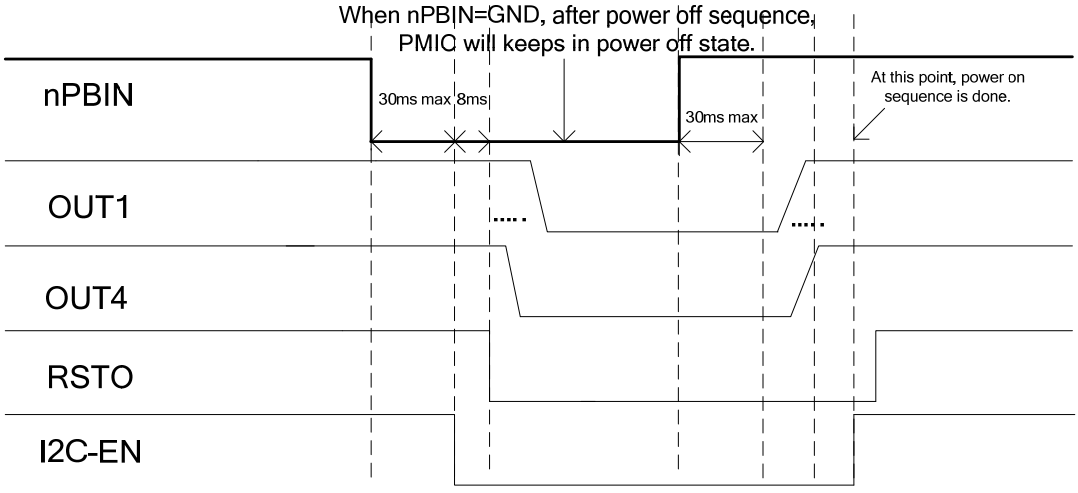


Figure 6: Repower-On Sequence (Manual Reset Control)

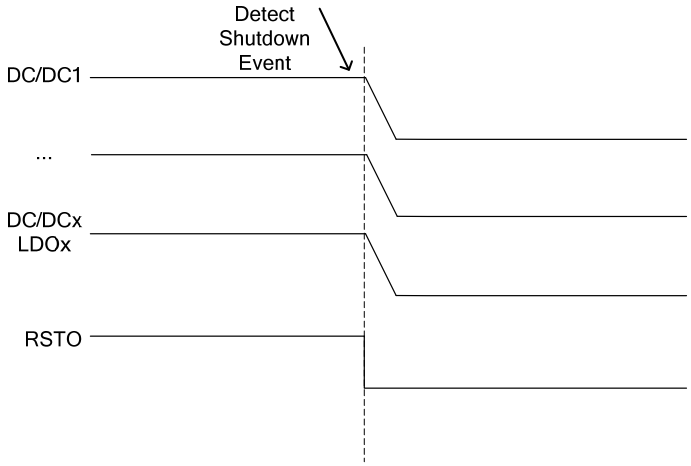


Figure 7: Shutdown Sequence

2. High Efficiency Buck Regulator

Buck1 to Buck4 are synchronous, step-down, DC/DC converters with built-in UVLO, soft-start, compensation, and hiccup current limit protection. Fixed-frequency constant-on-time (COT) control provides fast transient response. The switching clock is phase-shifted from Buck1 to Buck4 during continuous conduction mode (CCM) operation. Buck2 and Buck4 support 100% duty cycle mode.

Power Supply and UVLO

VIN1 is the power supply of Buck1. VIN2 is the power supply of Buck2, LDORTC, LDO2, and LDO3. VIN3 is the power supply of Buck3. VIN4 is the supply of Buck4. VIN5 is the power supply of LDO4 to LDO5.AVIN is power input to the bias internal logic blocks.

VIN1, VIN3, VIN5, and AVIN have their own UVLO threshold with a proper hysteresis.VIN2 and VIN4 share the same UVLO threshold. Once AVIN ramps up and exceeds the UVLO rising threshold, the nPBIN logic is enabled and ready to accept start-up and shutdown commands. LDORTC is active once VIN2 exceeds the rising threshold. Before the power key turn-on, the input shutdown current is typically 15μA.

Internal Soft Start (SS)

The soft-start (SS) function is implemented to prevent the PMIC output voltage from overshooting during start-up. When the PMIC starts up, the internal circuitry of each power rail generates a soft-start voltage that ramps up from 0V. The soft-start period lasts until the voltage on the soft-start capacitor exceeds the reference voltage. At this point, the reference voltage takes over. For four channel buck outputs, their soft-start times are fixed internally at 450μs.For the LDO2-LDO5 outputs, their soft-start times are fixed at 70μsinternally.For LDORTC, the soft-start slew rate is consistent at 35mV/μs.

Output Discharge

To discharge the energy of the output capacitor during a power-off sequence, there is an active discharge path from the DC/DC converters and LDO regulators output to ground. The discharge path is turned on when the corresponding channel is disabled. The typical discharge resistance is 7Ω. The discharge function can be enabled or disabled through the I^2C interface.

3. System Control Signals

3.1 nPBIN Functions

nPBIN is a multi-function pin that supports push-button detection and manual reset functions. There is an internal pull-up current to pull up nPBIN's voltage to AVIN. TheMP5416distinguishesbetweenthe push-button and manual reset functions by the different pull-low resistances. Connect nPBIN to ground for a manual reset function. Connect nPBIN to ground through a 49.9kΩ resistor to generate a push-button signal.

A push-button event and manual reset event can both generate an interrupt signal and set

the corresponding interrupt bit high. See the Status2 register on page 31 for details.

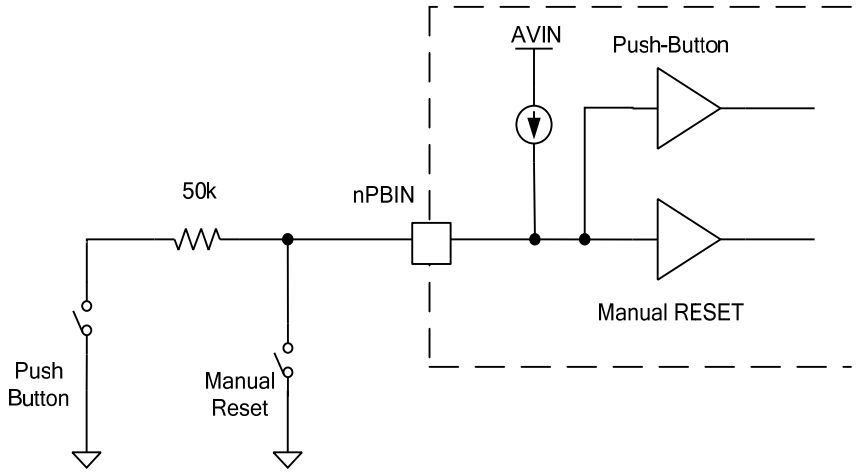


Figure 8: nPBIN Functional Block Diagram

3.1.1 Push Button Control

Long Press1/Start-Up

When PMIC is in the power-off state, if AVIN is higher than the UVLO threshold, and the push button is asserted low for more than two seconds, the power-on sequence begins. The power-on sequence must be completed before the backside CPU can take over control. The power-on sequence complete signal is RSTO switching high (see Figure 9).

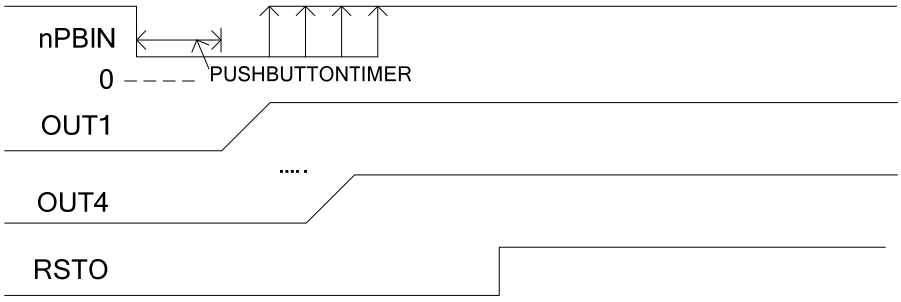


Figure 9: nPBIN Push Button Long Press1: Start-Up

Long Press2/Shutdown

During the power-on state, once the push button is asserted low for more than eight seconds, the power-off sequence begins. The MP5416 turns off all regulators and LDOs (excluding OUTRTC). The power-off sequence is the reverse of start-up.

If nPBIN is pulled low through a 49.9kΩ resistor constantly, the MP5416remains in the power-off state (see Figure 10).

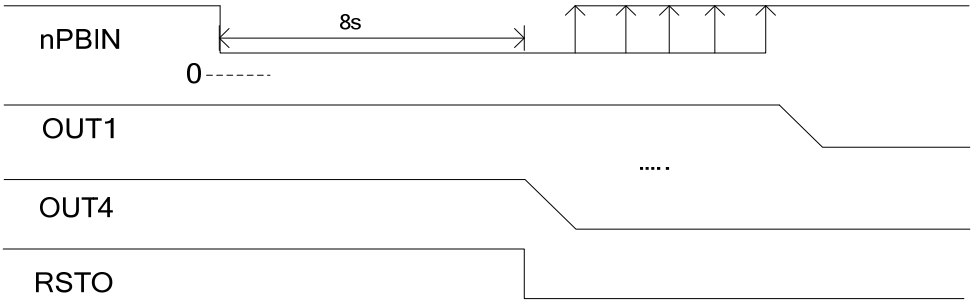


Figure 10: nPBIN Push Button Long Press2: Shutdown

3.1.2 Manual Reset Control

Short Press and Release/Manual Reset

If theMP5416 is in a power-off state, a short press on nPBIN pulls the nPBIN voltage below the manual reset threshold with 30msof maximum debounce time, and the MP5416begins the power-on sequence. When the MP5416is turned on, a short press makes the nPBIN voltage lower than the manual reset threshold with 30ms of maximum debounce time and triggers the manual reset function (see Figure 11).

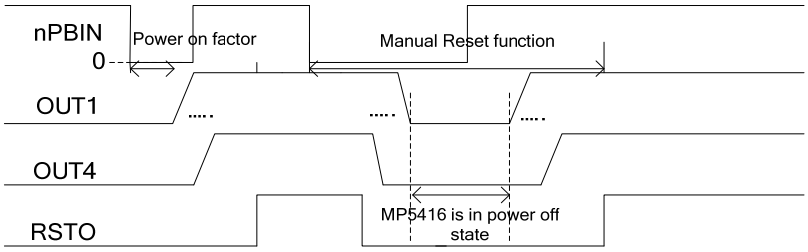


Figure 11: nPBIN Push Button Short Press to Ground

When the manual reset function is detected, the PMIC enters and remains in power-off mode until the manual reset button is released. The PMIC enters the power-on state again after 30ms of maximum debounce time.

3.2 Auto Turn-On

If the AUTOON bit in the OTP configuration table is set high, the system changes the default value of SYSEN to 1. The PMIC enters the power-on sequence automatically once the input voltage AVIN exceeds its UVLO threshold. The system can startup automatically without pressing the push button. After power-up, the push button can still support the manual power-on/-off control, and SYSEN can be read or written by the I^2C.

3.3 RSTO (Reset Output)

When Buck4's output voltage is ready (V_{FB}>90% V_{REF}), RSTO outputs high to enable the processer after an RSTO delay time. RSTO is an open-drain structure with an external pull-up resistor. RSTO is pulled low when Buck4's output is lower than 80% of the nominal value or the system detects a power-off factor, shutdown factor, or repower-on factor.

3.4Thermal Warning and Shutdown

Thermal warning and shutdown prevent the part from operating at exceedingly high temperatures. When the silicon die temperature exceeds 120°C, MP5416 sets the OTWARNING bit to 1.

If the die temperature exceeds 153°C, the MP5416sets the OTEMPP bit to 1.Meanwhile, the system enters the shutdown sequence. When the temperature recovers to 130°C, the regulator enters the power-on sequence again.

3.5 I^2C Timing Graph

The I^2C interface of the PMIC is powered by an internal, fixed, 2V power supply. During VIN power-up, when VIN exceeds its UVLO threshold, this 2V power supply is ready after a 0.5ms delay. After another 5ms of delay time, the I^2C is available (see Figure 12).

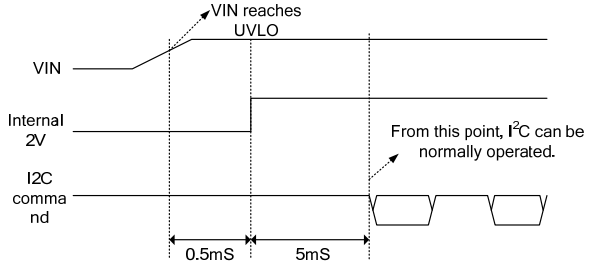


Figure 12: I^2C Timing Graph

I²C INTERFACE

I²CSerial Interface Description

I²C is a 2-wire, bidirectional, serial interface consisting of a data line (SDA) and a clock line (SCL). The lines are pulled to a bus voltage externally when they are idle. A master device connected to the line generates the SCL signal and device address and arranges the communication sequence. The MP5416 interface is an I²C slave, which supports both fast mode (400kHz) and high-speed mode (3.4MHz). The I²C interface adds flexibility to the power supply solution. The output voltage, transition slew rate, or other parameters can be controlled by the I²C interface instantaneously. When the master sends the address as an 8-bit value, the 7-bit address should be followed by a 0 or 1 to indicate a write or read operation.

Start and Stop Conditions

Start and stop are signaled by the master device, which signifies the beginning and end of the I²C transfer. The start condition is defined as the SDA signal transitioning from high to low while the SCL is high. The stop condition is defined as the SDA signal transitioning from low to high while the SCL is high (see Figure 13).

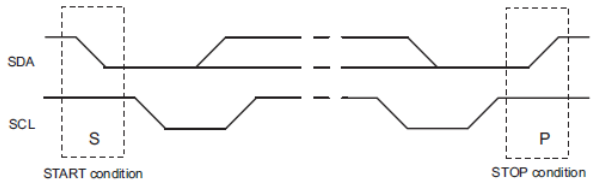


Figure 13: Start and Stop Conditions

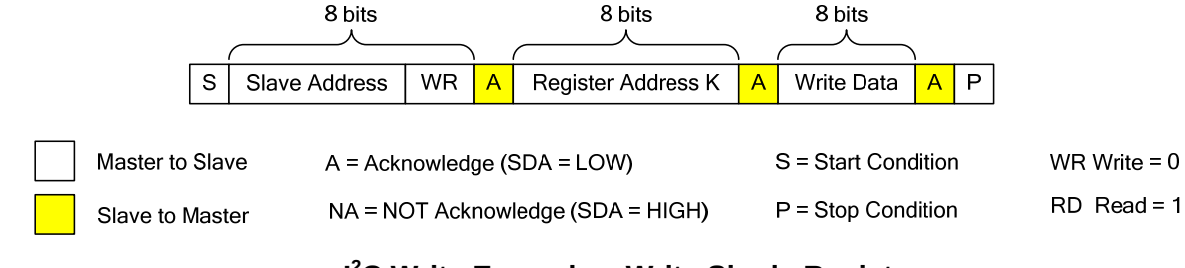
The master then generates the SCL clocks and transmits the device address and the read/write direction bit (r/w) on the SDA line.

Transfer Data

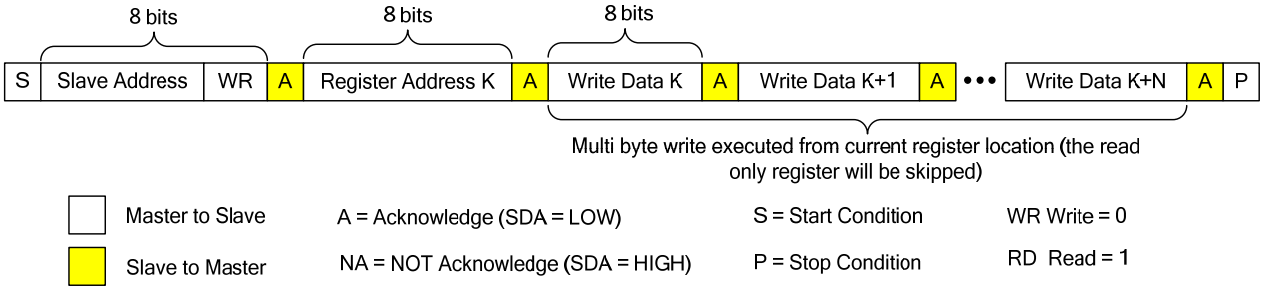
Data is transferred in 8-bit bytes by the SDA line. Each byte of data is to be followed by an acknowledge bit.

I²C Update Sequence

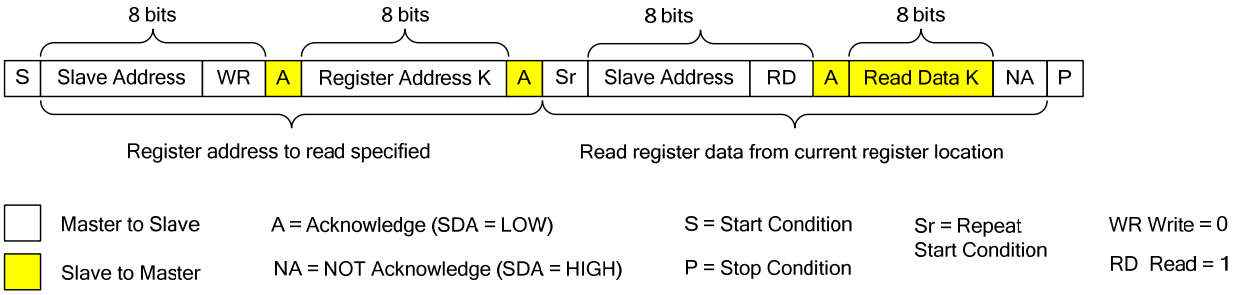
The MP5416 requires a start condition, a valid I²C address, a register address byte, and a data byte for a single data update. The MP5416 acknowledges the receipt of each byte by pulling the SDA line low during the high period of a single clock pulse. A valid I²C address selects the MP5416. The MP5416 performs an update on the falling edge of the LSB byte. Examples of an I²C write and read sequence are shown below.



I²C Write Example – Write Single Register



I²C Write Example – Write Multi Register



I²C Read Example – Read Single Register

REGISTER DESCRIPTION

OTP eFuse Configuration Table

#	NAME	D7	D6	D5	D4	D3	D2	D1	D0
00	CTL1	AUTOON	FREQUENCY		PUSHBUTTONTIMER			RSTODELAY	
01	CTL2	ILIMBUCK1		ILIMBUCK3		*N/A*	PWRONDELAYBUCK1		
02	CTL3	*MODEBUCK1*	*NOT NEED*	PWRONDELAYBUCK2			PWRONDELAYBUCK3		
03	CTL4	*MODEBUCK2*	*NOT NEED*	PWRONDELAYBUCK4			PWRONDELAYLDO2		
04	CTL5	*MODEBUCK3*	*NOT NEED*	PWRONDELAYLDO3			PWRONDELAYLDO4		
05	CTL6	*MODEBUCK4*	*NOT NEED*	PWRONDELAYLDO5			*N/A*		
06	VSET1	ENBUCK1	BUCK 1 VOUT SET: **0.6V-2.1V/100mV** STEP(10)				**I²C SLAVE ADDRESS A3, A2, A1**		
07	VSET2	ENBUCK2	BUCK 2 OUTPUT VOLTAGE SET: **0.8V-3.9V/100mV** STEP(10)					*N/A*	
08	VSET3	ENBUCK3	BUCK 3 VOUT SET: **0.6V-2.1V/100mV** STEP(10)				*N/A*		
09	VSET4	ENBUCK4	BUCK 4 OUTPUT VOLTAGE SET: **0.8V-3.9V/100mV** STEP(10)					*N/A*	
10	VSET5	Reserved	LDORTC OUTPUT VOLTAGE SET: **0.8V-3.9V/100mV** STEP					*N/A*	
11	VSET6	ENLDO2	LDO2 OUTPUT VOLTAGE SET: **0.8V-3.9V/100mV** STEP					*N/A*	
12	VSET7	ENLDO3	LDO3 OUTPUT VOLTAGE SET: **0.8V-3.9V/100mV** STEP					*N/A*	
13	VSET8	ENLDO4	LDO4 OUTPUT VOLTAGE SET: **0.8V-3.9V/100mV** STEP					**OTP VERSION D1, D0**	
14	VSET9	ENLDO5	LDO5 OUTPUT VOLTAGE SET: **0.8V-3.9V/100mV** STEP					**OTP VERSION D3, D2**	

OTP eFuse Selected Table by Default

OTP Items	Buck1	Buck2	Buck3	Buck4	LDORTC	LDO2	LDO3	LDO4	LDO5
Output Voltage	1.2V	1.5V	1.8V	3.3V	3.2V	3.3V	3.3V	1.1V	1.8V
Initial On/Off	On	On	On	On	On	On	Off	On	On
Mode	FPWM	PFM	FPWM	FPWM	N/A				
Power-On Delay/Time Slot #	2ms/1	4ms/2	4ms/2	0ms/0	Always on	4ms/2	6ms/3	2ms/1	4ms/2
Automatic Turn-On	Yes								
Switching Frequency	1.5MHz								
Push-Button Timer	2 seconds								
RSTO Delay	10ms								
Buck 1 Peak Current Limit	6.8A								
Buck 3 Peak Current Limit	5.6A								
I²C Slave Address	0x69								
OTP Version	0000								

NOTES:

10) In order to determine the most optimal output voltage configurations supported by this device, refer to application note AN139

.

Descriptions

<table>
<tr><th>NAME</th><th>BITS</th><th>DEFAULT</th><th>DESCRIPTION</th></tr>
<tr><td>AUTOON</td><td>D[7]</td><td>1</td><td>System automatic turn-on bit. If AUTOON is set high, the system enters the power-on sequence once AVIN exceeds the UVLO rising threshold. There is no need to press the push button (nPBIN).
The AUTOON bit information is loaded into the SYSEN register after AVIN reaches the UVLO rising threshold.</td></tr>
<tr><td>FREQUENCY</td><td>D[6:5]</td><td>01</td><td>Switching frequency set bit.
00: fs=1MHz
01: fs=1.5MHz
10: fs= 2MHz
11: fs=2.5MHz</td></tr>
<tr><td>PUSHBUTTON TIMER</td><td>D[4:2]</td><td>011</td><td>Set the push button long press1 power-on deglitch timer.
<table>
<tr><th></th><th>Fsw=1MHz</th><th>Fsw=1.5MHz</th><th>Fsw=2MHz</th><th>Fsw=2.5MHz</th></tr>
<tr><td>000</td><td>0.75s</td><td>0.5s</td><td>0.375s</td><td>0.3s</td></tr>
<tr><td>001</td><td>1.5s</td><td>1s</td><td>0.75s</td><td>0.6s</td></tr>
<tr><td>010</td><td>2.25s</td><td>1.5s</td><td>1.225s</td><td>0.9s</td></tr>
<tr><td>011</td><td>3s</td><td>2s</td><td>1.5s</td><td>1.2s</td></tr>
<tr><td>100</td><td>3.75s</td><td>2.5s</td><td>1.875s</td><td>1.5s</td></tr>
<tr><td>101</td><td>4.5s</td><td>3s</td><td>2.25s</td><td>1.8s</td></tr>
<tr><td>110</td><td>5.25s</td><td>3.5s</td><td>2.625s</td><td>2.1s</td></tr>
<tr><td>111</td><td>6s</td><td>4s</td><td>3s</td><td>2.4s</td></tr>
</table>
There is no corresponding data in the I^2C register table for the three bits.</td></tr>
<tr><td>RSTODELAY</td><td>D[1:0]</td><td>11</td><td>Reset output delay.
<table>
<tr><th></th><th>Fsw=1MHz</th><th>Fsw=1.5MHz</th><th>Fsw=2MHz</th><th>Fsw=2.5MHz</th></tr>
<tr><td>00</td><td>210ms</td><td>140ms</td><td>105ms</td><td>84ms</td></tr>
<tr><td>01</td><td>150ms</td><td>100ms</td><td>75ms</td><td>60ms</td></tr>
<tr><td>10</td><td>75ms</td><td>50ms</td><td>37.5ms</td><td>30ms</td></tr>
<tr><td>11</td><td>15ms</td><td>10ms</td><td>7.5ms</td><td>6ms</td></tr>
</table>
There is no corresponding data in the I^2C register table for the three bits.</td></tr>
<tr><td>PWRONDELAY BUCK1-4, LDO2-6</td><td>3 bit</td><td>---</td><td>Delay time from SYSEN=high to Buckx/LDOx beginning to switch.
000: 0ms – time slot 0
001:2ms– time slot 1
010:4ms– time slot 2
011:6ms– time slot 3
100: 8ms– time slot 4
101: 10ms– time slot 5
110: 12ms– time slot 6
111: 14ms– time slot 7
Delay time between neighbor slots are related with the PMIC default switching frequency. Refer to the Operation section on page 16for details.
There is no corresponding data in the I^2C register table for the three bits.</td></tr>
<tr><td>MODEBUCKX</td><td>1 bit</td><td>---</td><td>Select the mode (auto PFM/PWM mode or forced PWM mode).
0: auto PFM/PWM mode (Buck2 default mode)
1: forced PWM mode (Buck1, Buck3, and Buck4 default mode)
These bits are loaded into the I^2C register MODE BUCKx during VIN1 exceeding UVLO.</td></tr>
</table>

Descriptions*(continued)*

NAME	BITS	DEFAULT	DESCRIPTION
ILIMBUCK1/3	2 bit	10	Program the current limit threshold of the buck regulator: 00: 3.8A typical high-side peak current limit 01: 4.6A typical high-side peak current limit 10: 5.6A typical high-side peak current limit 11: 6.8A typical high-side peak current limit
I2C SLAVE ADDRESS A3, A2, A1	3 bit	001	Set the A3 to A1 bit of the slave I^2C address. Refer to the I^2C bus slave address on page 28.

I²C Register Map

ADD (HEX)	NAME	R/W	D7	D6	D5	D4	D3	D2	D1	D0
00	CTL0	r/w	SYSEN	SFRST	Reserved				Reserved	Reserved
01	CTL1	r/w	Reserved	MODEBUCK1	MODEBUCK2	MODEBUCK3	MODEBUCK4	DISCHGBUCK3	DISCHGBUCK2	DISCHGBUCK1
02	CTL2	r/w	DVS SLEW RATE		DISCHGBUCK4	DISCHGLDO2	DISCHGLDO3	DISCHGLDO4	DISCHGLDO5	Reserved
03	ILIMIT	r/w	ILIMBUCK1		ILIMBUCK3		ILIMBUCK2		ILIMBUCK4	
04	VSET1	r/w	ENBUCK1	BUCK1 OUTPUT VOLTAGE SET: **0.6V-2.1875V/12.5mV** STEP(10)						
05	VSET2	r/w	ENBUCK2	BUCK2 OUTPUT VOLTAGE SET: **0.8V-3.975V/25mV** STEP(10)						
06	VSET3	r/w	ENBUCK3	BUCK3 OUTPUT VOLTAGE SET: **0.6V-2.1875V/12.5mV** STEP(10)						
07	VSET4	r/w	ENBUCK4	BUCK4 OUTPUT VOLTAGE SET: **0.8V-3.975V/25mV** STEP(10)						
08	VSET5	r/w	ENLDO2	LDO2 OUTPUT VOLTAGE SET: 0.8V-3.975V/25mV STEP						
09	VSET6	r/w	ENLDO3	LDO3 OUTPUT VOLTAGE SET: 0.8V-3.975V/25mV STEP						
0A	VSET7	r/w	ENLDO4	LDO4 OUTPUT VOLTAGE SET: 0.8V-3.975V/25mV STEP						
0B	VSET8	r/w	ENLDO5	LDO5 OUTPUT VOLTAGE SET: 0.8V-3.975V/25mV STEP						
0C			RESERVED							
0D	Status1	r	PGLDO4	PGLDO3	PGLDO2	PGRTC	PG4	PG3	PG2	PG1
0E	Status2	r	KEYON	KEYOFF	MREST	SHORTKEYON	SFRST_ON	Reserved	Reserved	PGLDO5
0F	Status3	r	OTWARNING	OTEMPP	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
10			Reserved							
11	ID2	r	VENDOR ID				OTP VERSION			

Register Description

I²C Bus Slave Address(11)

The slave address is seven bits followed by an eights data direction bit (read or write). The A3, A2, and A1 bits are programmable by the OTP eFuse.

	A7	A6	A5	A4	A3	A2	A1
Setting Value	1	1	0	1	0(12)	0(12)	1(12)

NOTES:

11) By default, the slave address is 0x69, A[7:1]=1101 001.

12) This bit is programmable by the OTP eFuse.

1. Reg00 CTL0

NAME	BITS	DEFAULT	DESCRIPTION	RESET CONDITION
SYSEN	D[7]	BY OTP AUTOON	System enable on/off bit. When the MP5416 detects a power-on event, this bit is set to 1. Then the power-on sequence starts. The DC/DC converters and LDO regulators turn on sequentially according to its enable bit (e.g.: ENBUCK1=1) and power-on delay (POWERONDELAYBUCK1) setting. Set this bit from 1 to 0 to trigger a power-off sequence. Other I^2C registers are not reset when the I^2C sets SYSEN from 1 to 0. The MP5416is enabled again until the push button is pressed for a long time or a manual reset is asserted for more than 30ms of maximum debounce time.	AVIN<UVLO
SFRST	D[6]	0	Software reset. Once the SFRST bit is set high, the MP5416 waits for 8ms and restarts all power rails. When the RSTO signal switches from low to high, the MP5416 resets SFRST=0.	AVIN<UVLO or RSTO from low to high

2. Reg01CTL1

NAME	BITS	DEFAULT	DESCRIPTION	RESET CONDITION
MODEBUCKx	D[6:3]	BY OTP	PFM/PWM mode or forced PWM mode. 0: auto PFM/PWM 1: forced PWM mode	AVIN<UVLO or SFRST or manual reset or long press2
Regulator Discharge	D[2:0]	1	Output discharge enable bit. The output discharge function is active during the power-off sequence.	

3. Reg02CTL2

NAME	BITS	DEFAULT	DESCRIPTION	RESET CONDITION
DVS SLEW RATE	D[7:6]	01	Voltage scaling slew rate for the Buck1 to Buck4 converters. 00: 32mV/μs **01: 16mV/μs** 10: 8mV/μs 11: 4mV/μs	AVIN<UVLO or SFRST or manual reset or long press2
Regulator Discharge	D[5:0]	1	Output discharge enable bit. The output discharge function is active during the power-off sequence and active after shutdown.	

4. Reg03 ILIMIT

NAME	BITS	DEFAULT	DESCRIPTION	RESET CONDITION
ILIMBUCK1 ILIMBUCK3	D[X:X]	BY OTP	Program the current-limit threshold of the buck regulator. 00: 3.8A typical high-side peak current limit 01: 4.6A typical high-side peak current limit 10: 5.6A typical high-side peak current limit 11: 6.8A typical high-side peak current limit	AVIN<UVLO Or SFRST Or manual reset or long press2
ILIMBUCK2 ILIMBUCK4	D[X:X]	10	Program the current-limit threshold of the buck regulator. 00: 2.2A typical high-side peak current limit. 01: 3.2A typical high-side peak current limit. 10: 4.2A typical high-side peak current limit. 11: 5.2A typical high-side peak current limit.	

5. Reg04 to Reg0B VSET & EN

NAME	BITS	DEFAULT	DESCRIPTION	RESET CONDITION
ENX	D[7]	BY OTP	Enable bit of Buckx and LDOx. The default value is 1, but the default SYSEN is 0. Regulators are enabled when both ENx=1 and SYSEN=1.	AVIN<UVLO Or SFRST Or manual reset or long press2
BUCK1/3 VOUT SET	D[6:0]	BY OTP	Set the output voltage [10]from 0.6V to 2.1875V with 12.5mV step(see Table 2).	

Table 2: Output Voltage Chart of Buck1 and Buck3

D[6:0]	VOUT(V)	D[6:0]	VOUT(V)	D[6:0]	VOUT(V)	D[6:0]	VOUT(V)
0000000	0.6000	0100000	1.0000	1000000	1.4000	1100000	1.8000
0000001	0.6125	0100001	1.0125	1000001	1.4125	1100001	1.8125
0000010	0.6250	0100010	1.0250	1000010	1.4250	1100010	1.8250
0000011	0.6375	0100011	1.0375	1000011	1.4375	1100011	1.8375
0000100	0.6500	0100100	1.0500	1000100	1.4500	1100100	1.8500
0000101	0.6625	0100101	1.0625	1000101	1.4625	1100101	1.8625
0000110	0.6750	0100110	1.0750	1000110	1.4750	1100110	1.8750
0000111	0.6875	0100111	1.0875	1000111	1.4875	1100111	1.8875
0001000	0.7000	0101000	1.1000	1001000	1.5000	1101000	1.9000
0001001	0.7125	0101001	1.1125	1001001	1.5125	1101001	1.9125
0001010	0.7250	0101010	1.1250	1001010	1.5250	1101010	1.9250
0001011	0.7375	0101011	1.1375	1001011	1.5375	1101011	1.9375
0001100	0.7500	0101100	1.1500	1001100	1.5500	1101100	1.9500
0001101	0.7625	0101101	1.1625	1001101	1.5625	1101101	1.9625
0001110	0.7750	0101110	1.1750	1001110	1.5750	1101110	1.9750
0001111	0.7875	0101111	1.1875	1001111	1.5875	1101111	1.9875
0010000	0.8000	0110000	1.2000	1010000	1.6000	1110000	2.0000
0010001	0.8125	0110001	1.2125	1010001	1.6125	1110001	2.0125
0010010	0.8250	0110010	1.2250	1010010	1.6250	1110010	2.0250
0010011	0.8375	0110011	1.2375	1010011	1.6375	1110011	2.0375
0010100	0.8500	0110100	1.2500	1010100	1.6500	1110100	2.0500
0010101	0.8625	0110101	1.2625	1010101	1.6625	1110101	2.0625
0010110	0.8750	0110110	1.2750	1010110	1.6750	1110110	2.0750
0010111	0.8875	0110111	1.2875	1010111	1.6875	1110111	2.0875
0011000	0.9000	0111000	1.3000	1011000	1.7000	1111000	2.1000
0011001	0.9125	0111001	1.3125	1011001	1.7125	1111001	2.1125
0011010	0.9250	0111010	1.3250	1011010	1.7250	1111010	2.1250
0011011	0.9375	0111011	1.3375	1011011	1.7375	1111011	2.1375
0011100	0.9500	0111100	1.3500	1011100	1.7500	1111100	2.1500
0011101	0.9625	0111101	1.3625	1011101	1.7625	1111101	2.1625
0011110	0.9750	0111110	1.3750	1011110	1.7750	1111110	2.1750
0011111	0.9875	0111111	1.3875	1011111	1.7875	1111111	2.1875

6. Buck 2, Buck4, and LDO Regulator Output Voltage Set

NAME	BITS	DEFAULT	DESCRIPTION	RESET CONDITION
BUCK2/4, LDO VOUT SET	D[6:0]	BY OTP	Set the output voltage[10] from 0.8V to 3.975V with 25mV step(see Table 3).	AVIN<UVLO or SFRST or manual reset or long press2

Table 3: Output Voltage Chart of Buck2, Buck4, and all LDOs

D[6:0]	VOUT(V)	D[6:0]	VOUT(V)	D[6:0]	VOUT(V)	D[6:0]	VOUT(V)
0000000	0.800	0100000	1.600	1000000	2.400	1100000	3.200
0000001	0.825	0100001	1.625	1000001	2.425	1100001	3.225
0000010	0.850	0100010	1.650	1000010	2.450	1100010	3.250
0000011	0.875	0100011	1.675	1000011	2.475	1100011	3.275
0000100	0.900	0100100	1.700	1000100	2.500	1100100	3.300
0000101	0.925	0100101	1.725	1000101	2.525	1100101	3.325
0000110	0.950	0100110	1.750	1000110	2.550	1100110	3.350
0000111	0.975	0100111	1.775	1000111	2.575	1100111	3.375
0001000	1.000	0101000	1.800	1001000	2.600	1101000	3.400
0001001	1.025	0101001	1.825	1001001	2.625	1101001	3.425
0001010	1.050	0101010	1.850	1001010	2.650	1101010	3.450
0001011	1.075	0101011	1.875	1001011	2.675	1101011	3.475
0001100	1.100	0101100	1.900	1001100	2.700	1101100	3.500
0001101	1.125	0101101	1.925	1001101	2.725	1101101	3.525
0001110	1.150	0101110	1.950	1001110	2.750	1101110	3.550
0001111	1.175	0101111	1.975	1001111	2.775	1101111	3.575
0010000	1.200	0110000	2.000	1010000	2.800	1110000	3.600
0010001	1.225	0110001	2.025	1010001	2.825	1110001	3.625
0010010	1.250	0110010	2.050	1010010	2.850	1110010	3.650
0010011	1.275	0110011	2.075	1010011	2.875	1110011	3.675
0010100	1.300	0110100	2.100	1010100	2.900	1110100	3.700
0010101	1.325	0110101	2.125	1010101	2.925	1110101	3.725
0010110	1.350	0110110	2.150	1010110	2.950	1110110	3.750
0010111	1.375	0110111	2.175	1010111	2.975	1110111	3.775
0011000	1.400	0111000	2.200	1011000	3.000	1111000	3.800
0011001	1.425	0111001	2.225	1011001	3.025	1111001	3.825
0011010	1.450	0111010	2.250	1011010	3.050	1111010	3.850
0011011	1.475	0111011	2.275	1011011	3.075	1111011	3.875
0011100	1.500	0111100	2.300	1011100	3.100	1111100	3.900
0011101	1.525	0111101	2.325	1011101	3.125	1111101	3.925
0011110	1.550	0111110	2.350	1011110	3.150	1111110	3.950
0011111	1.575	0111111	2.375	1011111	3.175	1111111	3.975

7. Reg0D Status1

Status registers are non-latch type. It automatically updates according to its real-time status.

NAME	BITS	DESCRIPTION	RESET CONDITION
PGx	D[7:0]	Power good indicator for the buck and LDO. PG=1 when the output voltage is higher than 90% of the reference voltage. PG=0 when the output voltage is lower than 80% of the reference voltage. During the I^2C-controlled dynamic voltage scaling, the PG deglitch timer blanks the possible PG glitch.	AVIN<UVLO Or SFRST or manual reset or long press2

8. Reg0E Status2

NAME	BITS	DESCRIPTION		RESET CONDITION
KEYON	D[7]	Push button power-on event (long press1) is detected.	This bit is latched once it's triggered and cleared by a read action to the status register.	AVIN<UVLO
KEYOFF	D[6]	Push button power-off event (long press2) is detected.		
MREST	D[5]	Manual reset event is detected.		
SHORTKEYON	D[4]	If the MP5416 is in a power-off state, nPBIN is pulled to ground and lasts longer than the 30ms maximum debounce time. Then the SHORTKEYON bit is set high.		
SFRST_ON	D[3]	A software reset event is detected. When the SFRST bit is set high, the SFRST_ON bit goes high, and the high state is latched.		
PGx	D[0]	Power good indicator for LDO5. Non-latch type bits.		AVIN<UVLO or SFRST or manual reset or long press2

9. Reg0F Status3

NAME	BITS	DESCRIPTION		RESET CONDITION
OTWARNING	D[7]	Die temperature early warning bit. When the bit is high, the die temperature is higher than 120˚C.	This bit is latched once it's triggered and cleared by a read action to the status register.	AVIN<UVLO
OTEMPP	D[6]	Over-temperature indication. When the bit is high, the IC is in thermal shutdown.		

10. Reg11 ID2

NAME	BITS	DESCRIPTION
Vendor ID	D[7:4]	1000
OTP version	D[3:0]	0000

APPLICATION INFORMATION

Selecting the Inductor

For most applications, use a 0.47μHto2.2μH inductor with a DC current rating at least 25% higher than the maximum load current. For the highest efficiency, use an inductor with a DC resistance less than 15mΩ. For most designs, the inductance value can be derived from Equation (1):

$$L_1 = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{OSC}} \quad (1)$$

Where ΔI_L is the inductor ripple current.

Choose the inductor ripple current to be approximately 30% of the maximum load current. The maximum inductor peak current can be calculated with Equation (2):

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2} \quad (2)$$

Use a larger inductor for improved efficiency under light-load conditions(<100mA).

Selecting the Step-Down Converter Input Capacitor

The input current to the step-down converter is discontinuous and therefore requires a capacitor to supply AC current to the step-down converter while maintaining the DC input voltage. Use low ESR capacitors for the best performance. Ceramic capacitors with X5R or X7R dielectrics are recommended because of their low ESR and small temperature coefficients. For most applications, use a 22μF capacitor.

Since C1 absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated with Equation (3):

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (3)$$

The worst-case condition occurs at VIN = $2V_{OUT}$, shown in Equation (4):

$$I_{C1} = \frac{I_{LOAD}}{2} \quad (4)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, add a small, high-quality, ceramic capacitor (e.g.: 0.1μF) placed as close to the IC as possible. When using ceramic capacitors, ensure that they have enough capacitance to provide sufficient charge to prevent excessive voltage ripple at the input. The input voltage ripple caused by the capacitance can be estimated with Equation (5):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_S \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (5)$$

Selecting the Step-Down Converter Output Capacitor

The output capacitor for the step-down regulator maintains the DC output voltage. Use ceramic, tantalum, or low ESR electrolytic capacitors. For best results, use low ESR capacitors to keep the output voltage ripple low. The output voltage ripple can be estimated with Equation (6):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_S \times C2}\right) \quad (6)$$

Where L_1 is the inductor value, and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

For ceramic capacitors, the capacitance dominates the impedance at the switching frequency and causes the majority of the output voltage ripple. For simplification, the output voltage ripple can be estimated with Equation (7):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_S^2 \times L_1 \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (7)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated with Equation (8):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (8)$$

The characteristics of the output capacitor also affect the stability of the regulation.

Recommended External Components for DC/DC and LDO Converters

Table 4 lists recommended external components for the DC/DC converters and LDO regulators.

Table 4: Recommended External Components

	Value	Notes
Cin of VIN1	22μF	0805 size/10V ceramic capacitor
Cin of VIN2	22μF	0805 size/10V ceramic capacitor
Cin of VIN3	22μF	0805 size/10V ceramic capacitor
Cin of VIN4	22μF	0805 size/10V ceramic capacitor
Cin of VIN5	10μF	0805 size/10V ceramic capacitor
Cin of AVIN	1μF	0603 size/10V ceramic capacitor
Cout of Buck1	22μFx2	0805 size/10V ceramic capacitor
L of Buck1	1μH	I_{SAT}> current limit
Cout of Buck2	22μF	0805 size/10V ceramic capacitor
L of Buck2	1.5μH	I_{SAT}> current limit
Cout of Buck3	22μFx2	0805 size/10V ceramic capacitor
L of Buck3	1μH	I_{SAT}> current limit
Cout of Buck4	22μF	0805 size/10V ceramic capacitor
L of Buck4	1.5μH	I_{SAT}> current limit
Cout of RTCLDO	1μF	0603 size/6.3V ceramic capacitor
Cout of LDO2	2.2μF	0603 size/6.3V ceramic capacitor
Cout of LDO3	2.2μF	0603 size/6.3V ceramic capacitor
Cout of LDO4	2.2μF	0603 size/6.3V ceramic capacitor
Cout of LDO5	2.2μF	0603 size/6.3V ceramic capacitor
RSTO pull-up resistor	100kΩ	0603 or 0402 size film resistor
nPBIN pull-low resistor	49.9kΩ	Push button function. 0603 or 0402 size film resistor
AVIN series resistor to VIN1	10Ω	0603 or 0402 size film resistor

PCB Layout Guidelines [13]

Efficient PCB layout is critical for stable operation. A four-layer layout is recommended for the best performance. For best results, refer to Figure 14 and follow the guidelines below.

1. Connect the input ground to GND using the shortest and widest trace possible.
2. Connect the input capacitor to VIN using the shortest and widest trace possible.
3. Ensure that FB1-FB4 are Kelvin connected to the Buck1-Buck4 output capacitor. DO NOT directly connect FB to the inductor's output node.
4. Route SW away from sensitive analog areas, such as FB1 to FB4.

NOTE:

13) The recommended layout is based on Figure 15 on page 36.

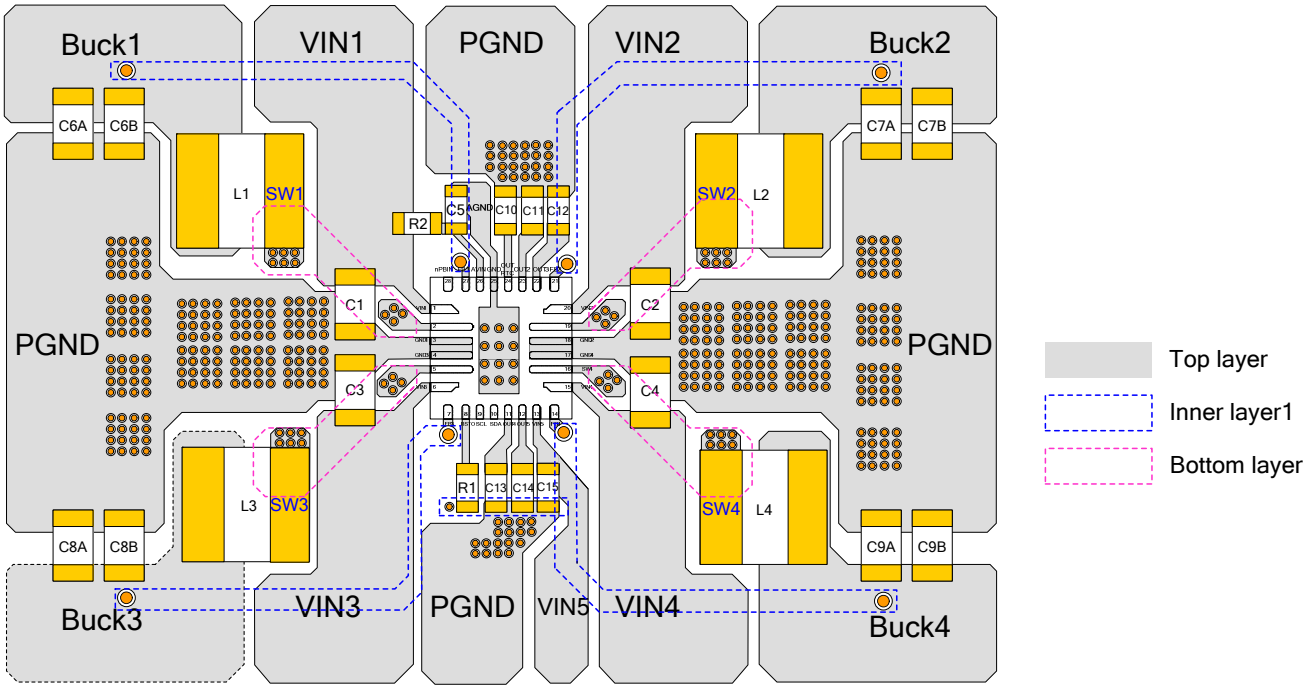


Figure 14: Recommended Layout(14)

NOTE:

14) It is recommended to separate Buck1/3 and Buck2/4's PGND on the top layer.

TYPICAL APPLICATION CIRCUIT

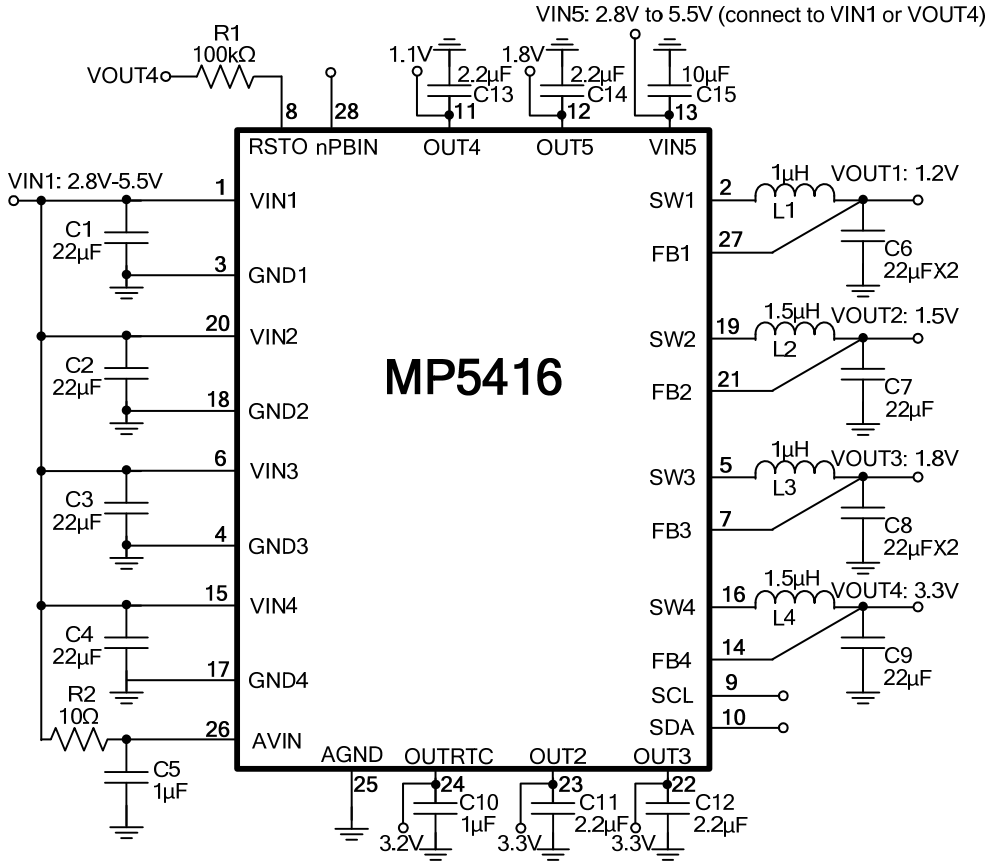


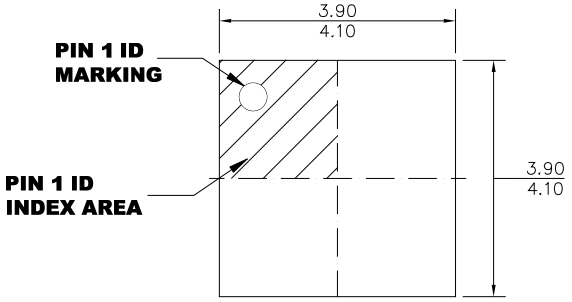
Figure 15: Typical Application Circuit(15)

NOTE:

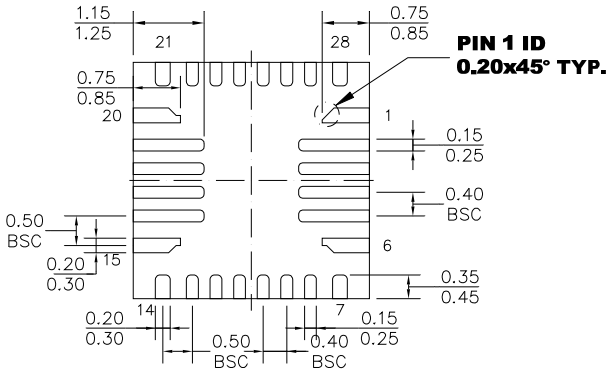
15) The minimum input voltage of VIN5 is equal to the maximum nominal output voltage of LDO4 and LDO5.

PACKAGE INFORMATION

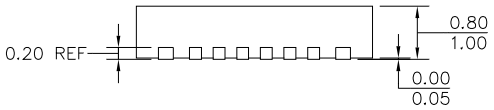
QFN-28 (4mmx4mm)



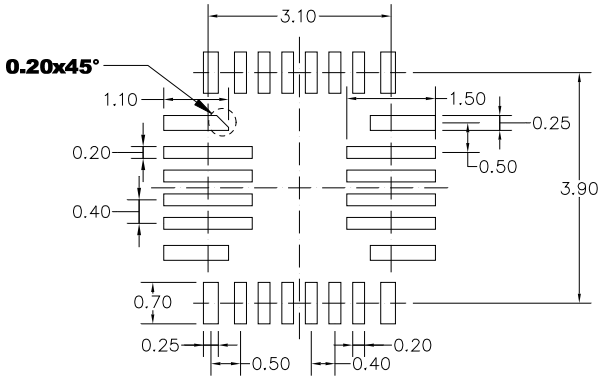
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) LAND PATTERNS OF PIN1,6,15 AND 20 HAVE THE SAME LENGTH AND WIDTH.
2) LAND PATTERNS OF PIN7,14,21 AND 28 HAVE THE SAME LENGTH AND WIDTH.
3) ALL DIMENSIONS ARE IN MILLIMETERS.
4) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
5) DRAWING CONFORMS TO JEDEC MO-220.
6) DRAWING IS NOT TO SCALE.