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FDMA2002NZ

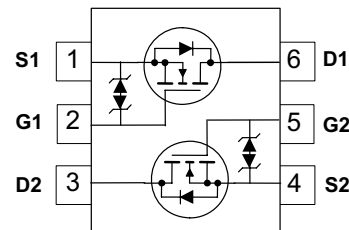
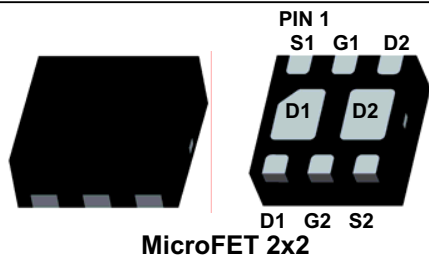
Dual N-Channel PowerTrench[®] MOSFET

General Description

This device is designed specifically as a single package solution for dual switching requirements in cellular handset and other ultra-portable applications. It features two independent N-Channel MOSFETs with low on-state resistance for minimum conduction losses. The MicroFET 2x2 offers exceptional thermal performance for its physical size and is well suited to linear mode applications.

Features

- 2.9 A, 30 V $R_{DS(ON)} = 123\text{ m}\Omega @ V_{GS} = 4.5\text{ V}$
 $R_{DS(ON)} = 140\text{ m}\Omega @ V_{GS} = 3.0\text{ V}$
 $R_{DS(ON)} = 163\text{ m}\Omega @ V_{GS} = 2.5\text{ V}$
- Low profile – 0.8 mm maximum – in the new package MicroFET 2x2 mm
- HBM ESD protection level = 1.8kV (Note 3)
- RoHS Compliant
- Free from halogenated compounds and antimony oxides



Absolute Maximum Ratings

$T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DS}	Drain-Source Voltage	30	V
V_{GS}	Gate-Source Voltage	± 12	V
I_D	Drain Current – Continuous ($T_C = 25^\circ\text{C}$, $V_{GS} = 4.5\text{V}$)	2.9	A
	– Continuous ($T_C = 25^\circ\text{C}$, $V_{GS} = 2.5\text{V}$)	2.7	
	– Pulsed	10	
P_D	Power Dissipation for Single Operation (Note 1a)	1.5	W
	Power Dissipation for Single Operation (Note 1b)	0.65	
T_J, T_{STG}	Operating and Storage Temperature	-55 to $+150$	$^\circ\text{C}$

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	83 (Single Operation)	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1b)	193 (Single Operation)	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1c)	68 (Dual Operation)	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1d)	145 (Dual Operation)	

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
002	FDMA2002NZ	7"	8mm	3000 units

Electrical Characteristics $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV _{DSS}	Drain–Source Breakdown Voltage	V _{GS} = 0 V, I _D = 250 μA	30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I _D = 250 μA, Referenced to 25°C		25		mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 24 V, V _{GS} = 0 V			1	μA
I _{GSS}	Gate–Body Leakage Current	V _{GS} = ± 12 V, V _{DS} = 0 V			±10	μA
On Characteristics						
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250 μA	0.4	1.0	1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	I _D = 250 μA, Referenced to 25°C		–3		mV/°C
R _{DS(on)}	Static Drain–Source On–Resistance	V _{GS} = 4.5V, I _D = 2.9A		75	123	mΩ
		V _{GS} = 3.0V, I _D = 2.7A		84	140	
		V _{GS} = 2.5V, I _D = 2.5A		92	163	
		V _{GS} = 4.5V, I _D = 2.9A, T _C = 85°C		95	166	
		V _{GS} = 3.0V, I _D = 2.7A, T _C = 150°C		138	203	
		V _{GS} = 2.5V, I _D = 2.5A, T _C = 150°C		150	268	
Dynamic Characteristics						
C _{iss}	Input Capacitance	V _{DS} = 15 V, V _{GS} = 0 V, f = 1.0 MHz		190	220	pF
C _{oss}	Output Capacitance			30	40	pF
C _{rss}	Reverse Transfer Capacitance			20	30	pF
Switching Characteristics (Note 2)						
t _{d(on)}	Turn–On Delay Time	V _{DD} = 15 V, I _D = 1 A, V _{GS} = 4.5 V, R _{GEN} = 6 Ω		6	12	ns
t _r	Turn–On Rise Time			8	16	ns
t _{d(off)}	Turn–Off Delay Time			12	21	ns
t _f	Turn–Off Fall Time			2	10	ns
Q _g	Total Gate Charge	V _{DS} = 15 V, I _D = 2.9 A, V _{GS} = 4.5 V		2.4	3.0	nC
Q _{gs}	Gate–Source Charge			0.35		nC
Q _{gd}	Gate–Drain Charge			0.75		nC
Drain–Source Diode Characteristics and Maximum Ratings						
I _S	Maximum Continuous Source–Drain Diode Forward Current				2.9	A
V _{SD}	Source–Drain Diode Forward Voltage	I _S = 2.0 A		0.9	1.2	V
		I _S = 1.1 A		0.8	1.2	
t _{rr}	Diode Reverse Recovery Time	I _F = 2.9 A, dI _F /dt = 100 A/μs		10		ns
Q _{rr}	Diode Reverse Recovery Charge			2		nC

Notes:

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in² oz. copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design.

(a) $R_{\theta JA} = 86\text{ }^{\circ}\text{C/W}$ when mounted on a 1 in² pad of 2 oz copper, 1.5 " x 1.5 " x 0.062 " thick PCB. For single operation.

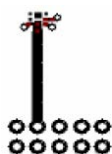
(b) $R_{\theta JA} = 173\text{ }^{\circ}\text{C/W}$ when mounted on a minimum pad of 2 oz copper. For single operation.

(c) $R_{\theta JA} = 69\text{ }^{\circ}\text{C/W}$ when mounted on a 1 in² pad of 2 oz copper, 1.5 " x 1.5 " x 0.062 " thick PCB. For dual operation.

(d) $R_{\theta JA} = 151\text{ }^{\circ}\text{C/W}$ when mounted on a minimum pad of 2 oz copper. For dual operation.



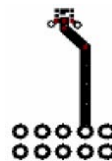
a) 86 °C/W when mounted on a 1 in² pad of 2 oz copper.



b) 173 °C/W when mounted on a minimum pad of 2 oz copper.



c) 69 °C/W when mounted on a 1 in² pad of 2 oz copper.



d) 151 °C/W when mounted on a minimum pad of 2 oz copper.

2. Pulse Test : Pulse Width < 300 us, Duty Cycle < 2.0%

3. The diode connected between the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.

Typical Characteristics

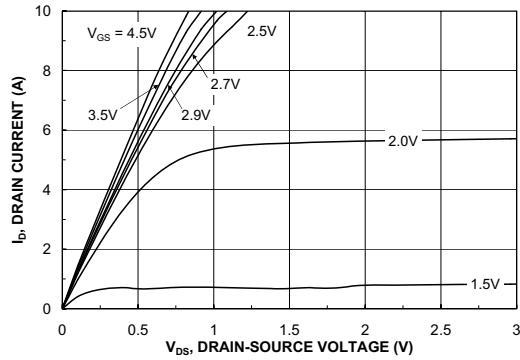


Figure 1. On-Region Characteristics.

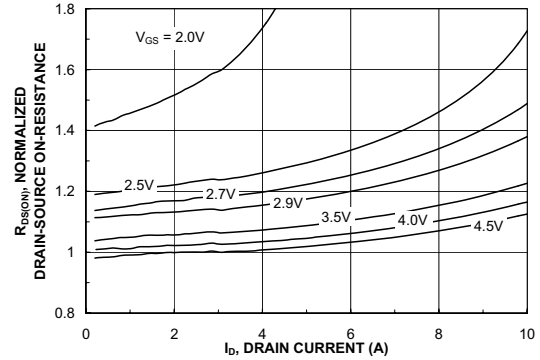


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

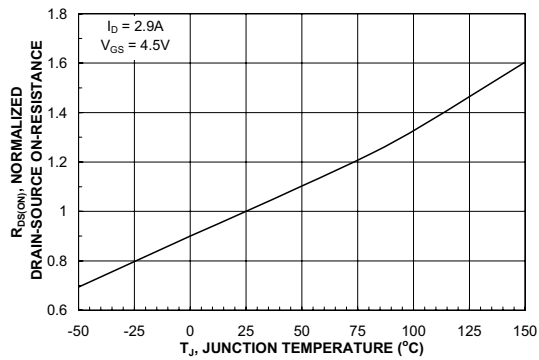


Figure 3. On-Resistance Variation with Temperature.

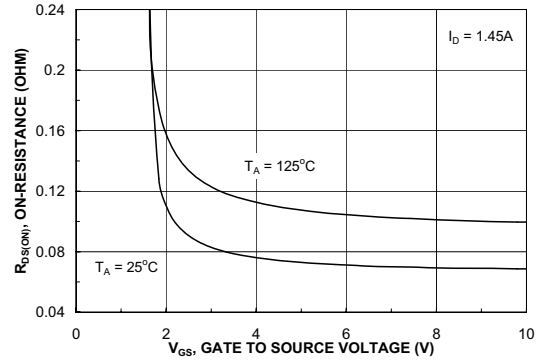


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

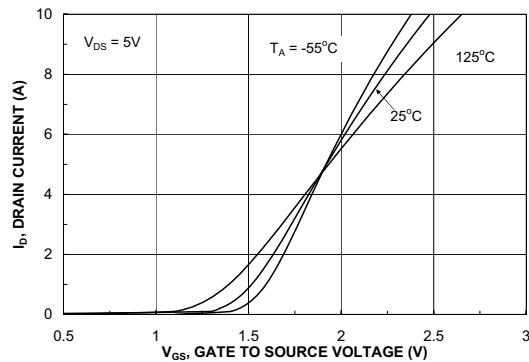


Figure 5. Transfer Characteristics.

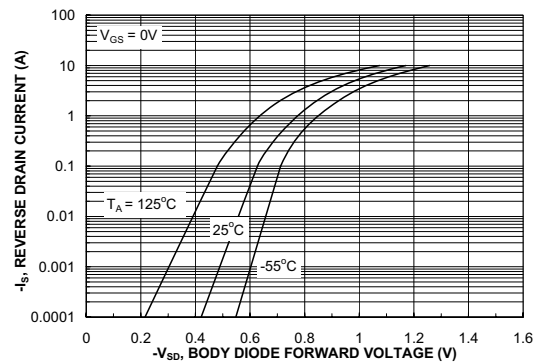
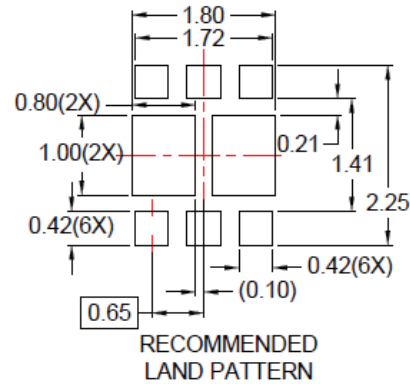
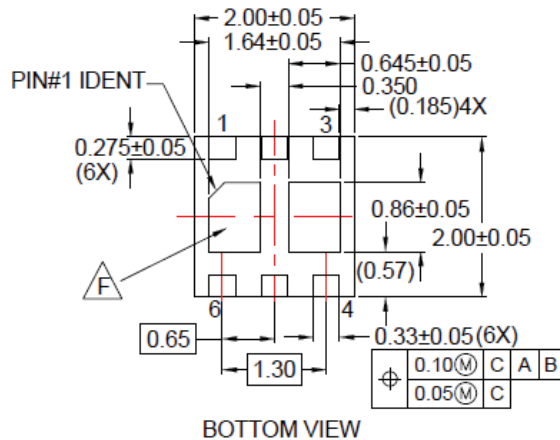
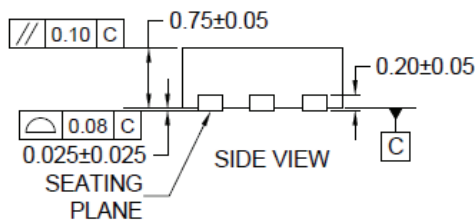
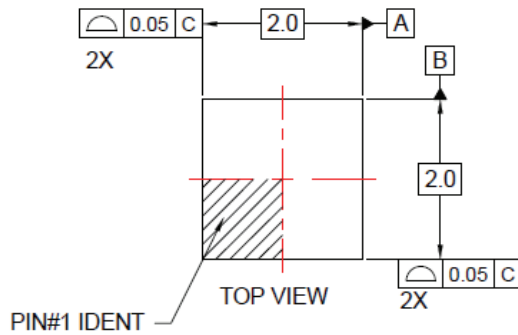


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Dimensional Outline and Pad Layout



NOTES:

- CONFORM TO JEDEC REGISTRATIONS MO-229, VARIATION VCCC, EXCEPT WHERE NOTED.
- DIMENSIONS ARE IN MILLIMETERS.
- DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
- LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.
- DRAWING FILENAME: MKT-UMLP16Erev4
- NON-JEDEC DUAL DAP



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