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April 2014

FAN501
Offline DCM / CCM Flyback PWM Controller for Charger Applications

Features

- WSaver® Technology Provides Ultra-Low Standby Power Consumption for Energy Star's 5-Star Level (<30 mW)
- Constant-Current (CC) Control without Secondary-Side Feedback Circuitry for Discontinuous Conduction Mode (DCM) and Continuous Conduction Mode (CCM)
- Dual-Frequency Function Changes Switching Frequency (140 kHz / 85 kHz) According to Input Voltage to Maximize Transformer Utilization and Improve Efficiency
- High Power Density and High Conversion Efficiency with CCM Operation in Typical 10 W to15 W Compact Charger Applications
- Frequency Hopping to Reduce EMI Noise
- High-Voltage Startup
- Precise Maximum Output Power Limit by CC Regulation through External Resistor Adjustment
- Peak-Current-Mode Control with Slope Compensation to Avoid Sub-Harmonic Oscillation
- Programmable Over-Temperature Protection with Latch Mode through External NTC Resistor
- V_S Over-Voltage Protection with Latch Mode
- V_S Under-Voltage Protection with Auto-Restart
- V_{DD} Over-Voltage-Protection with Auto-Restart
- Available in MLP 4 X 3 Package

Applications

- Battery Chargers for Smart Phones, Feature Phones, and Tablet PCs
- AC-DC Adapters for Portable Devices or Battery Chargers that Require CV / CC Control

Description

The advanced PWM controller, FAN501, simplifies isolated power supply design that requires CC regulation of the output. The output current is precisely estimated with only the information in the primary side of the transformer and controlled with an internal compensation circuit, removing the output current-sensing loss and eliminating external CC control circuitry. With an extremely low operating current (250 µA), Burst Mode maximizes light-load efficiency, allowing conformance to worldwide Standby Mode efficiency guidelines.

Compared with a conventional approach using external control circuit in the secondary side for CC regulation, the FAN501 can reduce total cost, component count, size, and weight; while increasing efficiency, productivity, and system reliability.

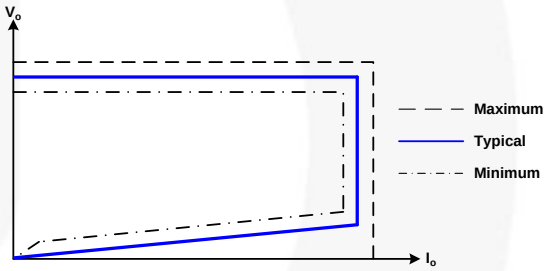


Figure 1. Typical Output V-I Characteristic

Ordering Information

Part Number	Operating Temperature Range	Package	Packing Method
FAN501MPX	-40°C to +125°C	10-Lead, MLP, QUAD, JEDEC MO-220 4 mm x 3 mm, 0.8 mm Pitch, Single DAP	Tape & Reel

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Application Diagram

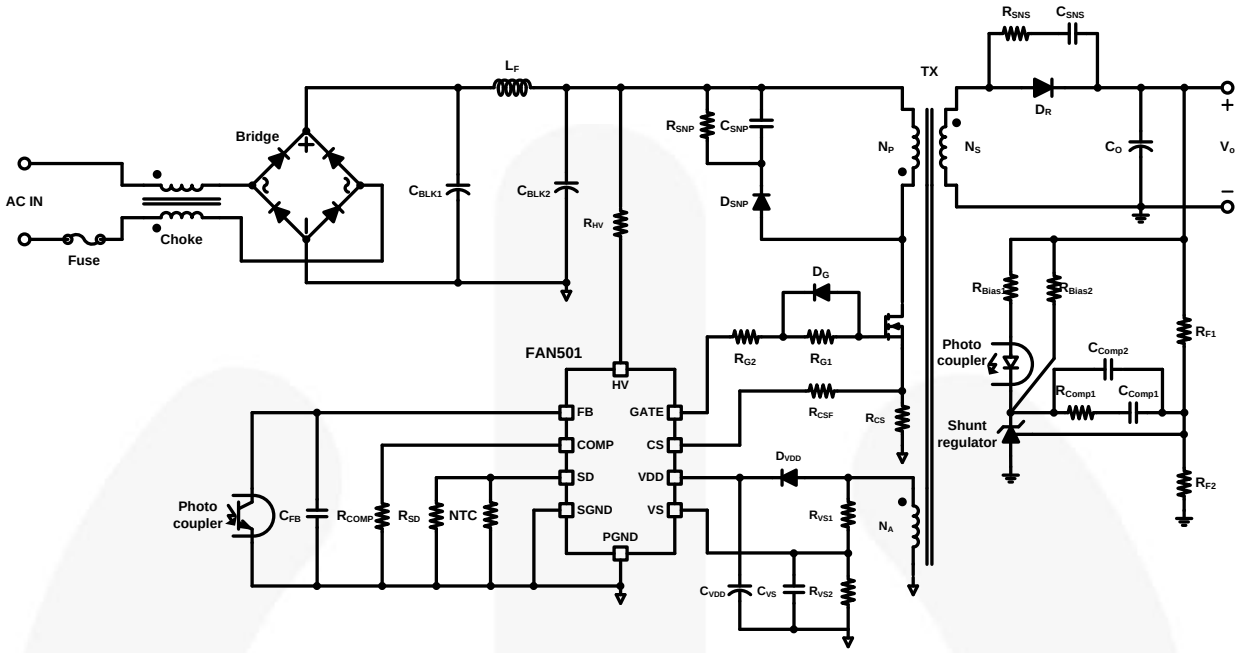


Figure 2. Typical Application

Internal Block Diagram

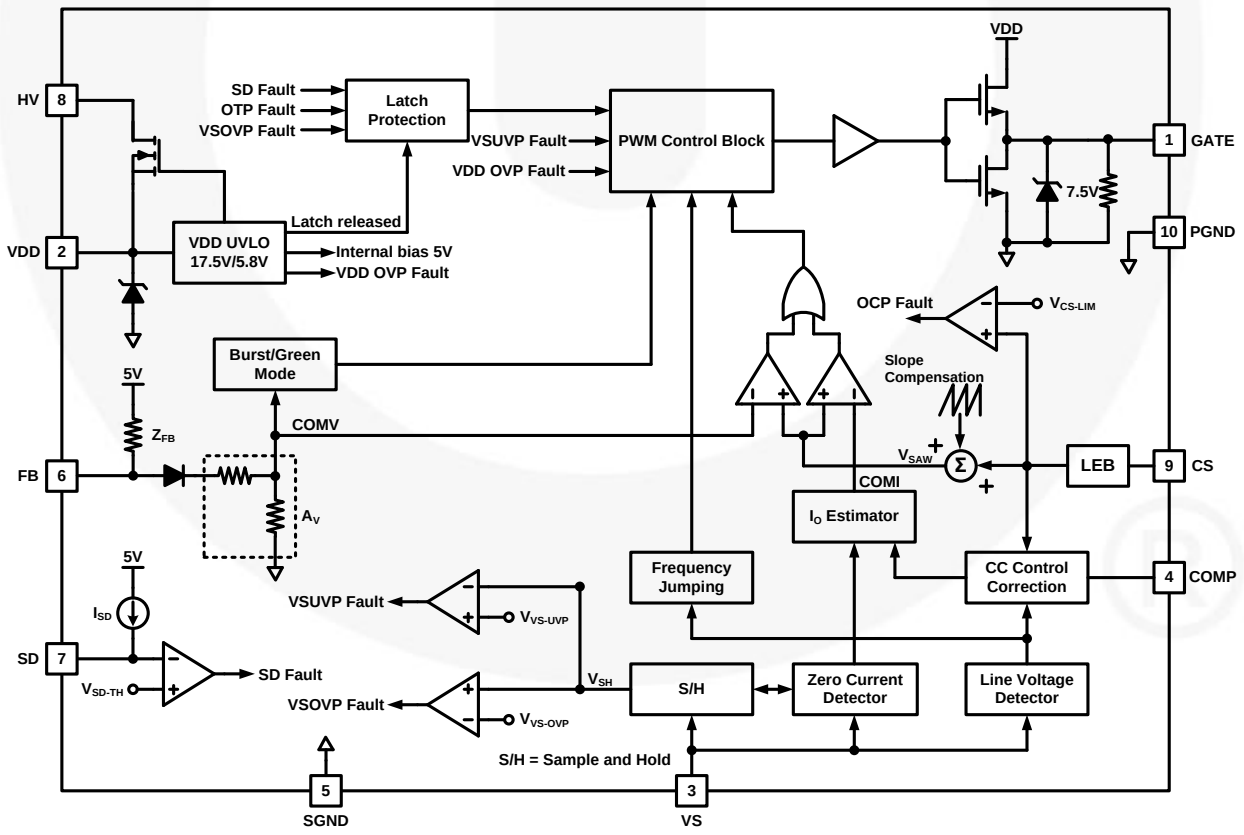
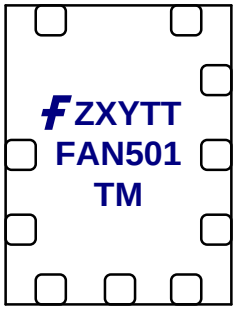


Figure 3. Function Block Diagram

Marking Information



F- Fairchild Logo
Z: Assembly Plant Code
X: Year Code
Y: Week Code
TT: Die Run Code
T: Package Type (MP=MLP)
M: Manufacture Flow Code

Figure 4. Top Mark

Pin Configuration

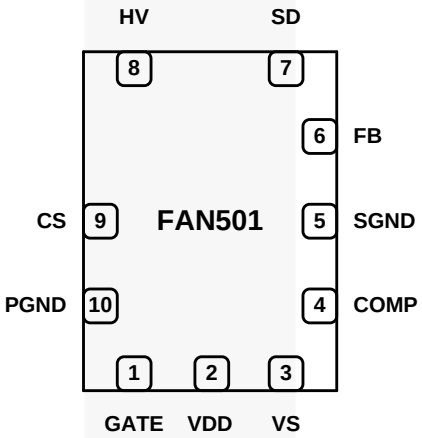


Figure 5. Pin Assignments

Pin Definitions

Pin #	Name	Description
1	GATE	PWM Signal Output. This pin has an internal totem-pole output driver to drive the power MOSFET. The gate driving voltage is internally clamped at 7.5 V.
2	VDD	Power Supply. IC operating current and MOSFET driving current are supplied through this pin. This pin is typically connected to an external capacitor.
3	VS	Voltage Sense. This pin detects the output voltage information and diode current discharge time based on the voltage of the auxiliary winding. It also senses sink current through the auxiliary winding to detect input voltage information.
4	COMP	CC Control Correction. This pin connects to external resistor to program the CC control correction weighting.
5	SGND	Signal Ground
6	FB	Feedback. An opto-coupler is typically connected to this pin to provide feedback information to the internal PWM comparator. This feedback is used to control the duty cycle in Constant-Voltage (CV) regulation.
7	SD	Shut Down. This pin is implemented for external over-temperature protection by connecting to an NTC thermistor.
8	HV	High Voltage. This pin connects to a DC bus for high-voltage startup.
9	CS	Current Sense. This pin connects to a current-sense resistor to detect the MOSFET current for Peak-Current-Mode control for output regulation. The current-sense information is also used to estimate the output current for CC regulation.
10	PGND	Power Ground

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Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{HV}	HV Pin Input Voltage			500	V
V_{VDD}	DC Supply Voltage			30	V
V_{VS}	VS Pin Input Voltage		-0.3	6.0	V
V_{CS}	CS Pin Input Voltage		-0.3	6.0	V
V_{FB}	FB Pin Input Voltage		-0.3	6.0	V
V_{COMP}	COMP Pin Input Voltage		-0.3	6.0	V
V_{SD}	SD Pin Input Voltage		-0.3	6.0	V
P_D	Power Dissipation (T_A=25°C)			850	mW
Θ_{JA}	Thermal Resistance (Junction-to-Air)			150	°C/W
Θ_{JC}	Thermal Resistance (Junction-to-Case)			10	°C/W
T_J	Operating Junction Temperature		-40	+150	°C
T_{STG}	Storage Temperature Range		-40	+150	°C
T_L	Lead Temperature (Wave soldering or IR, 10 Seconds)			+260	°C
ESD	Electrostatic Discharge Capability[3]	Human Body Model, ANSI/ESDA/JEDEC JS-001-2012 (Except HV Pin)		5.0	kV
		Charged Device Model, JEDEC:JESD22_C101 (Except HV Pin)		2.0	

Notes:

1. All voltage values, except differential voltages, are given with respect to the GND pin.
2. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device.
3. ESD ratings including HV pin: HBM=3.0 kV, CDM=750 V.

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Electrical Characteristics

V_{DD}=15 V and T_J=-40~125°C unless noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
HV Section						
V_{HV-MIN}	Minimum Startup Voltage on HV Pin				30	V
I_{HV}	Supply Current Drawn from HV Pin	V_{HV}=120 V, V_{DD}=0 V	1.2	2.0	5.0	mA
I_{HV-LC}	Leakage Current Drawn from HV Pin	V_{HV}=500 V, V_{DD}=V_{DD-OFF}+1 V		0.8	10.0	µA
V_{DD} Section						
V_{DD-ON}	Turn-On Threshold Voltage(4)	V_{DD} Rising	16.5	17.5	18.5	V
V_{DD-OFF}	Turn-Off Threshold Voltage	V_{DD} Falling	5.3	5.8	6.3	V
V_{DD-DLH}	Threshold Voltage for Latch Release(5)			2.50		V
I_{DD-ST}	Startup Current	V_{DD}=V_{DD-ON}-0.16 V		150	250	µA
I_{DD-OP}	Operating Supply Current	V_{CS}=5.0 V, V_S=3 V, V_{FB}=3 V, V_{DD}=15 V, C_{GATE}=1 nF		3.5	4.0	mA
$I_{DD-Burst}$	Burst Mode Operating Supply Current	V_{CS}=0.3 V, V_S=0 V, V_{FB}=0 V, V_{DD}=V_{DD-ON}→V_{DD-OVP}→10 V, C_{GATE}=1 nF		250	300	µA
V_{DD-OVP}	V_{DD} Over-Voltage Protection Level		26.5	28.0	29.5	V
Oscillator Section						
f_{OSC--H}	Operating Frequency, I_{VS} Below Threshold I_{VS-L}(Low Line)(4)	V_{CS}=5 V, V_S=2.5 V, V_{FB}=6 V	133	140	147	kHz
f_{OSC--L}	Operating Frequency, I_{VS} Over Threshold I_{VS-H}(High Line)(4)	V_{CS}=5 V, V_S=2.5 V, V_{FB}=4 V	79	85	91	kHz
$\Delta f_{Hopping-H}$	Frequency Hopping Range, High Line	V_{CS}=0.5 V, V_S=0.7 V, V_{FB}=3 V	±5.5	±7.0	±8.5	kHz
$\Delta f_{Hopping-L}$	Frequency Hopping Range, Low Line	V_{CS}=0.5 V, V_S=0.0 V, V_{FB}=3 V	±2.5	±4.0	±5.5	kHz
$\Delta t_{Hopping}$	Frequency Hopping Period			2.54		ms
Feedback Input Section						
Z_{FB}	FB Pin Input Impedance(4)		38	41	44	kΩ
A_V	Internal Voltage Attenuator of FB Pin(5)			1/2.5		V/V
$V_{FB-Open}$	FB Pin Pull-Up Voltage	FB Pin Open	5.00	5.50	5.90	V
$V_{FB-Burst-H}$	FB Threshold to Enable Gate Drive in Burst Mode(4)	V_{FB} Rising with V_{CS}=0.3 V, V_S=0 V	1.60	1.70	1.80	V
$V_{FB-Burst-L}$	FB Threshold to Disable Gate Drive in Burst Mode(4)	V_{FB} Falling with V_{CS}=0.3 V, V_S=0 V	1.55	1.65	1.75	V
Over-Temperature Protection Section						
T_{OTP}	Threshold Temperature for Over-Temperature Protection			140		°C
Shutdown Function Section						
I_{SD}	SD Pin Source Current	V_{CS}=0.3 V	85	100	115	µA
V_{SD-TH}	Threshold Voltage for Shutdown Function Enable	V_{CS}=0.3 V	0.85	1.00	1.15	V

Continued on the following page…

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Electrical Characteristics

V_{DD}=15 V and T_J=-40~125°C unless noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Voltage-Sense Section						
I_{TC}	Temperature-Independent Bias Current	V_{CS}=5 V, V_{FB}=3 V	8.75	10.00	11.25	µA
I_{VS-H}	V_S Source Current Threshold to f_{OSC-L} Operation(5)			750		µA
I_{VS-L}	V_S Source Current Threshold to f_{OSC-H} Operation(5)			680		µA
$I_{VS-Brownout}$	V_S Source Current Threshold to Enable Brownout			160		µA
V_{VS-OVP}	Output Over-Voltage Protection with V_S Sampling Voltage(4)		3.10	3.20	3.30	V
N_{VS-OVP}	Output Over-Voltage Protection Debounce Cycle Counts(4)			8		Cycle
V_{VS-UVP}	Output Under-Voltage Protection		1.45	1.55	1.65	V
$t_{VS-UVP-BLANK}$	Output Under-Voltage Protection Blanking Time at Startup(5)		30	45	60	ms
N_{VS-UVP}	Output Under-Voltage Protection Debounce Cycle Counts(5)			8		Cycle
Current-Sense Section						
V_{VR}	Internal Reference Voltage for CC Regulation		2.460	2.500	2.540	V
V_{CCR}	Variation Test Voltage on CS Pin for CC Regulation (Non-Inverting Input of Error Amplifier for CC Regulation, EAI)	V_{CS}=0.375 V, V_{COMP}= 1.59 V, V_S= 6 V	2.405	2.430	2.455	V
K_{CCM}	Design Parameter in CC Regulation(4)			12.0		V/V
V_{CS-LIM}	Current Limit Threshold Voltage		0.80	0.85	0.90	V
t_{PD}	GATE Output Turn-Off Delay			100	200	ns
t_{LEB}	Leading-Edge Blanking Time(4)			150	200	ns
V_{Slope}	Slope Compensation(4)	Maximum Duty Cycle		66.6		mV/µs
Constant Current Correction						
I_{COMP}	COMP Pin Source Current as V_S=0.3 V	V_{CS}=0.3 V, V_{FB}=2.5 V, V_S=0 V	42	50	58	µA
GATE Section						
t_{ON-MIN}	Minimum On Time	V_{CS}=0.6 V, V_S=0.3 V, V_{FB}=1.7 V	450	550	650	ns
$t_{ON-MIN-Limit}$	Limited Minimum On Time	V_{CS}=0.6 V, V_S=0.5 V, V_{FB}=1.7 V	0.95	1.20	1.45	µs
D_{CYMAX}	Maximum Duty Cycle	V_{CS}=0.6 V, V_S=0 V, V_{FB}=4 V	60.0	68.5	77.0	%
V_{GATE-L}	Gate Output Voltage Low		0		1.5	V
$V_{DD-PMOS-ON}$	Internal Gate PMOS Driver ON		7.0	7.5	8.0	V
$V_{DD-PMOS-OFF}$	Internal Gate PMOS Driver OFF		9.0	9.5	10.0	V
t_r	Rising Time	V_{CS}=0 V, V_S=0 V, C_{GATE}=1 nF	100	140	180	ns
t_f	Falling Time	V_{CS}=0 V, V_S=0 V, C_{GATE}=1 nF	30	50	70	ns
$V_{GATE-CLAMP}$	Gate Output Clamping Voltage	V_{DD}=25 V	7.0	7.5	8.0	V

Notes:

4. T_J guaranteed range at 25°C.
5. Design guaranteed.

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Typical Performance Characteristics

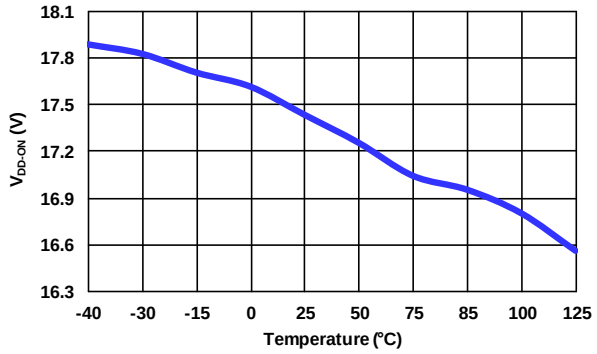


Figure 6. V_{DD} Turn-On Threshold Voltage (V_{DD-ON}) vs. Temperature

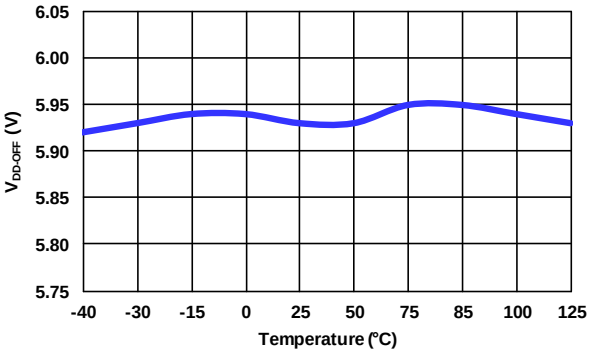


Figure 7. V_{DD} Turn-Off Threshold Voltage (V_{DD-OFF}) vs. Temperature

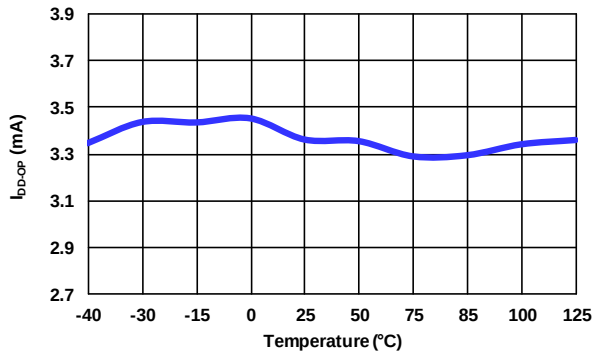


Figure 8. Operating Supply Current (I_{DD-OP}) vs. Temperature

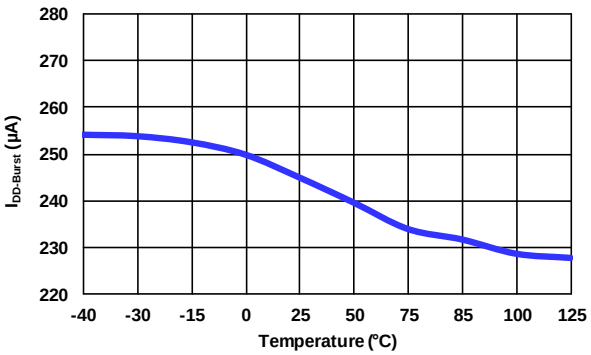


Figure 9. Burst Mode Operating Supply Current ($I_{DD-Burst}$) vs. Temperature

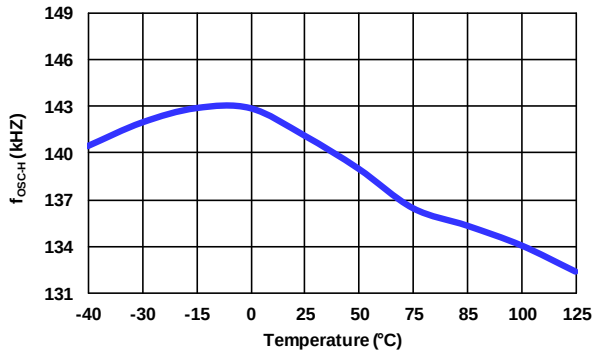


Figure 10. Operating Frequency, $I_{VS} < I_{VS-L}$ Threshold (f_{OSC-H}) vs. Temperature

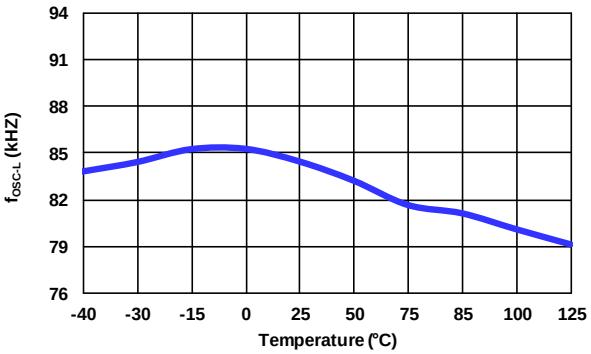


Figure 11. Operating Frequency while $I_{VS} < I_{VS-H}$ Threshold (f_{OSC-L}) vs. Temperature

Typical Performance Characteristics (Continued)

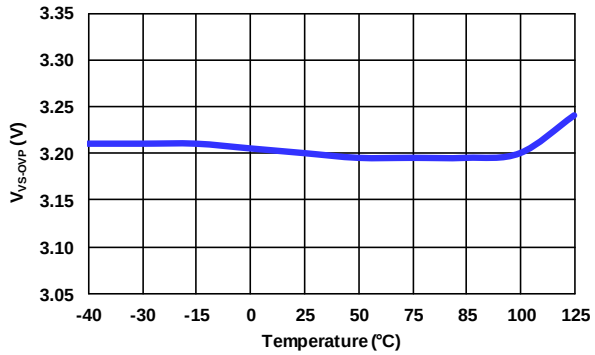


Figure 12. Output OVP with V_S Sampling Voltage (V_{VS-OVP}) vs. Temperature

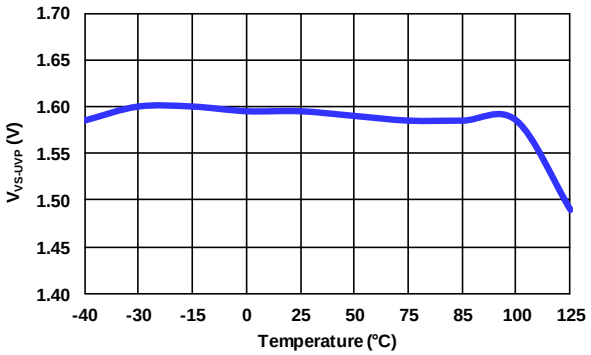


Figure 13. Output UVP with Vs Sampling Voltage (V_{VS-UVP}) vs. Temperature

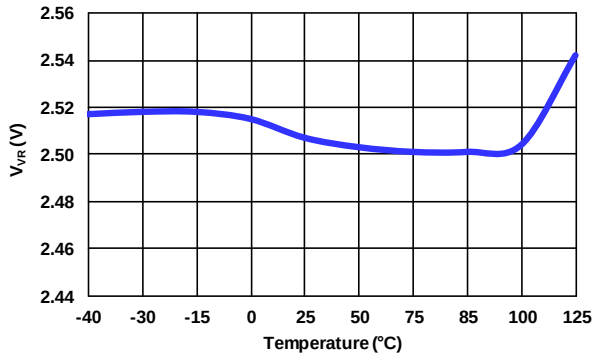


Figure 14. Internal Reference Voltage for CC Regulation (V_{VR}) vs. Temperature

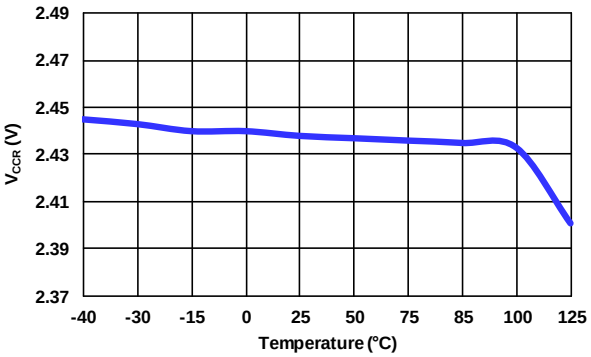


Figure 15. Variation Test Voltage on CS Pin for CC Regulation (V_{CCR}) vs. Temperature

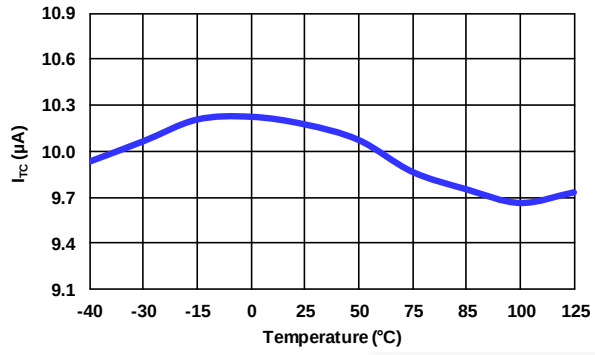


Figure 16. Temperature-Independent Bias Current (I_{TC}) vs. Temperature

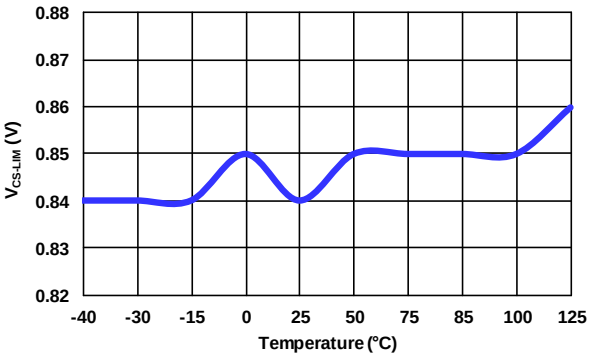


Figure 17. Current Limit Threshold Voltage (V_{CS-LIM}) vs. Temperature

Typical Performance Characteristics (Continued)

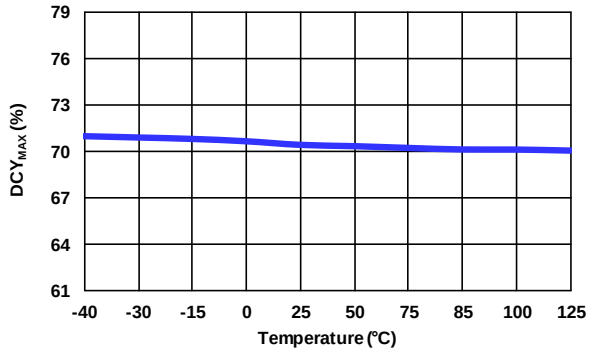


Figure 18. Maximum Duty Cycle (DCY_{MAX}) vs. Temperature

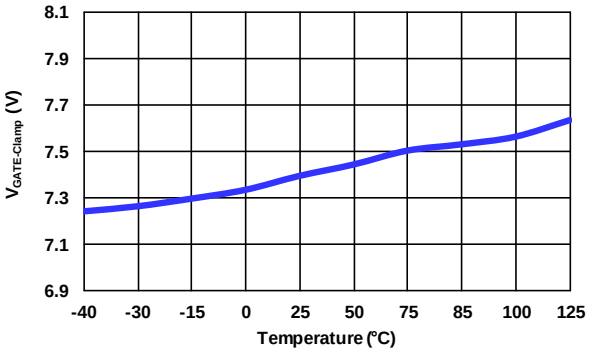


Figure 19. Gate Output Clamping Voltage ($V_{GATE-Clamp}$) vs. Temperature

Functional Description

FAN501 is an offline flyback converter controller that offers constant output voltage (CV) regulation through opto-coupler feedback circuitry and constant output current (CC) regulation with primary-side control. Advanced output current estimation technology allows stable CC regulation regardless of the power stage operation mode: Continuous Conduction Mode (CCM) or Discontinuous Conduction Mode (DCM).

Dual-switching-frequency operation adaptively selects the operational frequency between 85 kHz and 140 kHz according to the line voltage. As a result, the transformer can be fully utilized and high efficiency is maintained over entire line range. A frequency-hopping function is incorporated to reduce EMI noise.

Line voltage information through transformer auxiliary winding is used for dual-switching frequency selection and CC control correction.

mWSaver® technology, including high-voltage startup and ultra-low operating current in Burst Mode, enables system compliance with Energy Star's 5-star requirement of <30 mW standby power consumption.

Protections such as V_{DD} Over-Voltage Protection (V_{DD} OVP), V_S Over-Voltage Protection (V_S OVP), V_S Under-Voltage Protection (V_S UVP), internal Over-Temperature Protection (OTP), Brownout protection and externally triggered shut-down function improve reliability.

All these innovative technologies allow the FAN501 to offer low total cost, reduced component counts, small size / weight, high conversion efficiency, and high power density for compact charger / adapter applications requiring CV / CC control.

CV / CC PWM Operation Principle

Figure 20 shows a simplified CV / CC PWM control circuit of the FAN501. The Constant Voltage (CV) regulation is implemented in the same manner as the conventional isolated power supply, where the output voltage is sensed using a voltage divider and compared with the internal reference of the shunt regulator to generate a compensation signal. The compensation signal is transferred to the primary side through an opto-coupler and scaled down by attenuator AV to generate a COMV signal. This COMV signal is applied to the PWM comparator to determine the duty cycle.

The Constant Current (CC) regulation is implemented internally with primary-side control. The output current estimator calculates the output current using the transformer primary-side current and diode current discharge time. By comparing the estimated output current with internal reference signal, a COMI signal is generated to determine the duty cycle.

These two control signals, COMV and COMI, are compared with an internal sawtooth waveform (V_{SAW}) by two PWM comparators to determine the duty cycle. Figure 21 illustrates the outputs of two comparators, combined with an OR gate, to determine the MOSFET turn-off instant. Of COMV and COMI, the lower signal determines the duty cycle. As shown in Figure 21, during CV regulation, COMV determines the duty cycle while COMI is saturated to HIGH level. During CC regulation, COMI determines the duty cycle while COMV is saturated to HIGH level.

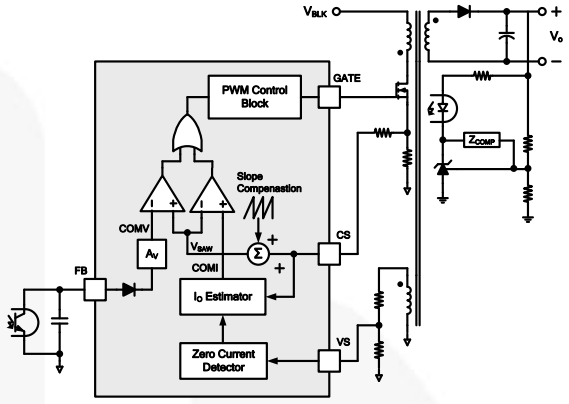


Figure 20. Simplified CV / CC PWM Control Circuit

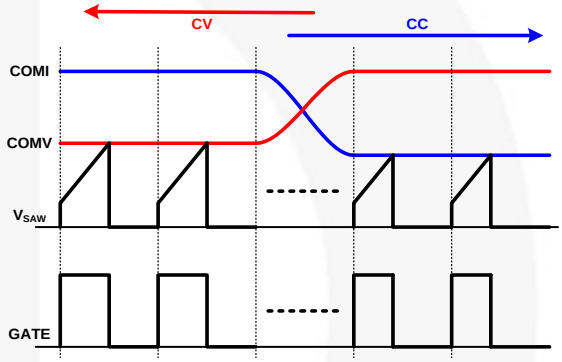


Figure 21. PWM Operation for CV / CC Regulation

Primary-Side Constant Current Operation

Figure 22 and Figure 23 show the key waveforms of a flyback converter operating in DCM and CCM, respectively. The output current of each mode is estimated by calculating the average of output diode current over one switching cycle:

$$I_O = < I_D >_{t_S} = \frac{\int_0^{t_S} I_D(t)dt}{t_S} = \frac{[I_D]_{AREA}}{t_S} \quad (1)$$

The area of output diode current in both DCM and CCM operation can be expressed in a same form, as a product of diode current discharge time (t_{DIS}) and diode current at the middle of diode discharge ($I_{D\text{-}Mid}$), such as:

$$[I_D]_{AREA} = I_{D-Mid} \cdot t_{DIS} \quad (2)$$

In steady state, I_{D_Mid} can be expressed as:

$$I_{D-Mid} = I_{DS_Mid} \cdot \frac{N_P}{N_S} \quad (3)$$

where I_{DS_Mid} is primary-side current at the middle of MOSFET conduction time and N_P/N_S is primary-to-secondary turn ratio.

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The unified output current equation both for DCM and CCM operation is obtained as:

$$I_O = \frac{N_P}{N_S} \cdot I_{DS_Mid} \cdot \frac{t_{DIS}}{t_S} = \frac{N_P}{N_S} \cdot \frac{V_{CS_Mid}}{R_{CS}} \cdot \frac{t_{DIS}}{t_S} \quad (4)$$

V_{CS_Mid} is obtained by sampling the current-sense voltage at the middle of the MOSFET conduction time. The diode current discharge time is obtained by detecting the diode current zero-crossing instant. Since the diode current cannot be sensed directly in the primary side, Zero-Crossing Detection (ZCD) is accomplished indirectly by monitoring the auxiliary winding voltage in the primary side. When the diode current reaches zero, the transformer winding voltage begins to drop sharply. To detect the corner voltage, the V_S is sampled, called V_{SH}, at 85% of diode current discharge time (t_{DIS}) of the previous switching cycle and compared with the instantaneous V_S voltage. When instantaneous voltage of the VS pin drops below V_{SH} by more than 200 mV, the ZCD of diode current is obtained, as shown in Figure 24.

The output current can be programmable by setting current sensing resistor as:

$$R_{CS} = \frac{1}{I_O} \cdot \frac{N_P}{N_S} \cdot \frac{V_{CCR}}{K_{CC}} \quad (5)$$

where V_{CCR} is the internal voltage for CC control and K_{CC} is the IC design parameter, 12 for the FAN501.

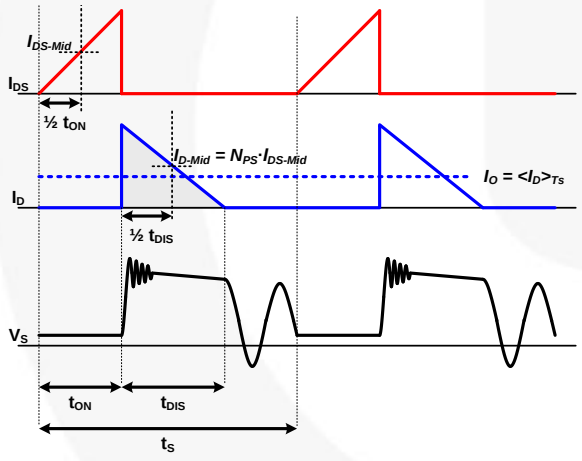


Figure 22. Waveforms of DCM Flyback Converter

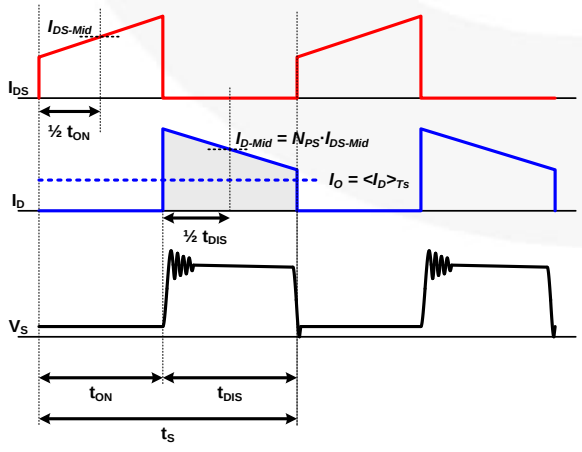


Figure 23. Waveforms of CCM Flyback Converter

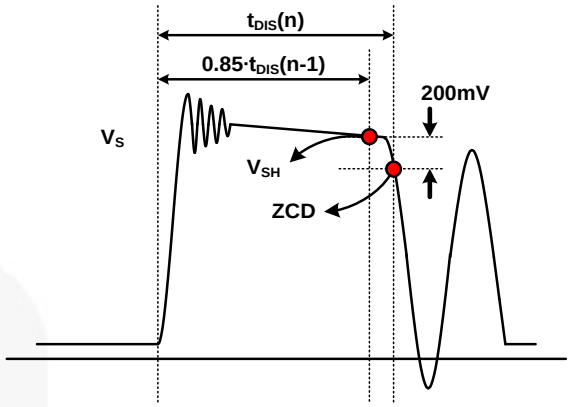


Figure 24. Operation Waveform for ZCD Function

Line Voltage Detection and its Utilization

The FAN501 indirectly senses line voltage using the current flowing out of the VS pin while the MOSFET is turned on, as illustrated in Figure 26 and Figure 27. During the MOSFET turn-on period, auxiliary winding voltage, V_{Aux}, reflects input bulk capacitor voltage, V_{BLK}, by the transformer coupling between primary and auxiliary. During MOSFET conduction time, the line voltage detector clamps the VS pin voltage ~0.5 V and the current, I_{VS}, flowing from the VS pin is expressed as:

$$I_{VS} = \frac{N_A / N_P \cdot V_{BLK}}{R_{VS1}} + \frac{0.5}{R_{VS1} // R_{VS2}} \quad (6)$$

Typically, the second term in Equation (6) can be ignored because it is much smaller than the first term. The current, I_{VS}, is approximately proportional to the line voltage, calculated as:

$$I_{VS} \cong \frac{N_A / N_P}{R_{VS1}} \cdot V_{BLK} \quad (7)$$

The I_{VS} current, reflecting the line voltage information, is used for dual switching frequency operation, CC control correction weighting, and brownout protection; as illustrated in Figure 26.

Dual Switching Frequency

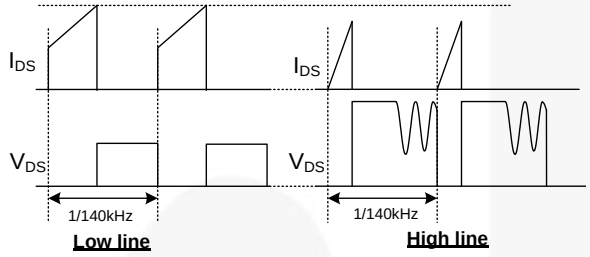
The FAN501 changes the switching frequency between 85 kHz and 140 kHz according to the line voltage. It is typical to design the flyback converter to operate in CCM for low line and DCM in high line. Therefore, the peak transformer current decreases as the operation mode changes from CCM to DCM, as shown in Figure 25(a), for single-frequency operation. The transformer is not fully utilized at high line when a single switching frequency is used. The peak transformer current can be maintained almost constant when the flyback converter operates at lower frequency at high line, as illustrated in Figure 25(b). This allows full transformer utilization and improves the efficiency by decreasing the switching losses at high line.

When I_{VS} is larger than I_{VS-H} (750 µA), the switching frequency is set at f_{OSC-L} (85 kHz) in CV Mode. When I_{VS} is less than I_{VS-L} (680 µA), the switching frequency is set at f_{OSC-H} (140 kHz) in CV Mode. For the universal line range, the frequency change should occur between 132 ~ 180 V_{AC} to avoid the transition within the actual

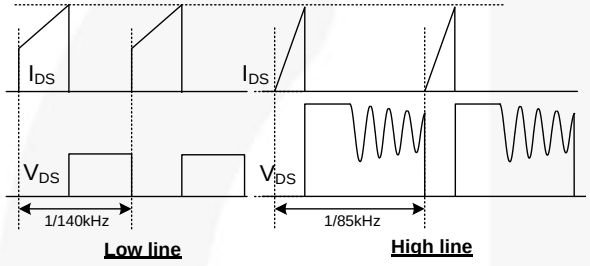
operation range. It is typical to design the voltage divider for the VS pin such that frequency change occurs at 170 V_{AC} (V_{DC}-170 V_{AC} = 240 V); calculated as:

$$R_{VS1} = \frac{N_A / N_P}{I_{VS-H}} \cdot 240 \quad (8)$$

With the value of R_{VS1} determined from Equation (8), the switching frequency drops to 85 kHz as line voltage increases above 170 V_{AC}, while switching frequency increases to 140 kHz, as line voltage drops <155 V_{AC}.



(a) Single frequency operation



(b) Dual frequency operation

Figure 25. Peak Switch Current, Single- and Dual-Frequency Operation

Brownout Protection

Line voltage information is also used for brownout protection. When the I_{VS} current out of the VS pin during the MOSFET conduction time is less than 160 µA for longer than 30 ms, the brownout protection is triggered. When setting R_{VS1} as calculated in Equation (8), the brownout level is set at 30 V_{AC}.

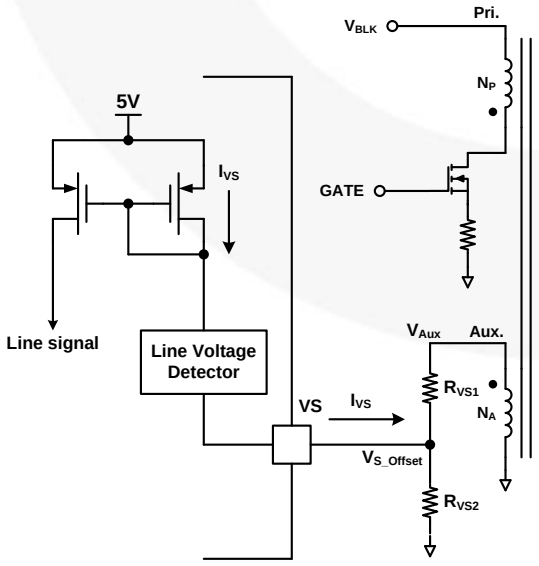


Figure 26. Line Voltage Detection Circuit

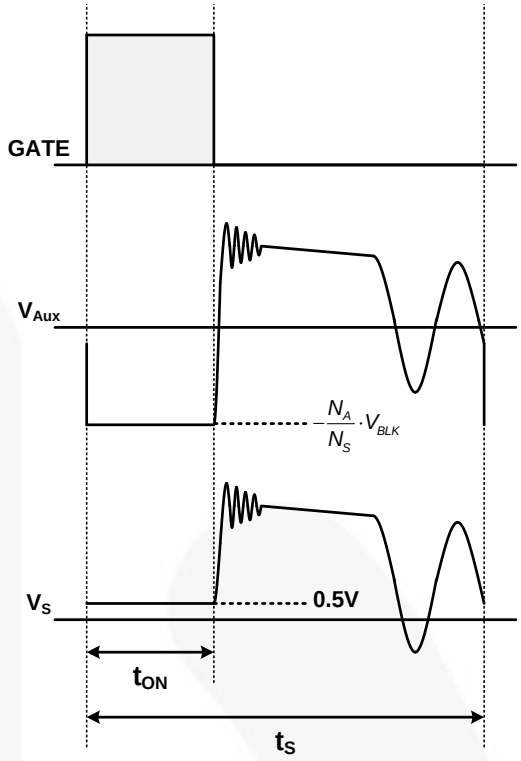


Figure 27. Waveforms for Line Voltage Detection

Maximum Power Limit by Precision CC Control

Primary-side current-sensing voltage is used to estimate the output current for CC regulation. However, the actual output current regulation is also affected by the turn-off delay of the MOSFET, as illustrated in Figure 28. While FAN501 samples the CS pin voltage at the half on-time of gate drive signal, the actual turn-off is delayed by the MOSFET gate charge and driving current resulting in peak current detection error as:

$$\Delta I_{DS}^{PK} = \frac{V_{DL}}{L_m} t_{OFF.DLY} \quad (9)$$

where L_m is the primary side magnetic inductance.

As can be seen, the error is proportional to the line voltage. FAN501 has an internal correction function to improve CC regulation, as shown in Figure 29. Line information is obtained through the line voltage detector as shown in Figure 26 and Figure 27 and this information is used for the CC control correction. The correction gain can be programmed using external resistor R_{COMP} on the COMP pin. This correction current, I_{LVF}, flows through internal resistor, R_{LVF}, and external resistor, R_{CSF}, to introduce offset voltage on current sensing voltage. Thus, the primary current detection error affected by line voltage and turn-off delay is corrected for better CC regulation. The R_{COMP} resistor can be calculated as:

$$R_{COMP} = \frac{N_P}{N_A} \cdot \frac{R_{CS}}{R_{LVF} + R_{CSF}} \cdot R_{VS1} \cdot \frac{t_{OFF.DLY}}{L_m} \cdot K_{COMP} \quad (10)$$

where R_{LVF} is the internal resistor on the IC, which is 2.0 kΩ, and K_{COMP} is the design factor of the IC, which is 3.745 MΩ.

The turn-off delay should be obtained by measuring the time between the falling edge and actual turn-off instant of MOSFET, as illustrated in Figure 28.

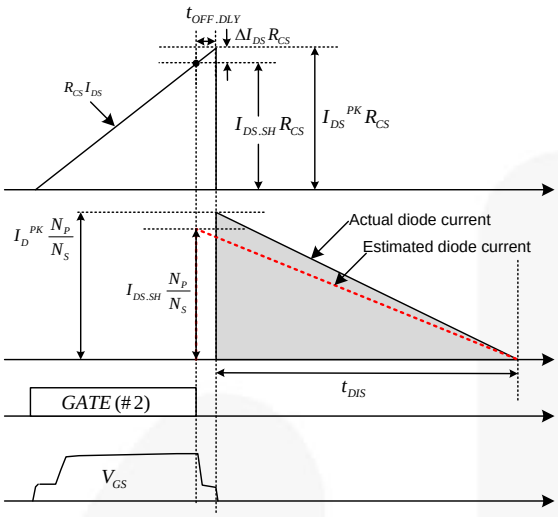


Figure 28. CC Control Correction Concept

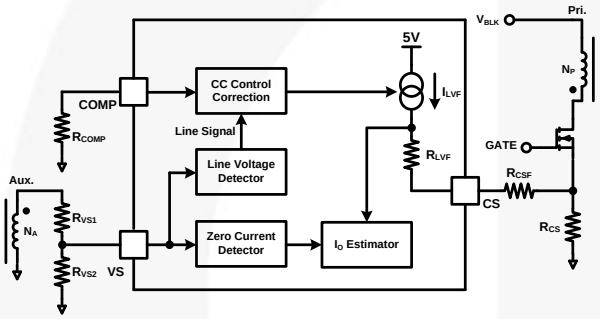


Figure 29. CC Correction Circuit

Pulse-by-Pulse Current Limit

Since the peak transformer current is controlled by a feedback loop, the peak transformer current is not properly controlled when the feedback loop is saturated to HIGH, which typically occurs under startup or overload conditions. To limit the current, a pulse-by-pulse current limit forces the gate drive signal to turn off when the CS pin voltage reaches the current-limit threshold (V_{CS-LIM}) in normal operation.

Burst Mode Operation

The power supply enters Burst Mode at no-load or extremely light-load condition. As shown in Figure 30, when V_{FB} drops below $V_{FB-Burst-L}$, the PWM output shuts off and the output voltage drops at a rate dependent on load current. This causes the feedback voltage to rise. Once V_{FB} exceeds $V_{FB-Burst-H}$, the internal circuit starts to provide a switching pulse. The feedback voltage then falls and the process repeats. In this manner, Burst Mode alternately enables and disables switching of the MOSFET to reduce the switching losses in Standby Mode. In Burst Mode, the operating current is reduced from 3.5 mA to 250 μA to minimize power consumption.

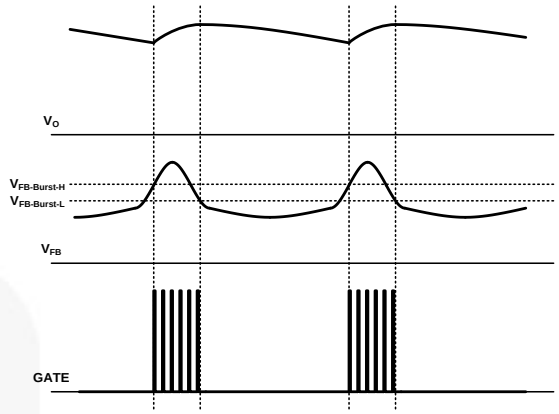


Figure 30. Burst-Mode Operation

Frequency Hopping

EMI reduction is accomplished by frequency hopping, which spreads the energy over a wider frequency range than the bandwidth of the EMI test equipment, allowing compliance with EMI limitations.

Slope Compensation

The sensed voltage across the current-sense resistor is used for current-mode control and pulse-by-pulse current limiting. A synchronized ramp signal with a positive slope is added to the current-sense information at each switching cycle, improving noise immunity during current mode control and avoiding sub-harmonic oscillation during CCM operation.

Leading-Edge Blanking (LEB)

Each time the power MOSFET is switched on, a turn-on spike occurs at the sense resistor. To avoid premature termination of the switching pulse by the spike, a 150 ns leading-edge blanking time is incorporated. Conventional RC filtering can therefore be omitted. During this blanking period, the current-limit comparator is disabled and it cannot switch off the gate driver.

Noise Immunity

Noise from the current sense or the control signal can cause significant pulse-width jitter. Though slope compensation helps alleviate this problem, precautions should be taken to improve the noise immunity. Good placement and layout practices are important. Avoid long PCB traces and component leads and locate bypass capacitor as close to the PWM IC as possible.

High Voltage (HV) Startup

Figure 31 shows the high-voltage (HV) startup circuit for FAN501 applications. The JFET is used to internally implement the high-voltage current source *(see Figure 32 for characteristics)*. Technically, the HV pin can be directly connected to voltage (V_{BLK}) on an input bulk capacitor. To improve reliability and surge immunity, however, it is typical to use a ~100 kΩ resistor between the HV pin and bulk capacitor voltage. The actual HV current with a given bulk capacitor voltage and startup resistor is determined by the intersection of V-I characteristics line and load line, as shown in Figure 32.

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During startup, the internal startup circuit is enabled and the bulk capacitor voltage supplies the current, I_{HV}, to charge the hold-up capacitor, C_{VDD}, through R_{HV}. When V_{DD} reaches V_{DD-ON}, the internal HV startup circuit is disabled and the IC starts PWM switching. Once the HV startup circuit is disabled, the energy stored in C_{VDD} should supply the IC operating current until the transformer auxiliary winding voltage reaches the nominal value. Therefore, C_{VDD} should be designed to prevent V_{DD} from dropping to V_{DD-OFF} before the auxiliary winding builds up enough voltage to supply V_{DD}.

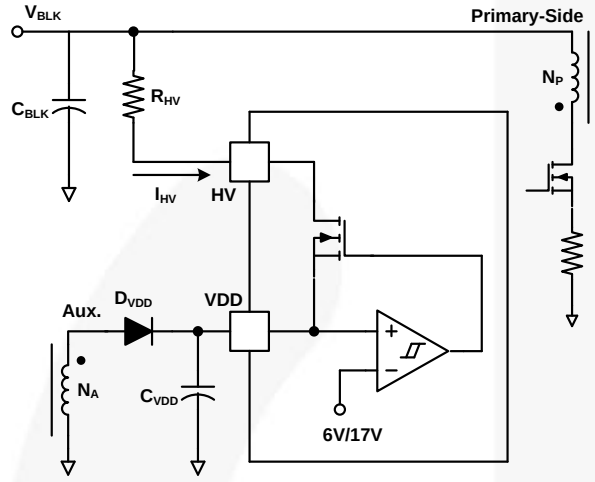


Figure 31. HV Startup Circuit

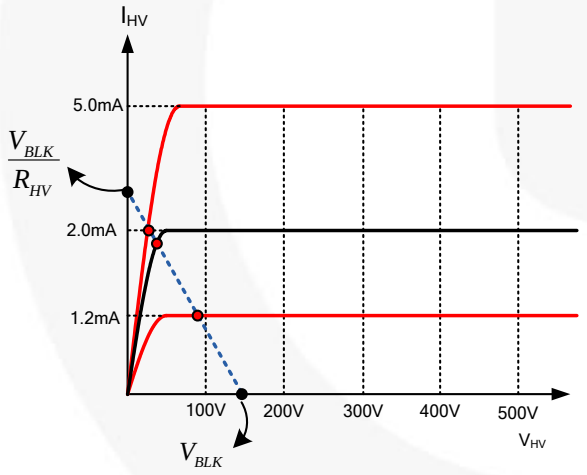


Figure 32. V-I Characteristic of HV Pin

Protections

The protection functions include V_{DD} Over-Voltage Protection (V_{DD} OVP), brownout protection, V_S Over-voltage Protection (V_S OVP), V_S Under-Voltage Protection (V_S UVP), internal Over-Temperature Protection (OTP), and externally triggered shutdown (SD) protection. The V_{DD} OVP and brownout protection are implemented as Auto-Restart Mode. V_S OVP, OTP, and SD protections are implemented as Latch Mode.

When an Auto-Restart Mode protection is triggered, switching is terminated and the MOSFET remains off, causing V_{DD} to drop. When V_{DD} drops to the V_{DD} turn-off voltage of 5.8 V; the protection is reset, the internal startup circuit is enabled, and the supply current drawn from the HV pin charges the hold-up capacitor. When V_{DD} reaches the turn-on voltage of 17.5 V, normal operation resumes. In this manner, Auto-Restart Mode alternately enables and disables MOSFET switching until the abnormal condition is eliminated, as shown in Figure 33.

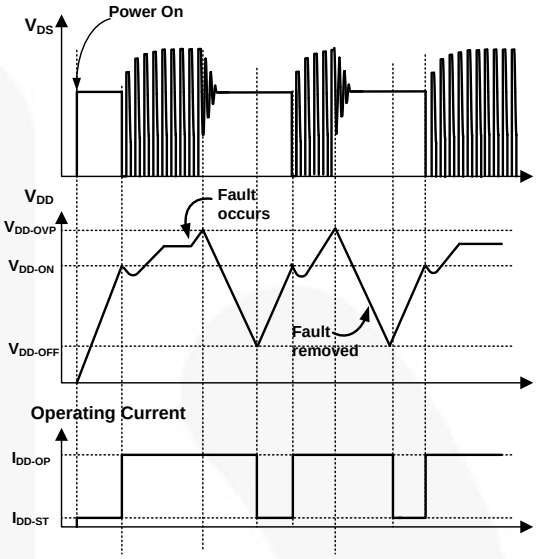


Figure 33. Auto-Restart Mode Operation

When a Latch Mode protection is triggered, PWM switching is terminated and the MOSFET remains off, causing V_{DD} to drop. When V_{DD} drops to the V_{DD} turn-off voltage of 5.8 V, the internal startup circuit is enabled without resetting the protection and the supply current drawn from HV pin charges the hold-up capacitor. Since the protection is not reset, the IC does not resume PWM switching even when V_{DD} reaches the turn-on voltage of 17.5 V, disabling HV startup circuit. Then V_{DD} drops again down to 5.8 V. In this manner, Latch Mode protection alternately charges and discharges V_{DD} until there is no more energy in DC link capacitor. The protection is reset when V_{DD} drops to 2.5 V, which is allowed only after power supply is unplugged from the AC line, as shown in Figure 34.

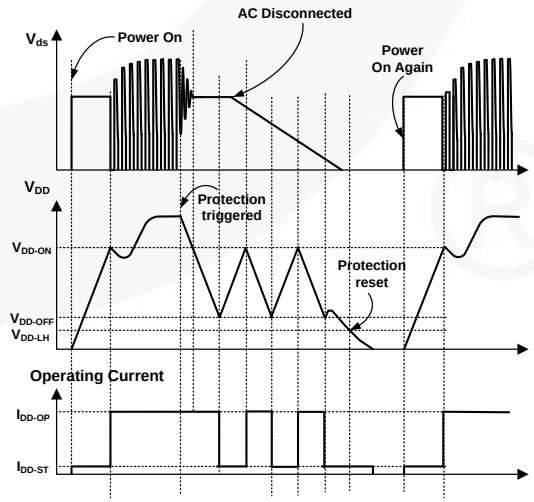


Figure 34. Latch Mode Operation

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V_{DD} Over-Voltage-Protection

V_{DD} over-voltage protection prevents damage from over-voltage exceeding the IC voltage rating. When V_{DD} exceeds 28 V due to an abnormal condition, protection is triggered. This protection is typically caused by an open circuit in the secondary-side feedback network.

Brownout Protection

Brownout protection is implemented through line voltage detection circuit using the auxiliary winding, as shown in Figure 26 and Figure 27. When the current flowing out of the VS pin during the MOSFET conduction time is smaller than 160 µA for longer than 30 ms, the brownout protection is triggered.

Over-Temperature Protection (OTP)

If the junction temperature exceeds 140°C (T_{OTP}), the internal temperature-sensing circuit shuts down PWM output and enters Latch Mode protection.

V_S Under-Voltage Protection (V_S UVP)

Generally, the fold-back point in CC regulation as output drops is determined by the V_{DD-OFF} level. Thus, the fold-back level mainly depends on the characteristics of the V_{DD} diode and transformer. V_S under-voltage protection provides accurate fold-back point control to minimize the effect from the external component tolerance. Figure 35 shows the internal circuit for V_S UVP. By sampling the auxiliary winding voltage on the VS pin around the end of diode conduction time, the output voltage is indirectly sensed. When V_S sampling voltage is less than V_{VS-UVP} (1.55 V) longer than debounce cycles N_{VS-UVP}, V_S UVP is triggered and the FAN501 enters Auto-Restart Mode.

To avoid V_S UVP triggering during the startup sequence, a startup blanking time, $t_{VS-UVP-BLANK}$, (45 ms) in included for system power on. For VS pin voltage divider design, R_{VS1} is obtained from Equation (11) and R_{VS2} is determined by V_S UVP protection function as:

$$R_{VS2} = R_{VS1} \cdot \left(\frac{V_{O-UVP}}{V_{VS-UVP}} \cdot \frac{N_A}{N_S} - 1\right)^{-1} \quad (11)$$

where V_{O-UVP} is the output under-voltage protection level.

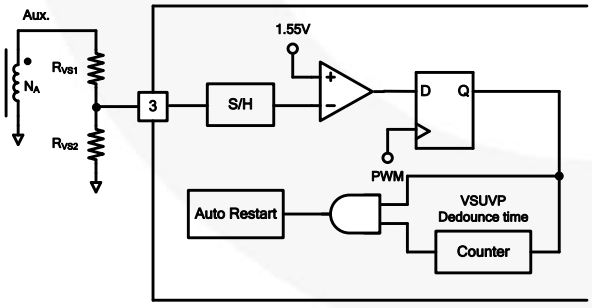


Figure 35. V_S UVP Protection Circuit

V_S Over-Voltage-Protect (V_S OVP)

V_S over-voltage protection prevents damage caused by output over-voltage condition. Figure 36 shows the internal circuit of V_S OVP. When abnormal system conditions occur that cause V_S sampling voltage to exceed V_{VS-OVP} (3.2 V) for more than debounce switching cycles (N_{VS-OVP}), PWM pulses are disabled and the FAN501 enters Latch Mode protection. V_S over-voltage conditions are usually caused by an open circuit in the secondary-side feedback network or a fault condition in the VS pin voltage divider resistors.

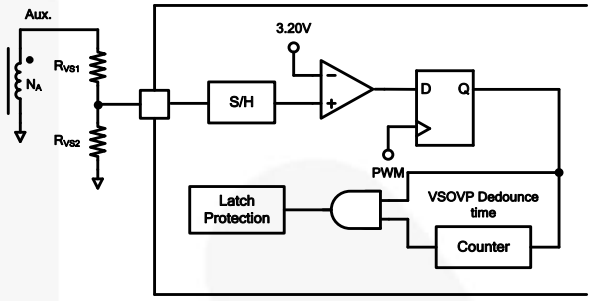


Figure 36. V_S OVP Protection Circuit

Externally Triggered Shutdown

By pulling the SD pin voltage below threshold voltage, V_{SD-TH} (1.0 V); shutdown can be externally triggered and the FAN501 enters Latch Mode protection. It can be also used for external OTP protection by connecting an NTC thermistor between the shutdown (SD) programming pin and ground. An internal constant current source, I_{SD} (100 µA), introduces voltage drop across the thermistor. Resistance of the NTC thermistor becomes smaller as the ambient temperature increases, which reduces the voltage drops across the thermistor. When the voltage of the SD pin is less than threshold voltage V_{SD-TH} (1.0 V), OTP protection is triggered.

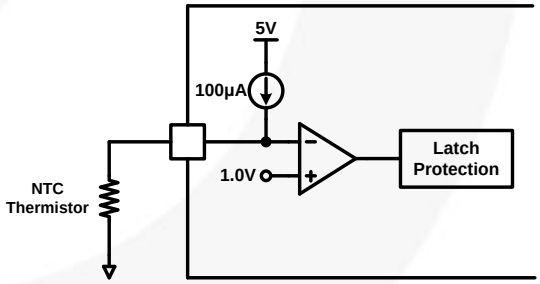
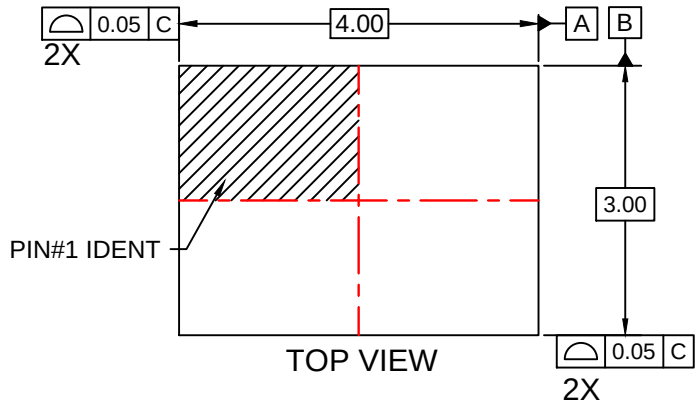
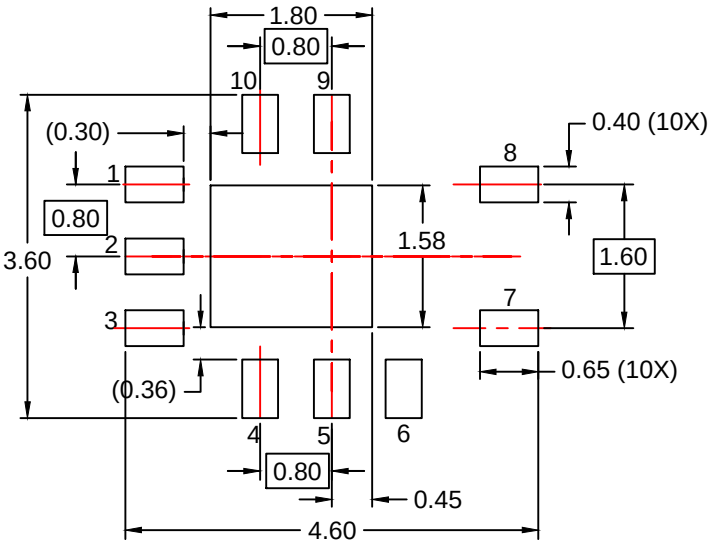
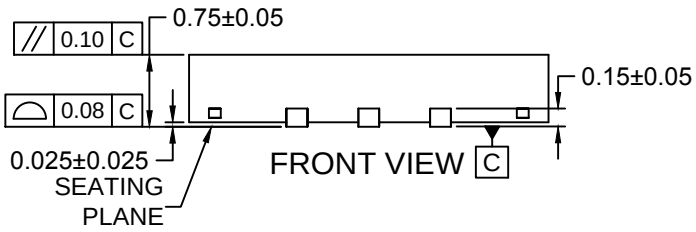


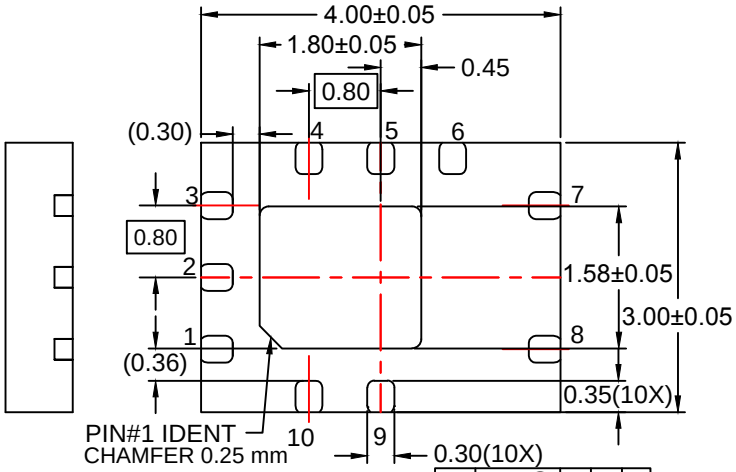
Figure 37. Thermal Shutdown Using SD Pin





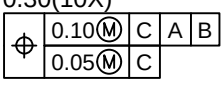
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SIDE VIEW

BOTTOM VIEW





SIDE VIEW

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