UM2120
User manual

EVALSTGAP1AS: demonstration board for STGAP1AS galvanically isolated single gate driver

Introduction

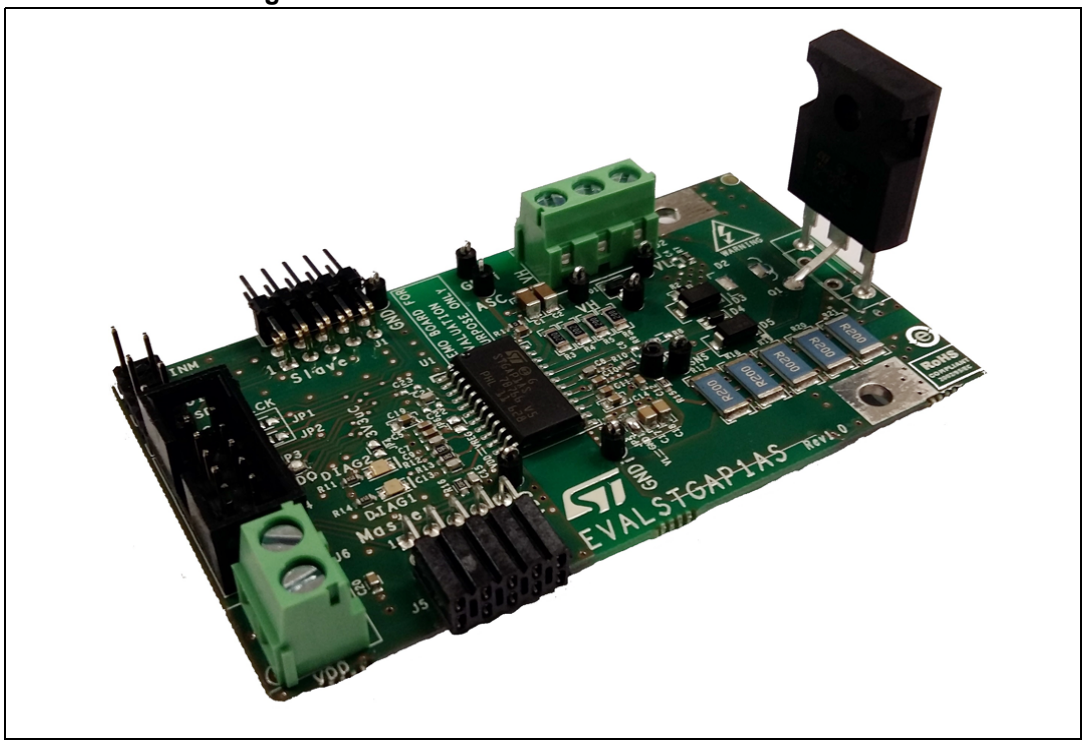
The STGAP1AS is a galvanically isolated single gate driver for N-channel MOSFETs and IGBTs with advanced protection, configuration and diagnostic features. The architecture of the STGAP1AS isolates the channel from the control and the low voltage interface circuitry through a true galvanic isolation.

The EVALSTGAP1AS board allows evaluating all of the STGAP1AS features while driving a power switch with a voltage rating up to 1500 V. Power switches in both TO-220 and TO-247 packages can be evaluated, and the board allows the connection of a heatsink in order to exploit the ability of the STGAP1AS to handle very high power applications.

In combination with the STEVAL-PCC009V2 communication board and the STGAP1AS evaluation software, the board allows to easily enable, configure or disable all of the driver's protection and control features through the SPI interface. Advanced diagnostic is also available thanks to the driver's status registers that can be accessed through the SPI.

Multiple boards can be connected together and share the same logic supply voltage and control signals in order to evaluate half bridge, interleaved or even more complex topologies. The board allows implementing the SPI daisy chain when more than one device is used.

Figure 1. EVALSTGAP1AS demonstration board



Contents

1 Hardware description and configuration

The STGAP1AS features an SPI interface that is used to set the device parameters, enable or disable the device functions and for advanced diagnostic. However for an easy device evaluation it is also possible to operate the STGAP1AS without using the SPI interface. In this case the driver works with default configuration values and protections. For more details refer to *Section 3.1: Using EVALSTGAP1AS in standalone mode on page 10*.

Table 1. STGAP1AS electrical specifications

Symbol	Parameter	Min.	Max.	Unit
VH	Positive supply voltage (VH vs. GNDISO)	4.5(1)	20(2)	V
VL	Negative supply voltage (VL vs. GNDISO)	GNDISO - 10(3)	GNDISO	V
VHL	Differential supply voltage (VH vs. VL)		36	V
VDD	Integrated 3.3 V voltage regulator input voltage vs. GND	4.5	5.5(4)	V
		3	3.6(5)	
V_{LOGIC}	Logic pins voltage vs. GND		VDD + 0.3	V
V_{IORM}	Maximum working voltage across isolation		1500	V
$V_{collector}$	Maximum COLLECTOR-GNDISO voltage		1200(6)	V

1. When UVLO is enabled this value is VH_{on_max}.
2. This value is limited by maximum gate-source voltage of Q1.
3. When UVLO is enabled this value is VL_{on_max}.
4. When JP6 = OPEN (VDD is not connected to VREG pin, refer to STGAP1AS DS).
5. When JP6 = CLOSED (VDD is connected to VREG pin, refer to STGAP1AS DS).
6. This value is limited by the voltage rating of Q1 and D5.

Table 2. Connector descriptions

Name	Type	Function
J1	Board extension connector	Used to connect an optional slave EVALSTGAP1AS board.
J2	Power supply connector	Used to feed supply voltage VH and optional negative supply voltage VL to the gate driving side.
J3	Control signals connector	Used for control (logic inputs and fault signals interfacing).
J4	Control signals connector	Used for the STGAP1AS SPI and diagnostic interfacing. Connector is suitable for interfacing to the STEVAL-PCC009V2 universal interface board.
J5	Board extension connector	Used to connect the master EVALSTGAP1AS board in 2-board configuration.
J6	Power supply connector	Used to feed supply voltage VDD to the logic control side.
C plate	Load connection	A plate hole for the load current input path (IGBT collector).
E plate	Load connection	A plate hole for the load current output path (IGBT emitter).

In applications requiring galvanic isolation, VH and VL must be generated by an isolated power supply. If a power supply with suitable isolation is not available the gate driver's supply voltages can be provided through a battery. In case the evaluation of driver's performance does not require galvanic isolation, any power supply with suitable functional isolation may be used.

Figure 2. Jumper and connector locations - top side

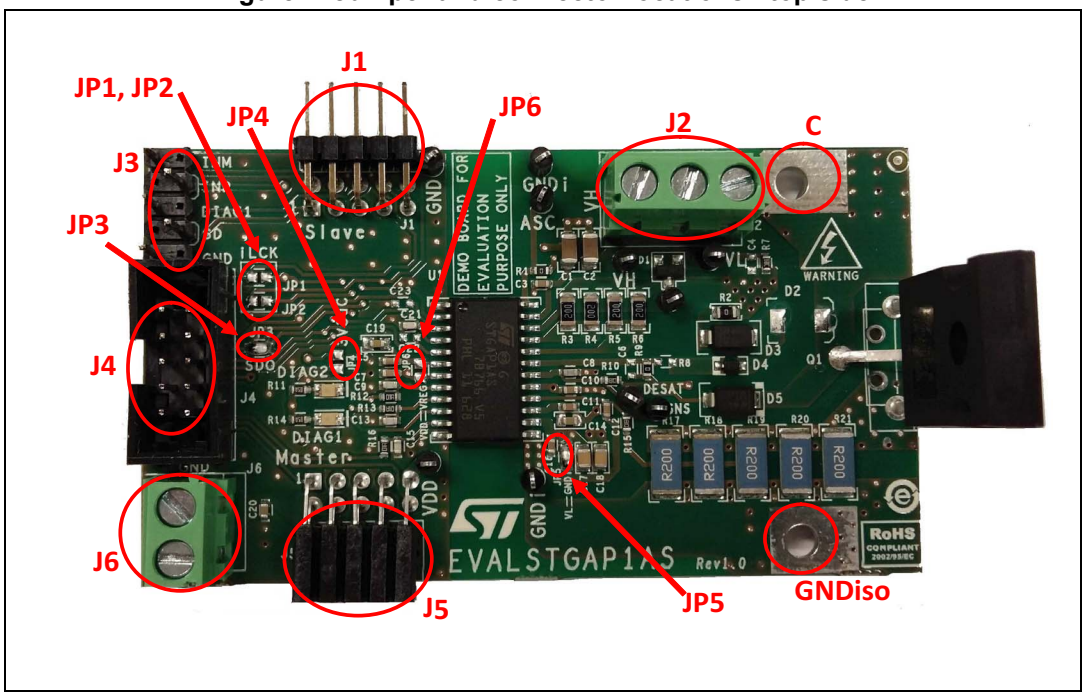


Figure 3. Jumper locations - bottom side

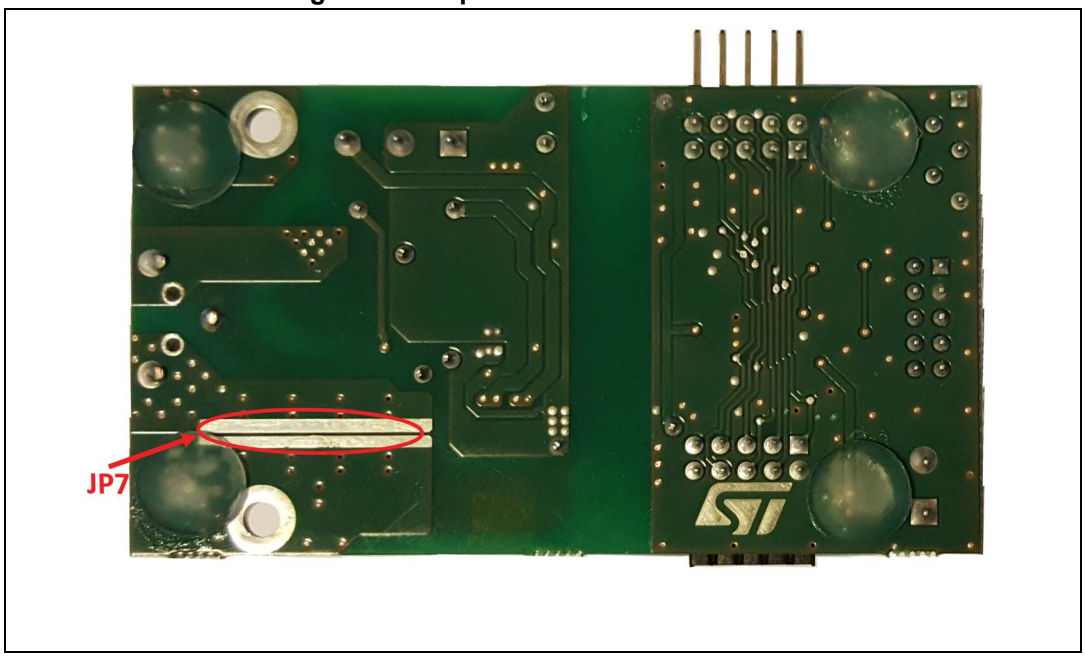


Table 3. Jumper descriptions

Name	Type	Function
JP1, JP2	Configuration jumpers	IN- and IN+ sharing in 2-board configuration.
JP3	Configuration jumper	For SPI daisy chaining in 2-board configuration.
JP4	Configuration jumper	To feed the STGAP1AS with VDD voltage coming from the µC board.
JP5	Configuration jumper	To connect VL and GNDISO if an optional negative power supply VL is not used.
JP6	Configuration jumper	To connect VDD and Vreg when working with VDD = 3.3 V.
JP7	Configuration jumper	To bypass shunt resistors when SENSE is not used.

Table 4. Jumper configurations for VDD power supply(1)

Operating voltage	Supply voltage source	Jumper configurations
VDD = 5 V	External power supply (from J6)	JP4 = OPEN JP6 = OPEN
VDD = 3.3 V	External power supply (from J6)	JP4 = OPEN JP6 = CLOSED
VDD = 3.3 V	µC supply voltage (from J4)	JP4 = CLOSED JP6 = CLOSED

1. Input signals logic levels shall be coherent with VDD voltage (3.3\5 V).

Table 5. Jumper configurations for VL power supply

Operating voltage	Supply voltage source	Jumper configurations
-10 V ≤ VL < 0 V	External power supply (J2)	JP5 = OPEN
VL not used	VL = GNDISO	JP5 = CLOSED

Table 6. Jumper configurations for SPI and input signals settings (single EVALSTGAP1AS)

Name	Function	Jumper configurations
JP1	IN+ connection to the optional slave EVALSTGAP1AS	DON'T CARE
JP2	IN-/DIAG2 connection to the optional slave EVALSTGAP1AS	DON'T CARE
JP3	Connects the SDO to the µC	CLOSED

Table 7. Jumper configurations for SENSE

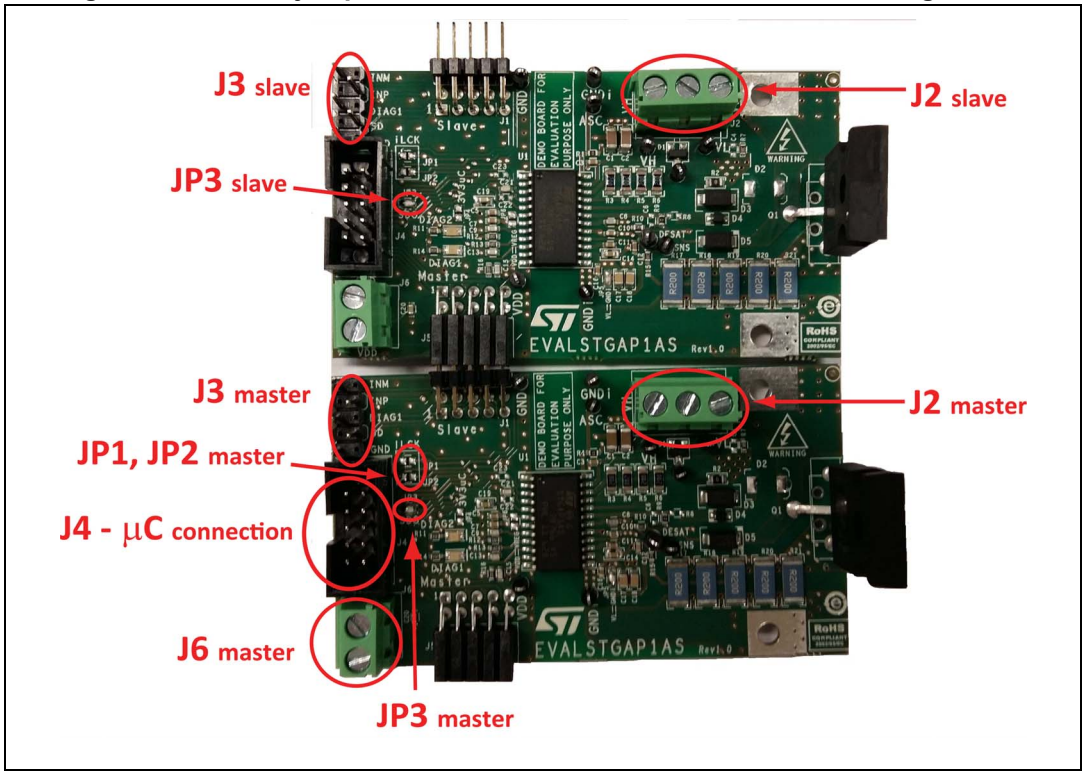
SENSE function	Jumper configurations
Used	JP7 = OPEN
Not used	JP7 = CLOSED(1)

1. This configuration is preferred (but not mandatory) to avoid dissipating power on shunt resistors.

2 Connection of two EVALSTGAP1AS boards

It is possible to connect two EVALSTGAP1AS boards through connectors J1 and J5: the lower board (master) shall be connected to the µC and the other one (slave) is configured through the daisy chain connection of the SPI bus.

Figure 4. Relevant jumper and connector locations for 2-board configuration



Connecting two EVALSTGAP1AS boards allows implementing independent, half bridge, or interleaved configuration of power switches $Q1_m$ and $Q1_s$.

The logic side power supply VDD shall be fed to the J6 of the master board, that will also supply the slave board through J1 - J5 connectors. The jumper JP4 and JP6 of each board shall be properly set (see *Table 4*). A setting of the $JP4_{slave}$ is not relevant.

Positive VH and optional negative VL power supplies for each board shall be independently provided by different sources to connectors $J2_{master}$ and $J2_{slave}$ unless an interleaved operation is required, in which case VH, GNDISO and VL nets of each board shall be externally connected. The jumper JP5 of each board shall be properly configured (see *Table 5*).

Table 8. Jumper configurations for SPI settings using two EVALSTGAP1AS boards

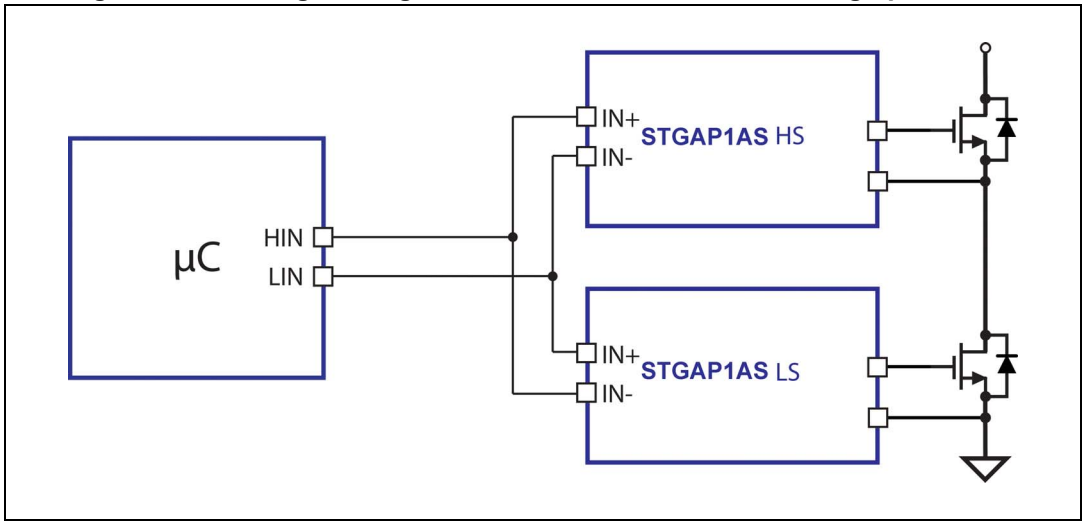
Name	Function	Jumper configurations
$JP3_{master}$	SPI daisy chain configuration	OPEN
$JP3_{slave}$	SPI daisy chain configuration	CLOSED

Lines SD and DIAG1 of both STGAP1AS drivers are shared, whereas it is possible to independently control IN+ and IN-/DIAG2 pins of each driver through appropriate lines of the $J3_{master}$ and $J3_{slave}$.

If the STGAP1AS devices are used in single input configuration both IN-/DIAG2 lines are independently present on the $J4_{master}$ for interfacing with the µC and diagnostic purposes.

If the two boards are used in half bridge configuration ($GNDISO_{slave}$ and C_{master} plate holes shall therefore be connected) it is possible to achieve cross conduction prevention by driving both drivers with only two µC lines as shown in *Figure 5*.

Figure 5. Half bridge configuration with hardware shoot-through protection



In order to use this configuration the STGAP1AS shall be used as 2-input device and the JP1 and JP2 jumpers shall be properly set (see *Table 9*).

Table 9. Jumper configurations for input signal settings

Gate driving configuration	Source of IN+ and IN- control signals	Jumper configurations
Single driver (*Figure 6*)	J3	$JP1_{master}$ = DON'T CARE $JP2_{master}$ = DON'T CARE
Half bridge with hardware shoot-through protection (*Figure 7*)	$J3_{master}$	$JP1_{master}$ = CLOSED $JP2_{master}$ = CLOSED
Half bridge with independent input signals (*Figure 8*)	$J3_{master}$ for master board $J3_{slave}$ for slave board	$JP1_{master}$ = OPEN $JP2_{master}$ = OPEN

Figure 6. Single driver configuration

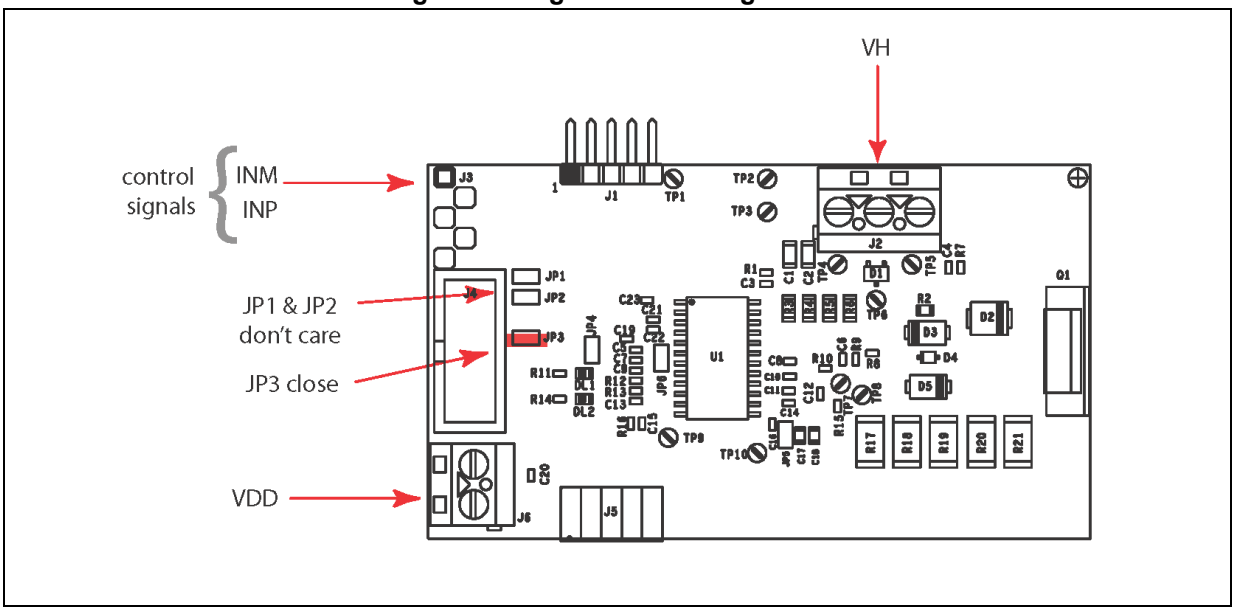


Figure 7. Half bridge with hardware shoot-through protection configuration

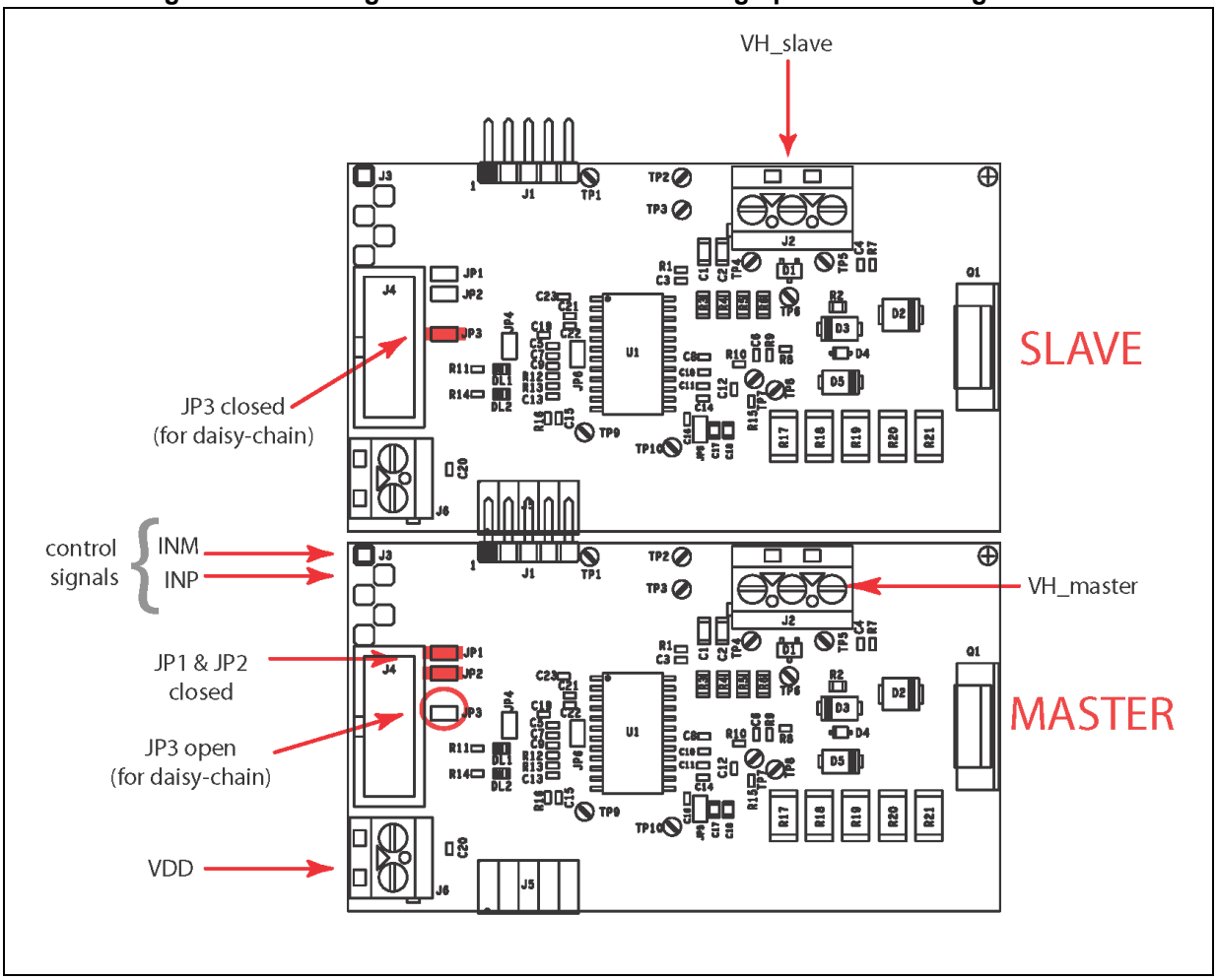
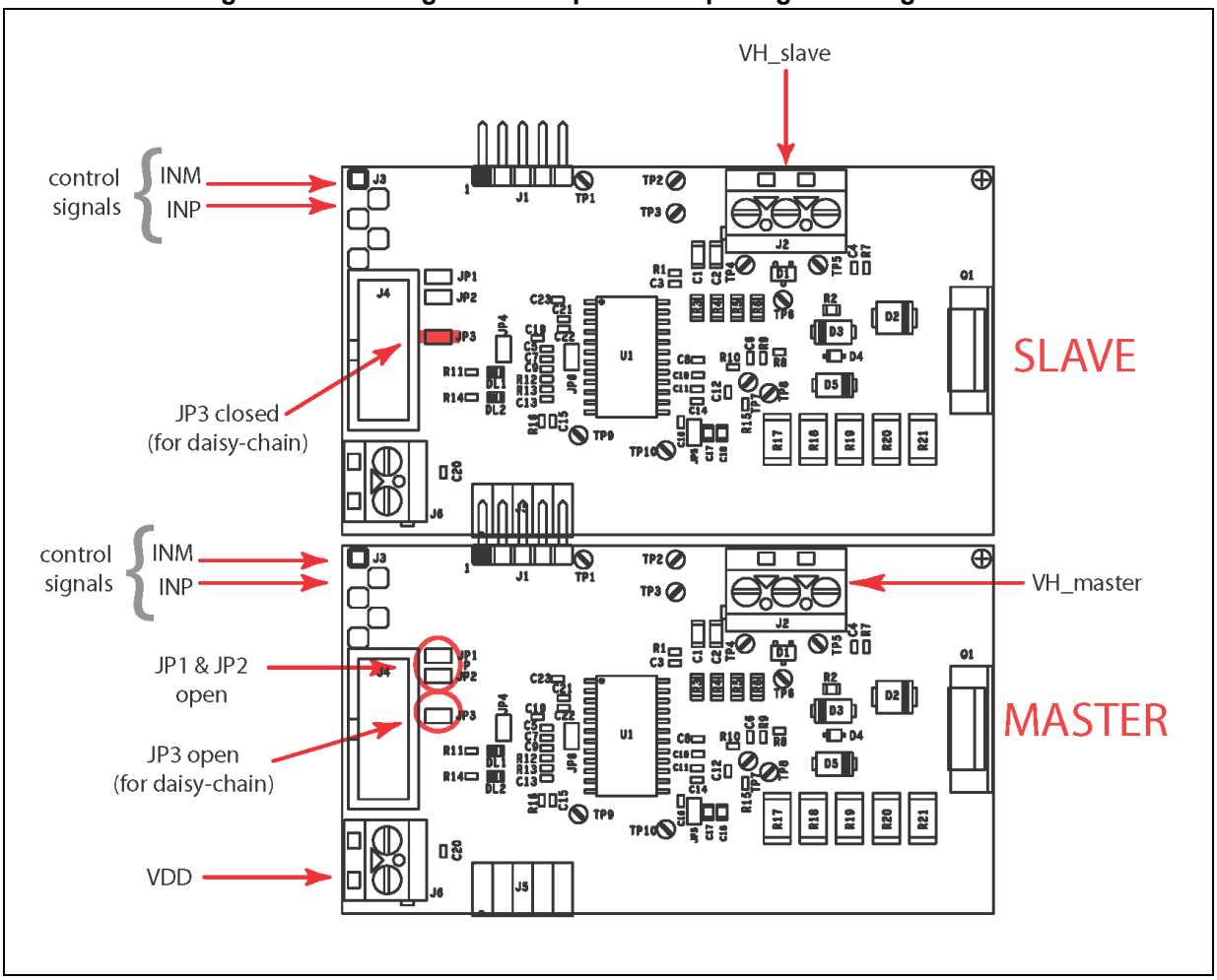


Figure 8. Half bridge with independent input signal configurations



3 Getting started

3.1 Using EVALSTGAP1AS in standalone mode

The STGAP1AS device can work also without SPI programming using the device default values.

3.1.1 Check list

- EVALSTGAP1AS board
- Two power supplies (VDD and VH supply voltage)
  Power supply for negative gate driving voltage VL is optional
- PWM function generator

3.1.2 EVALSTGAP1AS board setup example

1. VDD = 3.3 V or 5 V from external power supply (J6 connector)
2. VH from external power supply (J2 connector)
3. VL = GNDISO (JP5 closed)
4. PWM input signals can be applied to J3 connector (IN-, IN+)

If you have only one PWM signal available:

- To have gate output in phase with input command: PWM on IN+ and IN- = GND
- To have gate output out of phase with input command: PWM on IN- and IN+ = VDD

3.1.3 EVALSTGAP1AS board in standalone mode

1. Connect the power supply to the EVALSTGAP1AS VDD (J6 connector) and turn it on.
   The DIAG1 LED (DL2) on the EVALSTGAP1AS is turned on.
   The status of the DIAG2 depends on the voltage level forced on the IN- pin.
2. Connect the power supply to the EVALSTGAP1AS VH (J2 connector) and turn it on.
3. Set the SD pin low for at least 105 µs to clear the fault (J3 connector).
4. Set the SD pin to the 'High' logic level (which depends on VDD value): the DIAG1 LED (DL2) is switched off.
5. The device outputs will now follow the input signals coming from IN+ and IN-.

3.1.4 EVALSTGAP1AS default parameters

- IN-/DIAG2 configured as input
- Active Miller clamp enabled
- Desaturation detection enabled: $V_{DESATth}$ = 7 V and I_{DESAT} = 250 µA
- VDD OVLO function enabled
- Thermal shutdown protection enabled
- The DIAG1 pin reports the following faults event:
  - DESAT events
  - VDD supply failures
  - Missing VH
  - Thermal shutdown
  - Register error R and L
- All others features are disabled

3.2 Using EVALSTGAP1AS with STEVAL-PCC009V2 and STGAP1AS evaluation software

Using the EVALSTGAP1AS board in connection with the 'STGAP1AS evaluation software' and the STEVAL-PCC009V2 interface board it is possible to evaluate the device functionalities and driving two EVALSTGAP1AS boards implementing independent, half bridge, or interleaved configuration of power switches.

The software allows saving the device parameters configuration in a dedicated file that can be reloaded whenever it is necessary, for example after the board power-on. The 'Save' and 'Load' buttons on the bottom-left side of the STGAP1AS configuration panel (*Figure 10*) have these functions.

3.2.1 Check list

- Microsoft® Windows® 7 or Windows® XP PC with a free USB port
- EVALSTGAP1AS board
- STEVAL-PCC009V2 interface board
- STGAP1AS evaluation software (the right version for your OS)
- Power supply
- PWM function generator
- 10-pin flat cable and USB - MiniUSB cable

3.2.2 Single EVALSTGAP1AS board setup example

1. VDD = 3.3 V from the STEVAL-PCC009V2: closing JP4 and JP6
2. VH from external power supply (J2 connector)
3. VL = GNDISO (JP5 closed)
4. PWM input signals can be applied to the J3 connector (IN-, IN+)

If you have only one PWM signal available:

- To have gate output in phase with input command: PWM on IN+ and IN- = GND
- To have gate output out of phase with input command: PWM on IN- and IN+ = VDD

3.2.3 Connection to STEVAL-PCC009V2 interface board

The EVALSTGAP1AS shall be connected to the interface board and the following steps performed:

1. Connect the interface board to the PC through the USB cable: the red LED (POWER - D2) turns on
2. Connect the interface board 10-pin connector to the EVALSTGAP1AS J4 connector through the 10-pin flat cable

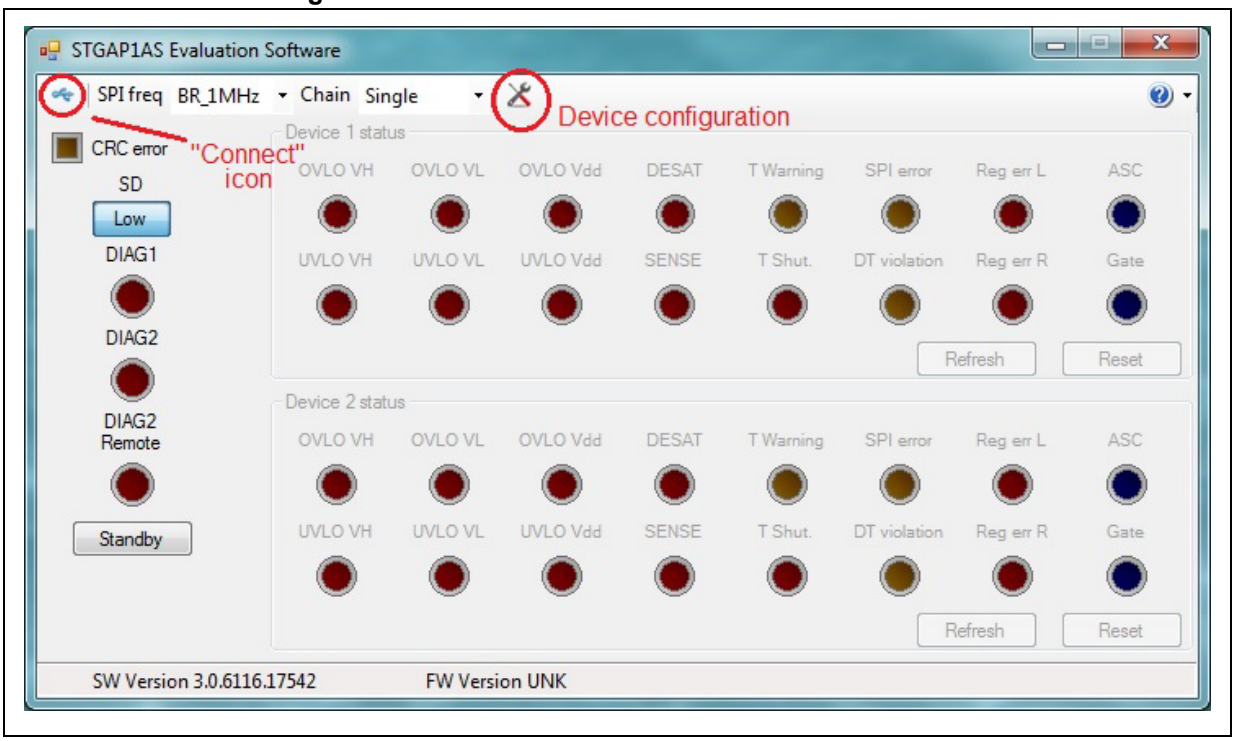
   The DIAG1 red LED (DL2) on the EVALSTGAP1AS turns-on
3. Connect the power supply to VH of the EVALSTGAP1AS (J2 connector) and turn it on
4. Start the EVALSTGAP1AS evaluation software
5. Click the icon 'Connect' on the top left side of the GUI window to establish a connection between the EVALSTGAP1AS and interface boards (see *Figure 9*)

   The DIAG1 LED (DL2) on the EVALSTGAP1AS is switched off
6. Press the 'Refresh' button and verify all fault lights are off. If OK jump to the next point, otherwise two options are available to clear the faults and make the device operative:
   a) Perform a double transition on SD (high => low => high) clicking on the SD button
   b) Perform a status reset clicking on the 'Reset' button and after set the SD button to 'High'
7. Set the SD button to 'High'
8. Connect IN- to GND and applying the PWM on IN+, the device outputs will follow the input signal

In order to read the device status, use the 'Refresh' button to update the status indicators according to driver's status registers.

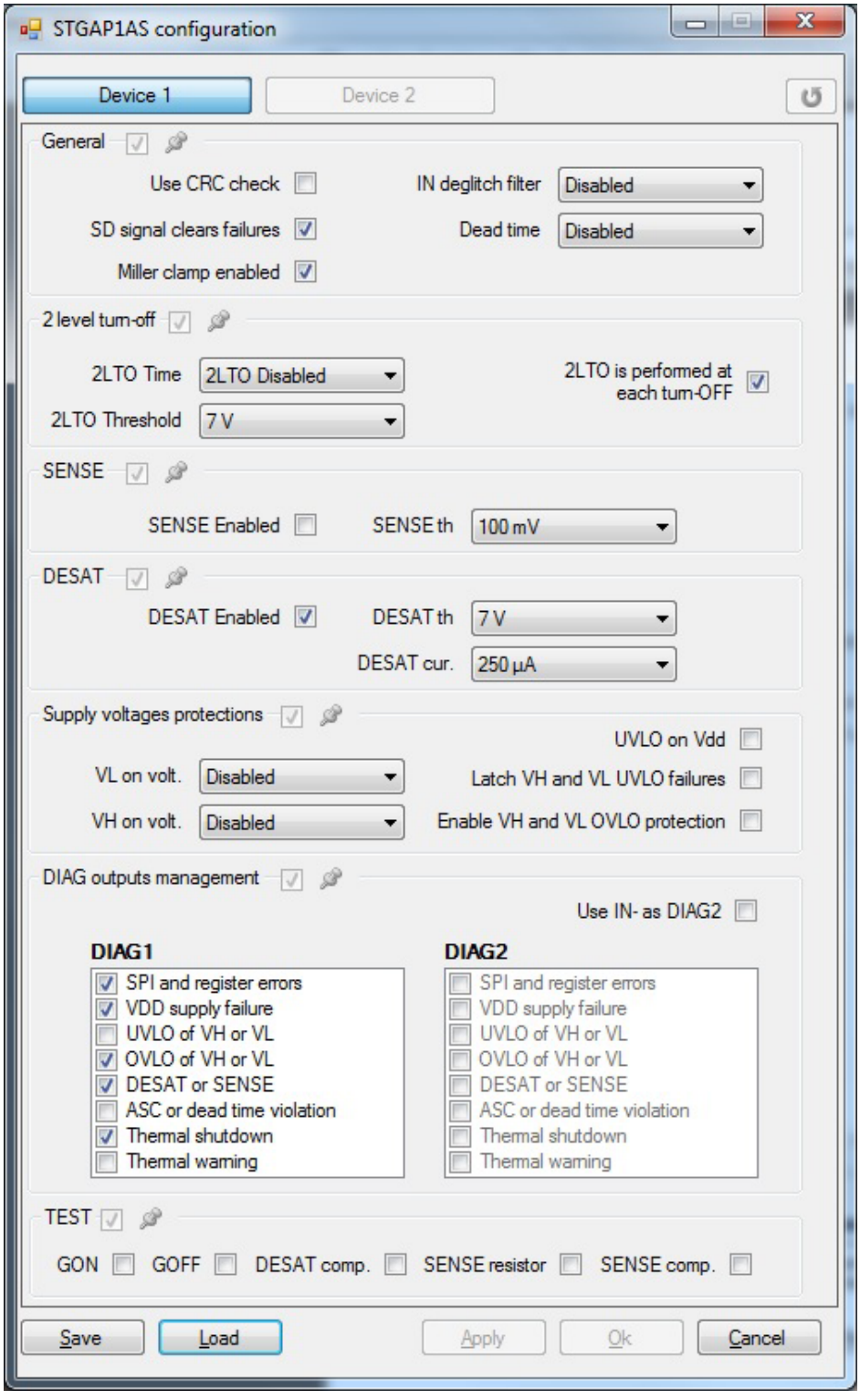
To customize the device parameters and functions open the 'STGAP1AS configuration' panel pushing the relative toolbar icon (refer to *Figure 9*).

Figure 9. STGAP1AS evaluation software screenshot



In the new window shown in *Figure 10*, it is possible to enable or disable the device functionalities and set the device parameters.

Figure 10. STGAP1AS configuration panel



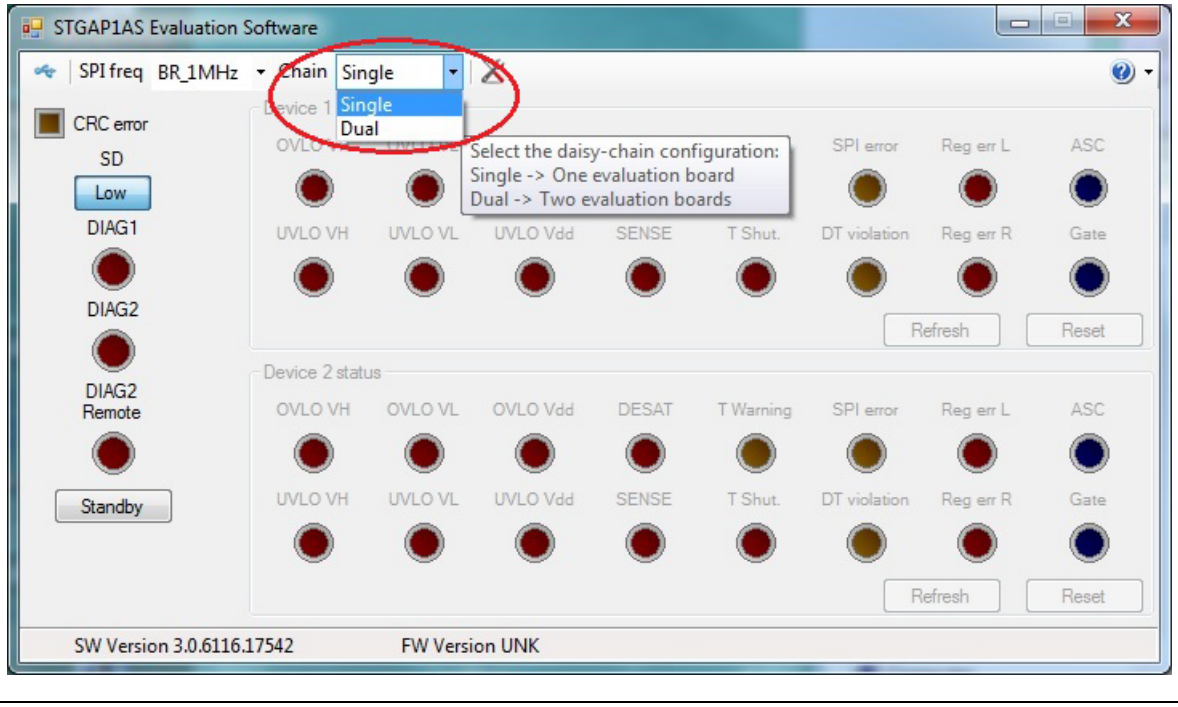
Note: The CRC error light will blink if the CRC check is not used ('Use CRC check' not ticked in the STGAP1AS configuration panel) as in the default settings.

3.2.4 Using two EVALSTGAP1AS boards in daisy chain configuration

If you want to drive two EVALSTGAP1AS boards refer to dedicated *Section 2: Connection of two EVALSTGAP1AS boards on page 6* for the board's connection and jumper's settings, then follow the steps of *Section 3.2.3: Connection to STEVAL-PCC009V2 interface board* up to point *5*.

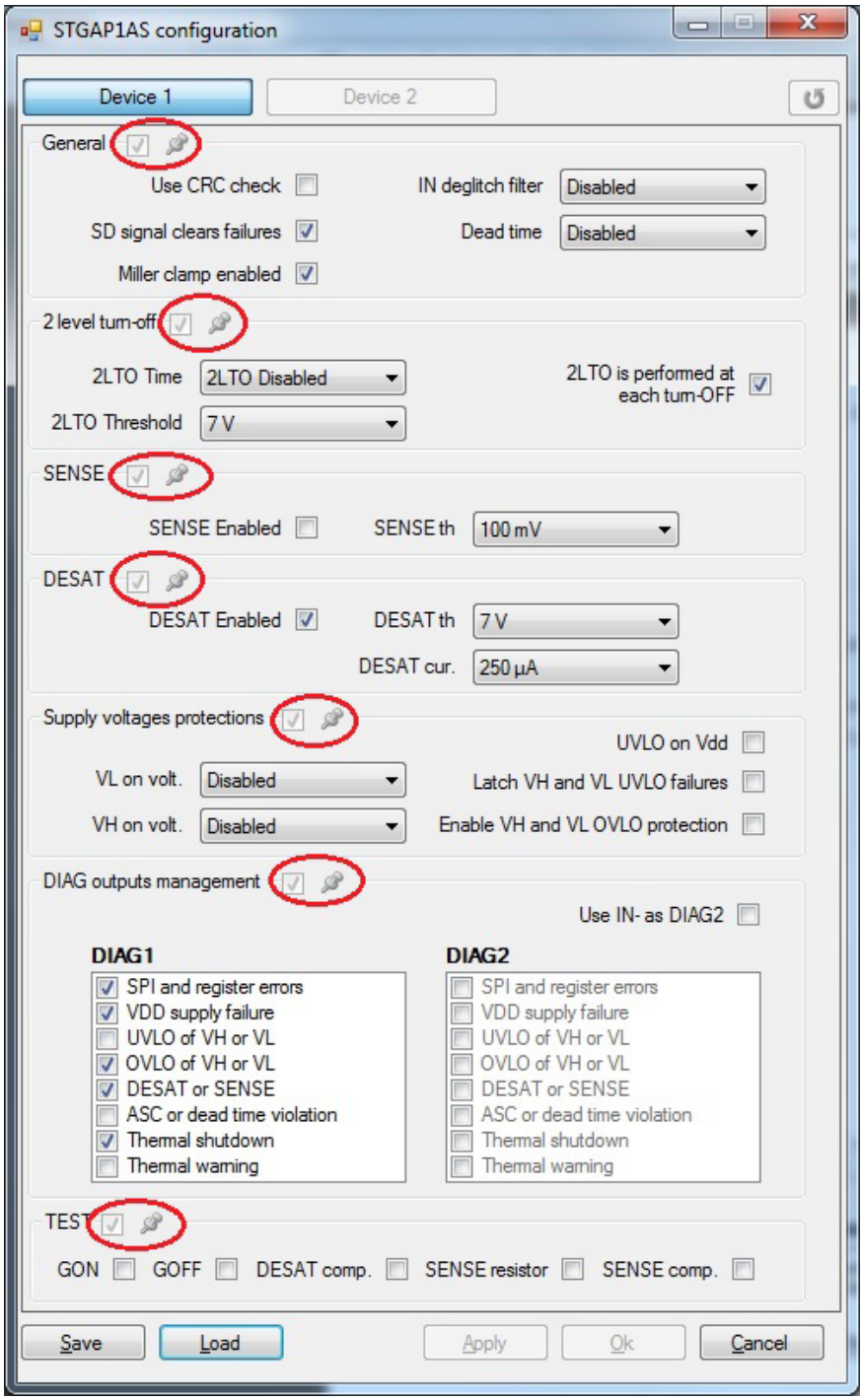
It is possible to set the driven device number using the drop down list in the software main panel.

Figure 11. How to drive two EVALSTGAP1AS boards with STGAP1AS evaluation software



When the 'Dual' option is selected the devices parameters can be set independently selecting the 'Device 1' or 'Device 2' in the STGAP1AS configuration panel. Otherwise it is possible to set some parameter values on both devices ticking one or more 'push-pin' boxes (refer to *Figure 12*).

Figure 12. How to set the same parameters in both devices



4 Revision history

Table 10. Document revision history

Date	Revision	Changes
03-Nov-2016	1	Initial release.