Zynq-7000 All Programmable SoC: ZC702 Evaluation Kit and Video and Imaging Kit (ISE Design Suite 14.5)

Getting Started Guide

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Revision History

The following table shows the revision history for this document.

Date	Version	Revision
05/25/2012	1.0	Initial Xilinx release.
05/29/2012	1.1	Added Figure 4-3 and the text just before and after it.
06/21/2012	1.2	Chapter 1, Introduction: Added a "Reference Designs and Demonstrations" group to section ZC702 Evaluation Kit Contents, page 8. Changed cable from Digilent USB JTAG to Digilent USB-to-JTAG. Added that the SD MMC card contains bootable configuration files for the Base TRD demo design files and Linux applications platform. Updated USB JTAG interface information and added details to the clock sources list in section For reference design files, documents, and board source files, go to the ZVIK Product Page at www.xilinx.com/ZVIK and click on the Docs & Designs tab., page 10. Changed FMC1 and FMC2 connector types to LPC I/O expansion connectors. Added tables of default settings to the section Default Jumper and Switch Settings, page 11. Chapter 2, ZC702 Evaluation Kit Built-In Self-Test: Updated switch settings in the Introduction, page 15. Added bring-up details through the chapter. Settings were added to section Run the BIST Application, page 22. Added Chapter 3, Getting Started with the Base Targeted Reference Design. Added Chapter 4, Using the AMS101 Evaluation Card. Additional references were added through the book and to Appendix A, Additional Resources.
09/18/2012	2.0	The ZC702 evaluation kit now includes a USB Micro-B to female A adapter. Added information about the Zynq-7000 AP SoC Video and Imaging Kit (ZVIK) to the Overview, page 7 and a new section Zynq-7000 AP SoC Video and Imaging Kit Contents, page 10. Photos are updated in Figure 1-3: *Feature Callout for the ZC702 Board* and Figure 2-2: *ZC702 with the UART and Power Cable Attached*. The TRD Demonstration Procedure, page 30 adds information on how to demo the video application using an external video source supporting use of the ZVIK. Added Table 3-1 and Table 3-2. Added support for 720p video resolution in the video demo application in Running the Video Demonstration for 720p Video Resolution, page 39.
11/12/2012	2.1	Updated for ISE® Design Suite v14.3. Document and web site references changed throughout the book. In BIST Setup Requirements, page 15, "A power adapter and power cable for the ZC702 board" was removed. In ZC702 Evaluation Board Setup, page 16, step 1 changed. In Install the USB-UART Driver, page 18,step 1 and step 2 changed. An introduction was added to Chapter 3. In Base TRD Key Features, page 27, "1 GB DDR3 running at 533 MHz" was removed. In Base TRD Hardware Setup Requirements, page 28, `zImage` and `ramdisk8M.image.gz` became `uImage` and `uramdisk8M.image.gz`. The USB stick (or key) is not included in the kit. Instead, download files from the ZC702 Product Page at www.xilinx.com/zc702 and click on the **Docs & Designs** tab. Standoffs and a new Figure 3-3 showing mounting hardware details were added to TRD Demonstration Procedure, page 30. Figure 3-6 and Figure 3-7 were replaced to illustrate the QT-based GUI and minimized GUI mode. USB key was removed from Chapter 4. *Next Steps* became Chapter 5.

Date	Version	Revision
01/24/2013	3.0	Updated for ISE Design Suite 14.5. Revised eighth bullet on page 28 to replace sentence ending in "to exercise the portions of the demo ..." to be "use the frame buffer console terminal that will come up, once user exit the demo." Added third note on page 29. Revised Figure 3-6, page 34 and Figure 3-7, page 35.
02/12/2013	3.0.1	Removed stray internal draft banner from the cover page, and from the first page in each chapter and appendix.
05/14/2013	4.0	Deleted "Key Features of the ZC702 Evaluation Board" section. The Base TRD Key Features, page 27 were updated for the Programmable Logic (PL) to "One Performance Monitor". The required binaries in Base TRD Hardware Setup Requirements, page 28 were updated to include "`zynq-zc702-base-trd.dts`". Port "P1" was labelled in Figure 3-2. Figure 3-6 and Figure 3-7 were replaced to illustrate the QT-based GUI and minimized GUI mode. In Running the Video Demonstration for 720p Video Resolution, page 39, the instructions were updated for running QT based GUI in 720p mode and running the UART Menu based Demonstration Application in 720p mode.

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Introduction

Overview

The Zynq™-7000 All Programmable SoC (AP SoC) ZC702 evaluation kit shown in Figure 1-1 is based on the XC7Z020 CLG484-1 AP SoC. For additional information, see the Zynq-7000 AP SoC product table [Ref 1]. A built-in self-test (BIST) is provided for the ZC702 evaluation kit. The BIST provides a convenient way to test many of the board's features on power-up. The tutorials and reference designs available on the ZC702 product page can be used to further explore the capabilities of the ZC702 board and the Zynq-7000 AP SoC [Ref 2]. For the most up-to-date information on the content provided with the ZC702 evaluation kit, see the Zynq-7000 SoC ZC702 Evaluation Kit Product Page www.xilinx.com/zc702. UG873, *Zynq-7000 All Programmable SoC: Concepts, Tools, and Techniques* shows the basic hardware and software flow using the ZC702 board. The Zynq-7000 AP SoC documentation page is also helpful [Ref 3].

Figure 1-1: **ZC702 Evaluation Kit**

The Zynq-7000 AP SoC Video and Imaging Kit (ZVIK) shown in Figure 1-2 is based on the ZC702 evaluation kit and includes all of the components of the ZC702 kit with the

addition of components enabling HD video input from an High-Definition Multimedia Interface (HDMI™) source or from the included HD image sensor. All of the information presented in this guide related to the ZC702 evaluation kit applies to the ZVIK. For the most current information on the content provided with the ZVIK, see the Zynq-7000 All Programmable SoC Video and Imaging Kit product page [Ref 4].

Figure 1-2: **Zynq-7000 AP SoC Video and Imaging Kit**

This user guide also describes a Base Targeted Reference Design (TRD) based on Zynq-7000 AP SoC architecture. The Base TRD showcases various features and capabilities of the Zynq Z-7020 AP SoC for the embedded domain in a single package.

TRDs are key components of the Xilinx Targeted Design Platform (TDP) strategy. TDPs from Xilinx provide customers with basic scalable design platforms for the creation of FPGA-based solutions in a wide variety of applications and industries.

Note: In the remainder of this document, the Zynq-7000 AP SoC ZC702 evaluation kit is referred to as the *ZC702 Evaluation Kit* and the Zynq-7000 AP SoC Video and Imaging Kit is referred to as *ZVIK*.

ZC702 Evaluation Kit Contents

The ZC702 evaluation kit includes the following items:

- ZC702 evaluation board featuring the XC7Z020 CLG484-1
- Agile Mixed Signal (AMS) evaluation board
- Full seat ISE® Design Suite Embedded Edition design tools
  - Device-locked to the Zynq-7000 XC7Z020 CLG484-1 device

- Board design files
  - Schematics
  - Board layout files
  - Bill of materials
- Documentation
  - *Getting Started Guide* (this document)
  - Hardware user guide (UG850, *ZC702 Evaluation Board for the Zynq-7000 XC7Z020 All Programmable SoC User Guide*)
  - TRD user guide (UG925, *Zynq-7000 All Programmable SoC ZC702 Base Targeted Reference Design User Guide*)
- Reference Designs and Demonstrations
  - BIST Utility and Demonstration
  - Targeted Reference Design (TRD), demonstrating a video processing pipeline.

    Note: The video demonstration contains the licensed IPs with no timeout. To recompile this design, the user needs to register for an evaluation IP license for the Video IP.
  - AMS demonstration, providing an overview of the analog capabilities of the Zynq-7000 AP SoC devices.
- 12V AC adapter power supply
- Cables
  - RJ-45 Ethernet cable
  - HDMI cable
  - USB Type-A to USB Micro-B cable (Digilent USB-to-JTAG Programing Port)
  - USB Type-A to USB Mini-B cable (serial UART)
  - USB Micro-B to female A adapter (for connecting USB hub, keyboard, and mouse)
- Secure Digital Multimedia Card (SD MMC) (contains bootable configuration files for the Base TRD demonstration design files and Linux platform applications)

The kit contains the software and reference designs, a demonstration, and documents to help the user get started quickly.

For reference design files, documents, and board source files, go to the ZC702 Product Page at www.xilinx.com/zc702 and click on the **Docs & Designs** tab.

Zynq-7000 AP SoC Video and Imaging Kit Contents

The ZVIK contains all of the items included in the ZC702 evaluation kit plus the following items. For more information on the HDMI input/output FMC module and ON Semiconductor image sensor, refer to the Avnet product page [Ref 10].

- HDMI input/output FPGA mezzanine card (FMC) module
- ON Semiconductor VITA 2000 Color Image Sensor module
- Standard interchangeable $^{2}/_{3}$-inch 8 mm C-mount lens
- Infrared (IR) cut filter
- Camera tripod
- Lens holder
- Cables
  - Second HDMI cable
  - LCEDI image sensor cable

For reference design files, documents, and board source files, go to the ZVIK Product Page at www.xilinx.com/ZVIK and click on the **Docs & Designs** tab.

Key Features of the ZVIK

Key features of the additional components of the Zynq-7000 AP SoC Video and Imaging kit include:

- HDMI input/output FMC module
  - HDMI input
  - HDMI output
  - Video clock synthesizer
  - Interface for ON Semiconductor VITA image sensor module
- ON Semiconductor VITA 2000 color image sensor module
  - Supports up to WXGA resolution: 1920 (H) x 1200 (V) format
  - 92 frames per second (fps) at full resolution
  - 4.8 µm x 4.8 µm pixel size $^{2}/_{3}$-inch optical format
  - Pipelined and triggered global shutter, rolling shutter

- Random programmable region of interest (ROI) readout
- Automatic exposure control (AEC)

- Standard interchangeable $^{2}/_{3}$-inch, 8 mm C-mount lens

Default Jumper and Switch Settings

Figure 1-3 calls out the major features on the ZC702 board. See UG850, *ZC702 Evaluation Board for the Zynq-7000 XC7Z020 All Programmable SoC User Guide* for more detailed information about the ZC702 board.

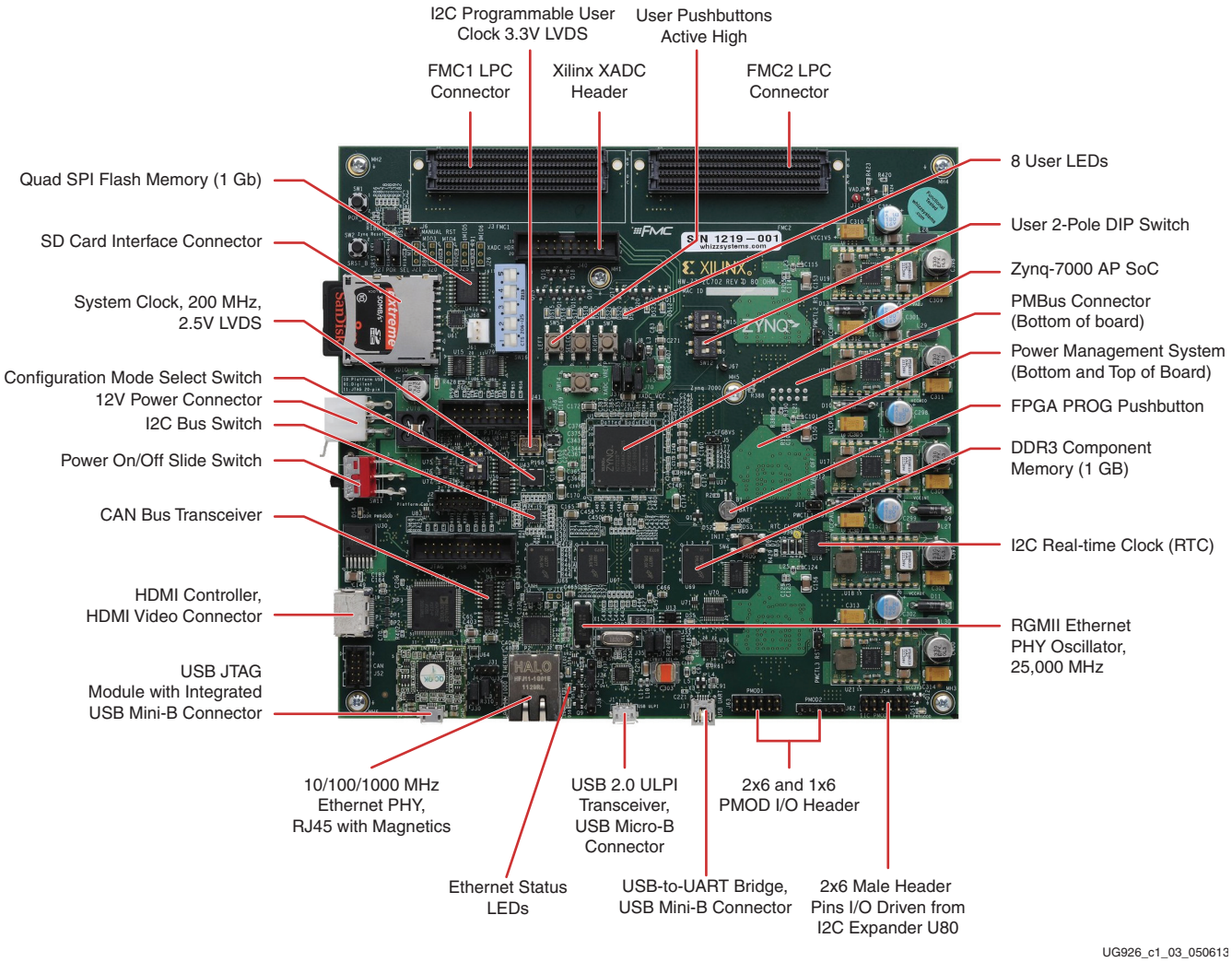


Figure 1-3: **Feature Callout for the ZC702 Board**

Default factory settings of jumpers and switches on the ZC702 board are highlighted in Figure 1-4. Default switch and jumper settings are listed in Table 1-1 and Table 1-2.

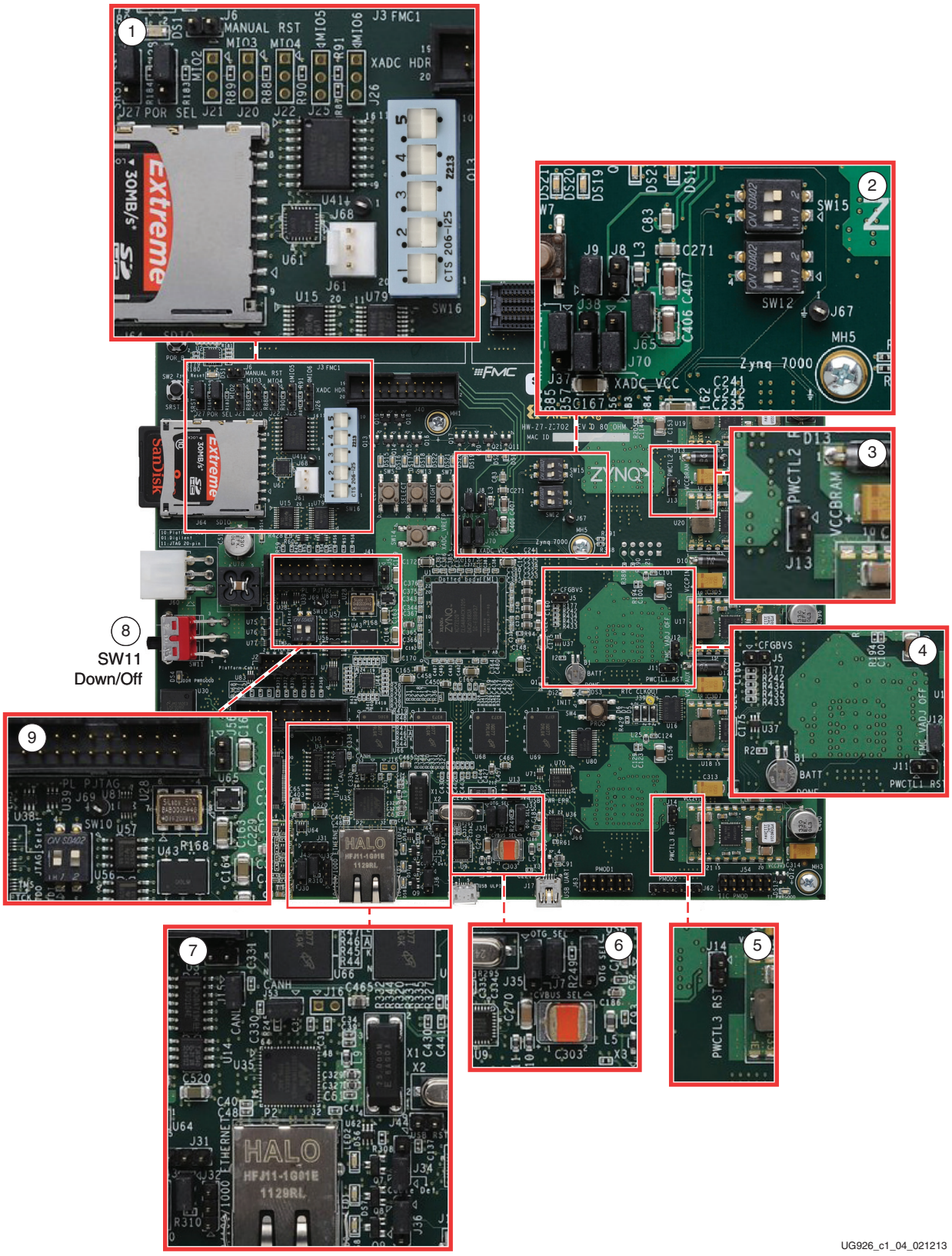


Figure 1-4: **Default Jumper and Switch Settings on the ZC702 Board**

Table 1-1: **Default Switch Settings**

Switch	Position	Setting	Figure 1-4 Callout
SW10 (JTAG chain input select two-position DIP switch)	1	Off	9
	2	On	
SW12 (two-position DIP switch)	1	Off	2
	2	Off	
SW15 (two-position DIP switch)	1	Off	2
	2	Off	
SW16 (five-position DIP switch)	1	Right	1
	2	Right	
	3	Right	
	4	Right	
	5	Right	
SW11 (power slide switch)		Off	8
	1	Down	

Default jumper positions are shown in Figure 1-4 and listed in Table 1-2.

Table 1-2: **Default Jumper Settings**

Jumper	Function	Default Position	Figure 1-4 Callout
HDR_1 X 2			
J5	CFGBVS short to GND	OFF	4
J6	POR Master Reset	OFF	1
J7	USB 2.0 USB_VBUS_SEL	ON	6
J8	XADC GND L3 Bypass	OFF	2
J9	XADC GND	ON	2
J10	ARM HDR J41 pin 2 to VADJ	OFF	7
J11	UCD9248 U32 ADDR52 RESET_B	OFF	4
J12	FMC_VADJ_ON_B	ON	4
J13	UCD9248 U33 ADDR53 RESET_B	OFF	3
J14	UCD9248 U34 ADDR54 RESET_B	OFF	5
J15	CAN BUS COMMON-MODE CANH HDR	ON	7
J43	Ethernet PHY HDR	ON	7
J44	USB 2.0 USB_RESET_B	OFF	7
J53	CAN BUS COMMON-MODE CANL HDR	ON	7
J56	JTAG HDR J58 pin 2 3.3V SEL	OFF	9
J65	XADC_VCC5V0 = VCC5V0	ON	2

Table 1-2: **Default Jumper Settings *(Cont'd)***

Jumper	Function	Default Position	Figure 1-4 Callout
HDR_1 X 3			
J27	PS_SRST_B	1-2	1
J28	PS_POR_B	1-2	1
J30	Ethernet PHY HDR	1-2	7
J31	Ethernet PHY HDR	NONE	7
J32	Ethernet PHY HDR	NONE	7
J33	USB 2.0 Mode	2-3	6
J34	USB 2.0 J1 ID SEL	1-2	7
J35	USB 2.0 J1 VBUS CAP SEL	1-2	6
J36	USB 2.0 J1 GND SEL	1-2	7
J37	XADC_VREP SEL	1-2	2
J38	XADC_VCC SEL	2-3	2
J70	XADC_VREF Source SEL	2-3	2

ZC702 Evaluation Kit Built-In Self-Test

Introduction

The BIST tests many of the features offered by the ZC702 evaluation kit. The test is stored in the onboard nonvolatile Quad SPI flash memory and configures the AP SoC when mode switch SW16 is set to where SW1, 2, 3, and 5 are switched to the right and SW4 is switched to the left, indicating QSPI configuration. This exercise of running the BIST demonstration should take approximately 10 to 15 minutes.

Note: For a description of all the features on the ZC702 board, see UG850, *ZC702 Evaluation Board for the Zynq-7000 XC7Z020 All Programmable SoC User Guide*.

BIST Setup Requirements

These are the prerequisites for running the BIST demonstration.

- Hardware setup:
  - ZC702 evaluation board with XC7Z020 CLG484-1 part
  - USB Type-A to Mini-B cable (for UART)
  - AC power adapter (12 VDC)
- Windows software and driver setup:
  - Tera Term Pro [Ref 8] (or similar) terminal program (might already be installed)
  - USB-UART driver from Silicon Labs [Ref 9] (might already be installed)

Hardware BIST Board Setup

This section describes the hardware setup and use of the terminal program for running the BIST application. It contains step-by-step instructions for board bring-up.

ZC702 Evaluation Board Setup

The default jumper and switch settings of the ZC702 board are shown in Figure 1-4, Table 1-1, and Table 1-2.

1. Set the SW16 switch as shown in Figure 2-1, where position 1, 2, 3, and 5 are switched to the right and position 4 is switched to the left for the BIST to boot from Quad SPI device and run the system demonstration utility.

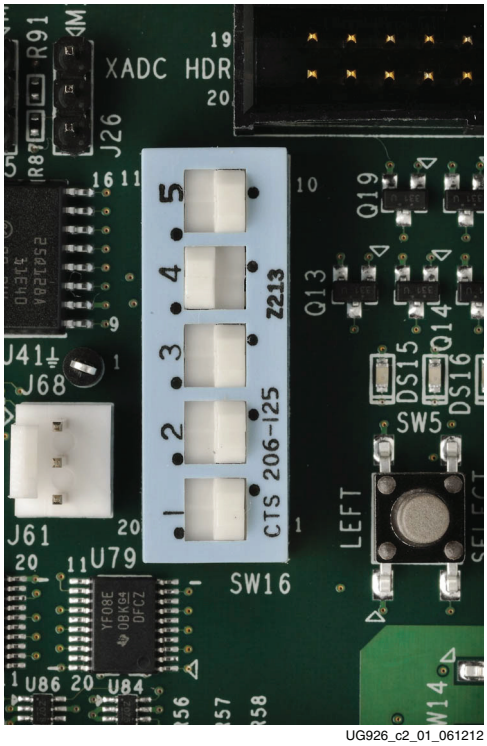


Figure 2-1: **Settings for the Mode Switch to Boot from Quad SPI Mode**

Hardware Bring-Up

This section describes the steps for hardware bring-up.

1. Be sure to have the SW16 Mode switch settings set to those shown in Figure 2-1.
2. With the ZC702 board switched OFF (SW11 in the down position, as shown in Figure 1-4), plug the USB Mini-B cable into the Mini USB port J17 labeled USB UART on the ZC702 board and the other end into a open USB port on your PC (Figure 2-2).

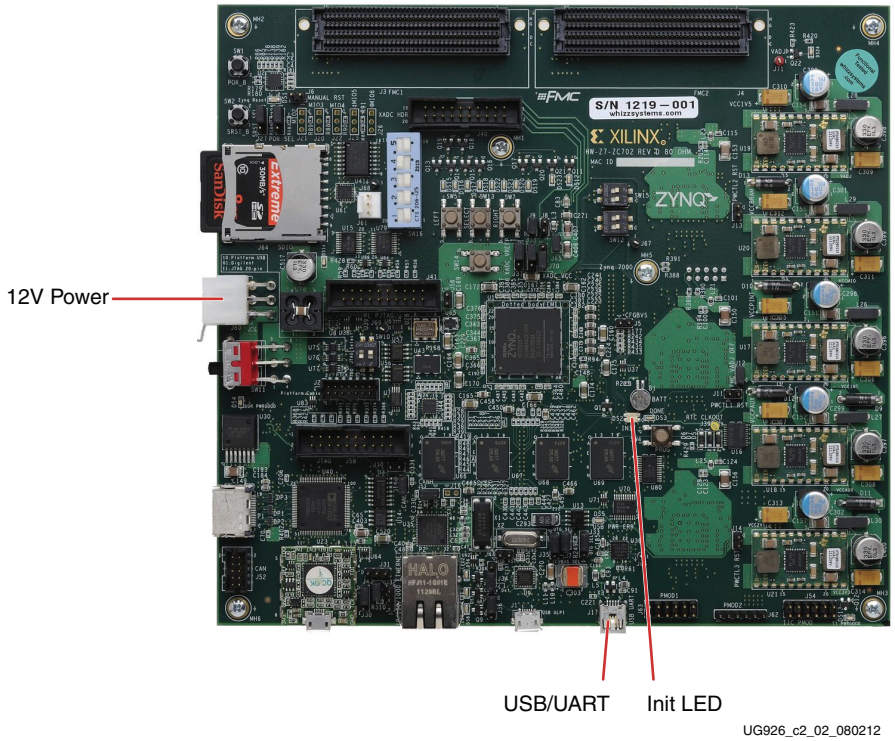


Figure 2-2: **ZC702 with the UART and Power Cable Attached**

3. Connect the power cable.
4. Switch the ZC702 board's power to ON (SW11 switched up as shown in Figure 1-4).

Install the USB-UART Driver

1. Run the downloaded executable UART-USB driver file, listed in BIST Setup Requirements, page 15. Running the executable file enables USB-to-UART communications with a host PC. This driver downloads and executes automatically when the board is powered up or it can be downloaded from the Silicon Laboratories web site [Ref 9].

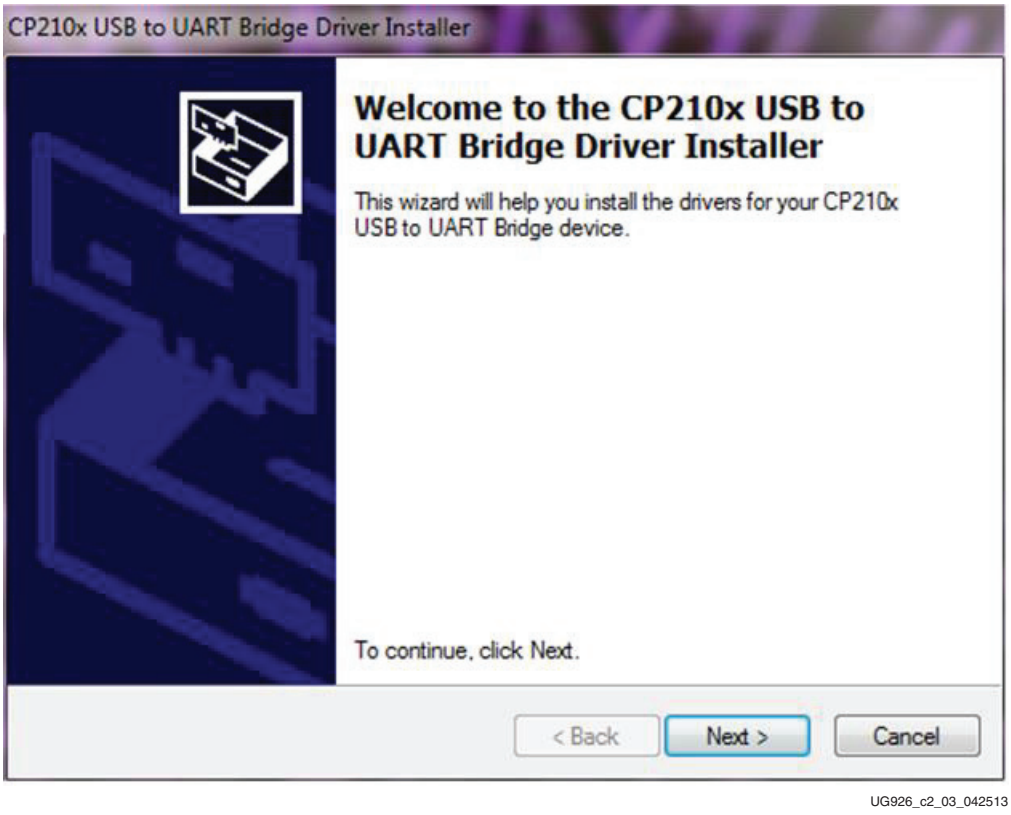


Figure 2-3: **UART Cable Driver Installation**

2. Set the USB-UART connection to a known COM Port and baud rate in the Device Manager.
   a. Left-click **Start Menu** and select **Control Panel** in Windows 7.
   b. Select **Device Manager** on the left side.
   c. Right-click the **Silicon Labs** device in the list and select **Properties.**
   d. Click the **Port Settings** tab. Click the **Advanced...** button.
   e. Select an open COM port between COM1 and COM4. This allows the computer to remember the assignment and not reassign it each time the board serial UART port is plugged in.
   f. Select the baud rate = **115200**, Data bits = **8**, Parity = **None**, Stop Bits = **1**, and Flow control = **None.** Click **OK**.

Note: Steps and diagrams refer to using a Windows XP or Windows 7 host PC.

Figure 2-4 through Figure 2-6 show the steps for setting the USB-UART port.

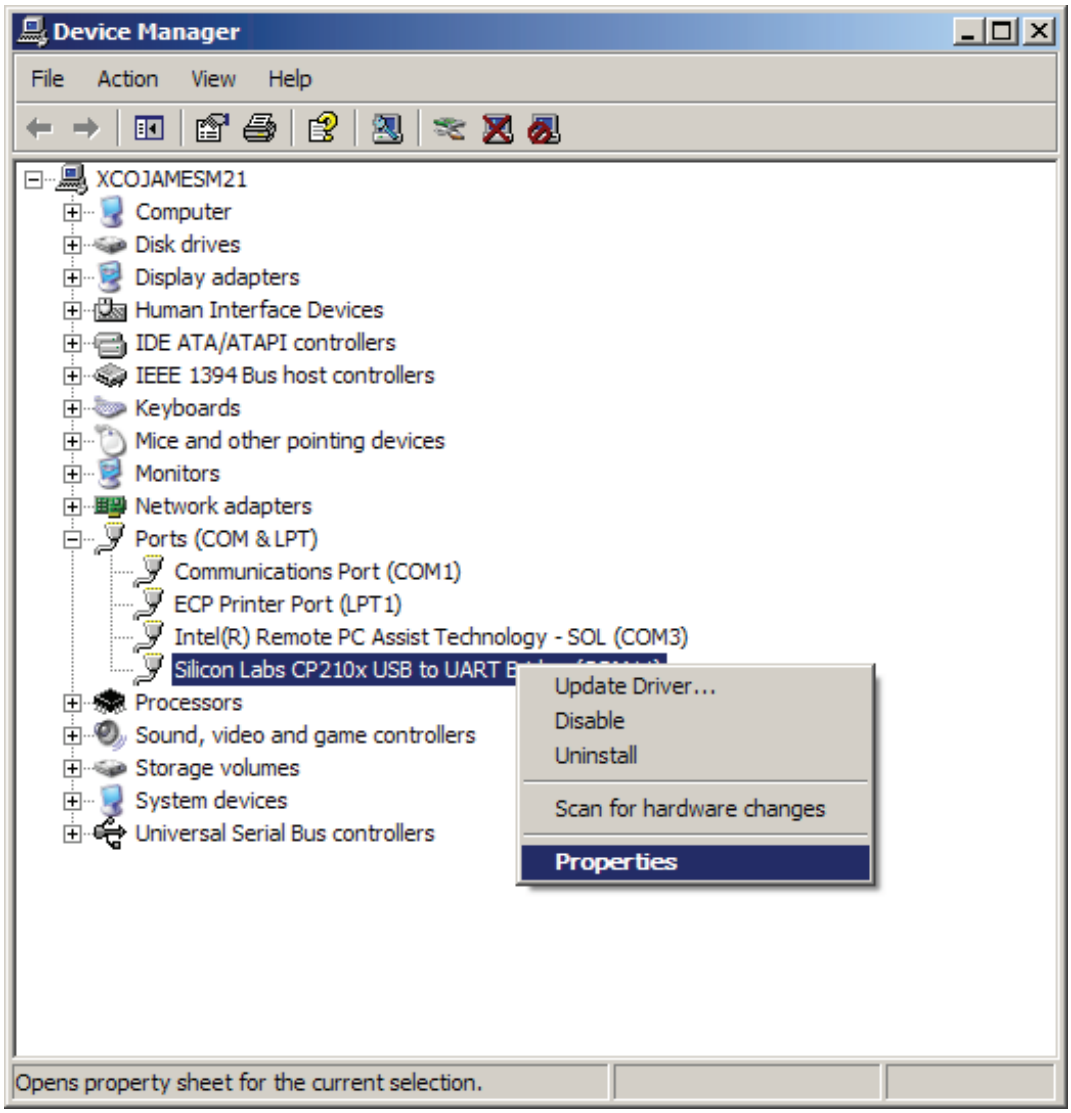


Figure 2-4: **Configuring the Driver**

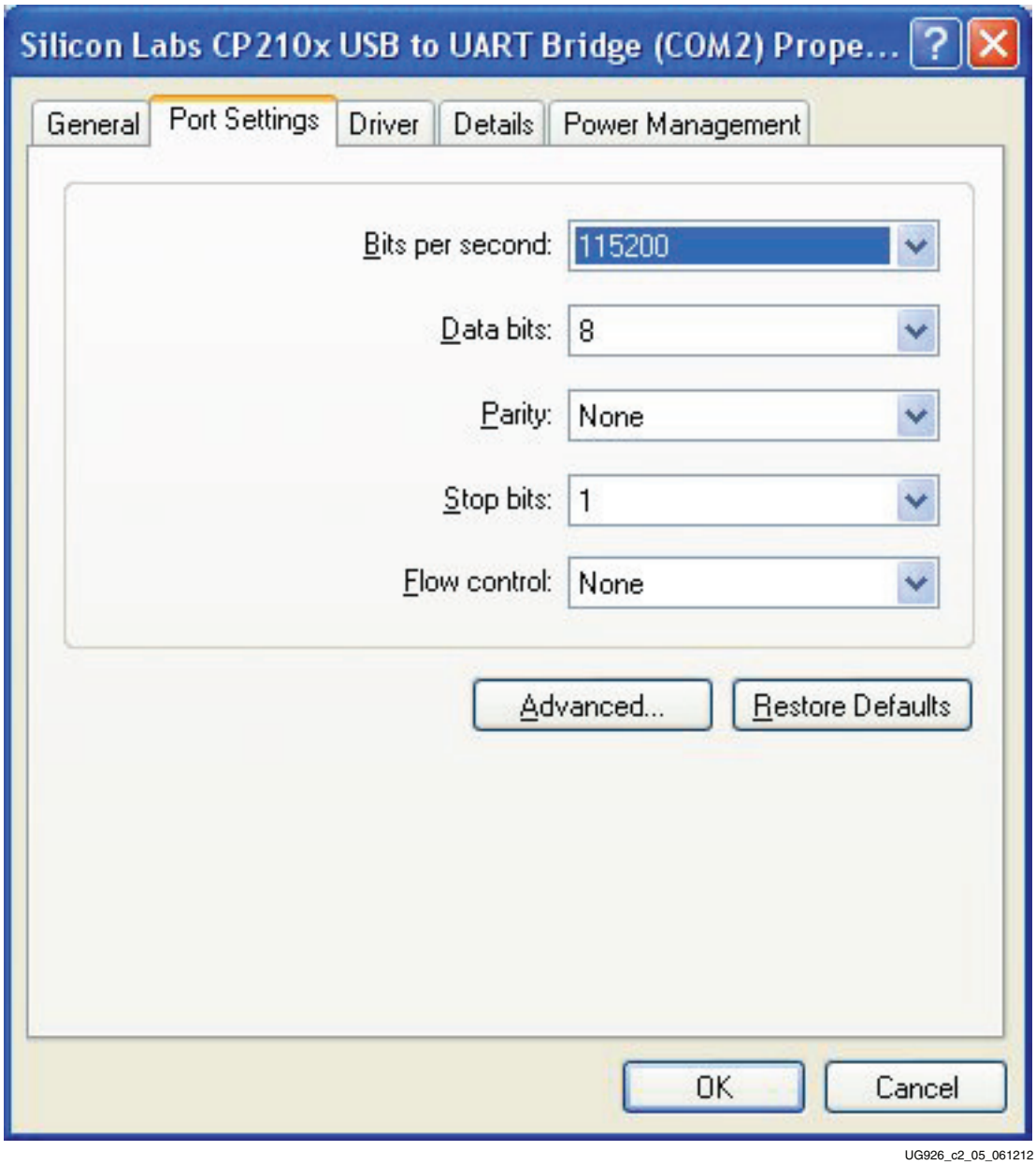


Figure 2-5: **UART Port Setting Tab**

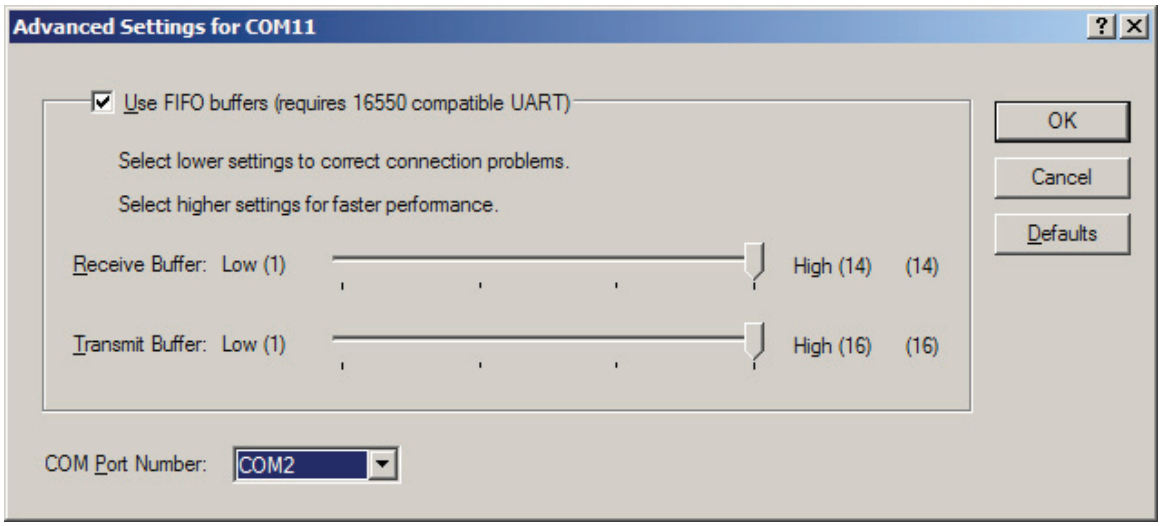


Figure 2-6: **Select a COM Port (between COM1 and COM4)**

Run the BIST Application

1. Start Tera Term or a comparable installed terminal program. Configure it to have the following settings:
   Baud = **115200**, Data = **8**, Parity = **None**, Stop = **1** and Flow = **None**.
2. Press POR_B (SW1) located in the top left corner of the ZC702 board and view the BIST output on the terminal window (Figure 2-7).

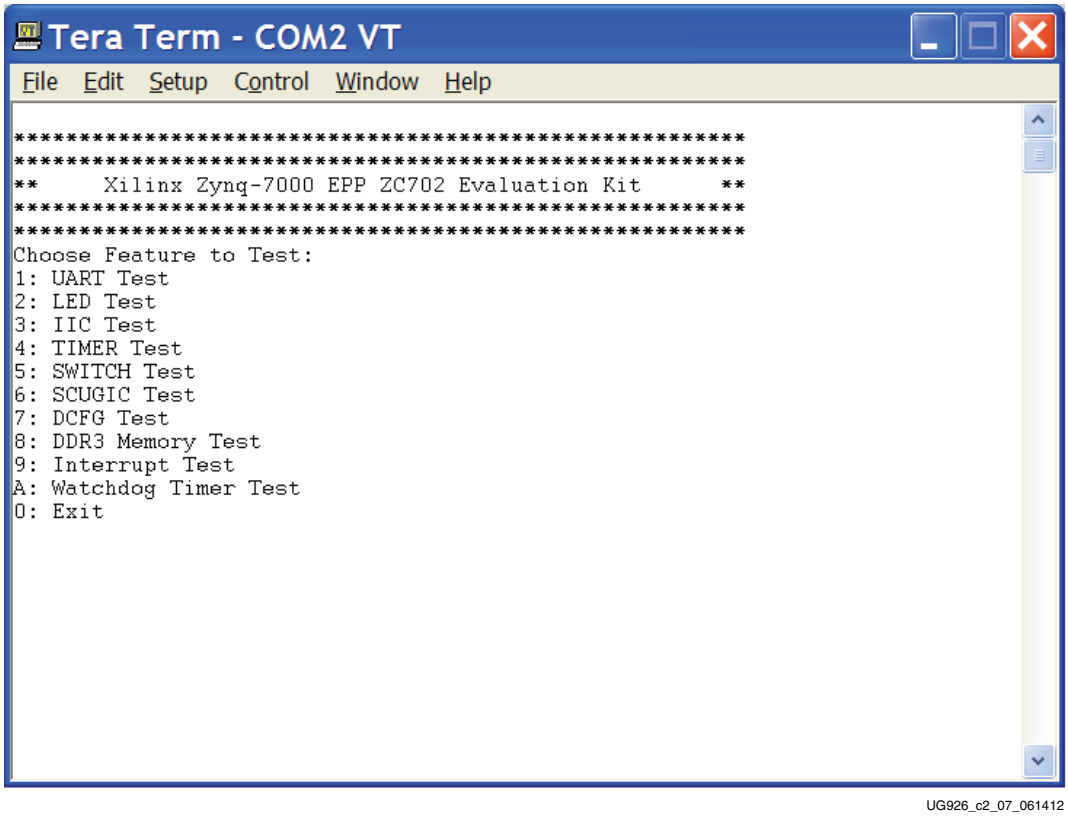


Figure 2-7: **BIST Main Menu**

3. Select each relevant test and observe the test results.

For more information on the BIST software and additional tutorials, including how to restore the default content of the onboard Quad SPI flash nonvolatile storage, see the ZC702 resource page [Ref 4].

For more detailed information about these BIST tests, refer to UG850, *ZC702 Evaluation Board for the Zynq-7000 XC7Z020 All Programmable SoC User Guide*. Also refer to the ZC702 BIST User Guide found in the **Docs & Designs** tab on www.xilinx.com/zc702, that is, the ZC702 BIST PDF file, XTP180.

If any of the BIST tests fail, check the settings of the switches and jumpers as shown in Figure 1-4, Table 1-1, and Table 1-2. If these settings are correct and the test still fails, please contact Xilinx Support at www.xilinx.com/support and open a WebCase.

Getting Started with the Base Targeted Reference Design

Introduction

This section provides step by step instructions for bringing up the board and running the video Targeted Reference Design (TRD). In this design, the Zynq-7000 AP SoC performs real-time processing of a 1080p60 video stream—either in Processing System (PS) software or Programmable Logic (PL) hardware accelerator. The video processing path is user-selectable through a graphical user interface (GUI) running on Linux in the Zynq-7000 AP SoC PS. The GUI also displays detailed information about system usage statistics and system performance.

Figure 3-1 shows the system block diagram for Zynq-7000 AP SoC Base TRD.

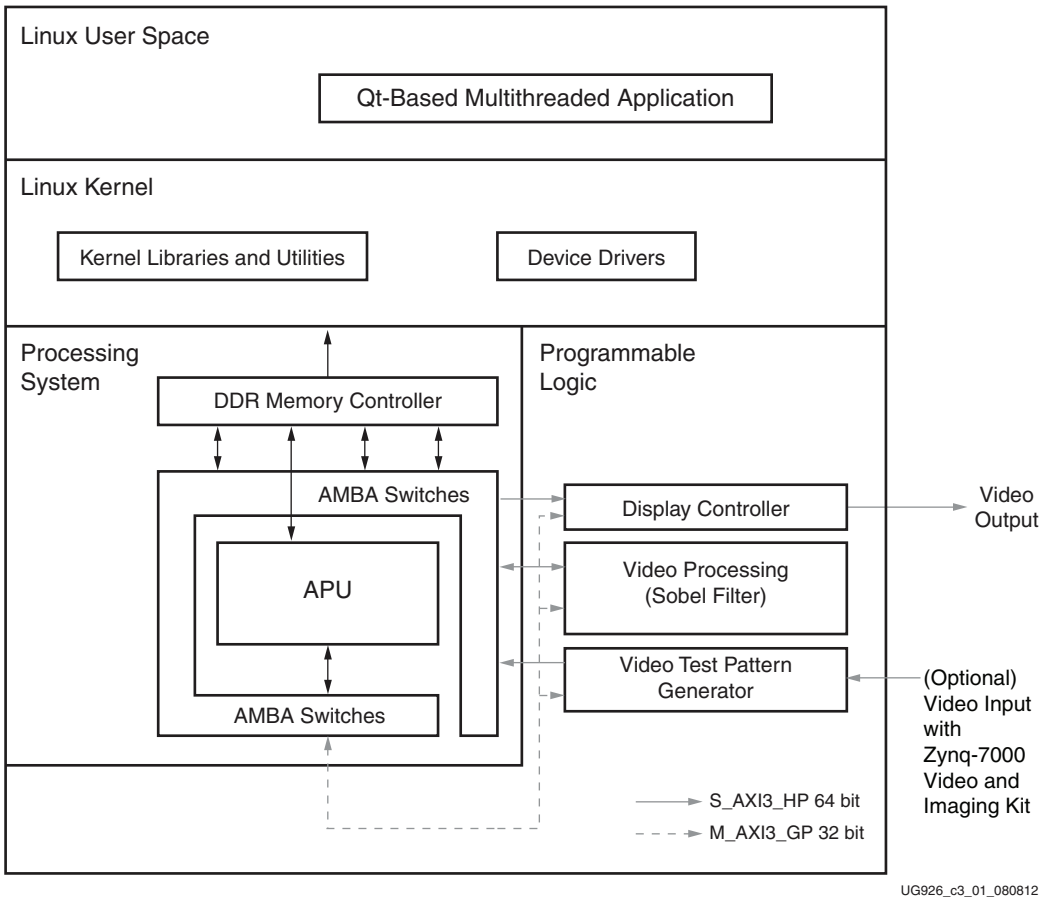


Figure 3-1: **Zynq-7000 AP SoC ZC702 and ZVIK Base TRD System Block Diagram**

The Base TRD showcases various features and capabilities of the Zynq Z-7020 AP SoC for the embedded domain in a single package. The Base TRD consists of two processing elements: The Zynq-7000 AP SoC processing system (PS) and an interconnect logic-based video accelerator. The AP SoC allows the user to implement a specific functionality either as a software program running on the Zynq-7000 AP SoC PS or as a hardware design inside the programmable logic (PL). The Base TRD demonstrates how the user can seamlessly switch between a software or a hardware implementation, contributing to ease of use. The TRD also demonstrates the value of offloading computation-intensive tasks onto PL, thereby freeing the CPU resources to be available for user-specific applications.

The ZC702 evaluation kit and ZVIK come with an SD card loaded with binaries that enable the user to run the video demonstration and software application. It also includes the binaries necessary to configure and boot the Zynq-7000 AP SoC board.

Note: The screen captures in this document are conceptual representations of their subjects and provide general information only.

Base TRD Key Features

The PS includes:

- Two ARM Cortex-A9 MPcore processors, each with a 32 KB instruction cache, a 32 KB data cache, and a NEON™ media processing engine and vector floating-point processor (VFPv3).
- 512 KB of level 2 cache
- 256 KB of on-chip RAM
- ARM AMBA® AXI interconnect
- Multi-protocol, 32-bit DDR DRAM controller
- Standard peripheral interfaces including USB, Ethernet, UART, I2C, SD MMC, and GPIO
- Clocks and reset for PL
- High bandwidth interconnect between PS and PL

The PL includes:

- Two AXI interconnects, 64-bit wide at 150 MHz
- One AXI interconnect, 32-bit wide at 75 MHz
- AXI VDMA(s)
- A full HD video input (ZVIK) and output interface
- A Sobel accelerator
- One Performance Monitor

The software includes:

- Xilinx Zynq-7000 AP SoC standard Linux kernel (based on Open Source Linux version 3.x)
- Linux device drivers for TRD-specific IPs.
- A Qt-based Linux application demonstrating the video processing pipeline
- A command line menu-based Linux application demonstrating the video processing pipeline

Note: The video demonstration contains the licensed IPs with no timeout.

Base TRD Hardware Setup Requirements

These items are required to run and test the Base TRD and the video demonstration:

- The ZC702 evaluation board with the XC7Z020 CLG484-1 part
- USB Type-A to USB Mini-B cable (for UART communications) and a Tera Term Pro (or similar) terminal program [Ref 8]
- USB-UART drivers from Silicon Labs [Ref 9]
- AC power adapter (12 VDC)
- An HDMI cable (two cables if using the ZVIK and the user desires to use an external video source for the demonstration)
- SD MMC flash card containing TRD binaries formatted with FAT32

  Note: The included SD MMC is pre-loaded with required binaries. The binaries are loaded into the first partition of the SD MMC card and include:

  - `BOOT.bin`
  - `devicetree.dtb`
  - `uImage`
  - `uramdisk.image.gz`
  - `qt_lib.img`
  - `init.sh`
  - `run_sobel.sh`
  - `sobel_cmd`
  - `sobel_qt`
  - `zynq-zc702-base-trd.dts`

  Note: The default binary device tree `devicetree.dtb` is for configuring the video-out resolution to 1080p. Additionally, the binaries should be loaded at its root level. If the files are not loaded on the SD card, copy the files from the `sd_image directory` to the SD card.
- USB Micro-B to female A adapter
- A USB hub is needed for connecting a keyboard and mouse (not included with the kit). If a USB hub is not available, it is still possible to run the demonstration with only a USB mouse, but the user will not be able use the frame buffer console terminal that will come up once the user exits the demo.
- USB mouse and keyboard (optional—not included with the kit)
- An HDMI-compatible display monitor that supports full HD resolution: 1920 x 1080p @ 60 Hz (not included with the kit). If the user wants to test at 720p video resolution, the display monitor should support 720p resolution: 1280 x 720p @ 60 Hz. If an HDMI monitor is not available, a DVI monitor can be used, but an HDMI to DVI-D

cable/connector adapter is required (not included with the kit). The connector adapter can be easily obtained at most electronic retailers or through a variety of online sources.

Instructions for running the demonstration at 720p are provided in Running the Video Demonstration for 720p Video Resolution, page 39.

Note: The example mentioned in this package has been tested with a Dell model #P2412H display monitor. However, the example should work well with any HDMI-compatible display device.

- For the ZVIK, if running with an external video input source is desired, use the FMC-IMAGEON HDMI input/output FMC module to connect an external video source. An HDMI video source is required to provide the external video input. If an HDMI source is not available, a DVI source can be used, but an HDMI to DVI-D cable/connector adapter is required (not included with the kit). The connector adapter can be easily obtained at most electronic retailers or through a variety of online sources. The external video source must be 1080P 60 Hz and must not deliver content with copy protection or Digital Rights Management (DRM) enabled. Many DVD and media players output content with DRM enabled even if the content is not DRM protected. A laptop or other source is recommended.

Note: This TRD does not support input from the camera provided in the ZVIK. Check the ZVIK product web page www.xilinx.com/ZVIK for additional designs and resources.

Note: When connecting an external video source to the FMC card:

- Connect the source only after the bit file is programmed. Connecting the source only after system boot-up is recommended.
- Ensure that the source resolution is set to the same resolution used by the demo (1080p or 720p). See Running the Video Demonstration for 720p Video Resolution, page 39 for more details.
- Ensure that the refresh rate for the source is set to 60 Hz.

TRD Demonstration Procedure

This section provides a procedure for setting up the ZC702 board or ZVIK and running the demonstration provided with the kit.

Board Setup

1. For customers using the ZVIK, assemble the FMC module to the ZC702 base board. The FMC module and HDMI video input are not required for either kit to run the TRD, but ZVIK customers can run the TRD demonstration using the external video input in addition to the built-in Test Pattern Generator if the FMC card is installed. Two sets of standoff hardware are in the box, which can be used to secure the FMC-IMAGEON FMC module on the ZC702 base board and support the free end of the board. Assemble the hardware as shown in Figure 3-3. Use the longer standoffs, screws, and rubber feet for the free end of the board.
2. Connect the cables as shown in Figure 3-2 to prepare the ZC702 board to run the TRD video demonstration.

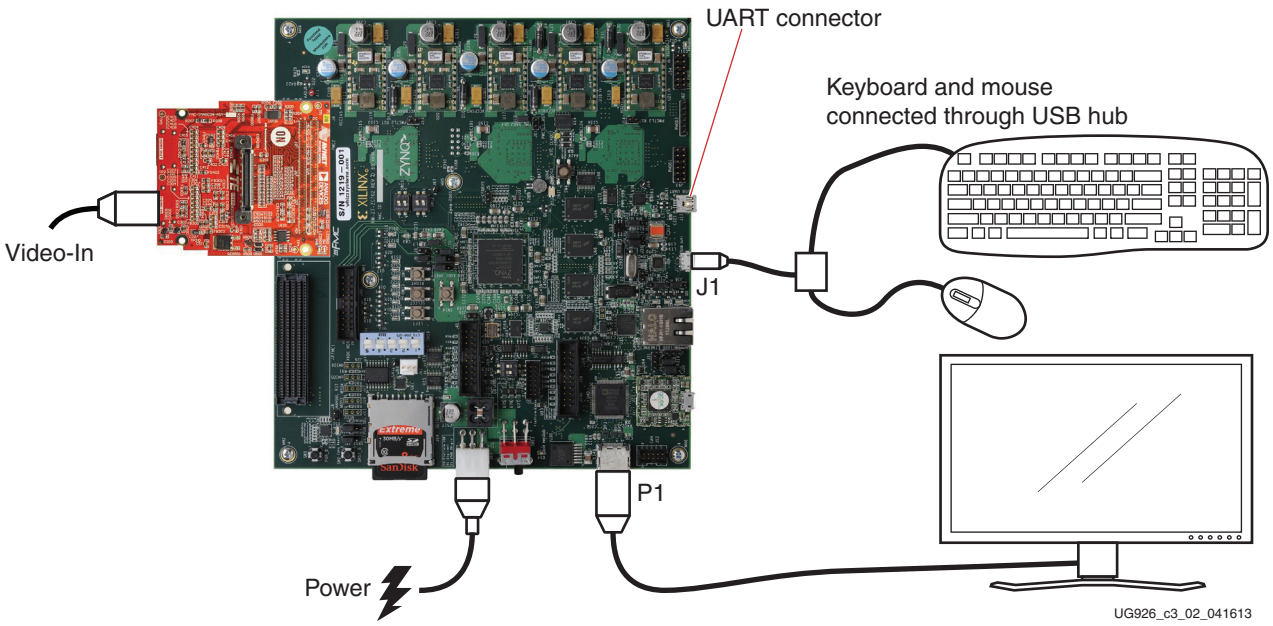


Figure 3-2: **ZC702 Board Setup for a Video Demonstration**

a. Connect an LCD monitor to the HDMI out port P1 of the ZC702 board using an HDMI cable.

b. Connect a keyboard and mouse to the USB hub, which is connected to the ZC702 board Micro-B USB connector J1 labeled **USB ULPI** through the USB Micro-B to female A adapter. If a USB hub is not available, the mouse can be plugged directly into the female USB connection of the USB Micro-B to female A adapter, but the user

will not be able to exercise the portions of the demonstration that require a keyboard.

c. Connect the USB Mini-B cable into the Mini USB port J17 labeled **USB UART** on the ZC702 board and the USB Type-A connector end of the cable into an open USB port on the host PC for UART communications.

d. For customers using the ZVIK, mount the FMC-IMAGEON HDMI input/output FMC module onto the FMC-2 slot present on the ZC702 board. Attach the FMC board to the ZC702 carrier board using the two short standoffs and four short screws as shown in Figure 3-3. Use the two long standoffs, four longer screws, and rubber feet to support the free end of the board. Connect an external video source to the FMC module HDMI input labeled **HDMI IN** with 1080p60 resolution. A 720p60 source can also be used, but it requires adjustment to the system as described in the section Running the Video Demonstration for 720p Video Resolution, page 39.

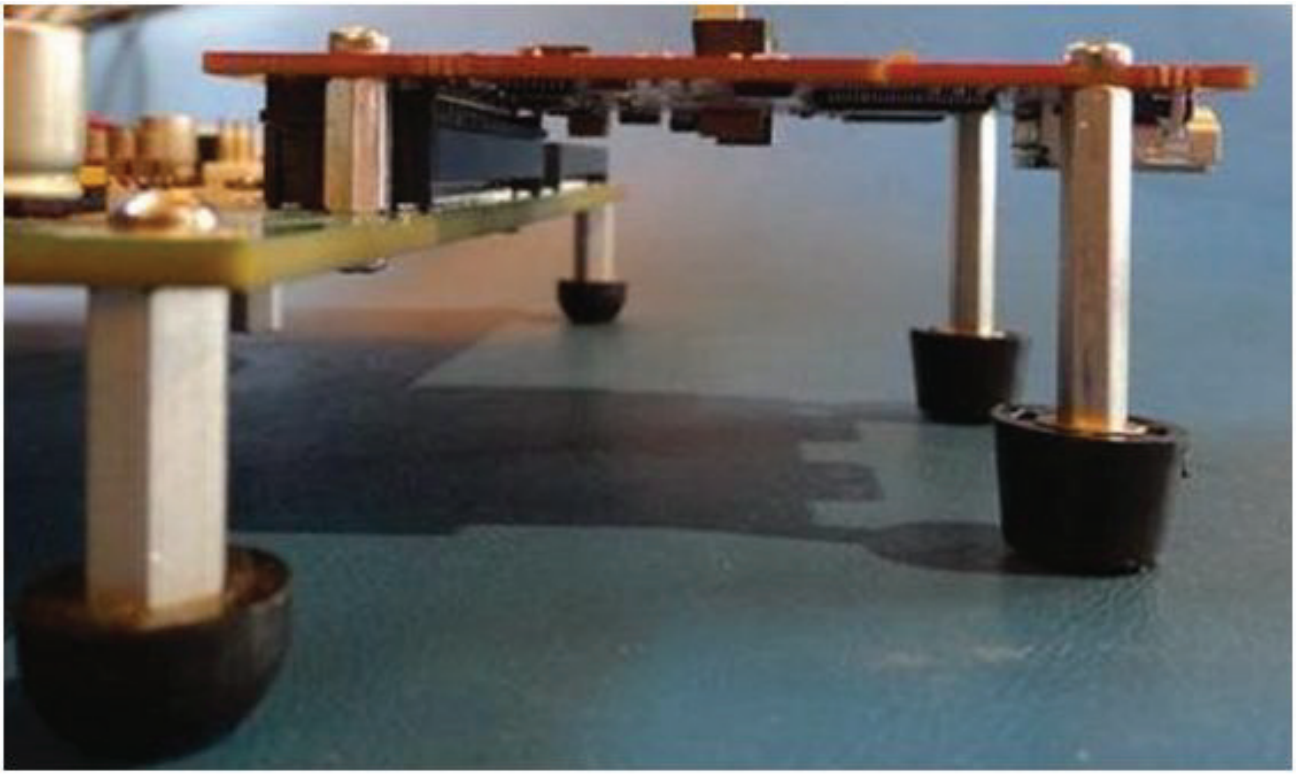


Figure 3-3: **ZVIK FMC Mounting Hardware Detail**

e. Connect the power supply to the ZC702 board connector J60. Do not switch the power on.

3. Insert the SD MMC, which contains the TRD binaries, into the SD slot on the ZC702 board.
   - Ensure the binary files are in the first partition of the FAT32-formatted SD MMC card at its root level.

Note: If the evaluation kit design files were downloaded online, copy all the files within the `zynq_base_trd_14.x/sd_image` folder directly onto the primary partition of the SD MMC card (which is formatted as FAT32) at the root level using an SD MMC card reader. The files in the SD MMC card should match the list described in SD MMC flash card containing TRD binaries formatted with FAT32, page 28.

4. Make sure the switches are set as shown in Figure 3-4, which allows the ZC702 board to boot from the SD MMC card.

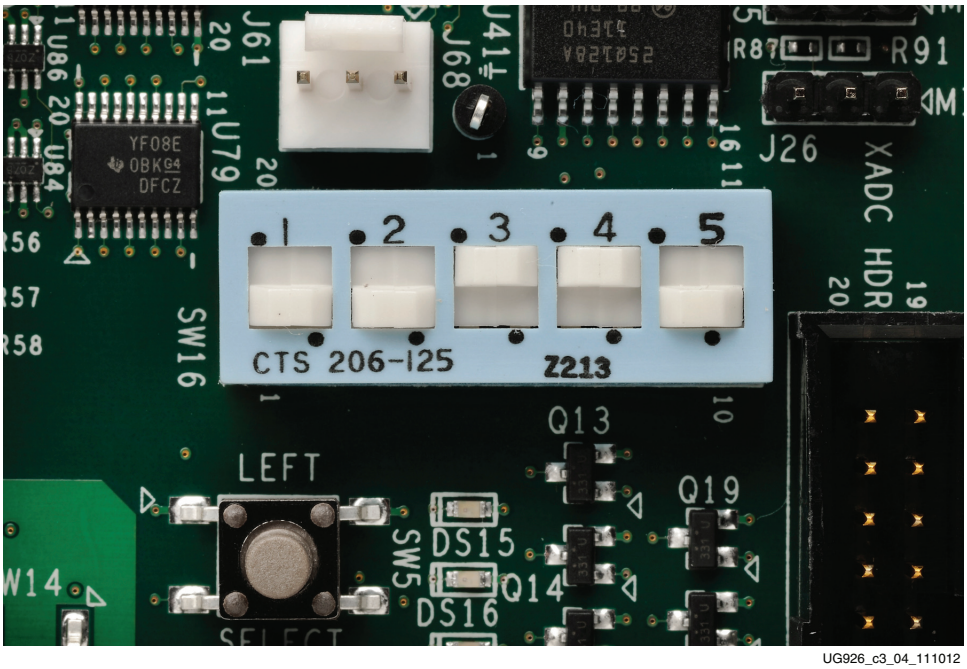


Figure 3-4: **Switch Settings for the Mode Switch to Boot from the SD MMC Card**

5. Make sure the display monitor is set for HDMI or DVI 1920 x 1080.

Running the Qt-Based GUI Application Demonstration

1. Power on the ZC702 board. The default binary Linux device tree (`devicetree.dtb`) configures and runs the video demonstration for 1080p video-out resolution.
2. Start the installed UART terminal program on your host PC (e.g., Tera Term Pro on a Windows PC, GtkTerm on a Linux PC).

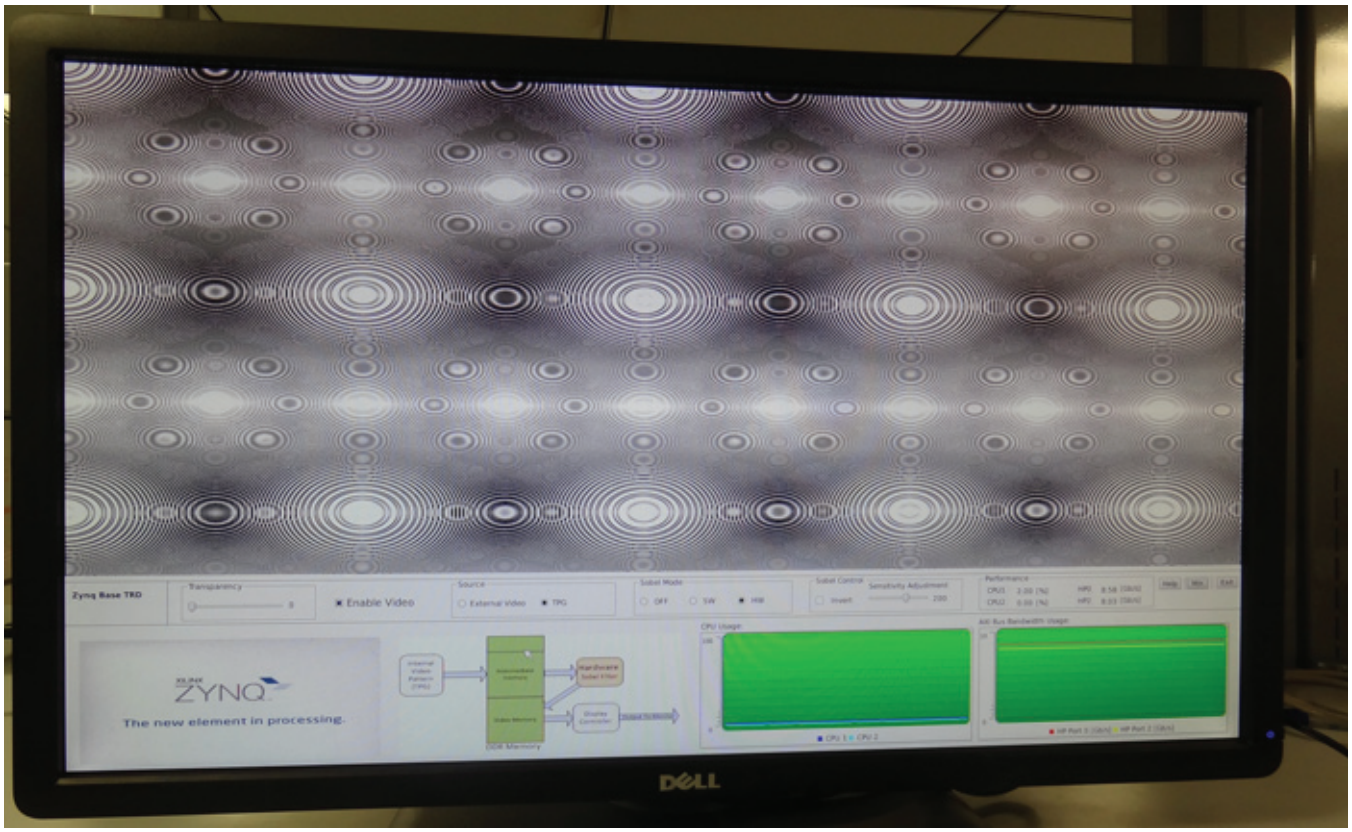
   Use the following UART configuration: Baud rate = **115200**, bits = **8**, parity = **none**, and stop bits = **1**.

   Note: This step is required to view debug information or to run the UART Menu-Based Demonstration application.

3. Wait for the ZC702 board to be configured and booted with Linux. The `XILINX ZYNQ` banner appears on the display monitor after approximately two minutes as shown in Figure 3-5.

Figure 3-5: **Zynq Linux Command Prompt**

4. The Qt-based video demonstration application starts. The GUI application shows up at the bottom of the screen (see Figure 3-6).



UG926_c3_06_041513

Figure 3-6: **Qt-Based GUI to Control the Video Pipeline**

5. The Qt-based application allows the user to experience the Base TRD video demonstration and is controlled through the mouse. The user can click **Help** for short messages and information about the control window of the QT application. The GUI can be minimized with the MIN button (See Figure 3-6) and can be brought back to the original size with the MAX button. The user can also control transparency of the GUI with the Transparency slider.

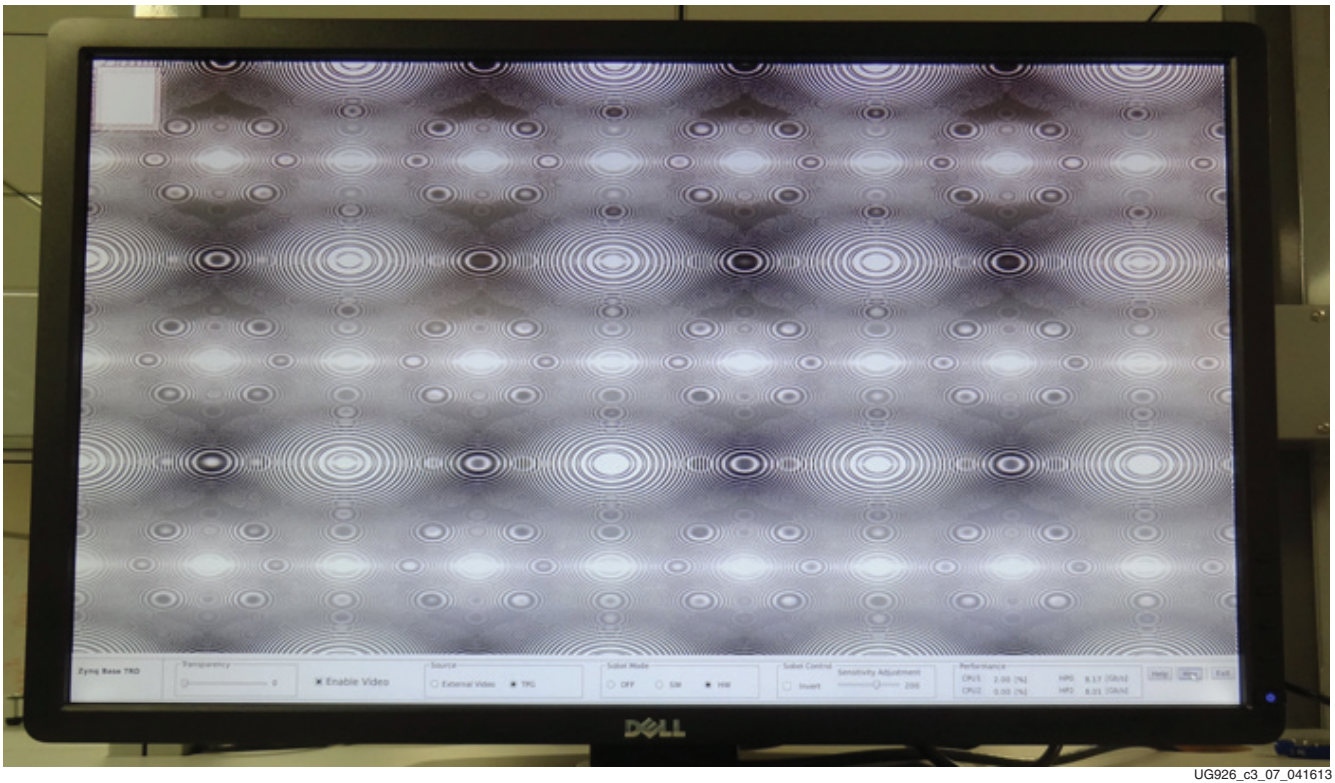


Figure 3-7: **Minimized GUI Mode**

6. Click **Enable Video** to start the internal Test Pattern Generator (TPG), which displays on the monitor.
7. Exercise different options by pressing the buttons available in the GUI to evaluate the different use cases mentioned in Table 3-1.

Table 3-1: **Zynq-7000 AP SoC Base TRD Video Demonstration Use Cases**

Use Case	Video Source Control	Sobel Filter Control
1	TPG interference	Sobel OFF
2	TPG interference	Sobel - SW
3	TPG interference	Sobel - HW
Additional ZVIK Options		
4	External video	Sobel OFF
5	External video	Sobel - SW
6	External video	Sobel - HW

Video source control modes are explained as follows:

- TPG interference
  - The input video is generated by the TPG IP implemented in the PL.

- External video (available with the optional ZVIK FMC module)
  - The input video is supplied by an external video source and is connected through the FMC-IMAGEON card.

Sobel Filter Modes are explained as follows:

Sobel OFF

- No processing done. Sobel filter is bypassed.

Sobel – SW

- Video processing (edge-detection filter) done by software code running on the PS.
- Observe CPU utilization going up to 100% for one of the two CPUs (this can be seen in the CPU usage graph). In this mode, the frame rate of the video also drops to about 3 fps to 10 fps depending upon resolution.

Sobel – HW

- Video processing (edge-detection filtering) done by PL.
- Observe CPU utilization going down (to approximately 0%) and the frame rate jumping to 60 fps.

Figure 3-8 shows the detected image edges of the video generated by the TPG, that is, case 1 versus case 2 or 3 of Table 3-1.

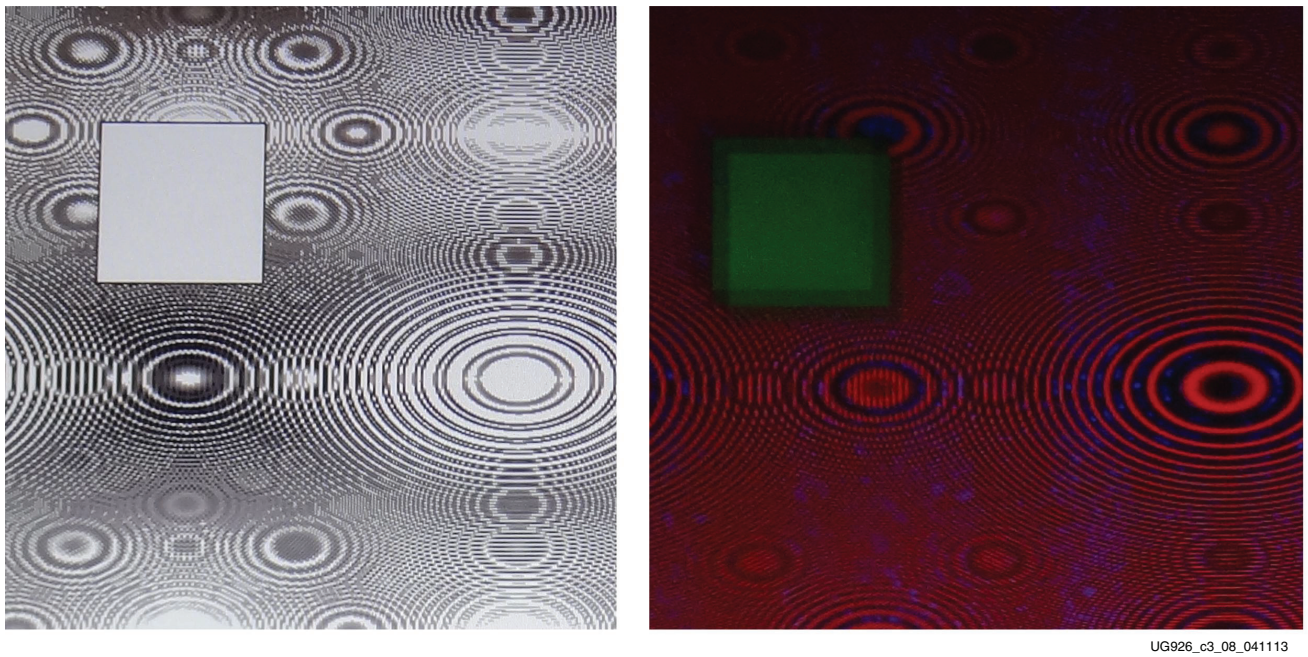


Figure 3-8: **Images with Sobel Filter On (Left) and with Sobel Filter Off (Right)**

While exercising the modes described above, one can observe AXI bus bandwidth utilization and CPU utilization on the graphs in the Qt GUI application.

8. Click **Exit** to quit the application and return the user to Linux console.
9. The application can be restarted by typing the following at the Linux command prompt:

```
zynq> cd /mnt

zynq> ./run_sobel.sh –qt
```

Running the UART Menu-Based Demonstration Application

A command line based Linux application demonstration is also provided with the package. This application presents the user with a command line menu-based UI to exercise different modes of the video demonstration.

To run the menu-based UI application demonstration, the Qt-based GUI application which was started (as explained in Running the Qt-Based GUI Application Demonstration, page 32) needs to be quit as per step 8, page 37.

The following steps explain how to start the UART menu-based application demonstration and exercise different application video use cases.

1. Go to the UART terminal started on your host PC as explained in step 2 from Running the Qt-Based GUI Application Demonstration, page 32.
2. Type these commands at the Linux command prompt into the host PC based terminal:

```
zynq> cd /mnt

zynq> ./run_sobel.sh –cmd
```

The menu-based video application demonstration starts as shown in Figure 3-9.

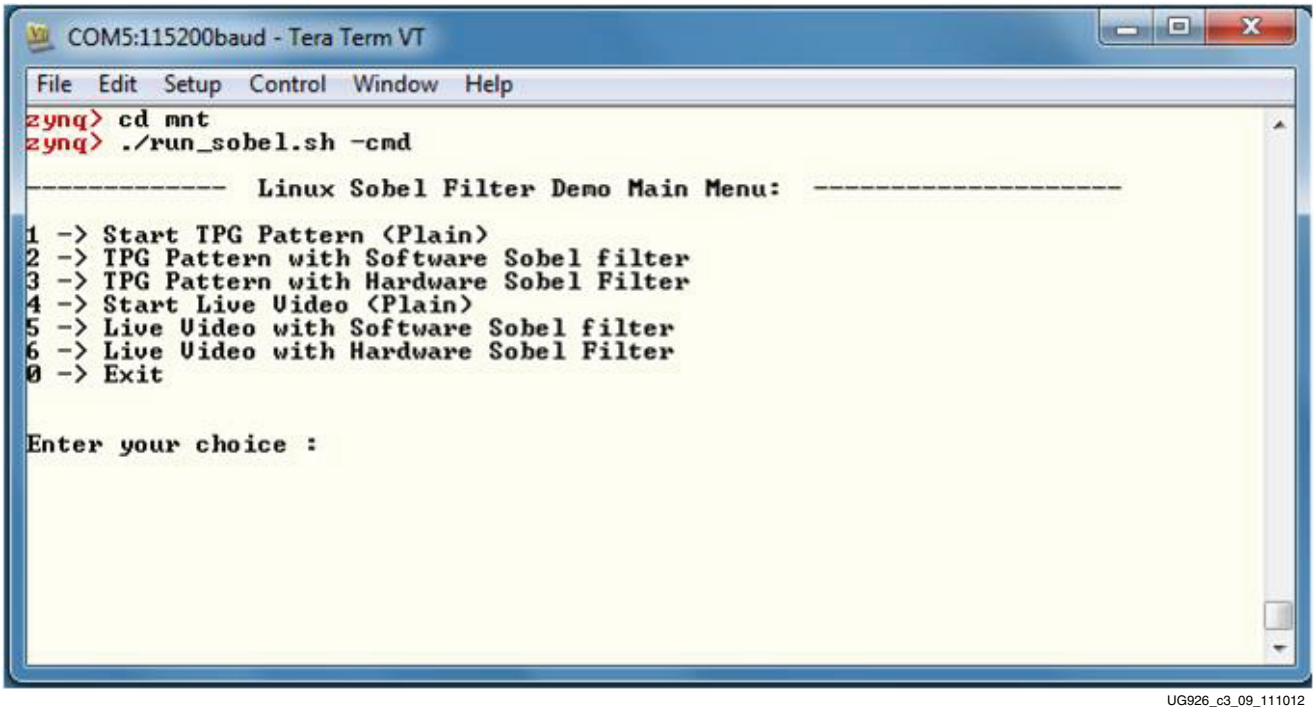


Figure 3-9: **Command Line Based UI Menu**

Exercise different options by entering the use case number displayed in Table 3-2 against `Enter your choice:` on the terminal.

Table 3-2: **Zynq-7000 AP SoC Base TRD Video Demonstration Use Cases**

Use Case	Video Source Control	Sobel Filter Control
1	TPG interference	Sobel OFF
2	TPG interference	Sobel - SW
3	TPG interference	Sobel - HW
Additional ZVIK Options		
4	External video	Sobel OFF
5	External video	Sobel - SW
6	External video	Sobel - HW

Video source control modes are explained as follows:

- TPG interference
  - The input video is generated by the TPG IP implemented in the PL.
- External video (available with the optional ZVIK FMC module)
  - The input video is supplied by an external video source and is connected through the FMC-IMAGEON card.

Sobel Filter Modes are explained as follows:

Sobel OFF

- No processing done. Sobel filter is bypassed.

Sobel – SW

- Video processing (edge-detection filter) done by software code running on PS

Sobel On – HW

- Video processing (edge-detection filter) done by PL

  Figure 3-8 shows the detected image edges of the video generated by the TPG, that is, case 1 versus case 2 or 3 of Table 3-2.

3. Enter **0** to exit the application and return to the command prompt.

Running the Video Demonstration for 720p Video Resolution

Configure the display monitor to 720p60 resolution: 1280 x 720p @ 60 Hz. If using the ZVIK with an external video source, configure the external video source to 1280 x 720 @ 60 Hz.

- Follow these steps for running QT based GUI demonstration application in 720p mode:
  a. Exit any previously running applications.
  b. Type these commands at the Linux command prompt into the host PC based terminal:

```
zynq> cd /mnt
zynq> ./run_sobel.sh –qt -res 1280x720
```

- Follow the steps for running UART Menu based Demonstration Application in 720p mode:
  a. Exit any previously running applications.
  b. Type these commands at the Linux command prompt into the host PC based terminal:

```
zynq> cd /mnt
zynq> ./run_sobel.sh –cmd -res 1280x720
```

For additional example designs, tutorials, software, and other information related to the ZVIK, please refer to Next Steps for the Zynq-7000 AP SoC Video and Imaging Kit (ZVIK), page 45.

Using the AMS101 Evaluation Card

Introduction

Each Xilinx Zynq-7000 AP SoC features two 1 MSPS, 12-bit, analog-to-digital converters (ADCs) built into the device for everything from simple analog monitoring to more signal processing-intensive tasks like linearization, calibration, over-sampling, and filtering. The ZC702 evaluation kit includes the hardware and software to evaluate this ADC feature and to determine its usefulness in the user's end system.

For evaluation of Xilinx Agile Mixed Signal (AMS) capability, the following items in the kit are needed:

- Access to the ZC702 XADC header
- AMS101 evaluation card (see Figure 4-1)
- Design and software files, which can be downloaded from the web
- Zynq-7000 AP SoC design programming files
- USB-UART drivers from Silicon Labs
- Blank SD MMC card

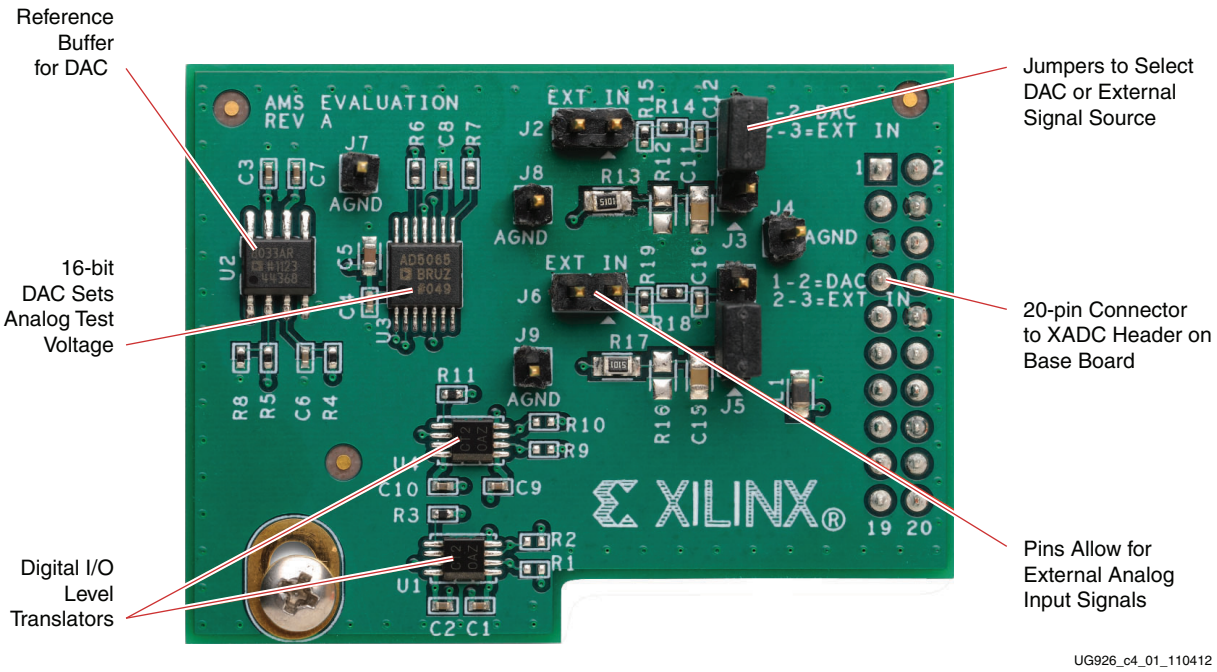


Figure 4-1: **AMS101 Evaluation Card**

Requirements to Get Started

1. The AMS101 evaluation requires a Windows host PC to install the National Instruments LabVIEW Run-Time engine.
2. Verify the USB/UART Silicon Labs drivers are installed as described in Install the USB-UART Driver, page 18.
3. Depending on the computer operating system, select and install one of these National Instruments LabVIEW 2011 Run-Time Engine AMS101 Installers for a 32-bit OS or a 64-bit OS:
   a. LabVIEW 32-bit Run-Time Engine: joule.ni.com/nidu/cds/view/p/id/2534/lang/en
   b. LabVIEW 64-bit Run-Time Engine joule.ni.com/nidu/cds/view/p/id/2536/lang/en
4. Unzip the `AMS_Eval_Demo_Files_<ISE_Version>` from the `ZC702_Reference_Designs` folder to access the AMS bitstream (`boot.bin`).
5. Copy the `boot.bin` file on an SD MMC card.

Evaluating AMS

1. Connect and power the hardware.
   a. Connect the ZC702 board to the AMS101 evaluation card, making sure the notch on the XADC header lines up correctly with the AMS101 evaluation card. see Figure 4-2.

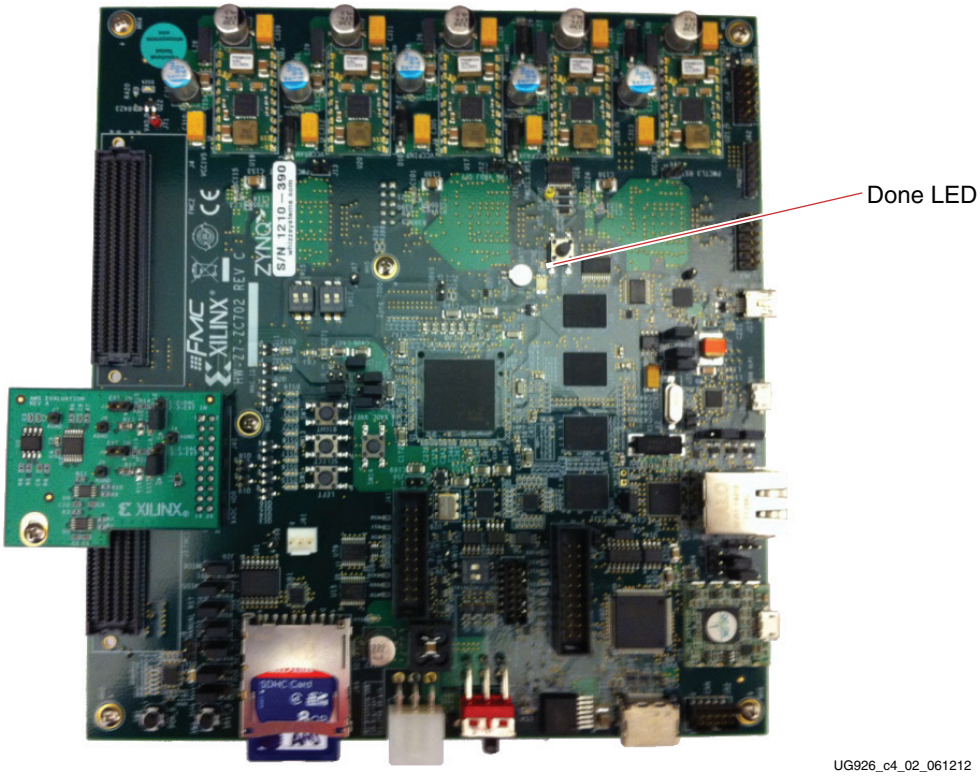


Figure 4-2: **ZC702 Board with AMS101 Evaluation Card Plugged into XADC Header**

2. Download the design to the Zynq-7000 AP SoC.
   a. Open `AMS101 Evaluator GUI V1.0.exe` from the directory and `AMS_Eval_Demo_Files_<ISE_Version>` from the location it was copied to.
   b. Copy the `boot.bin` file on the SD MMC card.
   c. Plug the SD MMC card into the ZC702 board.
   d. Set the ZC702 board switch settings to *boot from SD* mode (Figure 3-4).
   e. Power on the ZC702 board. After about 15 seconds, the Done LED (DS3) turns green, indicating the design file on the SD MMC card has properly loaded onto the Zynq-7000 AP SoC.
3. Run the AMS101 Evaluator LabVIEW GUI executable file.

a. On the Host PC, open `AMS101 Evaluator GUI V1.0.exe` from the directory and `AMS_Eval_Demo_Files_<ISE_Version>` from the location it was copied to.

The AMS Evaluator Tool allows designers to quickly evaluate the analog signals in the time and frequency domain, display linearity, verify the XADC register settings, and measure the internal temperature sensor and supply voltages.

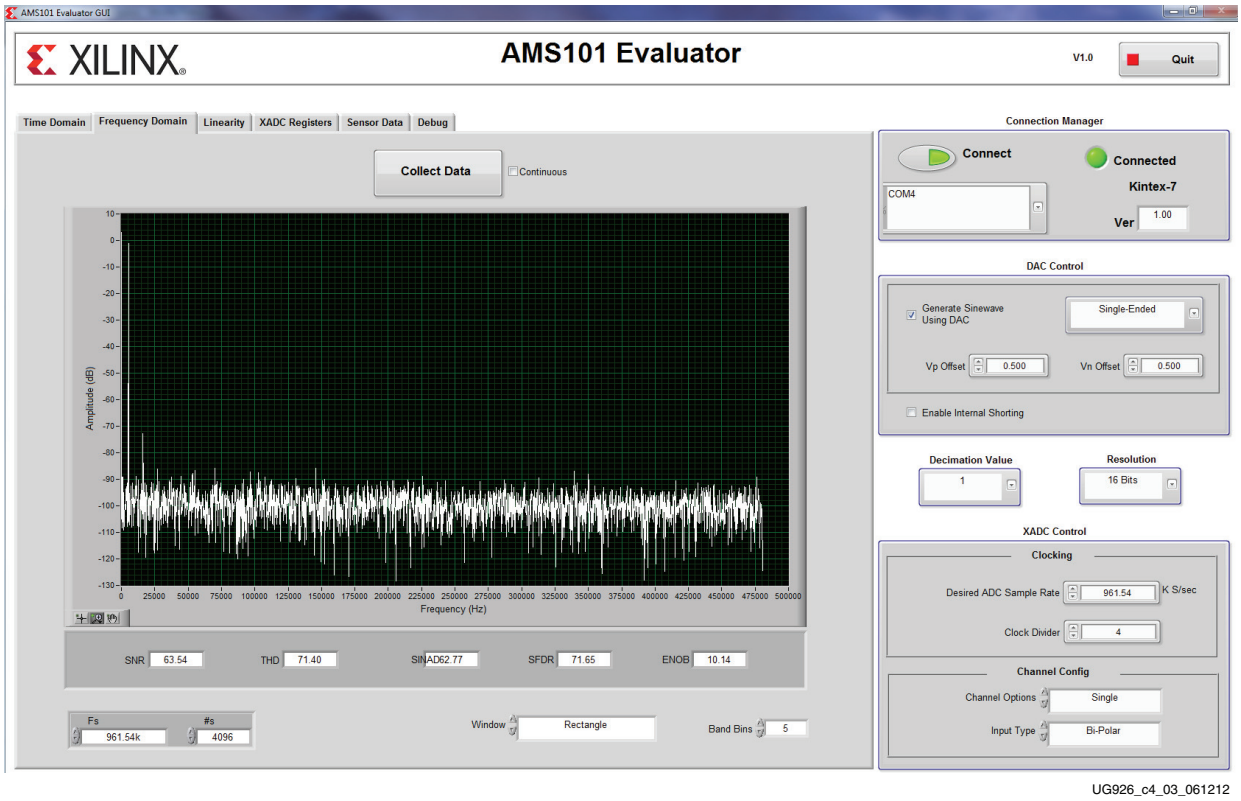


Figure 4-3: **AMS101 Evaluator GUI**

AMS Evaluator GUI source code is not provided.

For a more extensive explanation of the AMS101 evaluation card and the applicable files, refer to UG886, *AMS101 Evaluation Card User Guide*.

Next Steps

For more information on reference designs included in this kit, software, and additional tutorials, including how to restore the default content of the onboard nonvolatile storage, see the ZC702 product page at www.xilinx.com/zc702.

Next Steps for the Zynq-7000 AP SoC Video and Imaging Kit (ZVIK)

For more information on additional example designs (including a camera design), tutorials, software, and other information available for the ZVIK, see the Zynq-7000 All Programmable SoC Video and Imaging Kit product page www.xilinx.com/zvik.

Additional Resources

Xilinx Resources

For support resources such as Answers, Documentation, Downloads, and Forums, see the Xilinx Support website at:

www.xilinx.com/support.

For continual updates, add the Answer Record to your myAlerts:

www.xilinx.com/support/myalerts.

For a glossary of technical terms used in Xilinx documentation, see:

www.xilinx.com/company/terms.htm.

Solution Centers

See the Xilinx Solution Centers for support on devices, software tools, and intellectual property at all stages of the design cycle. Topics include design assistance, advisories, and troubleshooting tips.

Further Resources

The most up to date information related to the ZC702 board and its documentation is available on the following websites.

The Xilinx Zynq-7000 SoC ZC702 Evaluation Kit Product Page:

www.xilinx.com/zc702

The Zynq-7000 SoC ZC702 Evaluation Kit Master Answer Record:

www.xilinx.com/support/answers/47864.htm

These Xilinx documents provide supplemental material useful with this guide:

UG873, *Zynq-7000 All Programmable SoC: Concepts, Tools, and Techniques*

UG850, *ZC702 Evaluation Board for the Zynq-7000 XC7Z020 All Programmable SoC User Guide*

UG925, *Zynq-7000 All Programmable SoC ZC702 Base Targeted Reference Design User Guide*

UG886, *AMS101 Evaluation Card User Guide*

References

The following websites provide supplemental material useful with this guide:

1. Xilinx Zynq-7000 All Programmable SoC Product Table
   www.xilinx.com/publications/prod_mktg/zynq7000/Zynq-7000-combined-product-table.pdf
2. Xilinx Zynq-7000 All Programmable SoC page
   www.xilinx.com/products/silicon-devices/soc/zynq-7000/index.htm
3. XilinxZynq-7000 All Programmable SoC documentation
   www.xilinx.com/support/documentation/zynq-7000.htm
4. Xilinx Zynq-7000 AP SoC Video and Imaging Kit product page: www.xilinx.com/zvik
5. Xilinx Application Notes, Reference Designs, Video IP and Development Kits (a comprehensive listing of video and imaging application notes, white papers, reference designs, and related IP cores): www.xilinx.com/esp/video/refdes_listing.htm#ref_des
6. Xilinx Zynq-7000 All Programmable SoC Boards and Kits
   www.xilinx.com/products/boards_kits/zynq-7000.htm
7. Zynq-7000 Base TRD: wiki.xilinx.com/zc702-base-trd
8. Tera Term home page: en.sourceforge.jp/projects/ttssh2/releases/
9. Silicon Labs USB-UART drivers
   www.silabs.com/Support%20Documents/Software/CP210x_VCP_Windows.zip
10. Avnet Product Page: www.em.avnet.com/fmc-imageon-v2000c

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