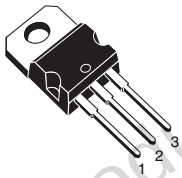
# STP75NF68

## N-channel 68 V, 0.010 Ω, 80 A, TO-220 STripFET™ II Power MOSFET

## Features

| Type | $V_{DSS}$ | $R_{DS(on)}$ max | $I_D$ |
|---|---|---|---|
| STP75NF68 | 68 V | < 0.014 Ω | 80 A |

- Exceptional dv/dt capability
- 100% avalanche tested




TO-220

## Application

- Switching applications

## Description

This Power MOSFET series realized with STMicroelectronics unique STripFET™ process has specifically been designed to minimize input capacitance and gate charge. It is therefore suitable in advanced high-efficiency switching applications.

**Figure 1. Internal schematic diagram**

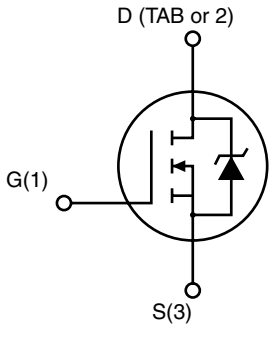



**Table 1. Device summary**

| Order code | Marking | Package | Packaging |
|---|---|---|---|
| STP75NF68 | 75NF68 | TO-220 | Tube |

Obsolete Product(s) - Obsolete Product(s)

# Contents

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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DS}$ | Drain-source voltage ($V_{GS}$ = 0) | 68 | V |
| $V_{GS}$ | Gate-source voltage | ± 20 | V |
| $I_D$ | Drain current (continuous) at $T_C$ = 25 °C | 80 | A |
| $I_D$ | Drain current (continuous) at $T_C$=100 °C | 56 | A |
| $I_{DM}$ (1) | Drain current (pulsed) | 320 | A |
| $P_{TOT}$ | Total dissipation at $T_C$ = 25 °C | 190 | W |
| | Derating factor | 1.27 | W/°C |
| dv/dt (2) | Peak diode recovery voltage slope | 13 | V/ns |
| $E_{AS}$ (3) | Single pulse avalanche energy | 700 | mJ |
| $T_{stg}$ | Storage temperature | -55 to 175 | °C |
| $T_J$ | Operating junction temperature | 175 | °C |

1. Pulse width limited by safe operating area
2. $I_{SD} \leq$ 80 A, di/dt ≤ 300 A/µs, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq T_{JMAX}$
3. Starting $T_J$ = 25 °C, $I_D$ = 40 A, $V_{DD}$ = 34 V

**Table 3. Thermal data**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $R_{thj\text{-}case}$ | Thermal resistance junction-case max | 0.79 | °C/W |
| $R_{thj\text{-}amb}$ | Thermal resistance junction-ambient max | 62.5 | °C/W |
| $T_l$ | Maximum lead temperature for soldering purpose(1) | 300 | °C |

1. 1.6mm from case for 10 sec

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# 2 Electrical characteristics

($T_{CASE}$=25°C unless otherwise specified)

**Table 4. On/off states**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage | $I_D$ = 250 µA, $V_{GS}$= 0 | 68 | | | V |
| $I_{DSS}$ | Zero gate voltage drain current ($V_{GS}$ = 0) | $V_{DS}$ = Max rating,<br>$V_{DS}$ = Max rating @125 °C | | | 1<br>10 | µA<br>µA |
| $I_{GSS}$ | Gate body leakage current ($V_{DS}$ = 0) | $V_{GS}$ = ±20 V | | | ±100 | nA |
| $V_{GS(th)}$ | Gate threshold voltage | $V_{DS}$= $V_{GS}$, $I_D$ = 250 µA | 2 | 3 | 4 | V |
| $R_{DS(on)}$ | Static drain-source on resistance | $V_{GS}$= 10 V, $I_D$= 40 A | | 0.010 | 0.014 | Ω |

**Table 5. Dynamic**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $g_{fs}$ (1) | Forward transconductance | $V_{DS}$ = 15 V, $I_D$ = 40 A | | 60 | | S |
| $C_{iss}$<br>$C_{oss}$<br>$C_{rss}$ | Input capacitance<br>Output capacitance<br>Reverse transfer capacitance | $V_{DS}$ =25 V, f = 1 MHz,<br>$V_{GS}$ = 0 | | 2550<br>550<br>175 | | pF<br>pF<br>pF |
| $Q_g$<br>$Q_{gs}$<br>$Q_{gd}$ | Total gate charge<br>Gate-source charge<br>Gate-drain charge | $V_{DD}$ = 34 V, $I_D$ = 80 A<br>$V_{GS}$ =10 V | | 75<br>17<br>30 | | nC<br>nC<br>nC |

1. Pulsed: pulse duration=300µs, duty cycle 1.5%

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**Table 6. Switching times**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $t_{d(on)}$<br>$t_r$<br>$t_{d(off)}$<br>$t_f$ | Turn-on delay time<br>Rise time<br>Turn-off delay time<br>Fall time | $V_{DD}$= 34 V, $I_D$= 40 A,<br>$R_G$=4.7 Ω, $V_{GS}$=10 V<br>*Figure 13 on page 8* | | 17<br>60<br>90<br>75 | | ns<br>ns<br>ns<br>ns |

**Table 7. Source drain diode**

| Symbol | Parameter | Test conditions | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{SD}$ | Source-drain current | | | | 80 | A |
| $I_{SDM}$(1) | Source-drain current (pulsed) | | | | 320 | A |
| $V_{SD}$(2) | Forward on voltage | $I_{SD}$ = 80 A, $V_{GS}$ = 0 | | | 1.5 | V |
| $t_{rr}$<br>$Q_{rr}$<br>$I_{RRM}$ | Reverse recovery time<br>Reverse recovery charge<br>Reverse recovery current | $I_{SD}$ = 80 A,<br>di/dt = 100 A/µs,<br>$V_{DD}$ = 25 V, $T_J$ = 150 °C<br>*Figure 15 on page 8* | | 70<br>160<br>4.7 | | ns<br>µC<br>A |

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300µs, duty cycle 1.5%

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## 2.1 Electrical characteristics (curves)

**Figure 2. Safe operating area**

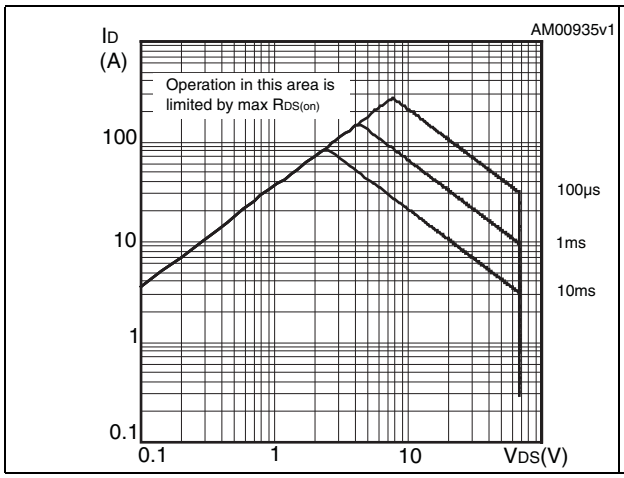



**Figure 3. Thermal impedance**

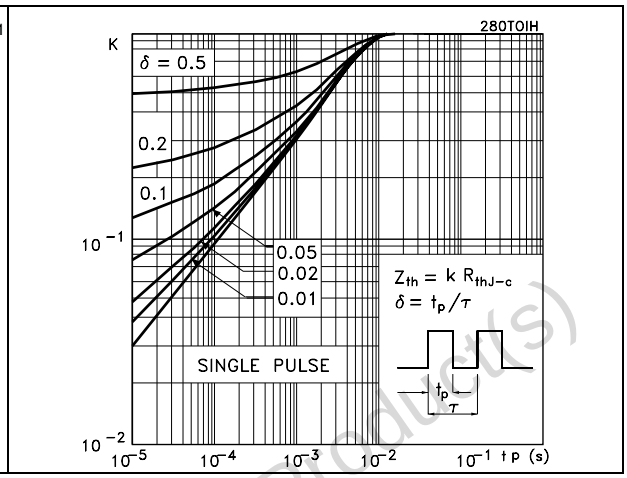



**Figure 4. Output characteristics**

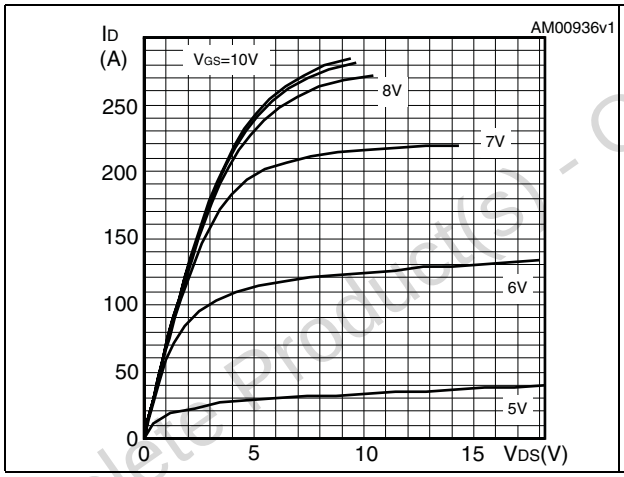



**Figure 5. Transfer characteristics**

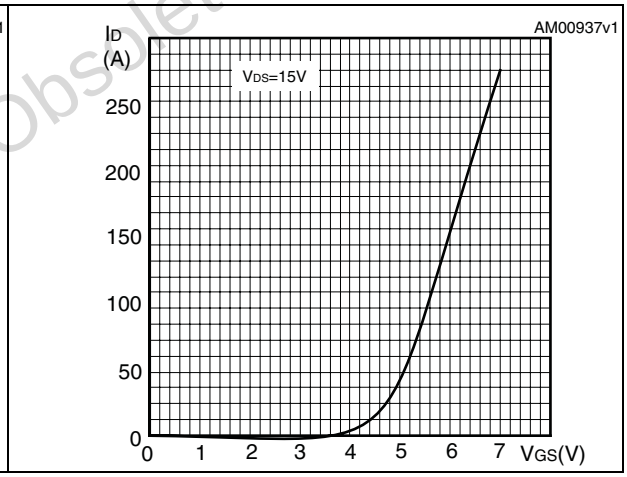



**Figure 6. Normalized $BV_{DSS}$ vs temperature**

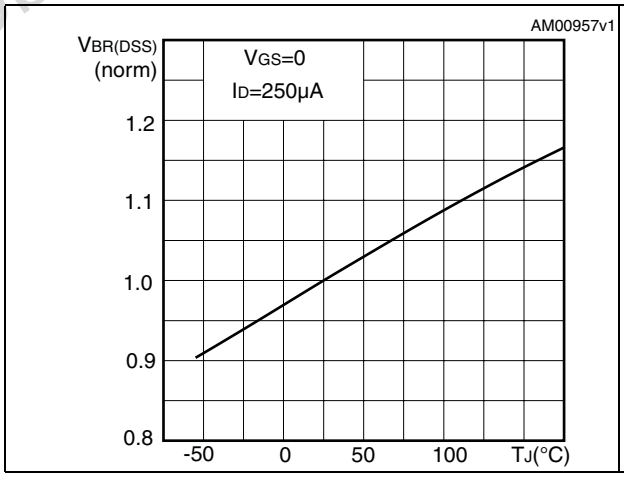
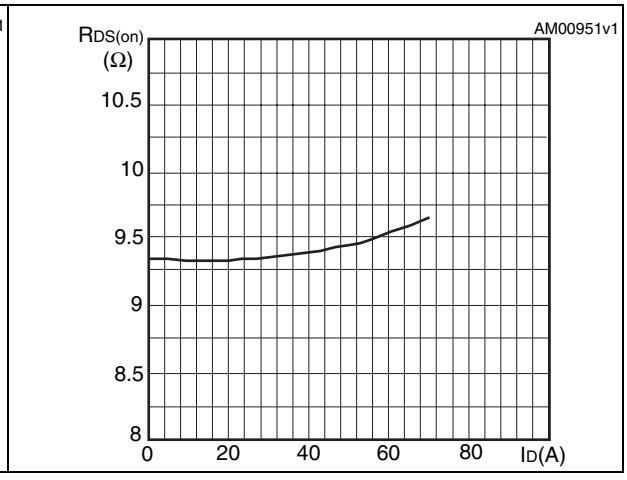



**Figure 7. Static drain-source on resistance**




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**Figure 8. Gate charge vs gate-source voltage**

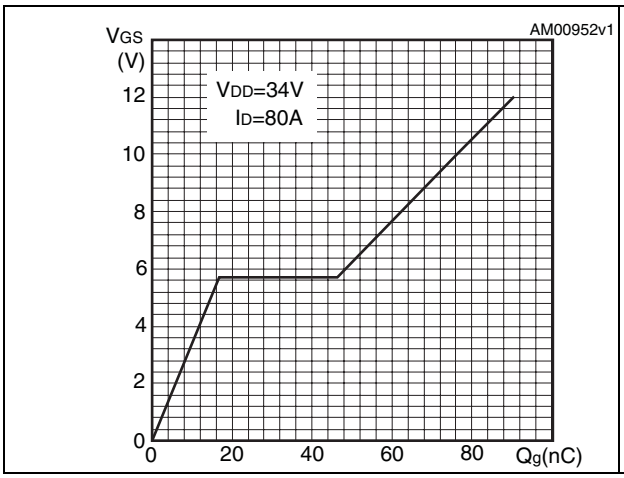



**Figure 9. Capacitance variations**

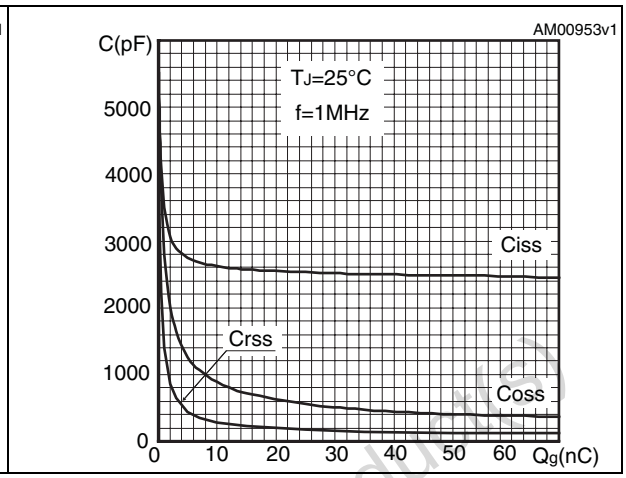



**Figure 10. Normalized gate threshold voltage vs temperature**

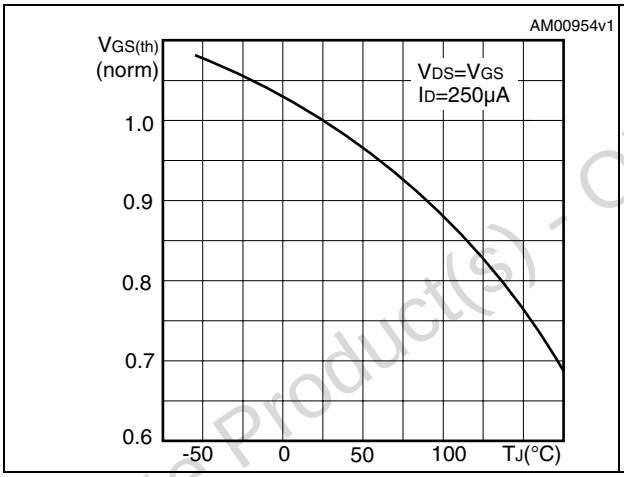



**Figure 11. Normalized on resistance vs temperature**

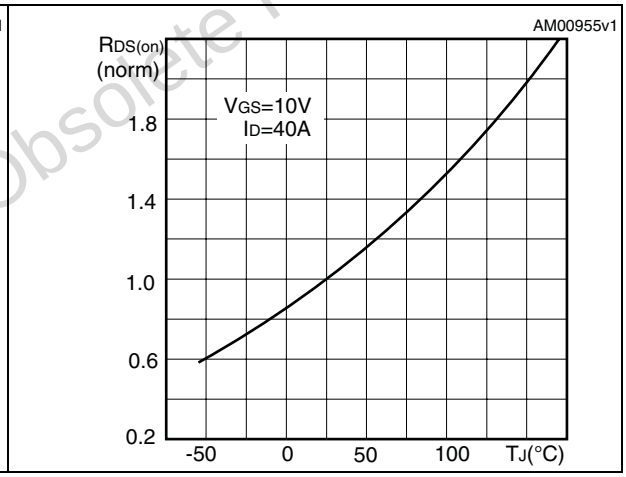
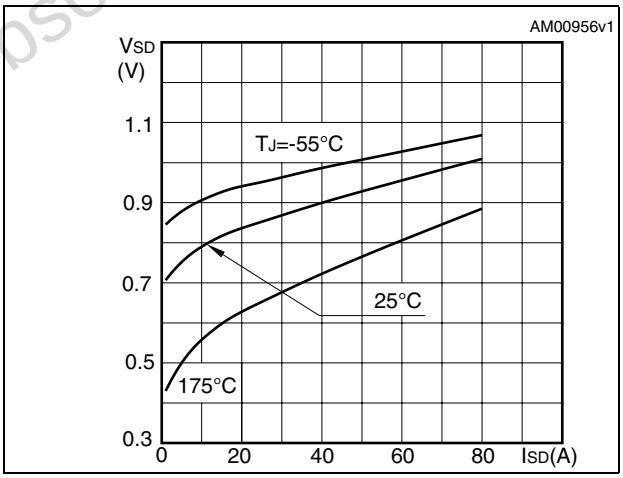



**Figure 12. Source-drain diode forward characteristics**




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# 3 Test circuits

**Figure 13. Switching times test circuit for resistive load**

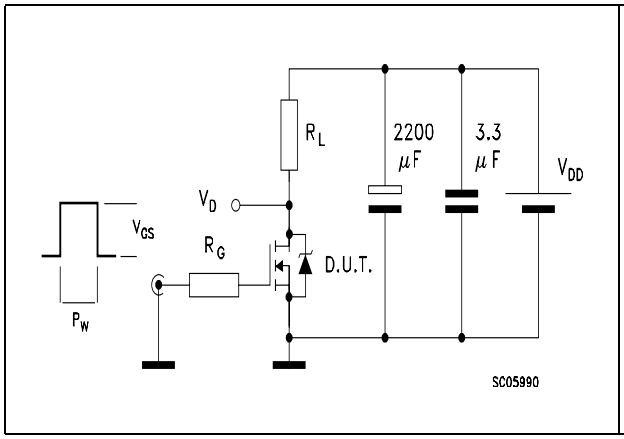



**Figure 14. Gate charge test circuit**

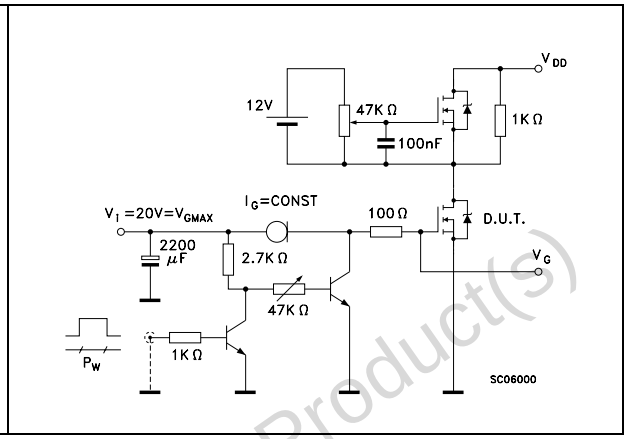



**Figure 15. Test circuit for inductive load switching and diode recovery times**

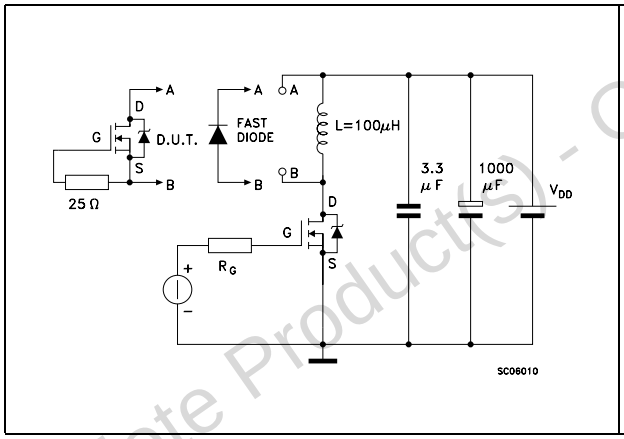



**Figure 16. Unclamped inductive load test circuit**

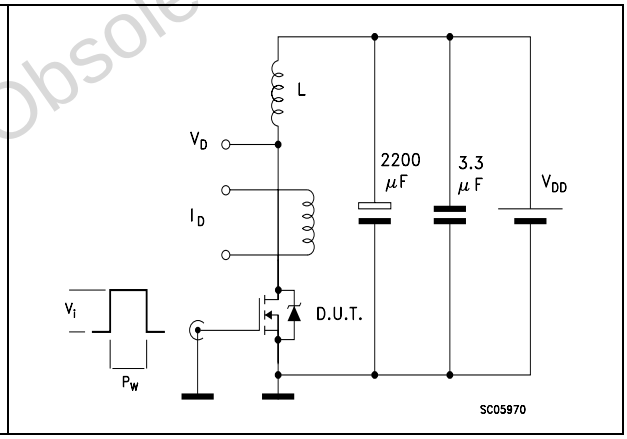
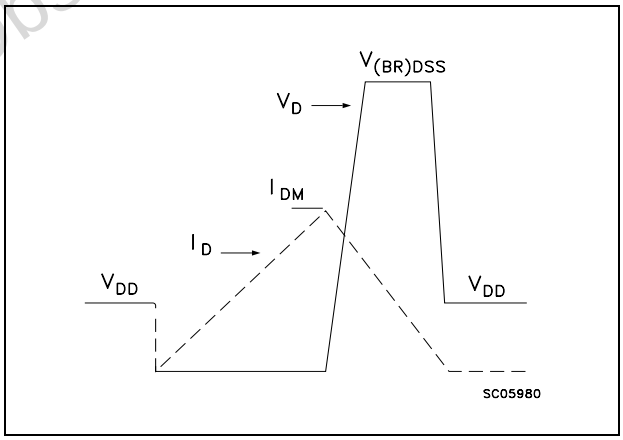



**Figure 17. Unclamped inductive waveform**




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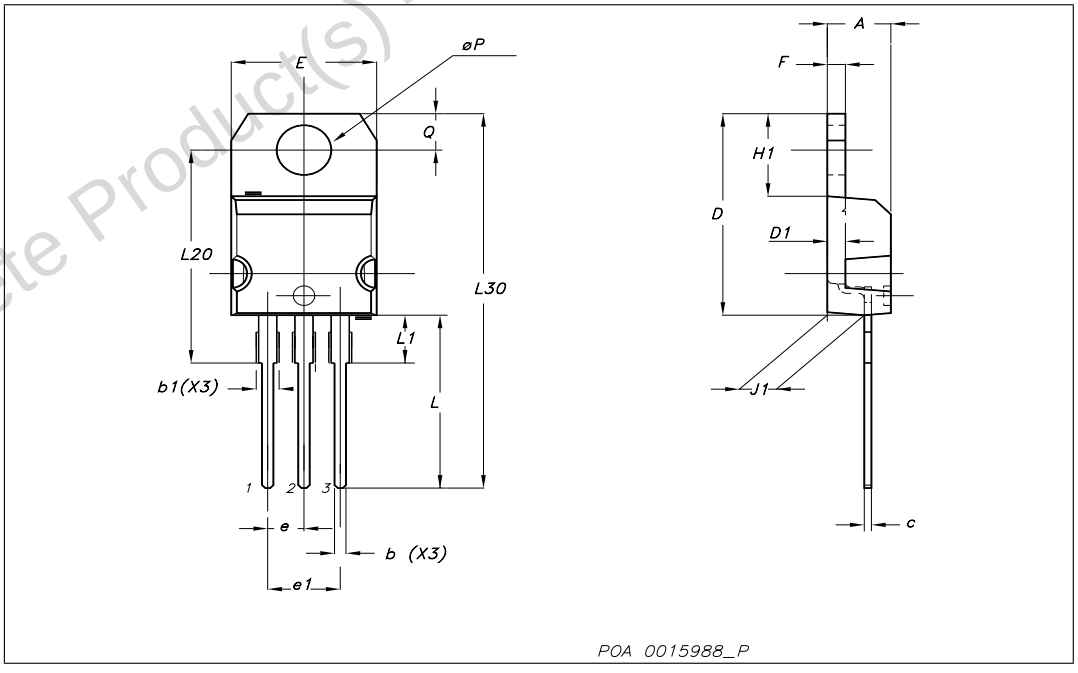
# 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: *www.st.com*

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## TO-220 mechanical data

| Dim | mm | | | inch | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | 4.40 | | 4.60 | 0.173 | | 0.181 |
| b | 0.61 | | 0.88 | 0.024 | | 0.034 |
| b1 | 1.14 | | 1.70 | 0.044 | | 0.066 |
| c | 0.49 | | 0.70 | 0.019 | | 0.027 |
| D | 15.25 | | 15.75 | 0.6 | | 0.62 |
| D1 | | 1.27 | | | 0.050 | |
| E | 10 | | 10.40 | 0.393 | | 0.409 |
| e | 2.40 | | 2.70 | 0.094 | | 0.106 |
| e1 | 4.95 | | 5.15 | 0.194 | | 0.202 |
| F | 1.23 | | 1.32 | 0.048 | | 0.051 |
| H1 | 6.20 | | 6.60 | 0.244 | | 0.256 |
| J1 | 2.40 | | 2.72 | 0.094 | | 0.107 |
| L | 13 | | 14 | 0.511 | | 0.551 |
| L1 | 3.50 | | 3.93 | 0.137 | | 0.154 |
| L20 | | 16.40 | | | 0.645 | |
| L30 | | 28.90 | | | 1.137 | |
| ∅P | 3.75 | | 3.85 | 0.147 | | 0.151 |
| Q | 2.65 | | 2.95 | 0.104 | | 0.116 |




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# 5 Revision history

**Table 8. Document revision history**

| Date | Revision | Changes |
|---|---|---|
| 24-Jul-2008 | 1 | First release |
| 06-Aug-2008 | 2 | Document status promoted from preliminary data to datasheet |

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