TPS2505 Integrated Dual USB Switches, Boost Converter and LDO

1 Features

- Integrated Synchronous Boost Converter, LDO, and Dual USB Current-Limited Switches
- 1.8-V to 5.25-V Input Voltage (2.2-V Minimum Start-Up Voltage)
- Adjustable Independent USB Current Limit
  - 100 mA to 1100 mA
- Auxiliary 5.1-V Output
- 3.3-V Linear Regulator Output
- Inrush Current < 100 mA
- Minimal External Components Required
- Deglitched Independent Fault Reporting
- Small 5-mm × 5-mm QFN-20 Package
- Industrial Temperature Range

2 Applications

- Portable Applications Using Single Li+ Cell
- Bus Powered USB Hosts
- USB Hosts Without Native 5-V Supplies
- Computer Peripherals

3 Description

The TPS2505 device provides an integrated solution to meet USB 5-V power requirements from a 1.8-V to 5.25-V input supply. The features include a 5.1-V, 1100-mA boost converter, a 200-mA, 3.3-V LDO linear regulator and dual USB 2.0 compliant power outputs with independent output switch enable, current limit, and overcurrent fault reporting.

The 1.8-V to 5.25-V input can be supplied by sources including DC-DC regulated supplies (for example, 3.3 V), or batteries such as single cell Li+, two-cell or three-cell NiCd, NiMH or alkaline.

The output trip current for the dual USB switches can be programmed through external resistors from as low as 100 mA to as high as 1100 mA.

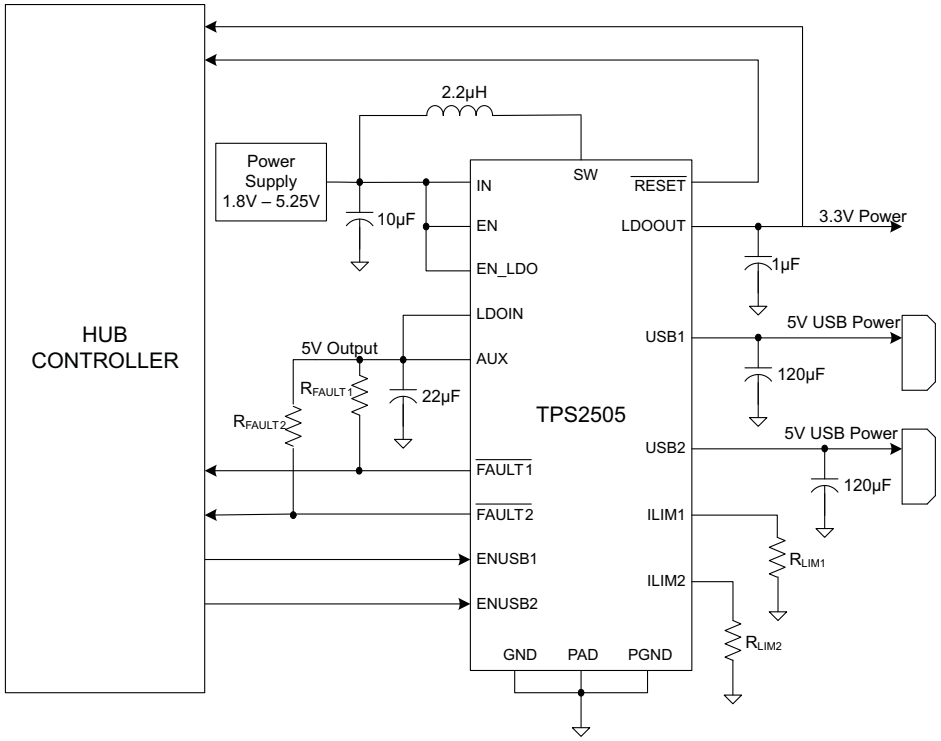
An auxiliary 5.1-V output is provided, where the total current supplied by the USB outputs and the auxiliary by cannot exceed 1100 mA.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS2505	VQFN (20)	5.00 mm × 5.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

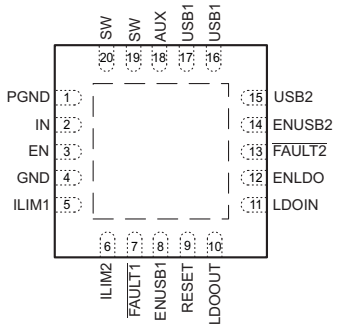
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (June 2010) to Revision C	Page
• Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1

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5 Pin Configuration and Functions

RGW Package
20-Pin VQFN With Exposed Thermal Pad
Top View



Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
AUX	18	O	Fixed 5.1-V boost converter output. Connect a low-ESR ceramic capacitor from AUX to PGND.
EN	3	I	Enable input for boost converter. Tie to IN to enable.
ENLDO	12	I	Enable input for the LDO. Tie to AUX to enable.
ENUSB1	8	I	Enable input for the USB1 switch. Tie to IN or AUX to enable.
ENUSB2	14	I	Enable input for the USB2 switch. Tie to IN or AUX to enable.
$\overline{\text{FAULT1}}$	7	O	Active low USB1 fault indicator (open drain).
$\overline{\text{FAULT2}}$	13	O	Active low USB2 fault indicator (open drain).
GND	4	P	Control / logic ground. Must be tied to PGND close to the IC externally.
ILIM1	5	I	Program the nominal USB1 switch current-limit threshold with a resistor to GND.
ILIM2	6	I	Program the nominal USB2 switch current-limit threshold with a resistor to GND.
IN	2	I	Input supply voltage for boost converter.
LDOIN	11	I	Input supply voltage for LDO. Connect to AUX.
LDOOUT	10	O	Fixed 3.3-V LDO output. Connect a low-ESR ceramic capacitor from LDOOUT to GND.
PGND	1	P	Source connection for the internal low-side boost converter power switch. Connect to GND with a low impedance connection to the input and output capacitors.
RESET	9	O	Active low LDO output good indicator (open drain).
SW	19	P	Boost and rectifying switch input. This node is switched between PGND and AUX. Connect the boost inductor from IN to SW.
SW	20	P	Boost and rectifying switch input. This node is switched between PGND and AUX. Connect the boost inductor from IN to SW.
USB1	16	O	Output of the USB1 power switch. Connect to the USB1 port.
USB1	17	O	Output of the USB1 power switch. Connect to the USB1 port.
USB2	15	O	Output of the USB2 power switch. Connect to the USB2 port.
Thermal Pad	—	—	Internally connected to PGND. Must be soldered to board ground for thermal dissipation.

(1) I = Input; O = Output; P = Power

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6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted).[1][2]

	MIN	MAX	UNIT
Input voltage on SW, AUX, IN, USB, ENUSB, EN, FAULT, ILIM	–0.3	7	V
FAULT sink current		25	mA
ILIM source current		1	mA
Operating junction temperature, T_J	–40	125	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Voltages are referenced to GND and PGND tied together.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1]	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[2]	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{IN}	Supply voltage at IN	1.8	5.25	V
V_{START}	Supply voltage at IN for start-up	2.2		V
	Enable voltage at EN, ENUSB1, ENUSB2, ENLDO	0	5.25	V
T_A	Operating free air temperature range	–40	85	°C
T_J	Operating junction temperature range	–40	125	°C

6.4 Thermal Information

THERMAL METRIC[1]		TPS2505 RGW (VQFN) 20 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	34.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	30	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	13.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	13.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

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6.5 Electrical Characteristics (Shared Boost, LDO and USB)

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
BIAS								
	Bias Current	V_{IN}	V_{IN} = 3.3 V, V_{AUX} = 5.2 V, V_{EN} = V_{IN}, V_{ENUSB1} = V_{AUX}, I_{AUX} = I_{USB} = 0 A			15	25	µA
		V_{AUX}				500	600	
	Shutdown current	V_{IN}	V_{IN} = 3.3 V, V_{EN} = V_{ENUSB} = 0 V, AUX and USB OPEN, –40°C ≤ T_J ≤ 85°C			5		µA
UVLO								
	Undervoltage lockout threshold on IN for boost converter		V_{IN} rising		2.08		2.20	V
			V_{IN} falling, V_{AUX} = 5.2 V	Threshold	1.69		1.85	
				Hysteresis		0.4		
			V_{IN} falling, V_{AUX} = OPEN	Threshold	1.93		2.05	
				Hysteresis		0.15		
	Undervoltage lockout threshold on AUX for USB switches		V_{AUX} rising		4.18		4.45	V
			V_{AUX} falling	Threshold	4.1		4.37	
				Hysteresis		0.09		
THERMAL SHUTDOWN								
	Full thermal shutdown thereshold				150			°C
	Hysteresis					10		°C
	USB only thermal shutdown				130			°C
	Hysteresis					10		°C

6.6 Electrical Characteristics (Boost Only)

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
APPLICATION SPECIFICATIONS						
V_{AUX}	AUX regulation voltage	Includes ripple and line/load regulation USB1/2 enabled $C_{USB1/2}$ = 100 µF	4.75	5.1	5.25	V
V_{RIPPLE}	AUX ripple voltage	PFM, I_O = 100 mA USB1/2 enabled $C_{USB1/2}$ = 100 µF			250	mV
		PWM, I_O = 1100 mA USB1/2 enabled $C_{USB1/2}$ = 100 µF			75	
	Load regulation(1)	I_O = 0 mA to 1100 mA (PWM operation only)			50	mV
	Line regulation	I_O = 1100 mA (PWM operation)			50	mV
		I_O = 1100 mA, V_{IN} = 3.6 V to 5.25 V			300(2)	
V_{REF}	Internal reference voltage			1.35		V
OSCILLATOR						
freq	Switching frequency, normal mode	V_{IN} < V_{LFM}	850	1000	1150	kHz
	Switching frequency, low-frequency mode	V_{IN} > V_{LFM}	225	250	275	kHz
V_{LFM}	Low-frequency mode input voltage threshold		4.25	4.35	4.45	V
	Hysteresis			200		mV

(1) Load regulation in No Frequency or Pass-Through is given by IR drop across SWP switch resistance..
(2) Includes voltage drop when transitioning to No Frequency or Pass-Through Mode, where V_{AUX} is no longer a closed loop regulated voltage and drops to $V_{NFM} – I_{LOAD}R_{SWP}$. For No Frequency or Pass-Through, $\Delta V_{AUX}/ \Delta V_{IN}$ = 1.

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Electrical Characteristics (Boost Only) (continued)

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{NFM}	No-frequency mode input voltage threshold (Boost SYNC MOSFET always on)	V_{IN} rising	4.9	5.05	5.17	V
	Hysteresis			75		mV
	Maximum duty cycle			85%		
	Minimum controllable on-time			85		ns
PULSE FREQUENCY MODE (PFM)						
$IIND_{LOW}$	Demanded peak current to enter PFM mode	Peak inductor current, falling		420		mA
AUX_{LOW}	AUX too low comparator threshold	Resume switching due to AUX, falling		0.98 × V_{AUX}		V
POWERSTAGE						
	Switch on resistance (SWN)				120	mΩ
I_{SW}	Peak switch current limit (SWN MOSFET)		3	4.5	6	A
	Switch ON-resistance (SWP)	$V_{sg} = V_{MAX}$			125	mΩ
	Switch ON-resistance (SWP + USB)	$V_{IN} > V_{NFM}$		125	185	mΩ
START UP(3)						
I_{START}	Constant current				0.1	A
V_{EXIT}	Constant current exit threshold ($V_{IN} – V_{AUX}$)			700		mV
$t_{startup}$	Boost startup time	V_{IN} = 5.1 V, C_{OUT} = 150 µF		25	40	ms
BOOST ENABLE (EN)						
	Enable threshold, boost converter		0.7		1	V
I_{EN}	Input current	V_{EN} = 0 V or 5.5 V	–0.5		0.5	µA

(3) V_{AUX} pin must be unloaded during start-up.

6.7 Electrical Characteristics (USB1/2 Only)

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
USB1, USB2						
$r_{DS(on)}$	USB switch resistance				80	mΩ
t_r	Rise time, output	V_{AUX} = 5.1 V, C_L = 100 µF, R_L = 10 Ω		2	3	ms
t_f	Fall time, output	V_{AUX} = 5.1 V, C_L = 100 µF, R_L = 10 Ω		2.5	3.5	ms
$V_{USB1/2}$	USB1/2 output voltage	Including ripple C_L = 100 µF	4.75		5.25	mV
USB ENABLE (ENUSB1, ENUSB2)						
	Enables threshold, USB switch		0.7		1	V
I_{ENUSB}	Input current	V_{ENUSB} = 0 V or 5.5 V	–0.5		0.5	µA
	Turnon time	C_L = 100 µF, R_L = 10 Ω			5	ms
	Turnoff time	C_L = 100 µF, R_L = 10 Ω			10	ms
/FAULT1, /FAULT2						
	Output low voltage	$I_{/FAULT}$ = 1 mA			150	mV
	Off-state current	$V_{/FAULT}$ = 5.5 V			1	µA
t_{DEG}	/FAULT deglitch	/FAULT assertion or deassertion due to over-current condition	6	8	10	ms

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Electrical Characteristics (USB1/2 Only) (continued)

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ILIM1, ILIM2						
I_{OS}	Short-circuit output current	R_{ILIM} = 100 kΩ	190		380	mA
		R_{ILIM} = 40 kΩ	550		875	
		R_{ILIM} = 20 kΩ	1140		1700	

6.8 Electrical Characteristics (LDO and Reset Only)

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LDO SPECIFICATIONS						
	Input voltage		3.8	5.1	5.25	V
	Output voltage	Including line/load regulation	3.2	3.3	3.4	V
	DC accuracy				±3%	
	Line regualtion	I_{LOAD}: 200 mA			5	mV
	Line transient	500 mV step at 50 mV/µs			15	mV
	Load regulation				20	mV
	Load transient	I_{LOAD}: 0 mA - 200 mA in 1 µs			120	mV
	Dropout voltage				300	mV
	Output overshoot				3%	
t_r	Rise time, output	V_{AUX} = 5.1 V, C_L = 1 µF			200	µs
t_f	Fall time, output	V_{AUX} = 5.1 V, C_L = 1 µF			1	ms
I_{OS}	Short-circuit output current		350		800	mA
	PSRR	20 Hz < f < 20 kHz, I_L = 100 mA		40		dB
RESET SPECIFICATIONS						
	Threshold voltage	V_{LDOOUT} rising	3.09	3.1	3.11	V
		V_{LDOOUT} falling	2.91	2.975	3.03	
	Deglitch timing	Low to high transition	150	175	200	ms
	Internal pullup resistance		8	10	12	kΩ

6.9 Recommended External Components

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
	Inductor	2.2		4.7	µH
	Boost input capacitance (ceramic capacitor, X5R, 10V, 0805)		10		µF
	Boost output capacitance (ceramic capacitor, X5R, 10V, 1210)		22		µF
	LDO input capacitance (ceramic capacitor, X5R)		4.7		µF
	LDO output capacitance (ceramic capacitor, X5R)	0.7	1		µF
R_{ILIM}	Current-limit set resistor from ILIM to GND	20		220	kΩ

6.10 Dissipation Ratings

PACKAGE	$R_{\theta JA}$	$T_A \leq 25°C$ POWER RATING
RGW	34.3 C°/W	2.4 W

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6.11 Typical Characteristics

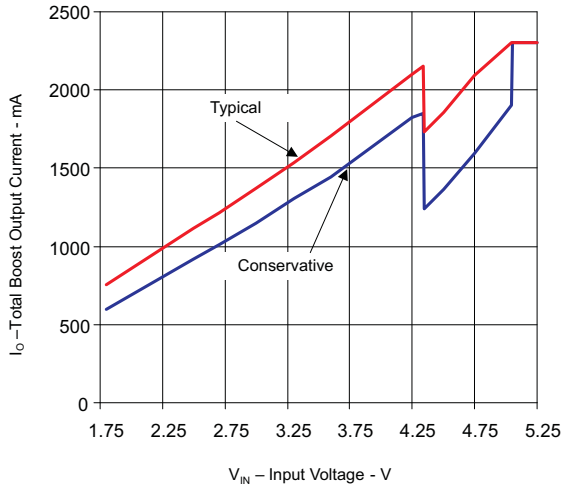


Figure 1. Maximum Total DC-DC Current vs Input Voltage

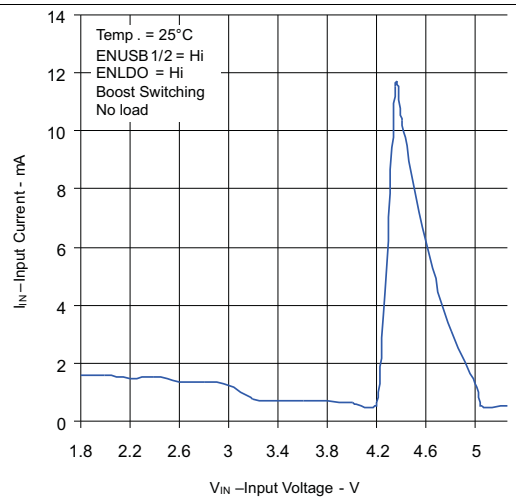


Figure 2. TPS2505 Typical On Input Current With No Load

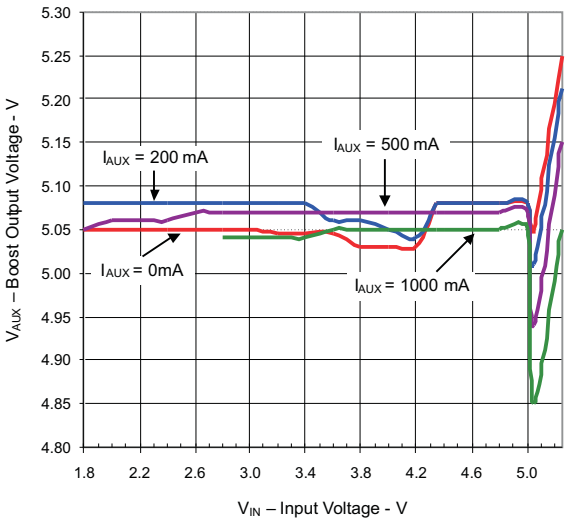


Figure 3. Boost Output Voltage vs Input Voltage

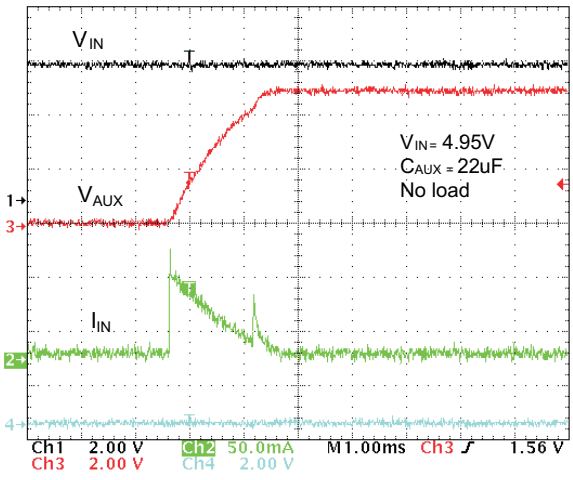


Figure 4. Boost Start-Up After Enable – No Load

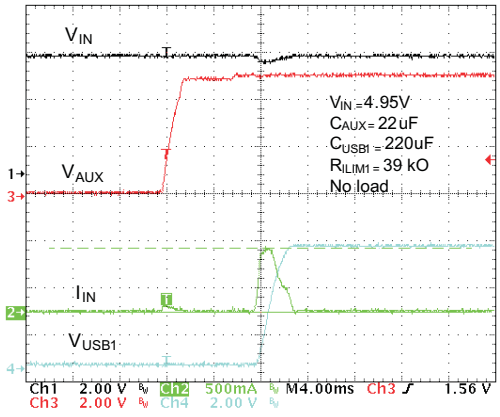


Figure 5. USB1 Start-Up After Enable – No Load

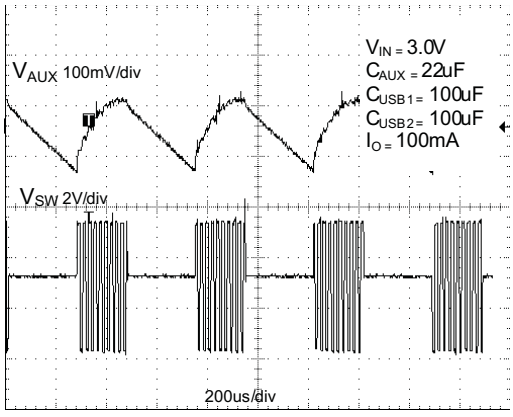


Figure 6. Boost Output Ripple in PFM Operation

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Typical Characteristics (continued)

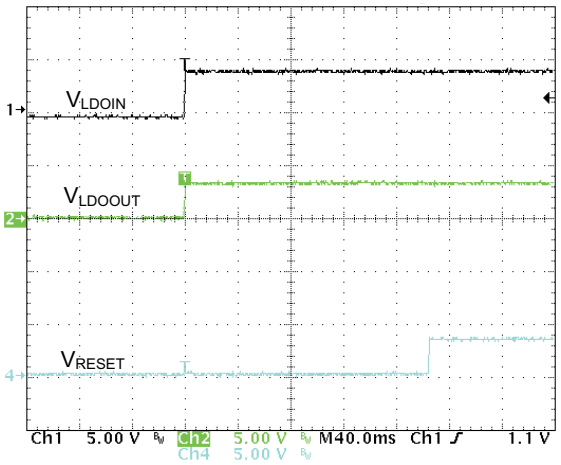


Figure 7. LDO RESET Deglitch Time

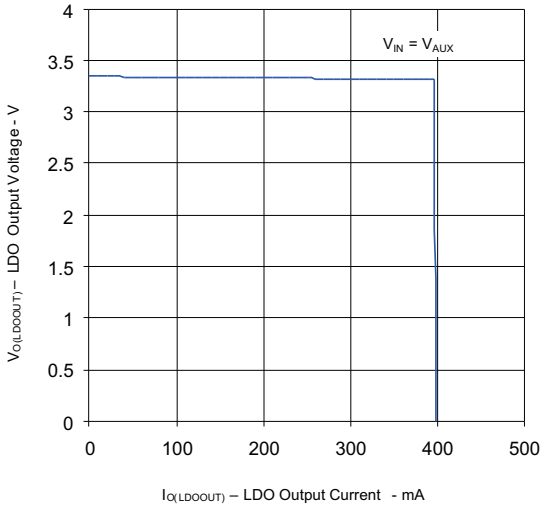


Figure 8. LDO Output Voltage vs Output Current

7 Parameter Measurement Information

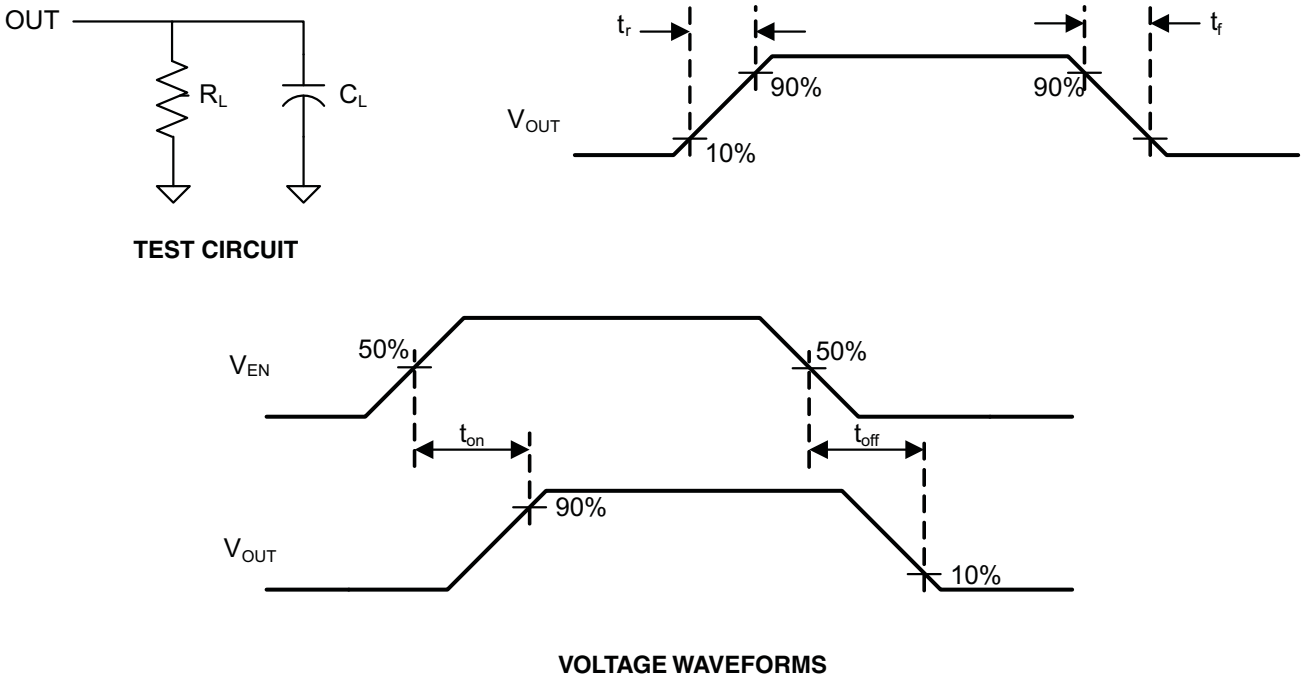


Figure 9. Test Circuit and Voltage Waveforms

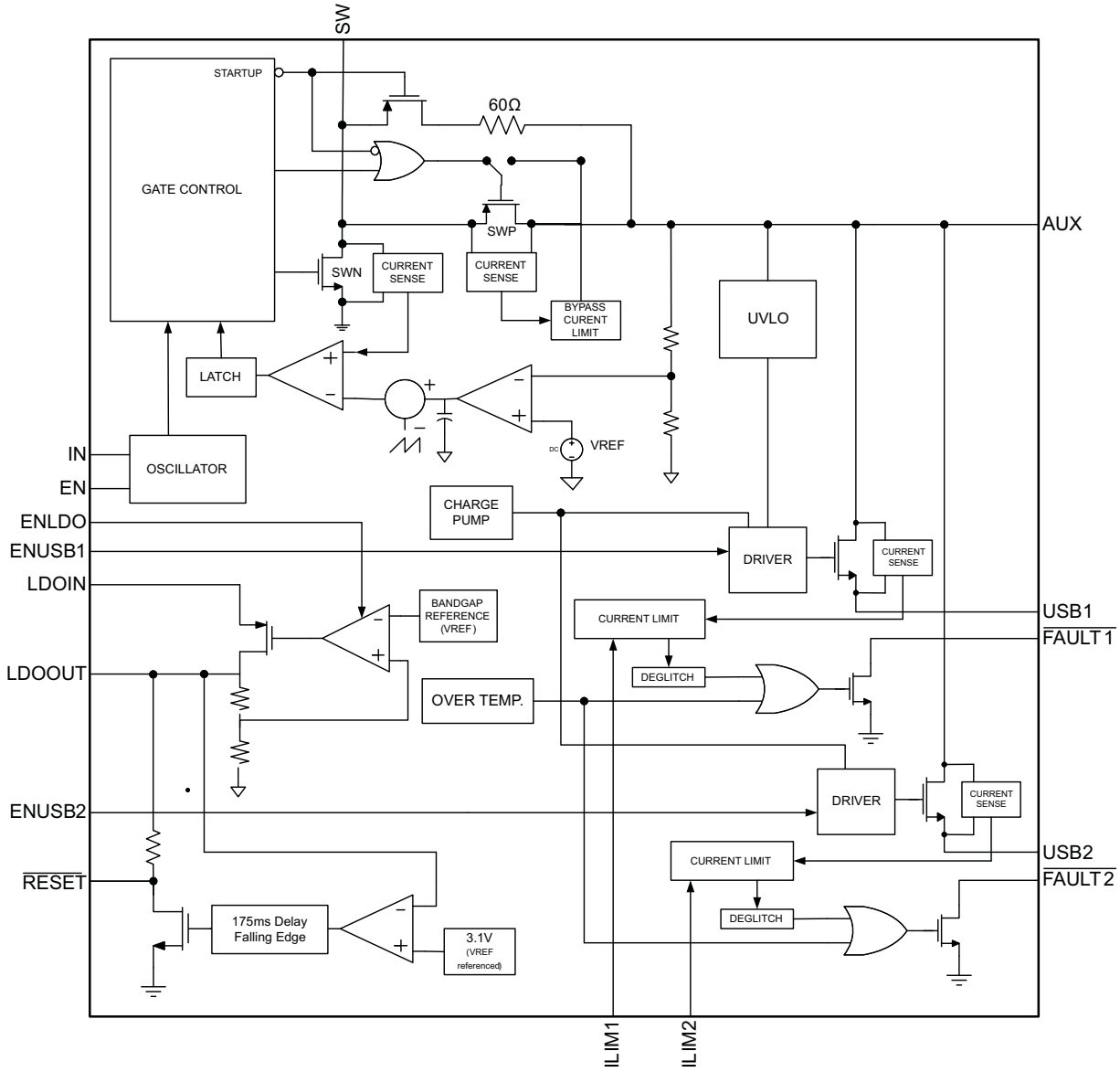
8 Detailed Description

8.1 Overview

This device targets applications for host-side USB devices where a 5-V power rail, required for USB operation, is unavailable. The TPS2505 integrates the functionality of a synchronous boost converter, 3.3-V LDO with power good RESET signal and dual USB switches into a monolithic integrated circuit so that lower-voltage rails can be used directly to provide USB power. The TPS2505 can also be powered by an upstream USB port as it limits the inrush current during power up to less than 100 mA to meet USB 2.0 specifications.

The boost converter is highly integrated, including the switching MOSFETs (low-side N-channel, high-side synchronous P-channel), gate-drive and analog-control circuitry, and control-loop compensation. Additional features include high-efficiency light-load operation, overload and short-circuit protection, and controlled monotonic soft start. The USB switch integrates all necessary functions, including back-to-back series N-channel MOSFETs, charge-pump gate driver, and analog control circuitry. The current-limit protection is user-adjustable by selecting the RILIM1/2 resistors from ILIM1/2 to GND.

8.2 Functional Block Diagram



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8.3 Feature Description

8.3.1 PGND

PGND is the internal ground connection for the source of the low-side N-channel MOSFET in the boost converter. Connect PGND to an external plane near the ground connection of the input and output capacitors to minimize parasitic effects due to high switching currents of the boost converter. Connect PGND to GND and the thermal pad externally at a single location to provide a star-point ground. See for further details.

8.3.2 IN

IN is the input voltage supply for the boost converter. Connect a 10-µF ceramic capacitor (minimum) from IN to PGND. See *Component Recommendations* for further details on selecting the input capacitor.

8.3.3 EN

EN is a logic-level input that enables the boost converter. Pull EN above 1 V to enable the device and below 0.7 V to disable the device. EN also disables the USB switches and LDO.

8.3.4 GND

Signal and logic circuits of the TPS2505 are referenced to GND. Connect GND to a quiet ground plane near the device. An optional 0.1-µF capacitor can be connected from VIN to GND close the device to provide local decoupling. Connect GND and PGND to the thermal pad externally at a single location to provide a star-point ground. See for further details.

8.3.5 ILIM1/2

Connect a resistor from ILIM1/2 to GND to program the current-limit threshold of the USB switches. Place this resistor as close to the device as possible to prevent noise from coupling into the internal circuitry. Do not drive ILIM1/2 with an external source. The current-limit threshold is proportional to the current through the RILIM resistor. See *Programming the Current-Limit Threshold Resistor R_{ILIM}* for details on selecting the current-limit resistor.

8.3.6 RESET

The RESET output indicates when the LDO output reaches 3.1 V. It has a 175-ms delay for deglitch in the low to high transition. The output has in internal 10-kΩ pull-up resistor to the LDO output.

8.3.7 LDOOUT

LDOOUT is the LDO output. Internal feedback regulates LDOOUT to 3.3 V. Connect a 1-µF ceramic capacitor from LDOOUT to PGND for compensation. See *Component Recommendations* for further details.

8.3.8 LDOIN

LDOIN is the input voltage supply for the LDO. Connect a 4.7-µF ceramic capacitor from LDOIN to PGND when not powered by AUX. See *Component Recommendations* for further details on selecting the input capacitor.

8.3.9 ENLDO

ENLDO is a logic-level input that enables the 3.3-V LDO. Pull EN above 1 V to enable the device and below 0.7 V to disable the device. The boost converter must be enabled in order for the LDO to be enabled. The boost converter is independent of ENLDO and continues to operate even when ENLDO disables the LDO.

8.3.10 FAULT1/2

FAULT1/2 are open-drain outputs that indicate when the USB switches are in an overcurrent or over-temperature condition. FAULT1/2 have a fixed internal deglitch of t_{DEG} to prevent false triggering from noise or transient conditions. FAULT1/2 assert low if the USB switches remain in an overcurrent condition for longer than t_{DEG}. FAULT1/2 de-assert when the overcurrent condition is removed after waiting for the same t_{DEG} period. Over-temperature conditions bypass the internal delay period and assert/de-assert the FAULT1/2 output immediately upon entering or leaving an over-temperature condition. FAULT1/2 are asserted low when V_{AUX} falls below V_{TRIP} (4.6 V, typical).

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Feature Description (continued)

8.3.11 ENUSB1/2

ENUSB1/2 are logic-level inputs that enable the USB switches. Pull ENUSB1/2 above 1 V to enable the USB switches and below 0.7 V to disable the USB switches. ENUSB1/2 only enables the USB switches. The boost converter is independent of ENUSB1/2 and continues to operate even when ENUSB disables the USB switch.

8.3.12 USB1/2

USB1/2 are the outputs of the USB switches and should be connected to the USB connectors to provide USB power. Although the device does not require it for operation, a bulk capacitor may be connected from USB to PGND to meet USB standard requirements. See the latest USB 2.0 specification for further details.

8.3.13 AUX

AUX is the boost converter output and provides power to the USB switches and to any additional load connected to AUX. Internal feedback regulates AUX to 5.1 V. Connect a 22-µF ceramic capacitor from AUX to PGND to filter the boost converter output. See *Component Recommendations* for further details. Additional external load can be connected to AUX as long as the total current drawn by the USB switches and external load does not overload the boost converter. See *Determining the Maximum Allowable AUX and USB1/2 Current* for details.

8.3.14 SW

SW is the internal boost converter connection of the low-side N-channel MOSFET drain and the high-side P-channel drain. Connect the boost inductor from IN to SW close to the device to minimize parasitic effects on the device operation.

8.3.15 Thermal Pad

The thermal pad connection is used to heat-sink the device to the printed-circuit board (PCB). The thermal pad may not be connected externally to a potential other than ground because it is connected to GND internally. The thermal pad must be soldered to the PCB to remove sufficient thermal energy in order to stay within the recommended operating range of the device.

8.3.16 Boost Converter

8.3.16.1 Start-Up

Input power to the TPS2505 is provided from IN to GND. The device has an undervoltage lockout (UVLO) circuit that disables the device until the voltage on IN exceeds 2.15 V (typical). The TPS2505 goes through its normal start-up process and attempts to regulate the AUX voltage to 5.1 V (typical).

The boost converter has a two-step start-up sequence. During the initial startup, the output of the boost is connected to V_{IN} through a resistive switch that limits the startup current, I_{START}, to be below 100 mA. This allows the TPS2505 to be USB 2.0 compliant when powered by an upstream USB port. The boost output must be unloaded during startup. I_{START} charges the output capacitance on V_{AUX} until V_{AUX} reaches $V_{IN} – V_{EXIT}$. The converter begins to switch once V_{AUX} exceeds $V_{IN} – V_{EXIT}$. The initial duty cycle of the device is limited by a closed-loop soft start that ramps the reference voltage to the internal error amplifier to provide a controlled, monotonic start-up on V_{AUX}. The boost converter goes through this cycle any time the voltage on V_{AUX} drops below $V_{IN} – V_{EXIT}$ due to overload conditions or the boost converter re-enables after normal shutdown.

The USB switches are powered directly from V_{AUX} and turns on once the UVLO of the USB switches is met (4.3 V typical). The turnon is controlled internally to provide a monotonic start-up on VUSB1/2.

8.3.16.2 Normal Operation

The boost converter runs at a 1-MHz fixed frequency and regulates the output voltage VAUX using a pulse-width modulating (PWM) topology that adjusts the duty cycle of the low-side N-channel MOSFET on a cycle-by-cycle basis. The PWM latch is set at the beginning of each clock cycle and commands the gate driver to turn on the low-side MOSFET. The low-side MOSFET remains on until the PWM latch is reset.

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Feature Description (continued)

Voltage regulation is controlled by a peak-current-mode control architecture. The voltage loop senses the voltage on V_{AUX} and provides negative feedback into an internal, transconductance-error amplifier with internal compensation and resistor divider. The output of the transconductance-error amplifier is summed with the output of the slope-compensation block and provides the error signal that is fed into the inverting input of the PWM comparator. Slope compensation is necessary to prevent subharmonic oscillations that may occur in peak-current mode control architectures that exceed 50% duty cycle. The PWM ramp fed into the noninverting input of the PWM comparator is provided by sensing the inductor current through the low-side N-channel MOSFET. The PWM latch is reset when the PWM ramp intersects the error signal and terminates the pulse width for that clock period. The TPS2505 stops switching if the peak-demanded current signal from the error amplifier falls below the zero-duty-cycle threshold of the device.

8.3.16.3 Low-Frequency Mode

The TPS2505 enters low-frequency mode above $V_{IN} = V_{LFM}$ (4.35 V typical) by reducing the dc/dc converter frequency from 1 MHz (typical) to 250 kHz (typical). Current-mode control topologies require internal leading-edge blanking of the current-sense signal to prevent nuisance trips of the PWM control MOSFET. The consequence of leading-edge blanking is that the PWM controller has a minimum controllable on-time (85 ns typical) that results in a minimum controllable duty cycle. In a boost converter, the demanded duty cycle decreases as the input voltage increases. The boost converter pulse-skips if the demanded duty cycle is less than what the minimum controllable ON-time allows, which is undesirable due to the excessive increase in switching ripple. When the TPS2505 enters low-frequency mode above $V_{IN} = V_{LFM}$, the minimum controllable duty cycle is increased because the minimum controllable on-time is a smaller percentage of the entire switching period. Low-frequency mode prevents pulse skipping at voltages larger than V_{LFM}. The TPS2505 resumes normal 1-MHz switching operation when V_{IN} decreases below V_{LFM}.

One effect of reducing the switching frequency is that the ripple current in the inductor and output AUX capacitors is increased. It is important to verify that the peak inductor current does not exceed the peak switch current limit I_{SW} (4.5 A typical) and that the increase in AUX ripple is acceptable during low-frequency mode.

8.3.16.4 No-Frequency Mode

The TPS2505 enters no-frequency mode above $V_{IN} = V_{NFM}$ (5.05 V typical) by disabling the oscillator and turning on the high-side synchronous PMOS 100% of the time. The input voltage is now directly connected to the AUX output through the inductor and high-side PMOS. Power dissipation in the device is reduced in no-frequency mode because there is no longer any switching loss and no RMS current flows through the low-side control NMOS, which results in higher system-level efficiency. The boost converter resumes switching when V_{IN} falls below V_{NFM}.

8.3.16.5 Pulsed Frequency Mode (PFM) Light-Load Operation

The TPS2505 enters the PFM control scheme at light loads to increase efficiency. The device reduces power dissipation while in the PFM control scheme by disabling the gate drivers and power MOSFETs and entering a pulsed-frequency mode (PFM). PFM works by disabling the gate driver when the PFM latch is set. During this time period there is no switching, and the load current is provided solely by the output capacitor. There are two comparators that determine when the device enters or leaves the PFM control scheme. The first comparator is the PFM-enter comparator. The PFM-enter comparator monitors the peak demanded current in the inductor and allows the device to enter the PFM control scheme when the inductor current falls below $IIND_{LOW}$ (420 mA typical). The second comparator is the AUX-low comparator. The AUX-low comparator monitors AUX and forces the converter out of the PFM control scheme and resumes normal operation when the voltage on AUX falls below AUXLOW (5 V typical). The PFM control scheme is disabled during low-frequency mode when $V_{IN} > V_{LFM}$ (4.35 V typical).

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Feature Description (continued)

8.3.16.6 Overvoltage Protection

The TPS2505 provides overvoltage protection on V_{AUX} to protect downstream devices. Overvoltage protection is provided by disabling the gate drivers and power MOSFETs when an overvoltage condition is detected. The TPS2505 uses a single AUX-high comparator to monitor the AUX voltage by sensing the voltage on the internal feedback node fed into the error amplifier. The AUX-high comparator disables the gate driver whenever the voltage on AUX exceeds the regulation point by 5% (typical). The gate driver remains disabled until the AUX voltage falls below the 5% high OVP threshold. The overvoltage protection feature is disabled when $VI_N > V_{NFM}$ (5.05 V typical) to prevent unwanted shutdown.

8.3.16.7 Overload Conditions

The TPS2505 boost converter uses multiple overcurrent protection features to limit current in the event of an overload or short-circuit condition. The first feature is the lower current-limit comparator that works on a cycle-by-cycle basis. This comparator turns off the low-side MOSFET by resetting the PWM latch whenever the current through the low-side MOSFET exceeds 4.5 A (typical). The low-side MOSFET remains off until the next switching cycle. The second feature is the upper current-limit comparator that disables switching for eight switching cycles whenever the current in the low-side MOSFET exceeds 6.7 A (typical). After eight switching cycles, the boost converter resumes normal operation. The third feature is the constant-current start-up I_{START} comparator that disables switching and regulates the current through the high-side MOSFET whenever the voltage on V_{AUX} drops below the input voltage by V_{EXIT} (700 mV typ). This feature protects the boost converter in the event of an output short circuit on V_{AUX}. I_{START} also current-limit protects the synchronous MOSFET in no-frequency mode when $V_{IN} > V_{NFM}$ (5.05 V typical). The converter goes through normal start-up operation once the short-circuit condition is removed. A fourth feature is the 85% (typical) maximum-duty-cycle clamp that prevents excessive current from building in the inductor.

8.3.16.8 Determining the Maximum Allowable AUX and USB1/2 Current

The maximum output current of the boost converter out of AUX depends on several system-level factors including input voltage, inductor value, switching frequency, and ambient temperature. The limiting factor for the TPS2505 is the peak inductor current, which cannot exceed I_{SW} (3 A minimum). The cycle-by-cycle current-limit turns off the low-side NMOS as a protection mechanism whenever the inductor current exceeds I_{SW}. Figure 1 can be used as a guideline for determining the maximum total current at different input voltages. The typical plot assumes nominal conditions: 2.2-µH inductor, 1-MHz/250-kHz switching frequency, nominal MOSFET on-resistances. The conservative plot assumes more pessimistic conditions: 1.7-µH inductor, 925-kHz/230-kHz switching frequency, and maximum MOSFET on-resistances. The graph accounts for the frequency change from 1-MHz to 250-kHz when $V_{IN} > V_{LFM}$ (4.35 V typical) and for the no-frequency mode when $V_{IN} > V_{NFM}$ (5.05 V typical), which explains the discontinuities of the graph.

Table 1. Maximum Total DC/DC Current (I_{AUX} + I_{USB1}+ I_{USB2}) at Common Input Voltages

INPUT VOLTAGE (V)	MAXIMUM TOTAL OUTPUT CURRENT (I_{AUX} + I_{USB1} + I_{USB2})	
	CONSERVATIVE (mA)	TYPICAL (mA)
1.8	599	757
2.5	916	1113
2.7	1008	1216
3	1148	1374
3.3	1308	1536
3.6	1445	1704
4.35	1241	1730
4.5	1364	1858
4.75	1593	2093
5.05	2300	2300
5.25	2300	2300

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8.3.17 USB Switches

8.3.17.1 Overview

The TPS2505 integrates a current-limited, power-distribution switches using N-channel MOSFETs for applications where short circuits or heavy capacitive loads are encountered. The current-limit threshold is user-programmable from 130 mA to 1.4 A (typical) by selecting an external resistor. The device incorporates an internal charge pump and gate-drive circuitry necessary to fully enhance the N-channel MOSFETs. The internal gate drivers controls turnon of the MOSFETs to limit large current and voltage surges by providing built-in soft-start functionality. The power switches have an independent undervoltage lockout (UVLO) circuit that disables them until the voltage on AUX reaches 4.3 V (typical). Built-in hysteresis prevents unwanted on/off cycling due to input voltage drop on AUX from current surges on the output of the power switch. The power switches have an independent logic-level enable control (ENUSB1/2) that gates power-switch turnon and bias for the charge pump, driver, and miscellaneous control circuitry. A logic-high input on ENUSB1/2 enables the drivers, control circuits, and power switches. The enable input are compatible with CMOS, TTL, LVTTL, 2.5-V, and 1.8-V logic levels.

8.3.17.2 Overcurrent Conditions

The TPS2505 power switches respond to overcurrent conditions by limiting its output current to the IOS level. The device maintains a constant output current and reduces the output voltage accordingly during an overcurrent condition. Two possible overload conditions can occur. The first condition is when a short circuit or partial short circuit is present on the output of the switch prior to device turn-on and the device is powered up or enabled. The output voltage is held near zero potential with respect to ground, and the TPS2505 ramps the output current to IOS. The TPS2505 power switches limit the current to IOS until the overload condition is removed or the device begins to cycle thermally. The second condition is when a short circuit, partial short circuit, or transient overload occurs while the device is already enabled and powered on. The current-sense amplifier is overdriven during this time and momentarily disables the power switch. The current-sense amplifier recovers and limits the output current to I_{OS}. The power switches thermally cycle if an overload condition is present long enough to activate thermal limiting in any of the foregoing cases. The power switches turns off when the junction temperature exceeds 130°C while in current-limit. The power switches remains off until the junction temperature cools 10°C and then restarts. The TPS2505 power switches cycles on/off until the overload is removed. The boost converter is independent of the power-switch thermal sense and continues to operate as long as the temperature of the boost converter remains less than 150°C and does not trigger the boost-converter thermal sense.

8.3.17.3 FAULT1/2 Response

The FAULT1/2 open-drain outputs are asserted low during an overcurrent condition that causes V_{USB} to fall below V_{TRIP} (4.6 V typical) or causes the junction temperature to exceed the shutdown threshold (130°C). The TPS2505 asserts the FAULT1/2 signals until the fault condition is removed and the power switches resume normal operation. The FAULT1/2 signals are independent of the boost converter or each other. The FAULT1/2 signals use an internal delay deglitch circuit (8-ms typical) to delay asserting the FAULT1/2 signals during an overcurrent condition. The power switches must remain in an overcurrent condition for the entire deglitch period or the deglitch timer is restarted. This ensures that FAULT1/2 are not accidentally asserted due to normal operation such as starting into a heavy capacitive load. The deglitch circuitry delays entering and leaving fault conditions. Overtemperature conditions are not deglitched and assert the FAULT1/2 signals immediately.

8.3.17.4 Undervoltage Lockout

The undervoltage lockout (UVLO) circuit disables the TPS2505 power switch until the input voltage on AUX reaches the power switch UVLO turn-on threshold of 4.3 V (typical). Built-in hysteresis prevents unwanted on/off cycling due to input-voltage drop from large current surges.

8.3.17.5 Programming the Current-Limit Threshold Resistor R_{ILIM}

The overcurrent thresholds are user programmable via external resistors. The TPS2505 uses an internal regulation loop to provide a regulated voltage on the ILIM1/2 pins. The current-limit thresholds are proportional to the current sourced out of ILIM1/2. The recommended 1% resistor range for RILIM1/2 is 16.1 kΩ ≤ R_{ILIM} ≤ 200 kΩ to ensure stability of the internal regulation loop. Many applications require that the minimum current limit is above a certain current level or that the maximum current limit is below a certain current level, so it is important to consider the tolerance of the overcurrent threshold when selecting a value for RILIM1/2. The following equations and Figure 10 can be used to calculate the resulting overcurrent threshold for a given external resistor value (RILIM1/2). Figure 10 includes current-limit tolerance due to variations caused by

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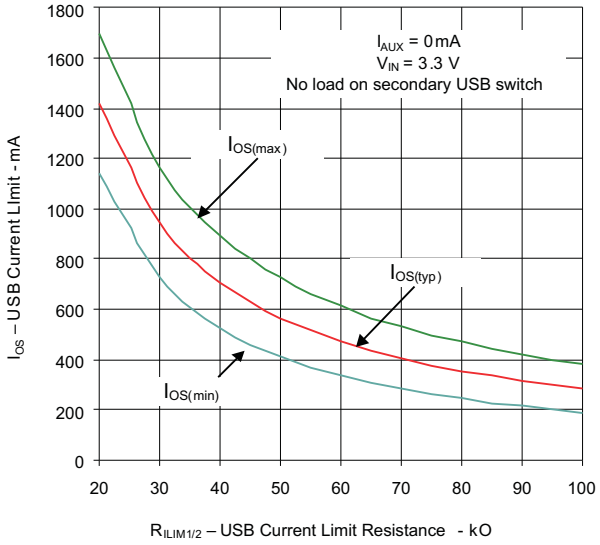
temperature and process. However, the equations do not account for tolerance due to external resistor variation, so it is important to account for this tolerance when selecting RILIM1/2. The traces routing the RILIM1/2 resistors to the TPS2505 should be as short as possible to reduce parasitic effects on the current-limit accuracy. RILIM1/2 can be selected to provide a current-limit threshold that occurs 1) above a minimum load current or 2) below a maximum load current.

To design above a minimum current-limit threshold, find the intersection of R_{ILIM} and the maximum desired load current on the $I_{OS(min)}$ curve and choose a value of R_{ILIM} below this value. Programming the current limit above a minimum threshold is important to ensure start up into full load or heavy capacitive loads. The resulting maximum current-limit threshold is the intersection of the selected value of RILIM1/2 and the $I_{OS(max)}$ curve. To design below a maximum current-limit threshold, find the intersection of R_{ILIM} and the maximum desired load current on the $I_{OS(max)}$ curve and choose a value of RILIM1/2 above this value. Programming the current limit below a maximum threshold is important to avoid current-limiting upstream power supplies, causing the input voltage bus to droop. The resulting minimum current-limit threshold is the intersection of the selected value of RILIM1/2 and the IOS(min) curve. Current-limit threshold equations (I_{OS}):

$$I_{OS(\max)}(mA) = \frac{27,570V}{R_{ILIM1/2}{}^{0.93} k\Omega} \quad (1)$$

$$I_{OS(typ)}(mA) = \frac{28,235V}{R_{ILIM1/2}{}^{0.998} k\Omega} \quad (2)$$

$$I_{OS(\min)}(mA) = \frac{32,114V}{R_{ILIM1/2}{}^{1.114} k\Omega} \quad (3)$$



V_{IN} = 3.3 V I_{AUX} = 0 A Secondary USB Switch Disabled

Figure 10. USB Current-Limit Threshold vs R_{ILIM} Overtemperature and Process

8.3.18 3.3-V LDO

The TPS2505 integrates a 3.3-V LDO with a maximum load capacity of 200 mA. The LDO can be powered by the AUX boost output to allow operation when there is only a low voltage supply such as an alkaline battery. The LDO will only turn on once V_{AUX} reaches the UVLO threshold. The LDO can also be connected to be powered to an external supply if no additional load to AUX is desired or to reduce power dissipation (in case the supply is lower than the 5.1-V boost output). However, the boost must be enabled to allow the LDO to operate, even if connected to a separate supply.

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8.3.19 Reset Comparator

The Reset Comparator integrated in the TPS2505 provides a power-good signal that indicates when the LDO output has reached a 3.1-V threshold. The comparator has a 175-ms deglitch delay for the low-to-high transition to prevent any glitches when the LDO is powering up. Hysteresis has been added to the comparator to increase noise immunity and avoid unwanted glitches in the output during LDO transients.

8.3.20 Thermal Shutdown

The TPS2505 self-protects using two independent thermal sensing circuits that monitor the operating temperatures of the boost converter and power switch independently and disable operation if the temperature exceeds recommended operating conditions. The boost converter and power switches each have an ambient thermal sensor that disables operation if the measured junction temperature in that part of the circuit exceeds 150°C. The boost converter continues to operate even if the power switch is disabled due to an overtemperature condition.

8.3.21 Component Recommendations

The main functions of the TPS2505 are integrated and meet recommended operating conditions with a wide range of external components. The following sections give guidelines and trade-offs for external component selection. The recommended values given are conservative and intended over the full range of recommended operating conditions.

8.3.21.1 Boost Inductor

Connect the boost inductor from IN to SW. The inductance controls the ripple current through the inductor. A 2.2-µH inductor is recommended, and the minimum and maximum inductor values are constrained by the integrated features of the TPS2505. The minimum inductance is limited by the peak inductor-current value. The ripple current in the inductor is inversely proportional to the inductance value, so the output voltage may fall out of regulation if the peak inductor current exceeds the cycle-by-cycle current-limit comparator (3 A minimum). Using a nominal 2.2-µH inductor allows full recommended current operation even if the inductance is 20% low (1.76 µH) due to component variation. The maximum inductance value is limited by the internal compensation of the boost-converter control loop. A maximum 4.7-µH (typical) inductor value is recommended to maintain adequate phase margin over the full range of recommended operating conditions.

8.3.21.2 IN Capacitance

Connect the input capacitance from IN to the reference ground plane (see for connecting PGND and GND to the ground plane). Input capacitance reduces the AC voltage ripple on the input rail by providing a low-impedance path for the switching current of the boost converter. The TPS2505 does not have a minimum or maximum input capacitance requirement for operation, but a 10-µF, X7R or X5R ceramic capacitor is recommended for most applications for reasonable input-voltage ripple performance. There are several scenarios where it is recommended to use additional input capacitance:

- The output impedance of the upstream power supply is high, or the power supply is located far from the TPS2505.
- The TPS2505 is tested in a lab environment with long, inductive cables connected to the input, and transient voltage spikes could exceed the absolute maximum voltage rating of the device.
- The device is operating in PFM control scheme near V_{IN} = 1.8 V, where insufficient input capacitance may cause the input ripple voltage to fall below the minimum 1.75-V (typical) UVLO circuit, causing device turnoff. Additionally, it is good engineering practice to use an additional 0.1-µF ceramic decoupling capacitor close to the IC to prevent unwanted high-frequency noise from coupling into the device.

8.3.21.3 AUX Capacitance

Connect the boost-converter output capacitance from AUX to the reference ground plane. The AUX capacitance controls the ripple voltage on the AUX rail and provides a low-impedance path for the switching and transient-load currents of the boost converter. It also sets the location of the output pole in the control loop of the boost converter. There are limitations to the minimum and maximum capacitance on AUX. The recommended minimum capacitance on AUX is a 22-µF, X5R or X7R ceramic capacitor. A 10-V rated ceramic capacitor is recommended to minimize the capacitance derating loss due to dc bias applied to the capacitor. The low ESR of the ceramic capacitor minimizes ripple voltage and power dissipation from the large, pulsating currents of the boost converter and provides adequate phase margin across all recommended operating conditions. In some applications, it is

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desirable to add additional AUX capacitance. Additional AUX capacitance reduces transient undershoot and overshoot voltages due to load steps and reduces AUX ripple in the PFM control scheme. Adding AUX capacitance changes the control loop, resulting in reduced phase margin, so it is recommended that no more than 220 µF of additional capacitance be added in parallel to the 22-µF ceramic capacitor. The combined output capacitance on AUX and USB should not exceed 500 µF.

8.3.21.4 USB Capacitance

Connect the USB1/2 capacitances from USB1/2 to the reference ground plane. The USB1/2 capacitances are on the outputs of the power switches and provide energy for transient load steps. The TPS2505 does not require any USB capacitance for operation. Additional capacitance can be added on USB1/2 outputs, but it is recommended to not exceed 220 µF to maintain adequate phase margin for the boost converter control loop. The combined output capacitance on AUX and USB should not exceed 500 µF. USB applications require a minimum of 120 µF on downstream facing ports.

8.3.21.5 ILIM1/2 and FAULT1/2 Resistors

Connect the ILIM1/2 resistors from ILIM1/2 to the reference ground plane. The ILIM1/2 resistors programs the current-limit threshold of the USB power switches (see *Programming the Current-Limit Threshold Resistor R_{ILIM}*). The ILIM1/2 pins are the output of internal linear regulators that provide a fixed 400-mV output. The recommended nominal resistor value using 1% resistors on ILIM1/2 is 16.1 kΩ ≤ R_{ILIM} ≤ 200 kΩ. This range should be adjusted accordingly if 1% resistors are not used. Do not overdrive ILIM1/2 with an external voltage or connect directly to GND. Connect the ILIM1/2 resistors as close to the TPS2505 as possible to minimize the effects of parasitics on device operation. Do not add external capacitance on the ILIM1/2 pins. The ILIM1/2 pins should not be left floating. Connect the FAULT1/2 resistors from the FAULT1/2 pins to an external voltage source such as V_{AUX} or V_{IN}. The FAULT1/2 pins are open-drain outputs capable of sinking a maximum current of 10 mA continuously. The FAULT1/2 resistors should be sized large enough to limit current to under 10 mA continuously. Do not tie FAULT1/2 directly to an external voltage source. The maximum recommended voltage on FAULT1/2 is 6.5 V. The FAULT1/2 pin can be left floating if not used.

8.4 Device Functional Modes

The device functional modes refer to the boost converter modes which are controlled by the Vin to the converter. They include Low frequency mode, No frequency mode, Pulse Frequency Modulation (PFM) mode, and normal mode.

In low frequency mode when the input voltage reaches 4.35 V (typical) the DC-DC switching frequency is reduced from 1 MHz to 250 kHz. This prevents pulse skipping at voltages larger than 4.35 V. This mode is disabled when Vin falls below 4.35 V.

No frequency mode occurs when Vin is greater than 5.05 V (typical). The oscillator is disabled at this time . This reduces power dissipation which in turn increases efficiency. This mode is disabled when Vin falls below 5.05 V.

PFM mode is used during light loads to increase efficiency. During this period there is no switching which reduces power dissipation, and load current is provided by output capacitor only. Two comparators control when the converter enters and leaves PFM mode. PFM mode is disabled during low-frequency mode.

In normal mode the converter runs at 1 MHz and regulates output voltage of VAUX, using pulse width modulation (PWM). For details on boost converter functional modes, see *Boost Converter*.

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9 Application and Implementation

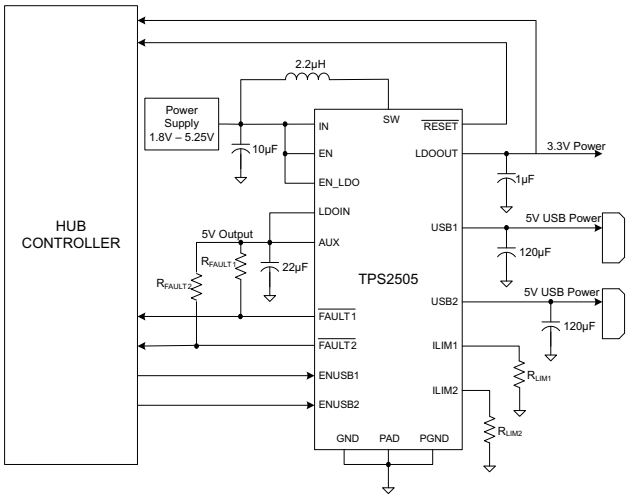
NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPS2505 is a USB switch device enabling a 5-V supply from a single Li-Ion battery, regulated supply, or 2- to 3-cell NiCd , NiMH, or alkaline. This device is targeted toward keyboard, printer, camera, picture frame applications, and other handheld or remote applications.

9.2 Typical Application



9.2.1 Design Requirements

For this design example, use the parameters listed in Table 2 as the input parameters.

Table 2. Design Parameters

PARAMETER	EXAMPLE VALUE
Input voltage range (V_{IN})	2.7 V to 4.2 V
AUX voltage (V_{AUX})	5.1 V (internally fixed)
Input ripple voltage (ΔV_{IN})	15 mV
AUX ripple voltage (ΔV_{AUX})	50 mV
AUX current (I_{AUX})	0.3 A
LDO current (ILDO) (powered from AUX)	0.1 A
USB1 current (I_{USB1})	0.5 A
USB2 current (I_{USB2})	0.1 A
Total current ($I_{TOTAL} = I_{AUX} + I_{LDO} + I_{USB1} + I_{USB2}$)	1 A
Efficiency target, nominal	90%
Switching frequency (f_{SW})	1 MHz

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9.2.2 Detailed Design Procedure

9.2.2.1 Step-by-Step Design Procedure

The following design procedure provides an example for selecting component values for the TPS2505.

The following design parameters are needed as inputs to the design process.

- Input voltage range
- Output voltage on AUX
- Input ripple voltage
- Output ripple voltage on AUX
- Output current rating of AUX rail
- Output current rating of USB rail
- Nominal efficiency target
- Operating frequency

A power inductor, input and output filter capacitors, and current-limit threshold resistor are the only external components required to complete the TPS2505 boost-converter design. The input ripple voltage, AUX ripple voltage, and total output current affect the selection of these components.

9.2.2.2 Switching Frequency

The switching frequency of the TPS2505 is internally fixed at 1 MHz for the specified V_{IN} range.

9.2.2.3 AUX Voltage

The AUX voltage of the TPS2505 is internally fixed at 5.1 V.

9.2.2.4 Determine Maximum Total Current (I_{AUX} + I_{LDO} + I_{USB1} + I_{USB2})

Using Figure 1, the maximum total current at V_{IN} = 2.7 V is 1 A using the conservative line. The design requirements are met for this application.

9.2.2.5 Power Inductor

The inductor ripple current, Δi, should be at least 20% of the average inductor current to avoid erratic operation of the peak-current-mode PWM controller. Assume an inductor ripple current, Δi, which is 30% of the average inductor current and a power-converter efficiency, η, of 90%. Using the minimum input voltage, the average inductor current at V_{IN} = 2.7 V is:

$$I_{IN} = \frac{V_{AUX} \times I_{TOTAL}}{V_{IN} \times \eta} = \frac{5.1V \times 1A}{2.7V \times 0.9} = 2.1A \tag{4}$$

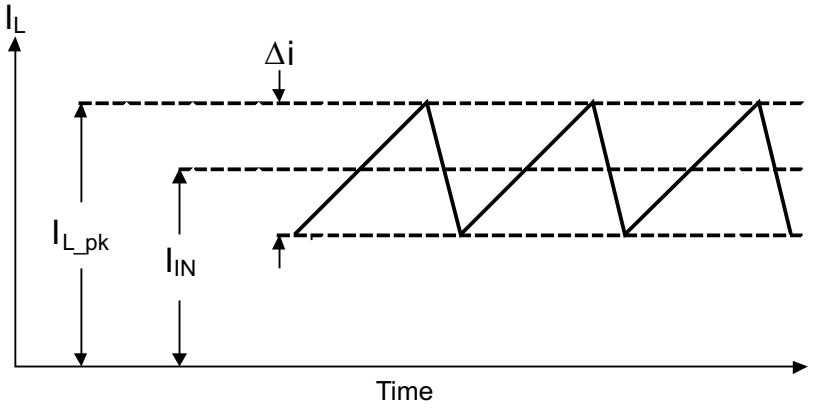


Figure 11. Waveform of Current in Boost Inductor

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The corresponding inductor ripple current is:

$$\Delta i = 0.3 \times I_{IN} = 0.3 \times 2.1A = 630mA \tag{5}$$

Verify that the peak inductor current is less than the 3-A peak switch current:

$$I_{L_pk} = I_{IN} + \frac{\Delta i}{2} = 2.42A < 3A \tag{6}$$

The following equation estimates the duty cycle of the low-side SWN MOSFET:

$$D = \frac{t_{on}}{t_{on} + t_{off}} = \frac{V_{AUX} - V_{IN} + I_{IN} \times (R_{SWP} + R_L)}{V_{AUX} + V_{IN} \times (R_{SWP} + R_{SWN})} = \frac{5.1V - 2.7V + 2.1A \times (0.1\Omega + 0.07\Omega)}{5.1V + 2.1A \times (0.1\Omega + 0.1\Omega)} = 0.54$$

where

- R_{SWN} is the low-side control MOSFET ON-resistance
- R_{SWP} is the high-side synchronous MOSFET ON-resistance
- R_L is an estimate of the inductor DC resistance

(7)

The following equation calculates the recommended inductance for this design.

$$L = \frac{V_{IN} \times D}{f \times \Delta i} = \frac{2.7V \times 0.54}{1 \times 10^6 Hz \times 0.63A} = 2.31\mu H \tag{8}$$

The RMS inductor current is:

$$I_{L_RMS} = \sqrt{{I_{IN}}^2 + \left(\frac{\Delta i}{2\sqrt{3}}\right)^2} = \sqrt{(2.1A)^2 + \left(\frac{0.63A}{2\sqrt{3}}\right)^2} = 2.11A \tag{9}$$

Select a Coilcraft LPS4018-222ML inductor. This 2.2-µH inductor has a saturation current rating of 2.7 A and an RMS current rating of 2.3 A. See *Component Recommendations* for specific additional information.

9.2.2.6 Output AUX Capacitor Selection

The AUX output capacitor, C_{AUX}, discharges during the PWM MOSFET on-time, resulting in an output ripple voltage of ΔV_{AUX}. ΔV_{AUX} is largest at maximum load current.

$$C_{AUX} = \frac{D \times I_{TOTAL}}{f \times \Delta V_{AUX}} \tag{10}$$

$$C_{AUX_\min} = \frac{0.54 \times 1A}{1 \times 10^6 Hz \times 50mV} = 10.8\mu F \tag{11}$$

Ceramic capacitors exhibit a DC bias effect, whereby the capacitance falls with increasing bias voltage. The effect is worse for capacitors in smaller case sizes and lower voltage ratings. X5R and X7R capacitors exhibit less DC bias effect than Y5V and Z5U capacitors.

Select a TDK C3225X5R1A226M 22-µF, 10-V X5R ceramic capacitor to allow for a 50% drop in capacitance due to the DC bias effect. See *Component Recommendations* for specific additional information.

9.2.2.7 Output USB1/2 Capacitor Selection

The USB1/2 output capacitors provide energy during a load step on the USB outputs. The TPS2505 does not require a USB output capacitor, but many USB applications require that downstream-facing ports be bypassed with a minimum of 120-µF, low-ESR capacitance.

Select a Panasonic EEVFK1A151P 150-µF, 10-V capacitor.

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9.2.2.8 Input Capacitor Selection

The ripple current through the input filter capacitor is equal to the ripple current through the inductor. If the ESL and ESR of the input filter capacitor are ignored, then the required input filter capacitance is:

$$C_{IN} = \frac{\Delta i}{8 \times f \times \Delta V_{IN}} = \frac{630mA}{8 \times 1 \times 10^{6} Hz \times 15mV} = 5.25\mu F \quad (12)$$

Select a TDK C2012X5R1A106K 10-µF, 10-V, X5R, size 805 ceramic capacitor. The capacitance drops 20% at 3.3-V bias, resulting in an effective capacitance of 8 µF.

An additional 0.1-µF ceramic capacitor should be placed locally from IN to GND to prevent noise from coupling into the device if the input capacitor cannot be located physically near to the device.

In applications where long, inductive cables connect the input power supply to the device, additional bulk input capacitance may be necessary to minimize voltage overshoot. See *Component Recommendations* for specific additional information.

9.2.2.8.1 Current-Limit Threshold Resistor R_{ILIM}

The current-limit threshold I_{OS} of the power switches are externally adjustable by selecting the RILIM1/2 resistors. To eliminate the possibility of false tripping, RILIM1/2 should be selected so that the minimum tolerance of the current-limit threshold is greater than the maximum specified USB load, I_{USB}.

It is also important to account for I_{OS} shifts due to variation in VIN and I_{AUX}. This shift due to the additional loading in AUX can add up to ±75 mA of variation to the I_{OS} as calculated according to *Programming the Current-Limit Threshold Resistor R_{ILIM}*. Select RILIM1 so that the minimum current-limit threshold equals 600 mA to ensure a minimum I_{USB1} current-limit threshold of 525 mA. In the same way, select RILIM2 so that the minimum current-limit threshold equals 200 mA to ensure a minimum I_{USB2} current-limit threshold of 125 mA.

$$R_{ILIM1/2} = \left(\frac{32.114}{I_{OS\min}} \right)^{\frac{1}{1.114}} \quad (13)$$

$$R_{ILIM1} = \left(\frac{32.114}{600mA} \right)^{\frac{1}{1.114}} = 35.62k\Omega \quad (14)$$

$$R_{ILIM2} = \left(\frac{32.114}{200mA} \right)^{\frac{1}{1.114}} = 95.49k\Omega \quad (15)$$

Choose the next smaller 1% resistor, which are 34.8 kΩ for RLIM1 and 95.3 kΩ for RLIM2.

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9.2.3 Application Curves

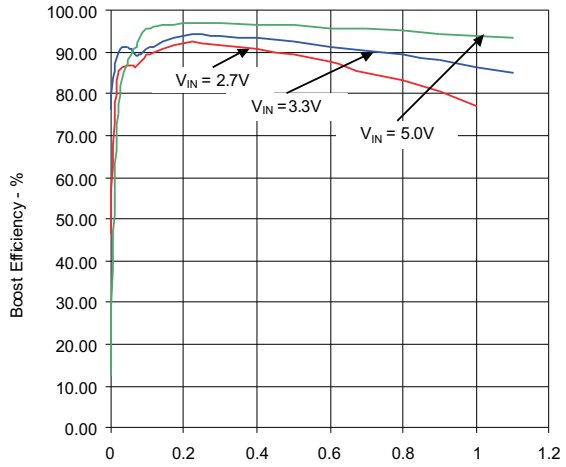


Figure 12. Boost Efficiency vs Output Current

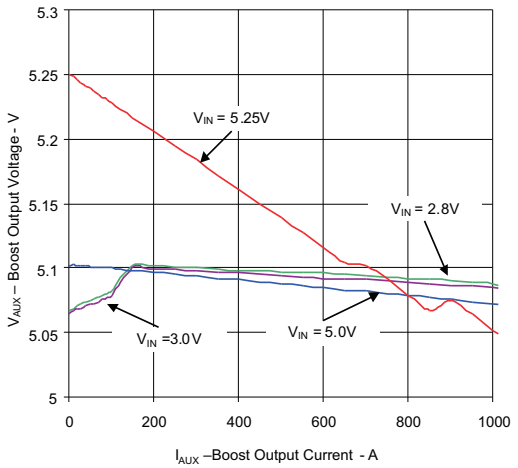


Figure 13. Boost Output Voltage vs Load Current

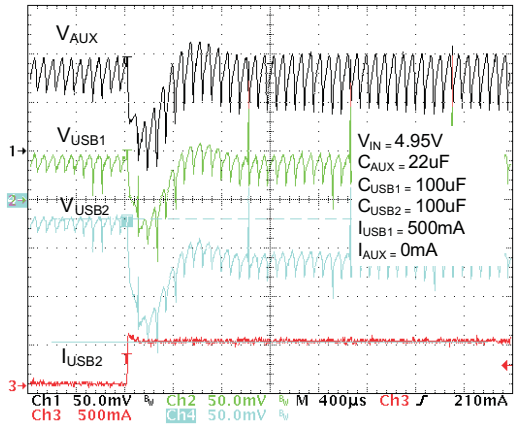


Figure 14. Boost Load Transient Response, 500 mA - 1 A, USB1/2 Enabled

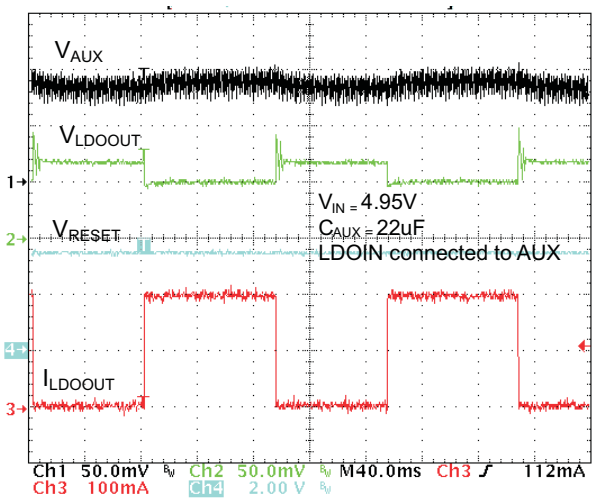


Figure 15. LDO Load Transient Response 0 mA - 200 mA

10 Power Supply Recommendations

The device is designed to operate with an input voltage supply range from 1.8 V to 5.25 V. This input supply can be from a single-cell Li-ion, two-cell or three-cell NiCd, NiMH or alkaline, or an externally regulated supply. If the input supply is located more than a few inches from the TPS2505, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. An electrolytic capacitor with a value of 10 µF is a typical choice.

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11 Layout

11.1 Layout Guidelines

Layout is an important design step due to the high switching frequency of the boost converter. Careful attention must be applied to the PCB layout to ensure proper function of the device and to obtain the specified performance. Potential issues resulting from poor layout techniques include wider line and load regulation tolerances, EMI noise issues, stability problems, and USB current-limit shifts. It is critical to provide a low-impedance ground path that minimizes parasitic inductance. Wide and short traces should be used in the high-current paths, and components should be placed as close to the device as possible. Grounding is an important part of the layout. The device has a PGND and a GND pin. The GND pin is the quiet analog ground of the device and should have its own separate ground pour; connect the quiet signals to GND including the RILIM1/2 resistors and any input decoupling capacitors to the GND pour. It is important that the RILIM1/2 resistors be tied to a quiet ground to avoid unwanted shifts in the current-limit threshold. The PGND pin is the high-current power-stage ground; the ground pours of the output (AUX) and bulk input capacitors should be tied to PGND. PGND and GND should to be tied together in one location at the IC thermal pad, creating a star-point ground.

The output filter of the boost converter is also critical for layout. The inductor and AUX capacitors should be placed to minimize the area of current loop through AUX–PGND–SW.The layout for the TPS2505EVM evaluation board is shown in Figure 16 and should be followed as closely as possible for best performance.

11.2 Layout Example

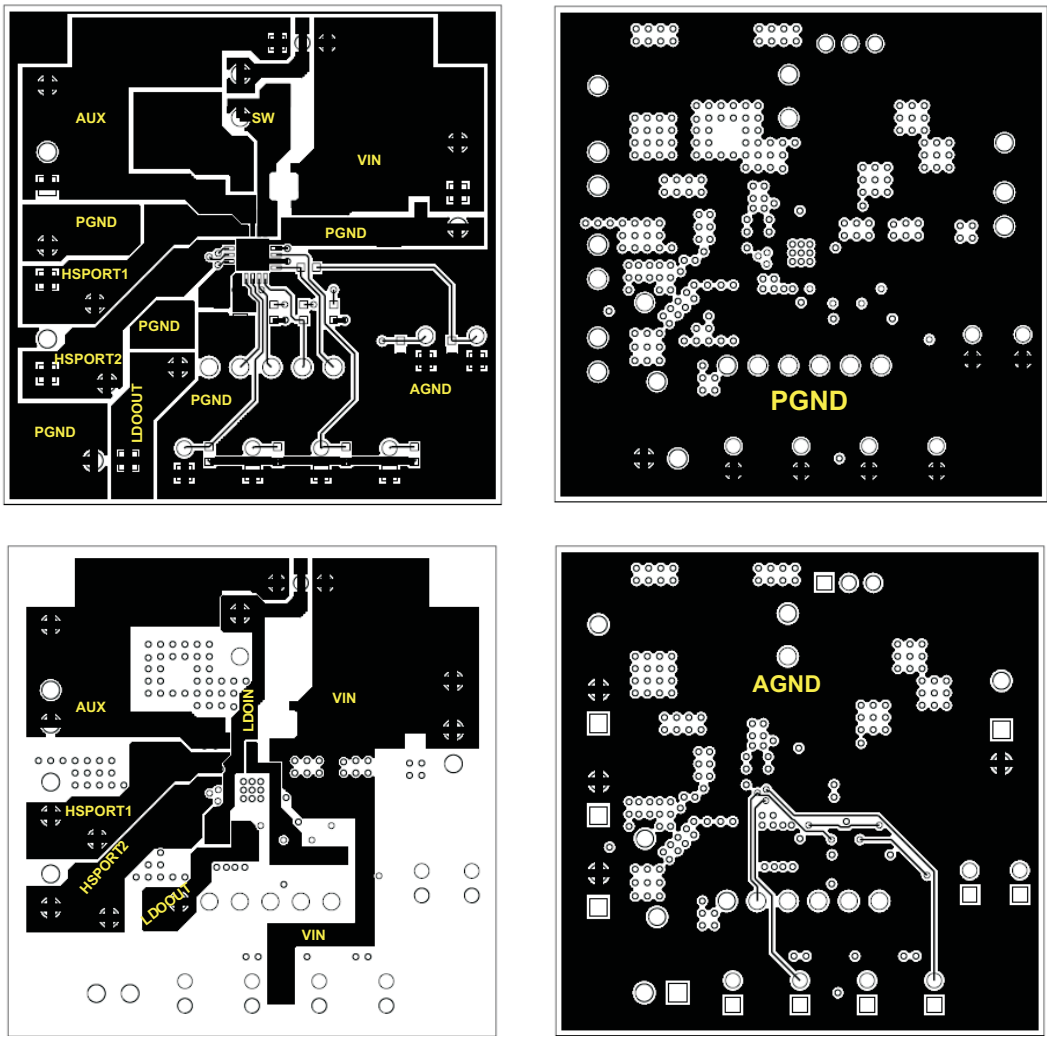


Figure 16. Layout Recommendation for TPS2505 Application – 4 Layer Board

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12 Device and Documentation Support

12.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.2 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS2505B1RGWR	ACTIVE	VQFN	RGW	20	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 2505B1	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

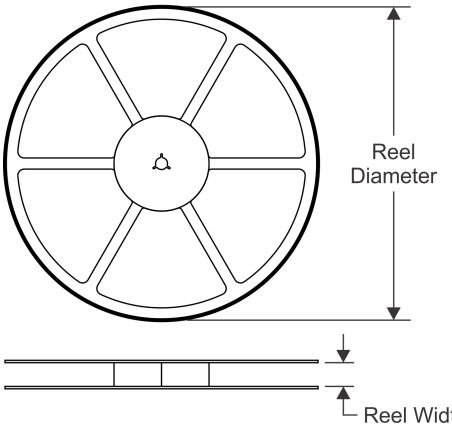
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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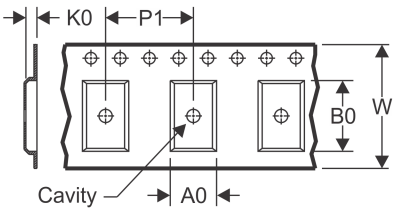
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

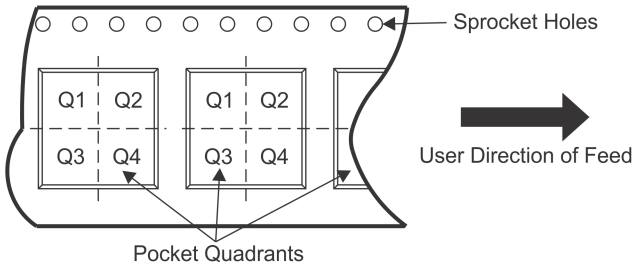


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

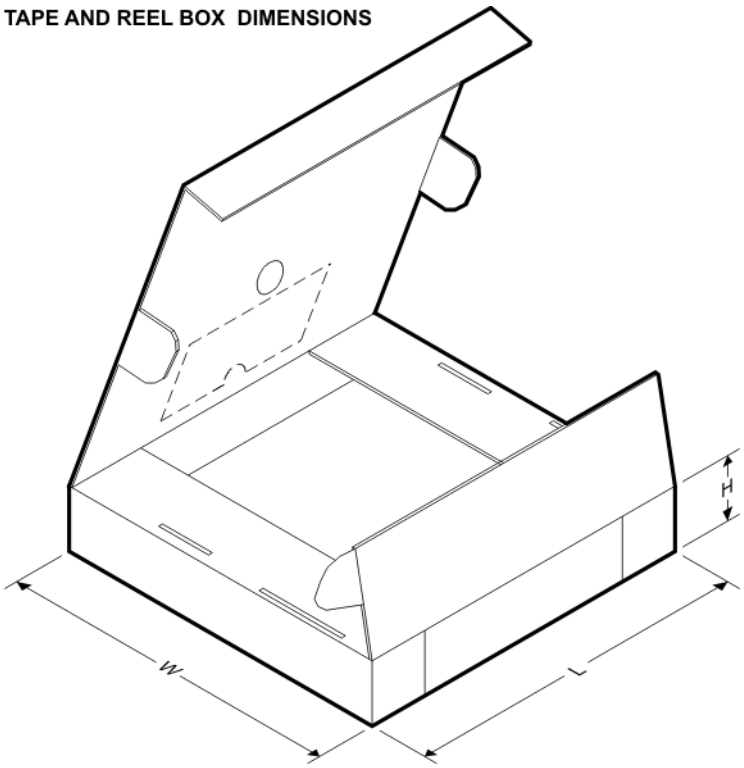
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS2505B1RGWR	VQFN	RGW	20	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2

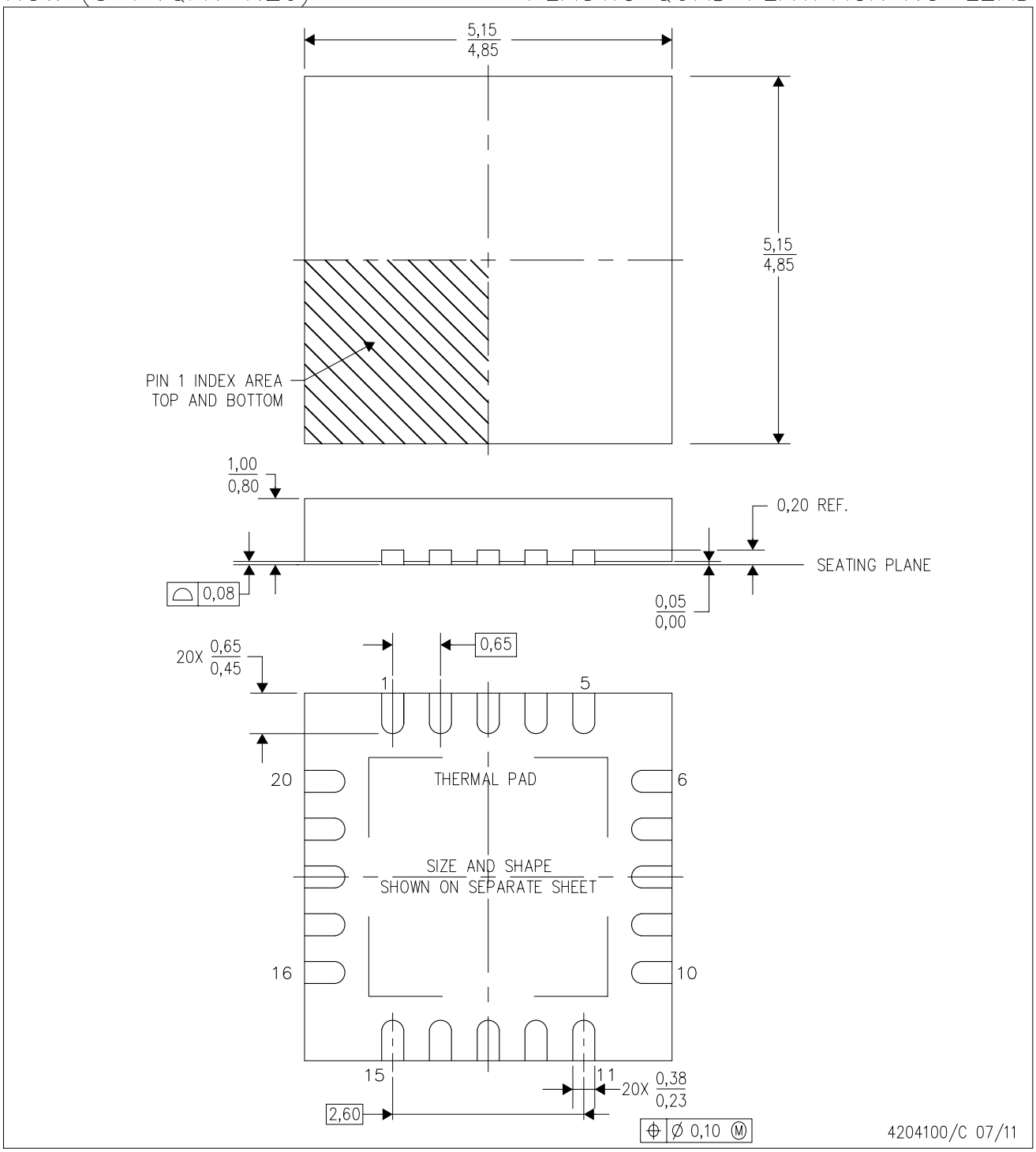
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS2505B1RGWR	VQFN	RGW	20	3000	367.0	367.0	35.0

RGW (S–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. Quad Flat pack, No–leads (QFN) package configuration
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

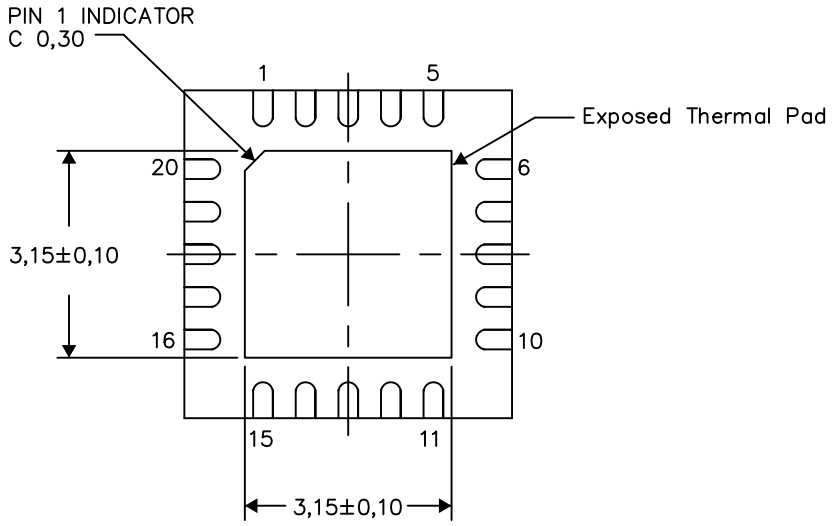
RGW (S–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



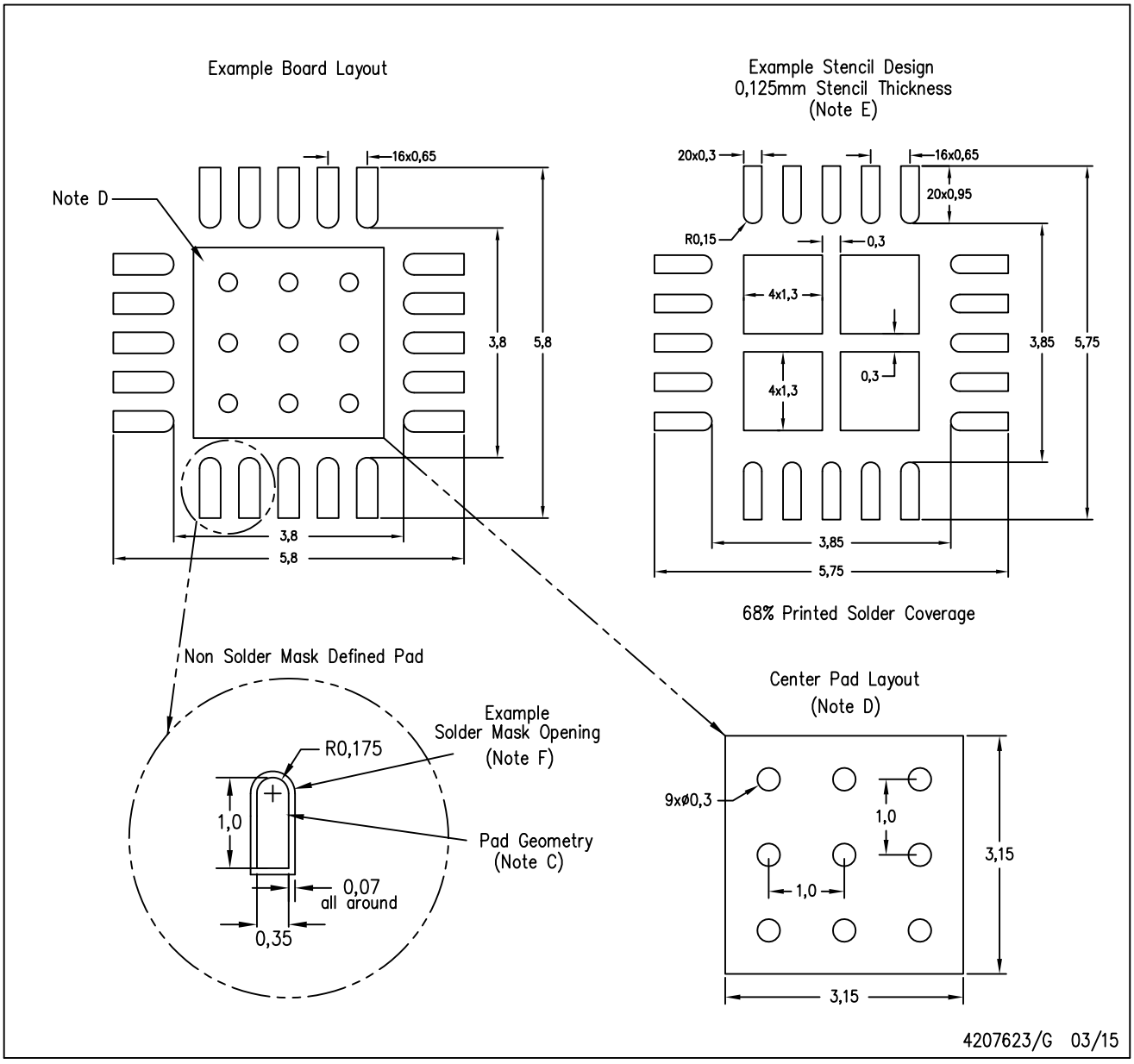
Bottom View

Exposed Thermal Pad Dimensions

4206352–2/M 06/15

NOTE: All linear dimensions are in millimeters

RGW (S–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.

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