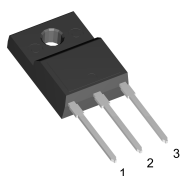
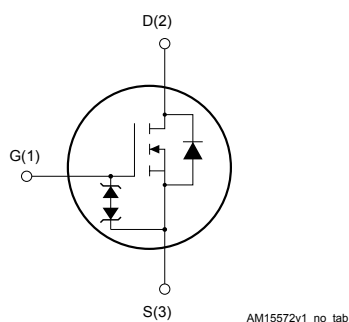


## N-channel 600 V, 520 mΩ typ., 6.4 A MDmesh M6 Power MOSFET in a TO-220FP wide creepage package



TO-220 FP wide creepage



### Features

| Order code  | $V_{DS} @ T_{Jmax}$ | $R_{DS(on)}$ max. | $I_D$ |
|-------------|---------------------|-------------------|-------|
| STFH10N60M6 | 650 V               | 600 mΩ            | 6.4 A |

- Reduced switching losses
- Lower  $R_{DS(on)}$  per area vs previous generation
- Low gate input resistance
- 100% avalanche tested
- Zener-protected

### Applications

- Switching applications
- LLC converters, resonant converters
- Boost PFC converters

### Description

The new MDmesh M6 technology incorporates the most recent advancements to the well-known and consolidated MDmesh family of SJ MOSFETs. STMicroelectronics builds on the previous generation of MDmesh devices through its new M6 technology, which combines excellent  $R_{DS(on)}$  per area improvement with one of the most effective switching behaviors available, as well as a user-friendly experience for maximum end-application efficiency.

The TO-220FP wide creepage package provides increased surface insulation for Power MOSFETs to prevent failure due to arcing, which can occur in polluted environments.



#### Product status link

[STFH10N60M6](#)

#### Product summary

|            |                        |
|------------|------------------------|
| Order code | STFH10N60M6            |
| Marking    | 10N60M6                |
| Package    | TO-220FP wide creepage |
| Packing    | Tube                   |

# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

| Symbol            | Parameter                                                                                                                               | Value       | Unit               |
|-------------------|-----------------------------------------------------------------------------------------------------------------------------------------|-------------|--------------------|
| $V_{GS}$          | Gate-source voltage                                                                                                                     | $\pm 25$    | V                  |
| $I_D^{(1)}$       | Drain current (continuous) at $T_C = 25\text{ }^{\circ}\text{C}$                                                                        | 6.4         | A                  |
| $I_D^{(1)}$       | Drain current (continuous) at $T_C = 100\text{ }^{\circ}\text{C}$                                                                       | 4           | A                  |
| $I_{DM}^{(2)(1)}$ | Drain current (pulsed)                                                                                                                  | 16.6        | A                  |
| $P_{TOT}$         | Total power dissipation at $T_C = 25\text{ }^{\circ}\text{C}$                                                                           | 20          | W                  |
| $dv/dt^{(3)}$     | Peak diode recovery voltage slope                                                                                                       | 15          | V/ns               |
| $dv/dt^{(4)}$     | MOSFET $dv/dt$ ruggedness                                                                                                               | 100         | V/ns               |
| $V_{ISO}$         | Insulation withstand voltage (RMS) from all three leads to external heat sink ( $t = 1\text{ s}$ ; $T_C = 25\text{ }^{\circ}\text{C}$ ) | 2.5         | kV                 |
| $T_{stg}$         | Storage temperature range                                                                                                               | - 55 to 150 | $^{\circ}\text{C}$ |
| $T_j$             | Operating junction temperature range                                                                                                    |             |                    |

- Limited by package.
- Pulse width limited by package.
- $I_{SD} \leq 6.4\text{ A}$ ,  $di/dt \leq 400\text{ A}/\mu\text{s}$ ;  $V_{DS(peak)} < V_{(BR)DSS}$ ,  $V_{DD} = 400\text{ V}$
- $V_{DS} \leq 480\text{ V}$

**Table 2. Thermal data**

| Symbol         | Parameter                           | Value | Unit                        |
|----------------|-------------------------------------|-------|-----------------------------|
| $R_{thj-case}$ | Thermal resistance junction-case    | 6.25  | $^{\circ}\text{C}/\text{W}$ |
| $R_{thj-amb}$  | Thermal resistance junction-ambient | 62.5  | $^{\circ}\text{C}/\text{W}$ |

**Table 3. Avalanche characteristics**

| Symbol   | Parameter                                                                                                              | Value | Unit |
|----------|------------------------------------------------------------------------------------------------------------------------|-------|------|
| $I_{AR}$ | Avalanche current, repetitive or not repetitive (pulse width limited by $T_{jmax}$ )                                   | 1.4   | A    |
| $E_{AS}$ | Single pulse avalanche energy (starting $T_j = 25\text{ }^{\circ}\text{C}$ , $I_D = I_{AR}$ ; $V_{DD} = 50\text{ V}$ ) | 120   | mJ   |

## 2 Electrical characteristics

( $T_C = 25\text{ }^{\circ}\text{C}$  unless otherwise specified)

**Table 4. On /off states**

| Symbol        | Parameter                         | Test conditions                                                                                      | Min. | Typ. | Max.    | Unit          |
|---------------|-----------------------------------|------------------------------------------------------------------------------------------------------|------|------|---------|---------------|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage    | $V_{GS} = 0\text{ V}$ , $I_D = 1\text{ mA}$                                                          | 600  |      |         | V             |
| $I_{DSS}$     | Zero gate voltage drain current   | $V_{GS} = 0\text{ V}$ , $V_{DS} = 600\text{ V}$                                                      |      |      | 1       | $\mu\text{A}$ |
|               |                                   | $V_{GS} = 0\text{ V}$ , $V_{DS} = 600\text{ V}$ , $T_C = 125\text{ }^{\circ}\text{C}$ <sup>(1)</sup> |      |      | 100     | $\mu\text{A}$ |
| $I_{GSS}$     | Gate-body leakage current         | $V_{DS} = 0\text{ V}$ , $V_{GS} = \pm 25\text{ V}$                                                   |      |      | $\pm 5$ | $\mu\text{A}$ |
| $V_{GS(th)}$  | Gate threshold voltage            | $V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$                                                   | 3.25 | 4    | 4.75    | V             |
| $R_{DS(on)}$  | Static drain-source on-resistance | $V_{GS} = 10\text{ V}$ , $I_D = 3.2\text{ A}$                                                        |      | 520  | 600     | m $\Omega$    |

1. Defined by design, not subject to production test.

**Table 5. Dynamic**

| Symbol                     | Parameter                     | Test conditions                                                                                                                               | Min. | Typ. | Max. | Unit     |
|----------------------------|-------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------|------|------|------|----------|
| $C_{iss}$                  | Input capacitance             | $V_{DS} = 100\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0\text{ V}$                                                                          | -    | 338  | -    | pF       |
| $C_{oss}$                  | Output capacitance            |                                                                                                                                               | -    | 26.2 | -    | pF       |
| $C_{rss}$                  | Reverse transfer capacitance  |                                                                                                                                               | -    | 3.88 | -    | pF       |
| $C_{oss\text{ eq.}}^{(1)}$ | Equivalent output capacitance | $V_{DS} = 0\text{ to }480\text{ V}$ , $V_{GS} = 0\text{ V}$                                                                                   | -    | 59   | -    | pF       |
| $R_G$                      | Intrinsic gate resistance     | $f = 1\text{ MHz}$ , $I_D = 0\text{ A}$                                                                                                       | -    | 7    | -    | $\Omega$ |
| $Q_g$                      | Total gate charge             | $V_{DD} = 480\text{ V}$ , $I_D = 6.4\text{ A}$ , $V_{GS} = 0\text{ to }10\text{ V}$<br>(see Figure 14. Test circuit for gate charge behavior) | -    | 8.8  | -    | nC       |
| $Q_{gs}$                   | Gate-source charge            |                                                                                                                                               | -    | 2.7  | -    | nC       |
| $Q_{gd}$                   | Gate-drain charge             |                                                                                                                                               | -    | 4.8  | -    | nC       |

1.  $C_{oss\text{ eq.}}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$

**Table 6. Switching times**

| Symbol       | Parameter           | Test conditions                                                                                                                                                                                                | Min. | Typ. | Max. | Unit |
|--------------|---------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|------|------|------|
| $t_{d(on)}$  | Turn-on delay time  | $V_{DD} = 300\text{ V}$ , $I_D = 3.2\text{ A}$ , $R_G = 4.7\text{ }\Omega$ ,<br>$V_{GS} = 10\text{ V}$ (see Figure 13. Test circuit for resistive load switching times and Figure 18. Switching time waveform) | -    | 11   | -    | ns   |
| $t_r$        | Rise time           |                                                                                                                                                                                                                | -    | 8    | -    | ns   |
| $t_{d(off)}$ | Turn-off delay time |                                                                                                                                                                                                                | -    | 23   | -    | ns   |
| $t_f$        | Fall time           |                                                                                                                                                                                                                | -    | 10   | -    | ns   |

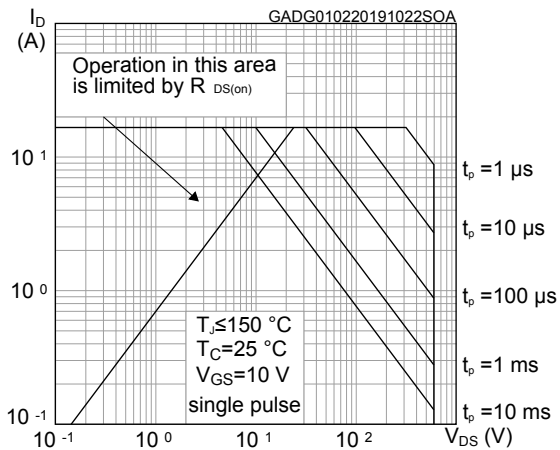
**Table 7. Source-drain diode**

| Symbol              | Parameter                     | Test conditions                                                                                             | Min. | Typ.  | Max. | Unit          |
|---------------------|-------------------------------|-------------------------------------------------------------------------------------------------------------|------|-------|------|---------------|
| $I_{SD}^{(1)}$      | Source-drain current          |                                                                                                             | -    |       | 6.4  | A             |
| $I_{SDM}^{(2) (1)}$ | Source-drain current (pulsed) |                                                                                                             | -    |       | 16.6 | A             |
| $V_{SD}^{(3)}$      | Forward on voltage            | $I_{SD} = 6.4 \text{ A}$ , $V_{GS} = 0 \text{ V}$                                                           | -    |       | 1.6  | V             |
| $t_{rr}$            | Reverse recovery time         | $I_{SD} = 6.4 \text{ A}$ , $di/dt = 100 \text{ A}/\mu\text{s}$                                              | -    | 155   |      | ns            |
| $Q_{rr}$            | Reverse recovery charge       | $V_{DD} = 60 \text{ V}$ (see Figure 15. Test circuit for inductive load switching and diode recovery times) | -    | 0.813 |      | $\mu\text{C}$ |
| $I_{RRM}$           | Reverse recovery current      |                                                                                                             | -    | 10.5  |      | A             |
| $t_{rr}$            | Reverse recovery time         | $I_{SD} = 6.4 \text{ A}$ , $di/dt = 100 \text{ A}/\mu\text{s}$                                              | -    | 250   |      | ns            |
| $Q_{rr}$            | Reverse recovery charge       | $V_{DD} = 60 \text{ V}$ , $T_J = 150 \text{ }^\circ\text{C}$                                                | -    | 1.35  |      | $\mu\text{C}$ |
| $I_{RRM}$           | Reverse recovery current      | (see Figure 15. Test circuit for inductive load switching and diode recovery times)                         | -    | 10.8  |      | A             |

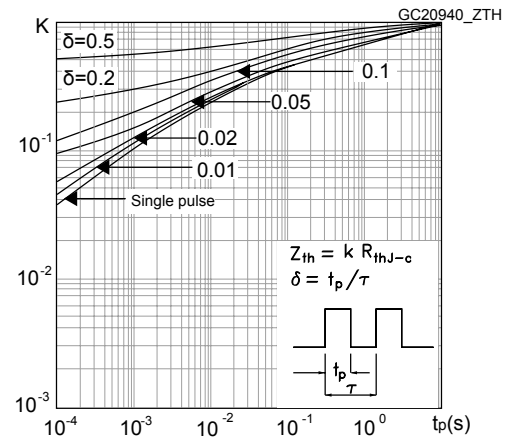
1. Limited by package.
2. Pulse width limited by safe operating area.
3. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%.

## 2.1 Electrical characteristics (curves)

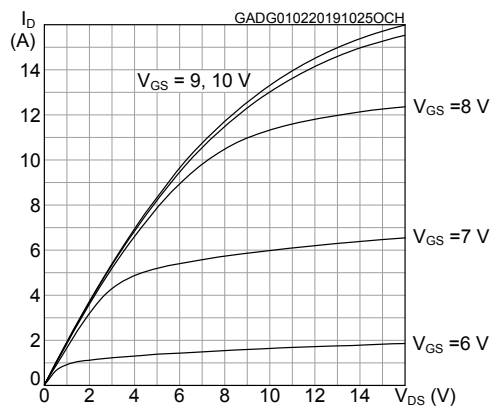
**Figure 1. Safe operating area**



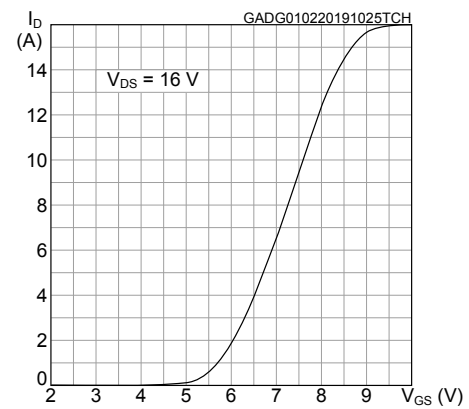
**Figure 2. Thermal impedance**



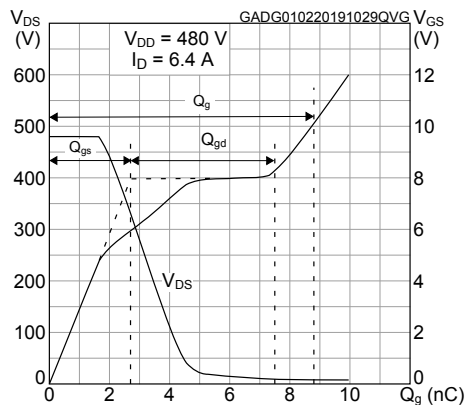
**Figure 3. Output characteristics**



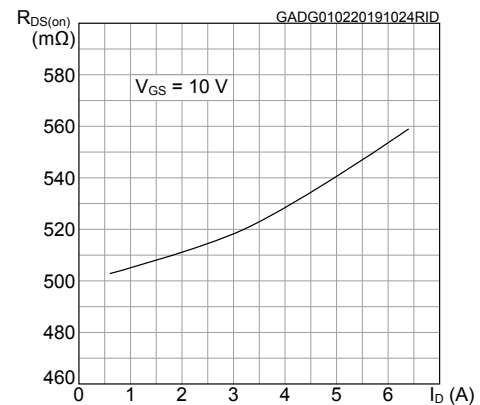
**Figure 4. Transfer characteristics**



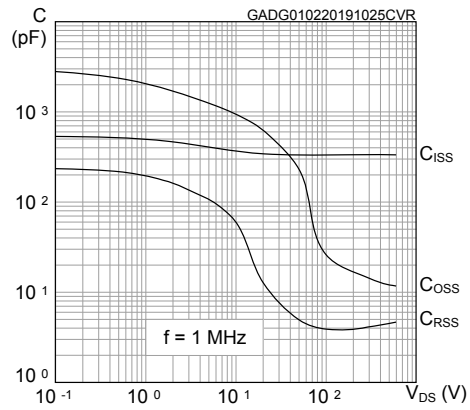
**Figure 5. Gate charge vs gate-source voltage**



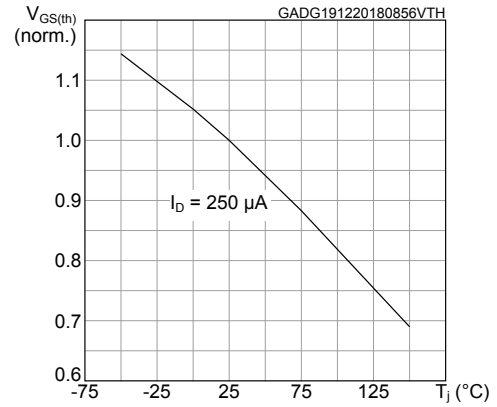
**Figure 6. Static drain-source on-resistance**



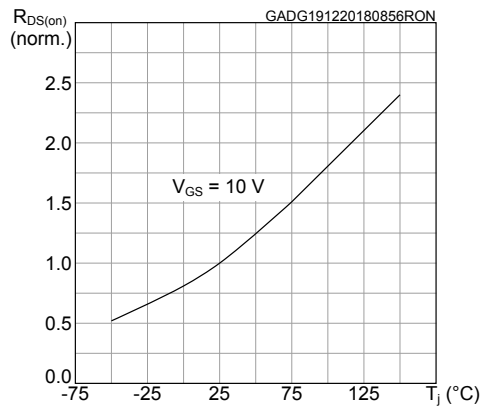
**Figure 7. Capacitance variations**



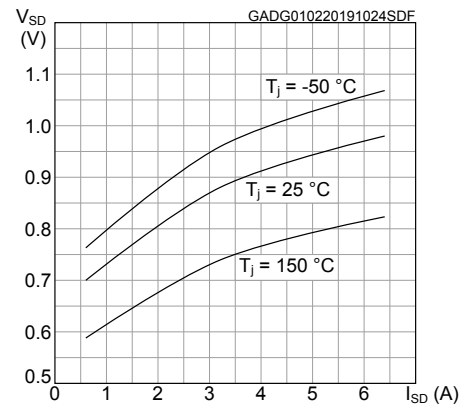
**Figure 8. Normalized gate threshold voltage vs. temperature**



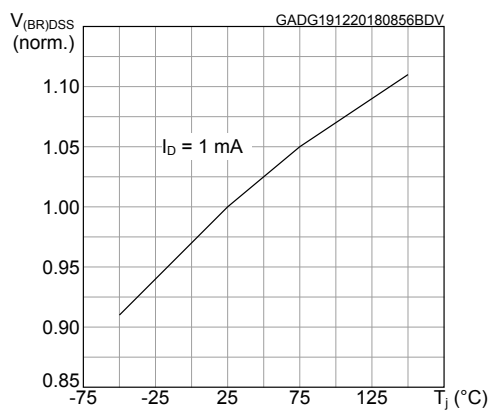
**Figure 9. Normalized on-resistance vs temperature**



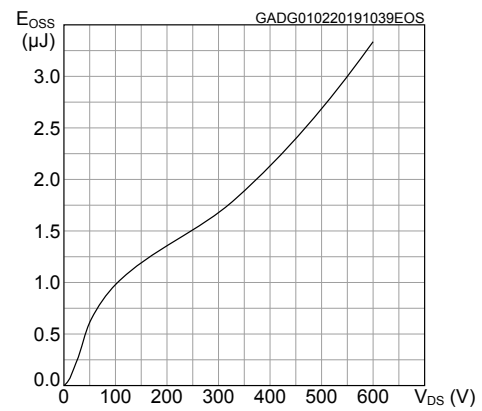
**Figure 10. Source-drain diode forward characteristics**



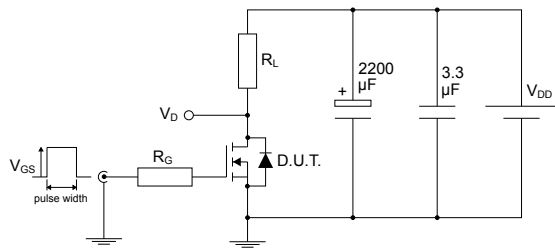
**Figure 11. Normalized  $V_{(BR)DSS}$  vs temperature**



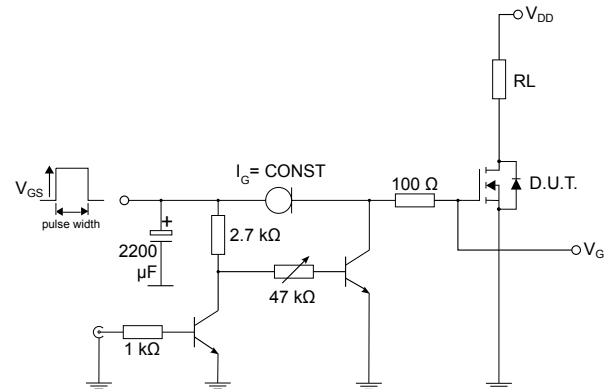
**Figure 12. Output capacitance stored energy**



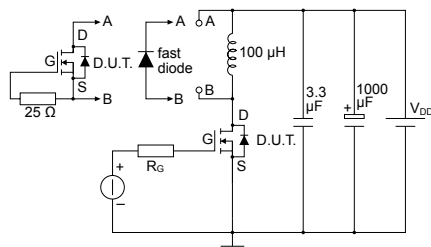
### 3 Test circuits

**Figure 13. Test circuit for resistive load switching times**


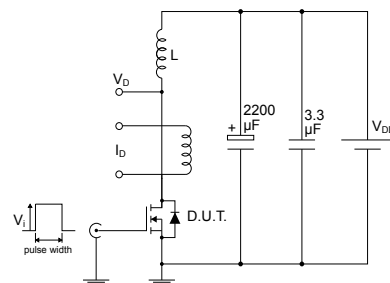
AM0146Bv1

**Figure 14. Test circuit for gate charge behavior**


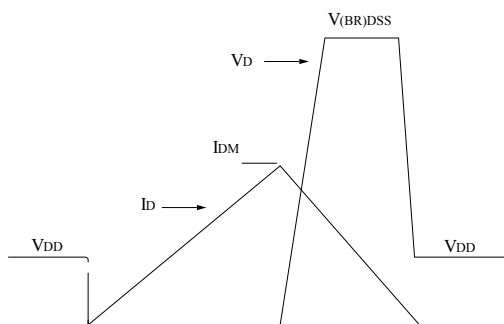
AM0146Bv10

**Figure 15. Test circuit for inductive load switching and diode recovery times**


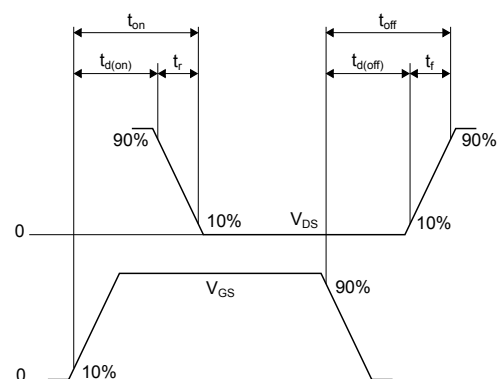
AM01470v1

**Figure 16. Unclamped inductive load test circuit**


AM01471v1

**Figure 17. Unclamped inductive waveform**


AM01472v1

**Figure 18. Switching time waveform**


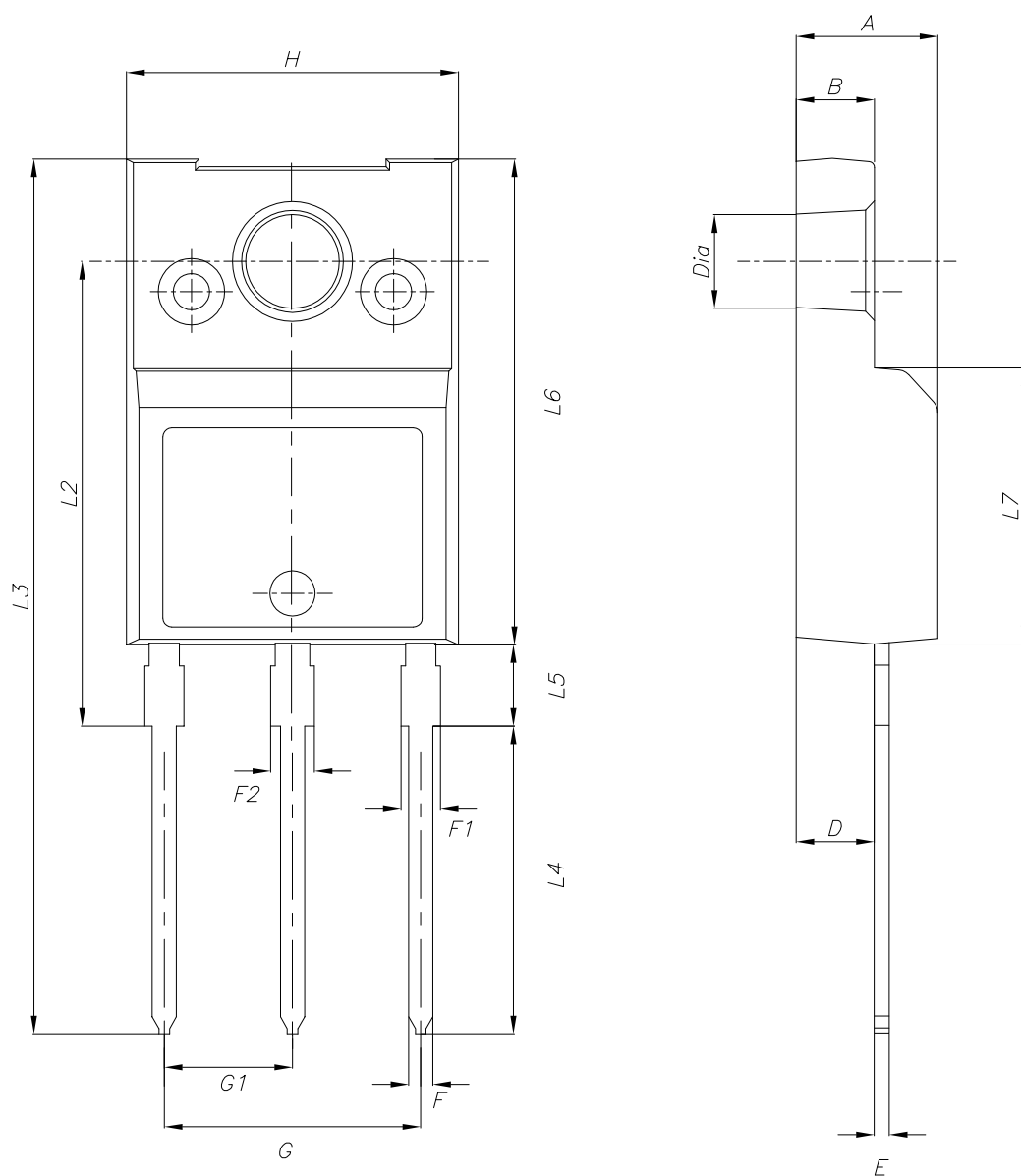
AM01473v1

## 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

### 4.1 TO-220FP wide creepage package information

**Figure 19. TO-220FP wide creepage package outline**



DM00260252\_1

**Table 8. TO-220FP wide creepage package mechanical data**

| Dim. | mm    |       |       |
|------|-------|-------|-------|
|      | Min.  | Typ.  | Max.  |
| A    | 4.60  | 4.70  | 4.80  |
| B    | 2.50  | 2.60  | 2.70  |
| D    | 2.49  | 2.59  | 2.69  |
| E    | 0.46  |       | 0.59  |
| F    | 0.76  |       | 0.89  |
| F1   | 0.96  |       | 1.25  |
| F2   | 1.11  |       | 1.40  |
| G    | 8.40  | 8.50  | 8.60  |
| G1   | 4.15  | 4.25  | 4.35  |
| H    | 10.90 | 11.00 | 11.10 |
| L2   | 15.25 | 15.40 | 15.55 |
| L3   | 28.70 | 29.00 | 29.30 |
| L4   | 10.00 | 10.20 | 10.40 |
| L5   | 2.55  | 2.70  | 2.85  |
| L6   | 16.00 | 16.10 | 16.20 |
| L7   | 9.05  | 9.15  | 9.25  |
| Dia  | 3.00  | 3.10  | 3.20  |

## Revision history

**Table 9. Document revision history**

| Date        | Revision | Changes                                                                                                                                          |
|-------------|----------|--------------------------------------------------------------------------------------------------------------------------------------------------|
| 11-Feb-2019 | 1        | First release.                                                                                                                                   |
| 30-May-2019 | 2        | Updated <a href="#">Table 7. Source-drain diode</a> and <a href="#">Section 2.1 Electrical characteristics (curves)</a> .<br>Minor text changes. |

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