# SN54ALS257A, SN54ALS258A, SN74ALS257A, SN74ALS258A, SN74AS257, SN74AS258
# QUADRUPLE 2-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS WITH 3-STATE OUTPUTS

SDAS124C − APRIL 1982 − REVISED AUGUST 1996

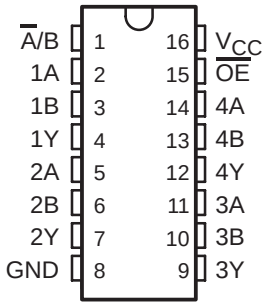
- **3-State Outputs Interface Directly With System Bus**
- **Provide Bus Interface From Multiple Sources in High-Performance Systems**
- **Package Options Include Plastic Small-Outline (D) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

## description

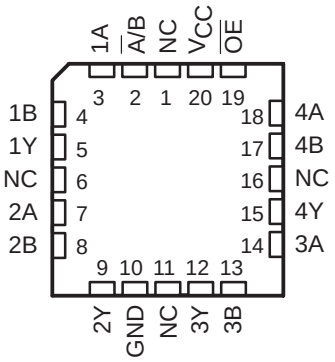
These data selectors/multiplexers are designed to multiplex signals from 4-bit data sources to 4-output data lines in bus-organized systems. The 3-state outputs do not load the data lines when the output-enable ($\overline{OE}$) input is at a high logic level.

The SN54ALS257A and SN54ALS258A are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS257A, SN74ALS258A, SN74AS257, and SN74AS258 are characterized for operation from 0°C to 70°C.

**SN54ALS257A, SN54ALS258A . . . J PACKAGE**
**SN74ALS257A, SN74ALS258A, SN74AS257,**
**SN74AS258 . . . D OR N PACKAGE**
**(TOP VIEW)**




**SN54ALS257A, SN54ALS258A . . . FK PACKAGE**
**(TOP VIEW)**




NC − No internal connection

**FUNCTION TABLE**

| INPUTS | | | | OUTPUT Y | |
|---|---|---|---|---|---|
| $\overline{OE}$ | $\overline{A}$/B | DATA A | DATA B | SN54ALS257A SN74ALS257A SN74AS257 | SN54ALS258A SN74ALS258A SN74AS258 |
| H | X | X | X | Z | Z |
| L | L | L | X | L | H |
| L | L | H | X | H | L |
| L | H | X | L | L | H |
| L | H | X | H | H | L |

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

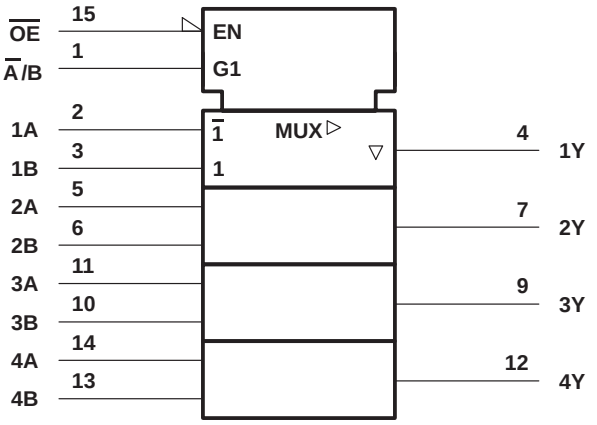
PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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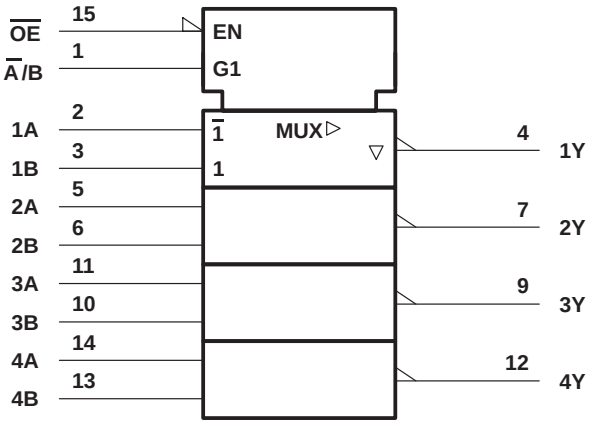
TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77251−1443

## logic symbols†

**SN54ALS257A, SN74ALS257A, SN74AS257**



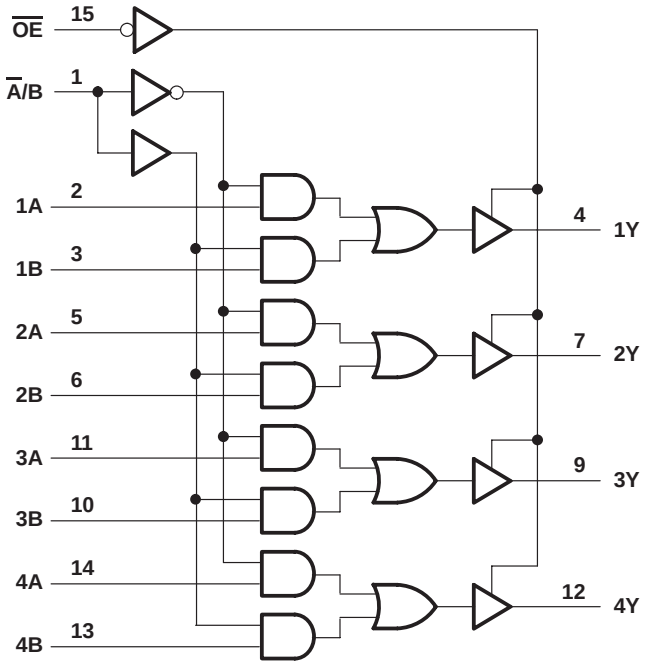

**SN54ALS258A, SN74ALS258A, SN74AS258**



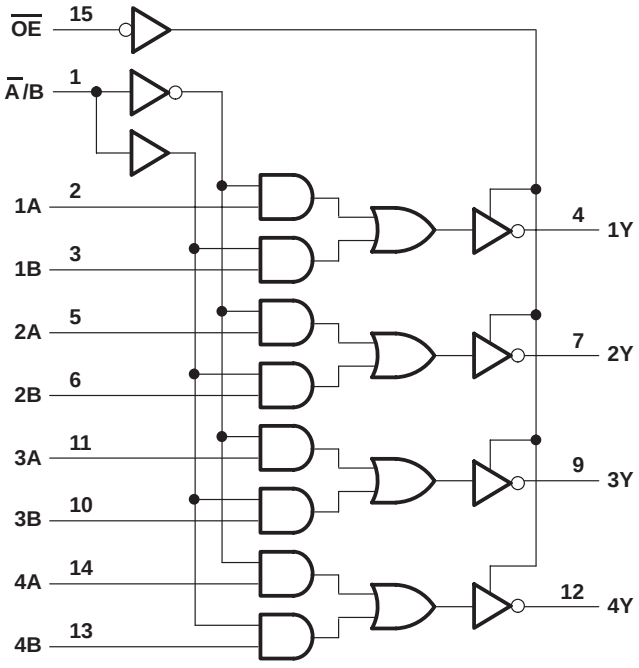

† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, and N packages.

## logic diagrams (positive logic)

**SN54ALS257A, SN74ALS257A, SN74AS257**




**SN54ALS258A, SN74ALS258A, SN74AS258**




Pin numbers shown are for the D, J, and N packages.

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, $V_{CC}$ . . . . . 7 V
Input voltage, $V_I$ . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Maximum power dissipation at $T_A$ = 55°C (in still air) (see Note 1): D package . . . . . 1.3 W
N package . . . . . 1.1 W
Operating free-air temperature range, $T_A$: SN54ALS257A, SN54ALS258A . . . . . −55°C to 125°C
SN74ALS257A, SN74ALS258A . . . . . 0°C to 70°C
Storage temperature range, $T_{stg}$ . . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

### recommended operating conditions

| | | SN54ALS257A SN54ALS258A | | | SN74ALS257A SN74ALS258A | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.7 | | | 0.8 | V |
| $I_{OH}$ | High-level output current | | | −1 | | | −2.6 | mA |
| $I_{OL}$ | Low-level output current | | | 12 | | | 24 | mA |
| $T_A$ | Operating free-air temperature | −55 | | 125 | 0 | | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | SN54ALS257A SN54ALS258A | | | SN74ALS257A SN74ALS258A | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP† | MAX | MIN | TYP† | MAX | |
| $V_{IK}$ | | $V_{CC}$ = 4.5 V, | $I_I$ = −18 mA | | | −1.5 | | | −1.5 | V |
| $V_{OH}$ | | $V_{CC}$ = 4.5 V to 5.5 V, | $I_{OH}$ = −0.4 mA | $V_{CC}$−2 | | | $V_{CC}$−2 | | | V |
| | | $V_{CC}$ = 4.5 V | $I_{OH}$ = −1 mA | 2.4 | 3.3 | | | | | |
| | | | $I_{OH}$ = −2.6 mA | | | | 2.4 | 3.2 | | |
| $V_{OH}$ | | $V_{CC}$ = 4.5 V | $I_{OL}$ = 12 mA | | 0.25 | 0.4 | | 0.25 | 0.4 | V |
| | | | $I_{OL}$ = 24 mA | | | | | 0.35 | 0.5 | |
| $I_{OZH}$ | | $V_{CC}$ = 5.5 V, | $V_O$ = 2.7 V | | | 20 | | | 20 | µA |
| $I_{OZL}$ | | $V_{CC}$ = 5.5 V, | $V_O$ = 0.4 V | | | −20 | | | −20 | µA |
| $I_I$ | | $V_{CC}$ = 5.5 V, | $V_I$ = 7 V | | | 0.1 | | | 0.1 | mA |
| $I_{IH}$ | | $V_{CC}$ = 5.5 V, | $V_I$ = 2.7 V | | | 20 | | | 20 | µA |
| $I_{IL}$ | | $V_{CC}$ = 5.5 V, | $V_I$ = 0.4 V | | | −0.1 | | | −0.1 | mA |
| $I_O$‡ | | $V_{CC}$ = 5.5 V, | $V_O$ = 2.25 V | −20 | | −112 | −30 | | −112 | mA |
| $I_{CC}$ | SN54ALS257A, SN74ALS257A | $V_{CC}$ = 5.5 V | Outputs high | | 3 | 8 | | 3 | 6 | mA |
| | | | Outputs low | | 8 | 12 | | 8 | 12 | |
| | | | Outputs disabled | | 9 | 14 | | 9 | 14 | |
| | SN54ALS258A, SN74ALS258A | $V_{CC}$ = 5.5 V | Outputs high | | 2.5 | 5 | | 2.5 | 4 | |
| | | | Outputs low | | 7 | 11 | | 7 | 11 | |
| | | | Outputs disabled | | 8 | 13 | | 8 | 13 | |

† All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, $I_{OS}$.

## switching characteristics (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 4.5 V to 5.5 V, $C_L$ = 50 pF, R1 = 500 Ω, R2 = 500 Ω, $T_A$ = MIN to MAX§ | | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | SN54ALS257A | | SN74ALS257A | | |
| | | | MIN | MAX | MIN | MAX | |
| $t_{PLH}$ | A or B | Any Y | 2 | 12 | 2 | 10 | ns |
| $t_{PHL}$ | | | 2 | 14 | 2 | 12 | |
| $t_{PLH}$ | $\overline{A}$/B | Any Y | 4 | 21 | 6 | 18 | ns |
| $t_{PHL}$ | | | 6 | 25 | 6 | 22 | |
| $t_{PZH}$ | $\overline{OE}$ | Any Y | 3 | 20 | 4 | 16 | ns |
| $t_{PZL}$ | | | 4 | 22 | 5 | 18 | |
| $t_{PHZ}$ | $\overline{OE}$ | Any Y | 2 | 12 | 2 | 10 | ns |
| $t_{PLZ}$ | | | 2 | 35 | 4 | 15 | |

§ For conditions shown MIN or MAX, use the appropriate value specified under recommended operating conditions.

## switching characteristics (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 4.5 V to 5.5 V, $C_L$ = 50 pF, R1 = 500 Ω, R2 = 500 Ω, $T_A$ = MIN to MAX† | | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | SN54ALS258A | | SN74ALS258A | | |
| | | | MIN | MAX | MIN | MAX | |
| $t_{PLH}$ | A or B | Any Y | 1 | 12 | 2 | 8 | ns |
| $t_{PHL}$ | | | 2 | 9 | 2 | 7 | |
| $t_{PLH}$ | $\overline{A}$/B | Any Y | 4 | 28 | 5 | 25 | ns |
| $t_{PHL}$ | | | 5 | 25 | 6 | 20 | |
| $t_{PZH}$ | $\overline{OE}$ | Any Y | 3 | 20 | 4 | 18 | ns |
| $t_{PZL}$ | | | 5 | 21 | 5 | 18 | |
| $t_{PHZ}$ | $\overline{OE}$ | Any Y | 2 | 12 | 2 | 10 | ns |
| $t_{PLZ}$ | | | 3 | 37 | 4 | 18 | |

† For conditions shown MIN or MAX, use the appropriate value specified under recommended operating conditions.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, $V_{CC}$ . . . . . 7 V
Input voltage, $V_I$ . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Maximum power dissipation at $T_A$ = 55°C (in still air) (see Note 1): D package . . . . . 1.3 W
N package . . . . . 1.1 W
Operating free-air temperature range, $T_A$: SN74AS257, SN74AS258 . . . . . 0°C to 70°C
Storage temperature range, $T_{stg}$ . . . . . −65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

## recommended operating conditions

| | | SN74AS257 SN74AS258 | | | UNIT |
|---|---|---|---|---|---|
| | | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $I_{OH}$ | High-level output current | | | −15 | mA |
| $I_{OL}$ | Low-level output current | | | 48 | mA |
| $T_A$ | Operating free-air temperature | 0 | | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | SN74AS257 SN74AS258 | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP† | MAX | |
| $V_{IK}$ | | $V_{CC}$ = 4.5 V, | $I_I$ = −18 mA | | | −1.2 | V |
| $V_{OH}$ | | $V_{CC}$ = 4.5 V to 5.5 V, | $I_{OH}$ = −2 mA | $V_{CC}$ −2 | | | V |
| | | $V_{CC}$ = 4.5 V, | $I_{OH}$ = −15 mA | 2.4 | 3.2 | | |
| $V_{OL}$ | | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 48 mA | | 0.35 | 0.5 | V |
| $I_{OZH}$ | | $V_{CC}$ = 5.5 V, | $V_O$ = 2.7 V | | | 50 | µA |
| $I_{OZL}$ | | $V_{CC}$ = 5.5 V, | $V_O$ = 0.4 V | | | −50 | µA |
| $I_I$ | A, B, or $\overline{OE}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 7 V | | | 0.1 | mA |
| | $\overline{A}$/B | | | | | 0.2 | |
| $I_{IH}$ | A, B, or $\overline{OE}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 2.7 V | | | 20 | µA |
| | $\overline{A}$/B | | | | | 40 | |
| $I_{IL}$ | A, B, or $\overline{OE}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 0.4 V | | | −0.5 | mA |
| | $\overline{A}$/B | | | | | −1 | |
| $I_O$‡ | | $V_{CC}$ = 5.5 V, | $V_O$ = 2.25 V | −30 | | −112 | mA |
| $I_{CC}$ | SN74AS257 | $V_{CC}$ = 5.5 V | Outputs high | | 12.1 | 19.7 | mA |
| | | | Outputs low | | 19 | 30.6 | |
| | | | Outputs disabled | | 19.7 | 31.9 | |
| | SN74AS258 | $V_{CC}$ = 5.5 V | Outputs high | | 8.4 | 13.5 | |
| | | | Outputs low | | 15.2 | 24.6 | |
| | | | Outputs disabled | | 15.5 | 25.2 | |

† All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, $I_{OS}$.

## switching characteristics (see Figure 1)

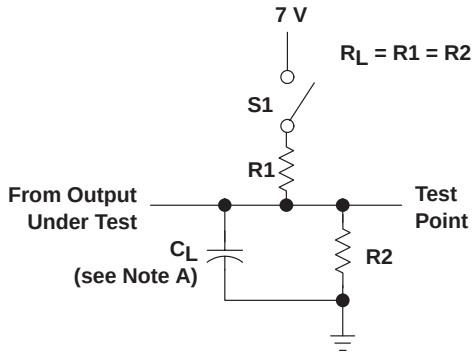
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 4.5 V to 5.5 V, $C_L$ = 50 pF, R1 = 500 Ω, R2 = 500 Ω, $T_A$ = MIN to MAX† | | UNIT |
|---|---|---|---|---|---|
| | | | SN74AS257 | | |
| | | | MIN | MAX | |
| $t_{PLH}$ | A or B | Any Y | 1 | 5.5 | ns |
| $t_{PHL}$ | | | 1 | 6 | |
| $t_{PLH}$ | $\overline{A}$/B | Any Y | 2 | 11 | ns |
| $t_{PHL}$ | | | 2 | 10 | |
| $t_{PZH}$ | $\overline{OE}$ | Any Y | 2 | 7.5 | ns |
| $t_{PZL}$ | | | 2 | 9.5 | |
| $t_{PHZ}$ | $\overline{OE}$ | Any Y | 1.5 | 6.5 | ns |
| $t_{PLZ}$ | | | 2 | 7 | |

## switching characteristics (see Figure 1)

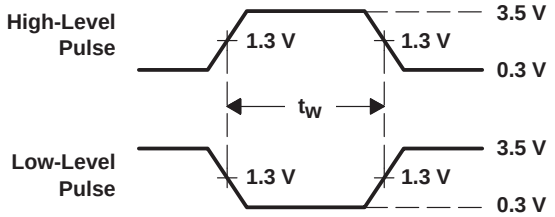
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 4.5 V to 5.5 V, $C_L$ = 50 pF, R1 = 500 Ω, R2 = 500 Ω, $T_A$ = MIN to MAX† | | UNIT |
|---|---|---|---|---|---|
| | | | SN74AS258 | | |
| | | | MIN | MAX | |
| $t_{PLH}$ | A or B | Any Y | 1 | 5 | ns |
| $t_{PHL}$ | | | 1 | 4 | |
| $t_{PLH}$ | $\overline{A}$/B | Any Y | 2 | 9.5 | ns |
| $t_{PHL}$ | | | 2 | 10 | |
| $t_{PZH}$ | $\overline{OE}$ | Any Y | 2 | 8 | ns |
| $t_{PZL}$ | | | 2 | 10 | |
| $t_{PHZ}$ | $\overline{OE}$ | Any Y | 1.5 | 6 | ns |
| $t_{PLZ}$ | | | 2 | 6.5 | |

† For conditions shown MIN or MAX, use the appropriate value specified under recommended operating conditions.

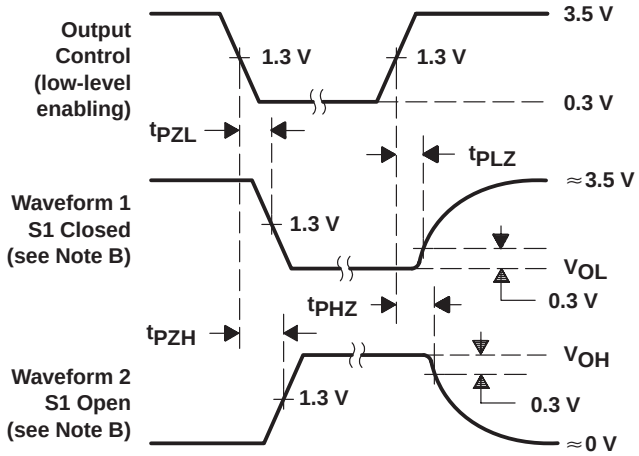
## PARAMETER MEASUREMENT INFORMATION
## SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



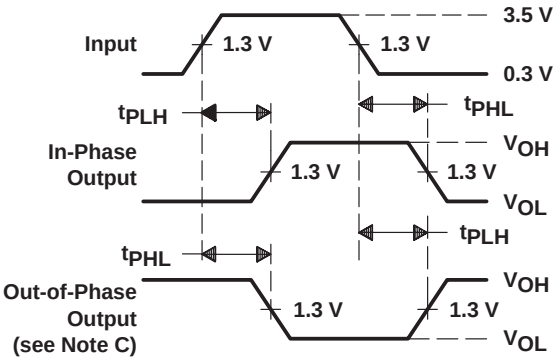

LOAD CIRCUIT
FOR 3-STATE OUTPUTS




VOLTAGE WAVEFORMS
PULSE DURATIONS




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
D. All input pulses have the following characteristics: PRR ≤ 1 MHz, $t_r = t_f$ = 2 ns, duty cycle = 50%.
E. The outputs are measured one at a time with one transition per measurement.

**Figure 1. Load Circuits and Voltage Waveforms**

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 5962-8862601EA | ACTIVE | CDIP | J | 16 | 1 | TBD | Call TI | N / A for Pkg Type | -55 to 125 | 5962-8862601EA SNJ54ALS258AJ | Samples |
| 85097012A | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | 85097012A SNJ54ALS 257AFK | Samples |
| 8509701EA | ACTIVE | CDIP | J | 16 | 1 | TBD | Call TI | N / A for Pkg Type | -55 to 125 | 8509701EA SNJ54ALS257AJ | Samples |
| SN74ALS257AD | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | ALS257A | Samples |
| SN74ALS257ADG4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | ALS257A | Samples |
| SN74ALS257ADR | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | ALS257A | Samples |
| SN74ALS257AN | ACTIVE | PDIP | N | 16 | 25 | Green (RoHS & no Sb/Br) | NIPDAU | N / A for Pkg Type | 0 to 70 | SN74ALS257AN | Samples |
| SN74ALS257ANE4 | ACTIVE | PDIP | N | 16 | 25 | Green (RoHS & no Sb/Br) | NIPDAU | N / A for Pkg Type | 0 to 70 | SN74ALS257AN | Samples |
| SN74ALS257ANSR | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | ALS257A | Samples |
| SN74ALS258AD | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | ALS258A | Samples |
| SN74ALS258AN | ACTIVE | PDIP | N | 16 | 25 | Green (RoHS & no Sb/Br) | NIPDAU | N / A for Pkg Type | 0 to 70 | SN74ALS258AN | Samples |
| SN74ALS258ANE4 | ACTIVE | PDIP | N | 16 | 25 | Green (RoHS & no Sb/Br) | NIPDAU | N / A for Pkg Type | 0 to 70 | SN74ALS258AN | Samples |
| SN74AS257D | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | AS257 | Samples |
| SN74AS257N | ACTIVE | PDIP | N | 16 | 25 | Green (RoHS & no Sb/Br) | NIPDAU | N / A for Pkg Type | 0 to 70 | SN74AS257N | Samples |
| SN74AS257NSR | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 74AS257 | Samples |
| SN74AS258N | ACTIVE | PDIP | N | 16 | 25 | Green (RoHS & no Sb/Br) | NIPDAU | N / A for Pkg Type | 0 to 70 | SN74AS258N | Samples |
| SNJ54ALS257AFK | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | 85097012A | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | | SNJ54ALS 257AFK | |
| SNJ54ALS257AJ | ACTIVE | CDIP | J | 16 | 1 | TBD | Call TI | N / A for Pkg Type | -55 to 125 | 8509701EA SNJ54ALS257AJ | Samples |
| SNJ54ALS258AJ | ACTIVE | CDIP | J | 16 | 1 | TBD | Call TI | N / A for Pkg Type | -55 to 125 | 5962-8862601EA SNJ54ALS258AJ | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF SN54ALS257A, SN54ALS258A, SN74ALS257A, SN74ALS258A :**

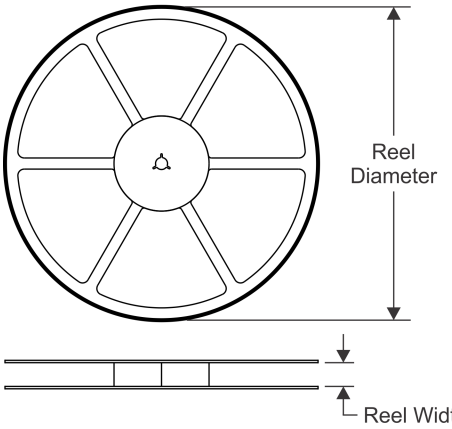
- Catalog: SN74ALS257A, SN74ALS258A
- Military: SN54ALS257A, SN54ALS258A

NOTE: Qualified Version Definitions:

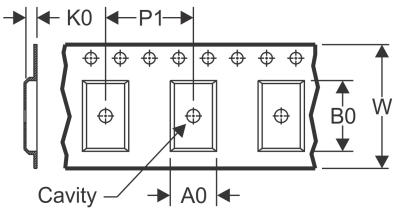
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

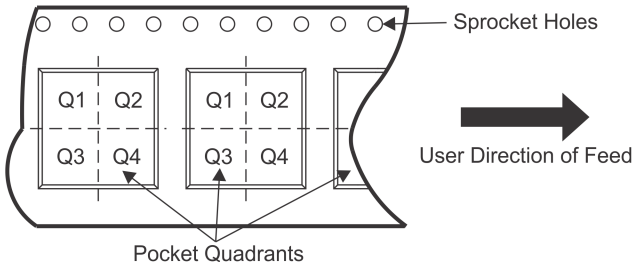



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

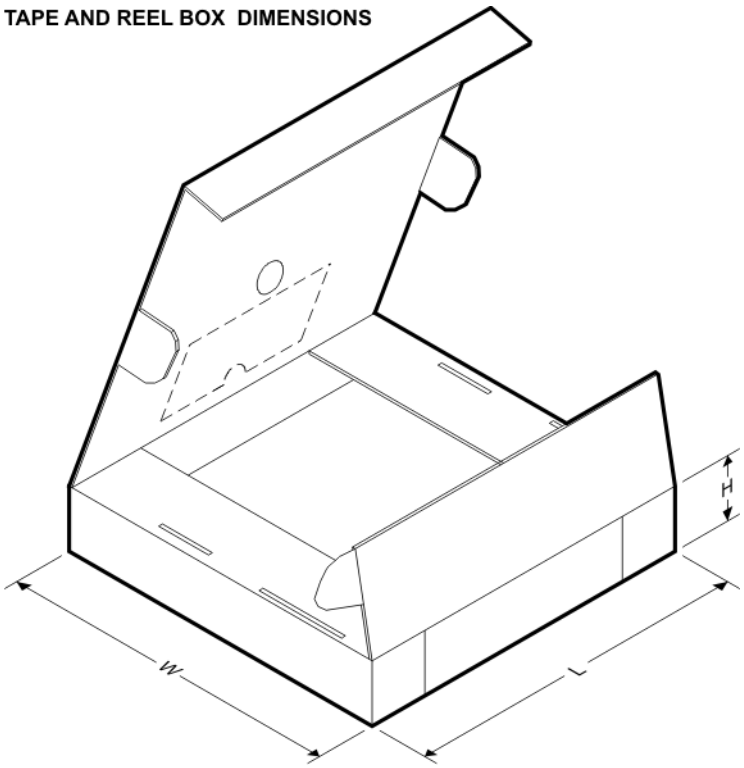
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74ALS257ADR | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74ALS257ANSR | SO | NS | 16 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74AS257NSR | SO | NS | 16 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



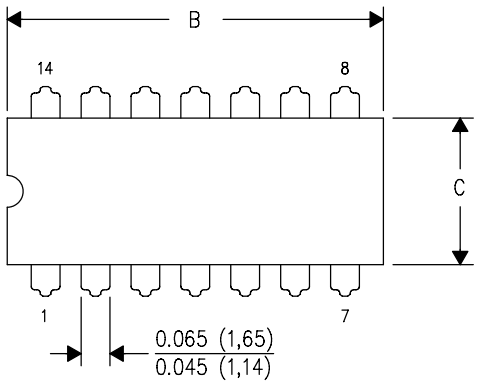

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN74ALS257ADR | SOIC | D | 16 | 2500 | 333.2 | 345.9 | 28.6 |
| SN74ALS257ANSR | SO | NS | 16 | 2000 | 367.0 | 367.0 | 38.0 |
| SN74AS257NSR | SO | NS | 16 | 2000 | 367.0 | 367.0 | 38.0 |

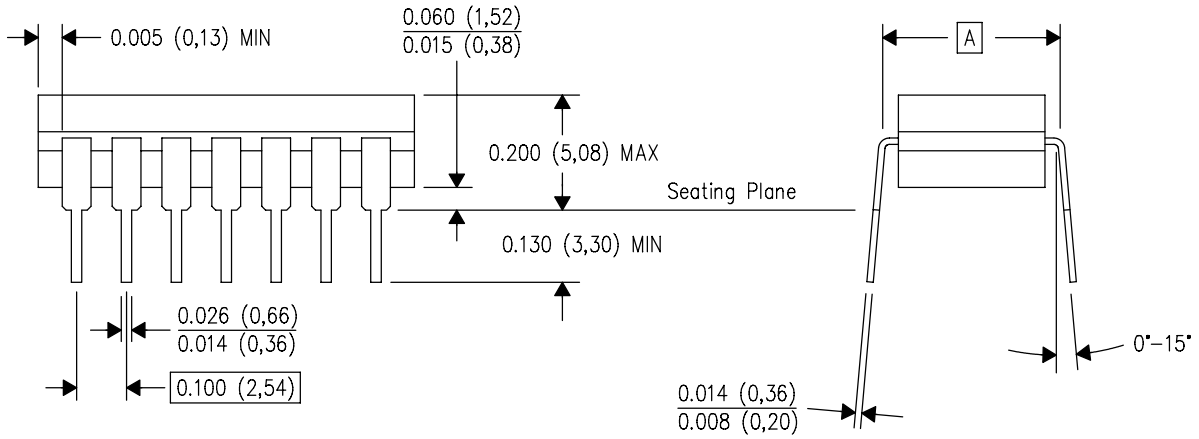
J (R–GDIP–T**)

14 LEADS SHOWN

# CERAMIC DUAL IN–LINE PACKAGE




| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |



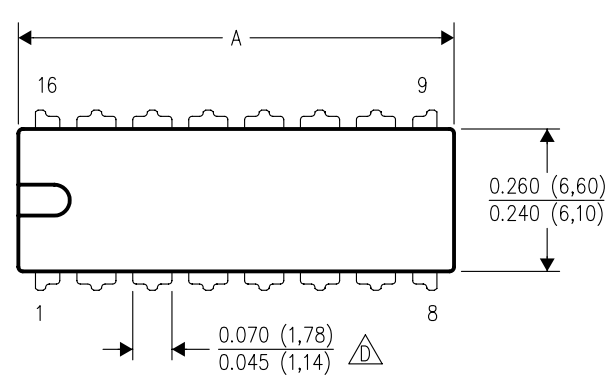

4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

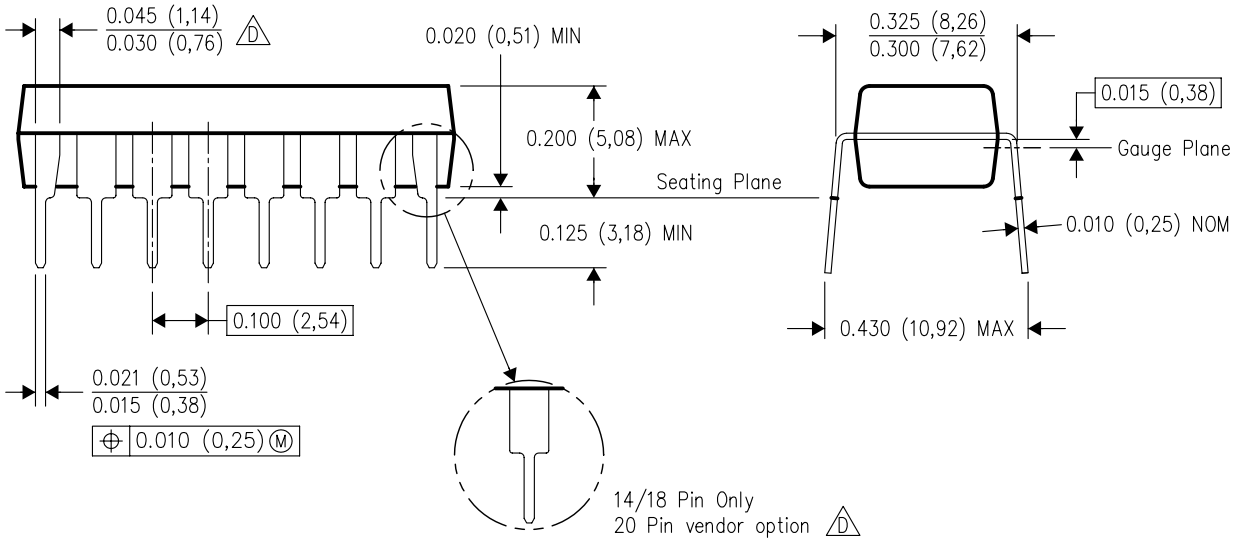
## N (R–PDIP–T**)

## PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN




| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS–001 VARIATION (C) | AA | BB | AC | AD |

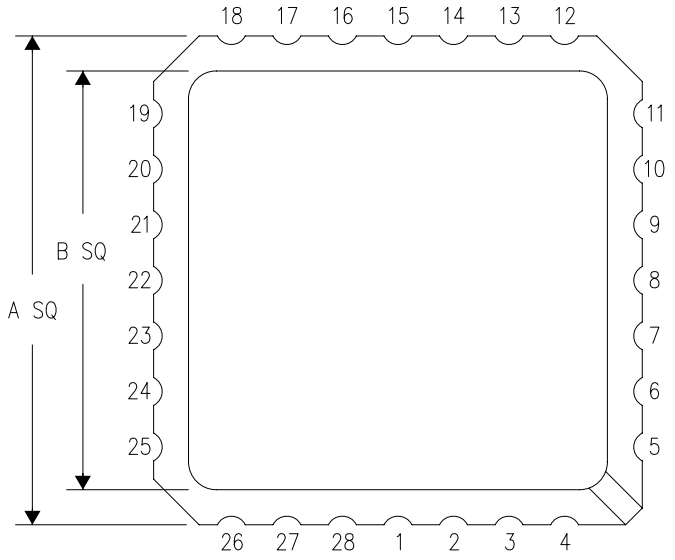



4040049/E 12/2002

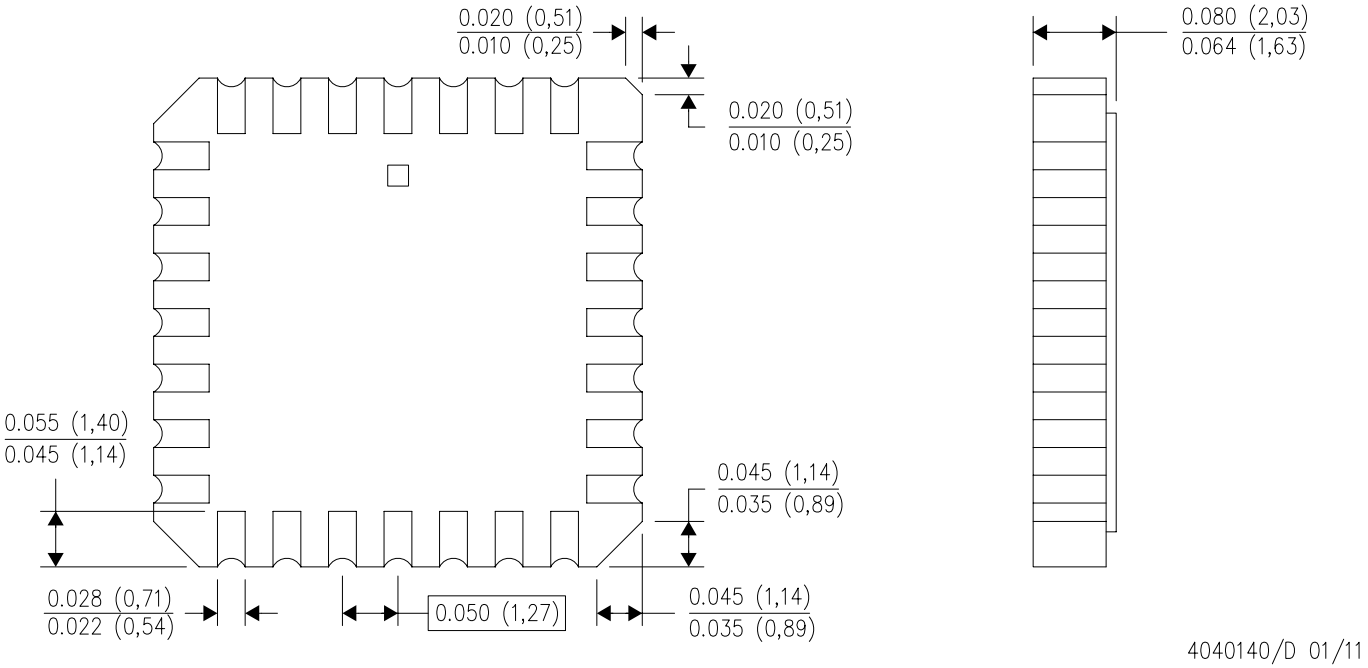
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

FK (S–CQCC–N**) LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



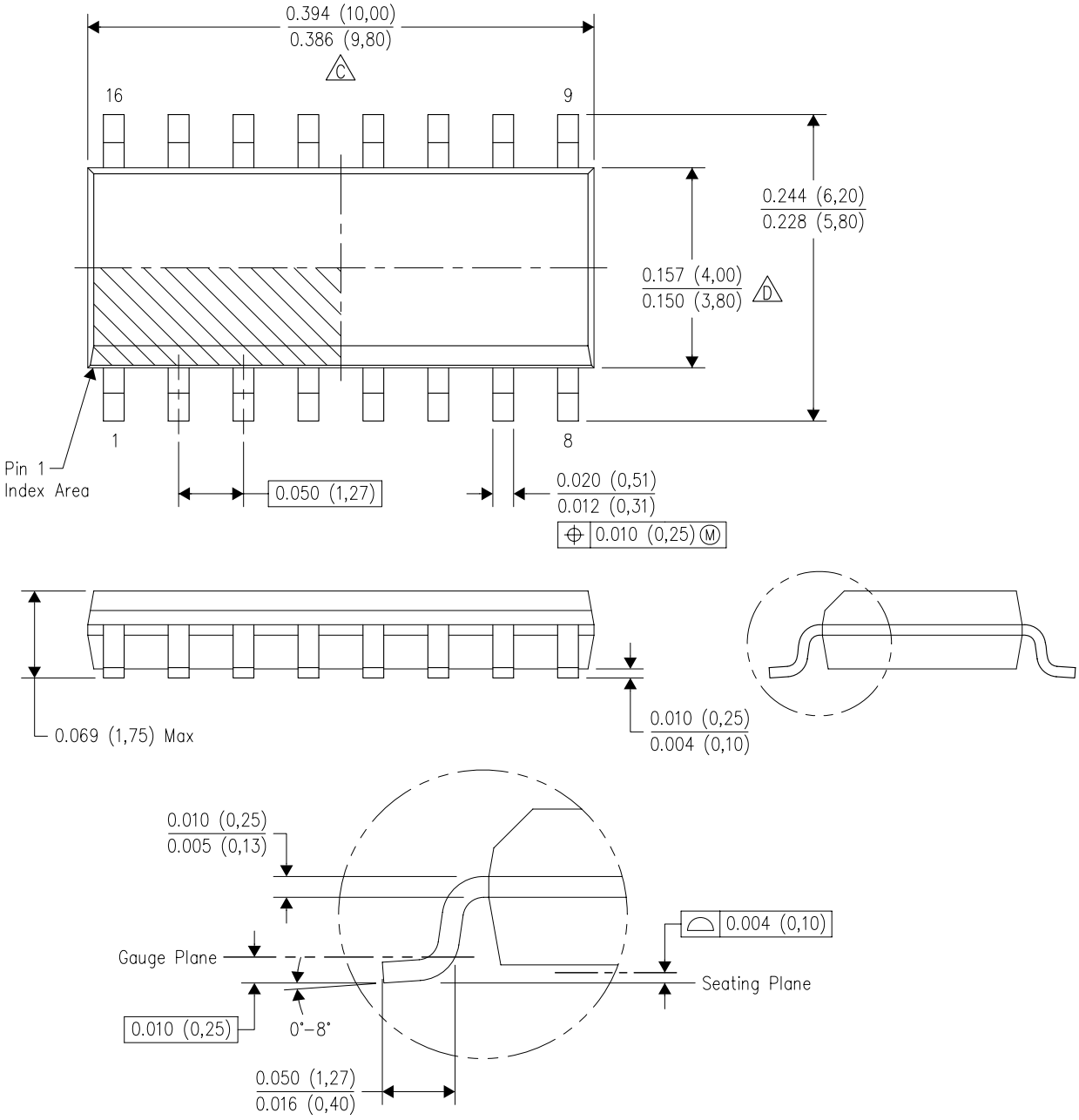

| NO. OF TERMINALS ** | A | | B | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| 20 | 0.342 (8,69) | 0.358 (9,09) | 0.307 (7,80) | 0.358 (9,09) |
| 28 | 0.442 (11,23) | 0.458 (11,63) | 0.406 (10,31) | 0.458 (11,63) |
| 44 | 0.640 (16,26) | 0.660 (16,76) | 0.495 (12,58) | 0.560 (14,22) |
| 52 | 0.740 (18,78) | 0.761 (19,32) | 0.495 (12,58) | 0.560 (14,22) |
| 68 | 0.938 (23,83) | 0.962 (24,43) | 0.850 (21,6) | 0.858 (21,8) |
| 84 | 1.141 (28,99) | 1.165 (29,59) | 1.047 (26,6) | 1.063 (27,0) |




4040140/D 01/11

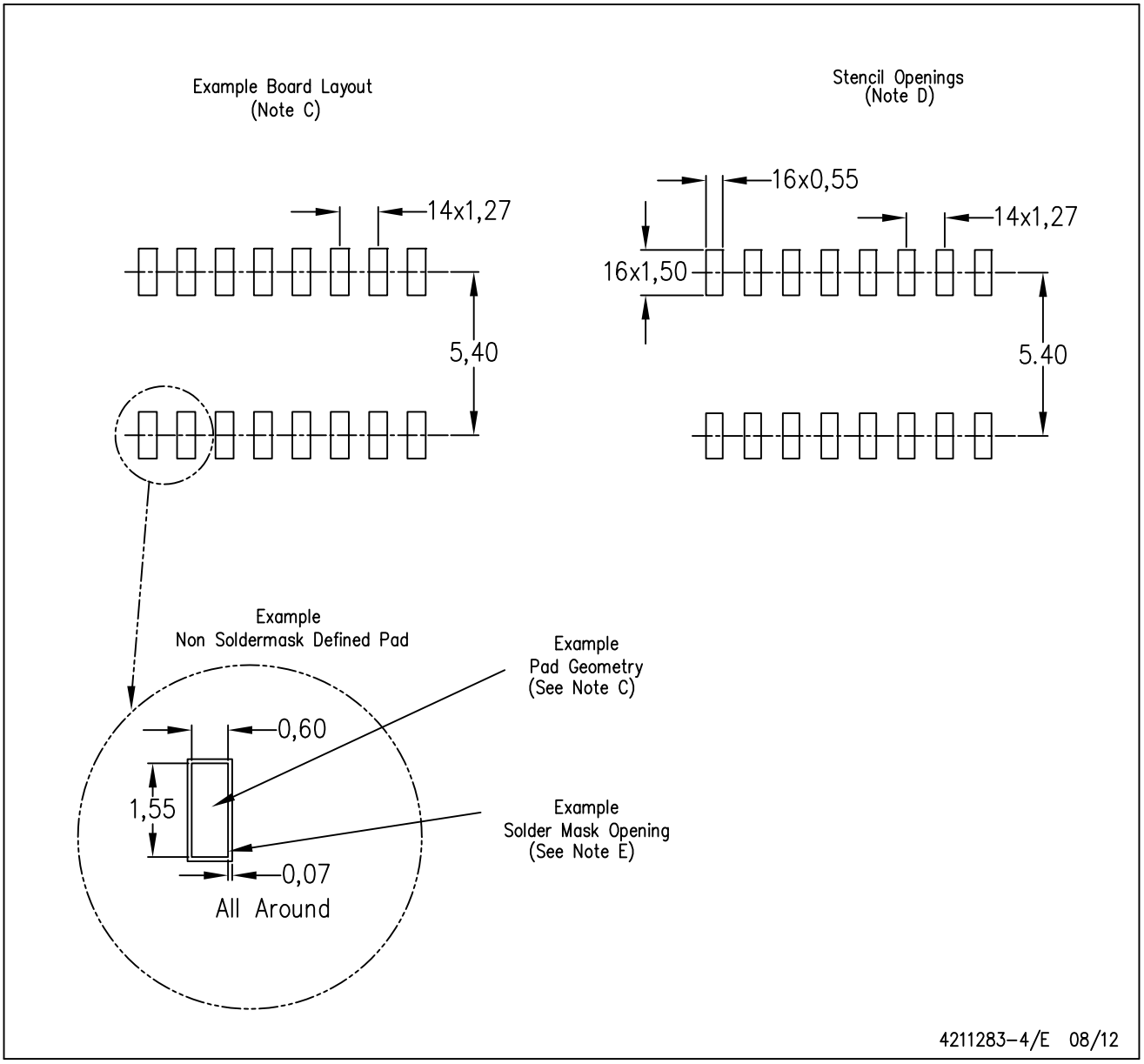
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. Falls within JEDEC MS–004

D (R–PDSO–G16) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE

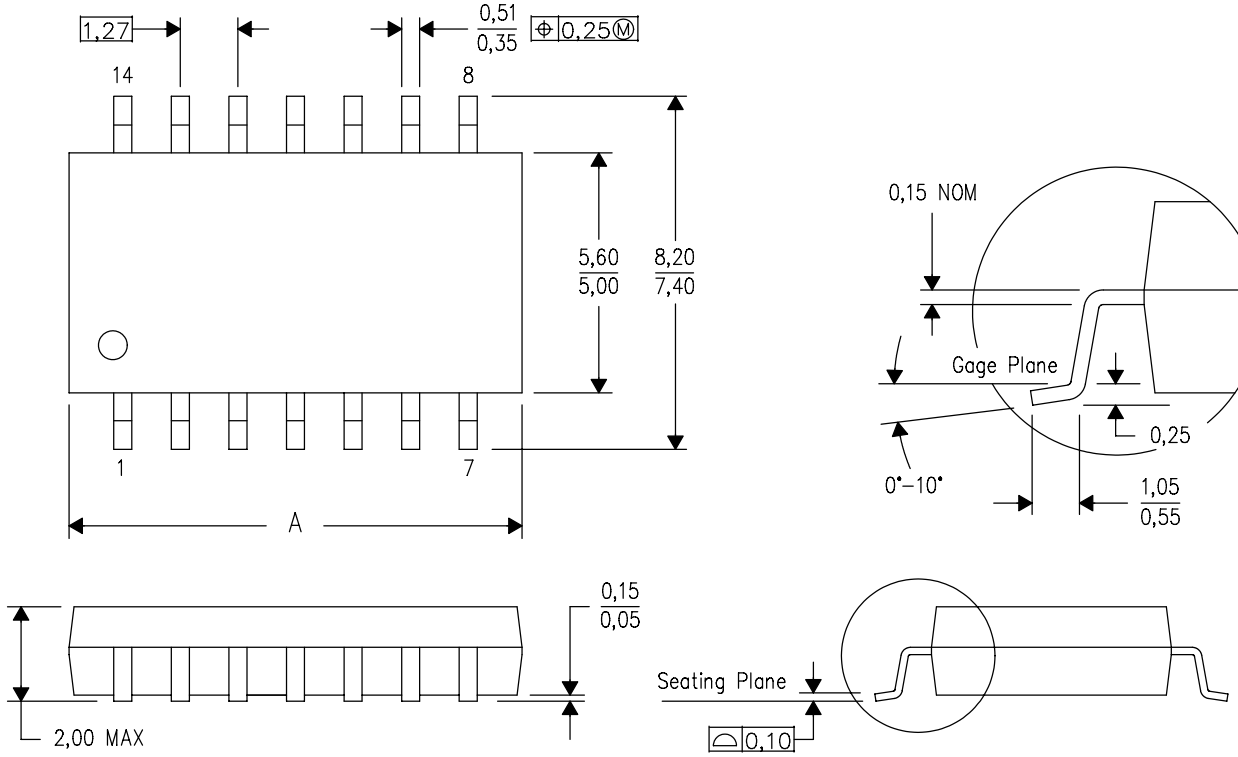



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

## MECHANICAL DATA

**NS (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

**14-PINS SHOWN**




| DIM \ PINS ** | 14 | 16 | 20 | 24 |
|---|---|---|---|---|
| A MAX | 10,50 | 10,50 | 12,90 | 15,30 |
| A MIN | 9,90 | 9,90 | 12,30 | 14,70 |

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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