PIC24FJ128GA310 Family Silicon Errata and Data Sheet Clarification

The PIC24FJ128GA310 family devices that you have received conform functionally to the current Device Data Sheet (DS30009996**G**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC24FJ128GA310 family silicon.

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**C0**).

Data Sheet clarifications and corrections start on Page 7, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers and emulation tools, which are available at the Microchip corporate website (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with MPLAB ICD 2 or PICkit™ 3:

1. Using the appropriate interface, connect the device to the MPLAB ICD 2 programmer/ debugger or PICkit™ 3.
2. From the main menu in MPLAB IDE, select *Configure>Select Device*, and then select the target part number in the dialog box.
3. Select the MPLAB hardware tool (*Debugger>Select Tool*).
4. Perform a "Connect" operation to the device (*Debugger>Connect*). Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note:	If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various PIC24FJ128GA310 family silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID(1)	Revision ID for Silicon Revision(2)	
		B2	C0
PIC24FJ64GA306	46C0h	4	6
PIC24FJ64GA308	46C4h		
PIC24FJ64GA310	46C8h		
PIC24FJ128GA306	46C2h		
PIC24FJ128GA308	46C6h		
PIC24FJ128GA310	46CAh		

Note 1: The Device IDs (DEVID and DEVREV) are located at the last two implemented addresses of configuration memory space. They are shown in hexadecimal in the format, "DEVID DEVREV".

2: Refer to the *"PIC24FJXXXDA1/DA2/GB2/GA3/GC0 Families Flash Programming Specification"* (DS39970) for detailed information on Device and Revision IDs for your specific device.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions(1)	
				B2	C0
A/D	Threshold Detect	1.	Auto-scan feature may not trigger correctly in Sleep mode.	X	
A/D	Threshold Detect	2.	In Auto-Scan mode, the highest number A/D channel may not cause an interrupt.	X	
A/D	Accuracy	3.	Noise injection on A/D input pin during A/D operation (when reading a high-impedance input).	X	X
Core	VBAT mode	4.	VBTBOR (CW3<7>) is not functional.	X	X
RTCC	—	5.	During a Power-on Reset, the RTCC may be enabled.	X	
A/D	DNL	6.	DNL will not meet data sheet specifications and possible missing codes.	X	
Core	Deep Sleep	7.	IPD maximum numbers are higher than in the data sheet.	X	X
A/D	DMA PIA Mode	8.	DMA with A/D in PIA mode will not work.	X	
Reset	Low-Voltage/ Retention Sleep	9.	POR and BOR bits may get set after Reset.	X	X
A/D	—	10.	Band gap input (VBG/2) is not functional.	X	X
Reset	VBAT and POR	11.	POR failure without proper voltage on VBAT pin.	X	
LCD	SEG37	12.	LCD pin, SEG37, does not work on 80-pin devices.	X	X
Power-on Reset	POR	13.	Power-on Reset is not getting re-initialized.	X	X
Core	Sleep	14.	Address trap may occur in Sleep mode with VREGS (RCON<8>) = 1 when the system clock is FRC.	X	X
Core	Low-Voltage/ Retention Sleep	15.	If the device is woken immediately after a Retention Sleep, the device may get a Reset.	X	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note:	Corrections are shown in bold. Where possible, the original bold text formatting.

1. Module: A/D (Threshold Detect)

When the auto-scan feature of the Threshold Detect is enabled (AD1CON5<15> = 1), the automatic scan may fail when these conditions occur together:

- The Device is in Sleep mode, and
- Timer1 is selected as the sample trigger clock source (AD1CON1<7:4> = 0110).

Timer1 and other timers will function correctly as sample triggers in other power-saving modes, such as Idle mode.

Work around

Use INT0 to trigger the A/D in Sleep mode.

Affected Silicon Revisions

B2	C0						
X							

2. Module: A/D (Threshold Detect)

In Auto-Scan mode (AD1CON5<15> = 1), when the Auto-Scan Interrupt mode bits are set to '11' (AD1CON5<9:8> = 11), the highest number channel selected for scanning in AD1CSSL, or AD1CSSH, may not trigger an interrupt on a valid comparison.

Work around

Add a dummy channel to the scanning sequence. For example, when scanning AN0 and AN1, set AD1CSSL to 0x0007 or 0x8003, or whatever is practical given the implementation.

Also, if the highest number channel needs to be scanned, the AD1CHITH register bits can be polled to observe a valid comparison.

Affected Silicon Revisions

B2	C0						
X							

3. Module: A/D (Accuracy)

Noise injection on the A/D input pin during A/D operation (when reading a high-impedance input) may adversely affect the conversion results.

Work around

Increase the sample time for the channel that is being converted or reduce the source impedance.

Affected Silicon Revisions

B2	C0						
X	X						

4. Module: Core (VBAT Mode)

VBTBOR (CW3<7>) will not work correctly. The behavior of this bit is different in Revision B2 and C0.

In Revision B2, it does not matter if this bit (CW3<7>) is '1' or '0', the feature will not work.

In Revision C0, the feature is available but may not work correctly, so it is recommended to maintain CW3<7> = 0 to disable the VBTBOR. If the bit is maintained as '1', the RTCC may be reset above VBT voltage (1.6V).

Work around

The application can monitor the VBAT voltage using ADC after a POR in VBAT mode. The ADC is internally connected to VBAT to measure VBAT/2 (CH0SB<4:0>= 11111).

The VBAT can be monitored using ADC, and if the VBAT has gone below VBT (1.6V), RTCC needs to be reconfigured with the correct date and time.

Affected Silicon Revisions

B2	C0						
X	X						

5. Module: RTCC

During a Power-on Reset, the RTCC may be enabled.

Work around

To ensure that the RTCC is not enabled, make sure to clear the RTCEN bit after a POR. This is recommended whether RTCC is used or not.

After a POR, execute the code shown in Example 1 to disable the RTCC.

Affected Silicon Revisions

B2	C0						
X							

EXAMPLE 1: DISABLING THE RTCC FOLLOWING POR

```
MOV     #NVMKEY,    W1              ;move the address of NVMKEY into W1
MOV     #0x55,      W2
MOV     W2,         [W1]            ;start 55/AA sequence
MOV     #0xAA,      W3
MOV     W3,         [W1]
BSET    RCFGCAL,    #13             ;set the RTCWREN bit
RCFGCALbits.RTCEN=0;
```

6. Module: A/D

The DNL will not meet the data sheet specification; the DNL will be ≤1.5. There may be possible missing codes in 12-bit mode in locations: 511, 1023, 1535, 2047, 2559, 3071, 3583.

Work around

None.

Affected Silicon Revisions

B2	C0						
X							

7. Module: Core (Deep Sleep)

The I_{PD} maximum number for Deep Sleep may not meet the data sheet specification (DC70).

The maximum value for Deep Sleep at 3.3V will be 6 µA.

Work around

None.

Affected Silicon Revisions

B2	C0						
X	X						

8. Module: A/D

The A/D will not work with DMA in PIA mode.

Work around

None.

Affected Silicon Revisions

B2	C0						
X							

9. Module: Reset

When the device is in Low-Voltage/Retention Sleep mode (Sleep with CW1<10> = 0 and RETEN = 1), if a Master Clear Reset is given, the POR (RCON<0>) and BOR (RCON<1>) bits may get set after the Reset.

Work around

Use registers, such as DSGPR0 or DSGPR1, to indicate the device was in Low-Voltage/Retention Sleep mode before the $\overline{MCLR}$ Reset is given.

Affected Silicon Revisions

B2	C0						
X	X						

10. Module: A/D

The internal VBG/2 input channel is not functional. When this input is selected as the channel to be converted, no conversion will occur and a device Reset will occur.

Work around

None.

Affected Silicon Revisions

B2	C0						
X	X						

11. Module: Reset (VBAT and POR)

For applications that use the VBAT feature, the device may fail to start/restart on POR if VBAT voltage is below 1.2V.

Work around

If the VBAT mode features will be used in the application, ensure that a VBAT source of at least 1.2V is always connected to the VBAT pin.

If the VBAT mode features are not to be used, always connect the VBAT pin to VDD, as recommended in the data sheet.

Affected Silicon Revisions

B2	C0						
X							

12. Module: LCD

LCD segment, SEG37, will not function as an LCD segment pin. The issue only exists in the 80-pin devices (PIC24FJ128GA308 and PIC24FJ64GA308). The SEG37 pin works correctly on 100-pin devices.

Work around

None.

Affected Silicon Revisions

B2	C0						
X	X						

13. Module: Power-on Reset

When the device is operating with Brown-out Reset (BOR) disabled, it is recommended to follow the data sheet specification of starting the VDD from VSS to ensure an internal Power-on Reset. Failing to do so may result in the device failing to start up or other unexpected behavior.

Work around

There are three work arounds to resolve the issue:

1. Enable the BOR to ensure that the device gets a proper Power-on Reset.
2. If the BOR cannot be enabled, always start the VDD from VSS to ensure a proper Power-on Reset (Parameter No. DC16 in Table 32-3 of **Section 32.0 "Electrical Characteristics"** in the data sheet).
3. Use an external voltage supervisor chip on the MCLR pin to hold the MCLR low when the power supply voltage is between 1.4V and 2.0V. Release MCLR after the VDD is in the operating range.

Affected Silicon Revisions

B2	C0						
X	X						

14. Module: Core

In Sleep mode, with the following conditions:

1. Sleep mode with VREGS (RCON<8>) = 1 (for faster wake-up).
2. System clock is used as the FRC.

An address trap may occur if an interrupt wakes up the device immediately after executing the SLEEP instruction (within 500 ns).

Work around

There are two ways to resolve the issue:

1. Select the FRCDIV as the system clock and use the following steps:
   a) Before going to Sleep, change the clock divider to the slowest speed (RCDIV<2:0> (CLKDIV<10:8>) = 111).
   b) Execute the SLEEP instruction.
   c) When the interrupt wakes up the device, switch the FRCDIV to the required clock (RCDIV<2:0> (CLKDIV<10:8>) = *required clock*).

   Repeat the above steps any time the device goes to Sleep and wakes up.

OR

2. Execute Sleep with VREGS (RCON<8>) = 0.

Affected Silicon Revisions

B2	C0						
X	X						

15. Module: Core

When the device wakes from a Low-Voltage/ Retention Sleep mode (Sleep with CW1<10> = 0 and RETEN = 1), if the wake-up event is within 1 ms after the SLEEP instruction, the device may go into Reset.

Work around

Enable the BOR to ensure that the device band gap is enabled during the Retention Sleep.

Affected Silicon Revisions

B2	C0						
X	X						

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS30009996**G**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

1. Module: Pin Diagrams

The following note has been added to the 64-Pin TQFP/QFN pin diagram on Page 3:

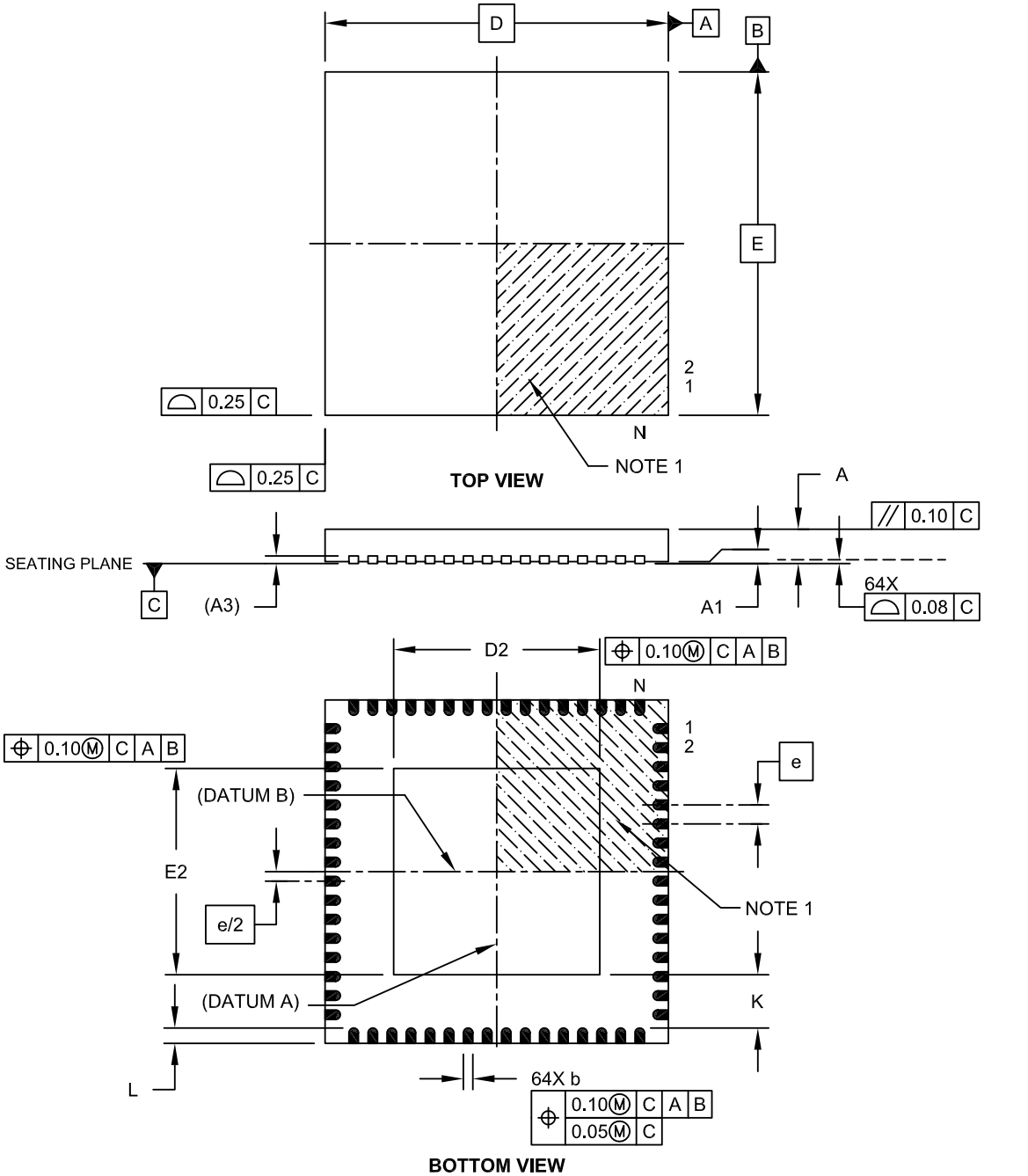
Note 2: It is recommended to connect the metal pad on the bottom of the 64-pin QFN package to VSS.

2. Module: Packaging Information

The 64-Lead Plastic Quad Flat, No Lead Package (MR) drawings on Pages 391 through 393 have been replaced with the C04-154A package drawings shown below.

64-Lead Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body with 5.40 x 5.40 Exposed Pad [QFN]

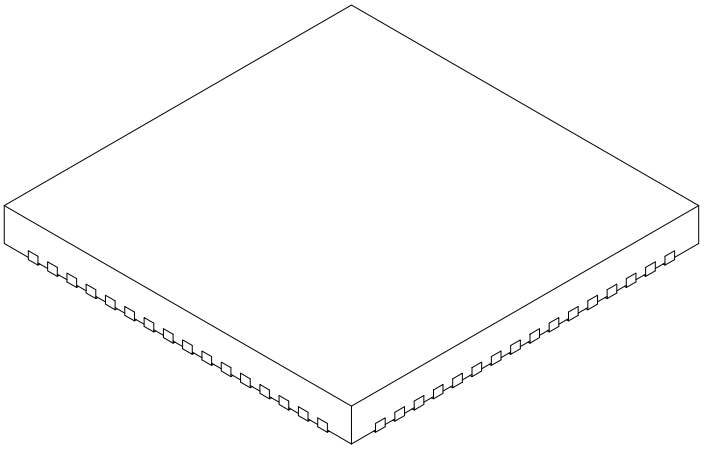
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-154A Sheet 1 of 2

64-Lead Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body with 5.40 x 5.40 Exposed Pad [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		64	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Width	E		9.00 BSC	
Exposed Pad Width	E2	5.30	5.40	5.50
Overall Length	D		9.00 BSC	
Exposed Pad Length	D2	5.30	5.40	5.50
Contact Width	b	0.20	0.25	0.30
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	-	-

Notes:

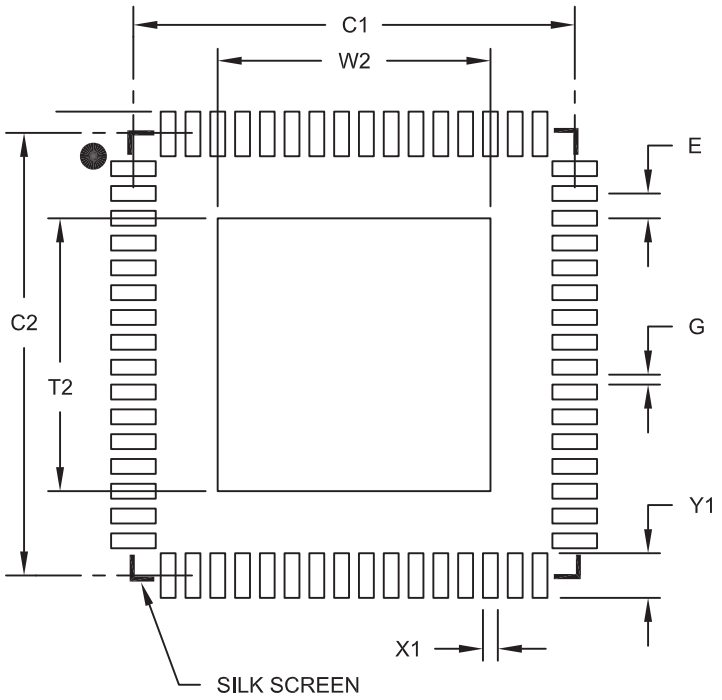
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-154A Sheet 2 of 2

64-Lead Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body [QFN]
With 0.40 mm Contact Length and 5.40x5.40mm Exposed Pad

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	W2			5.50
Optional Center Pad Length	T2			5.50
Contact Pad Spacing	C1		8.90	
Contact Pad Spacing	C2		8.90	
Contact Pad Width (X64)	X1			0.30
Contact Pad Length (X64)	Y1			0.85
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2154A

APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (11/2011)

Initial release of this document. Includes silicon issues 1 (A/D Conversion During Sleep), 2 (A/D Auto-Scan Mode), 3 (A/D Accuracy), 4 (VBTBOR) and 5 (RTCC). Added data sheet clarification 1 (Section 22.0 Real Time Clock and Calendar).

Rev B Document (4/2012)

Included changes to silicon issue 1 (A/D Conversion During Sleep) and added silicon issues 8 (A/D) and 9 (Reset), and added data sheet clarifications 2 (Special Features), 3 (Special Features), 4 (Special Features), 5 (Timer1), 6 (Pin Diagrams), 7 (Pin Diagrams), 8 (Guidelines for Getting Started with 16-Bit Microcontrollers), 9 (Memory Organization), 10 (I/O Ports), 11 (Memory Organization), 12 (I/O Ports), 13 (Electrical Characteristics), 14 (Electrical Characteristics), 15 (12-Bit A/D Converter with Threshold Scan), 16 (Real-Time Clock and Calendar – RTCC) and 17 (A/D Converter).

Rev C Document (7/2012)

Added silicon revision C0 to document, with existing silicon issues 3 (A/D, Accuracy) and 9 (Reset).

Added new silicon issues 10 (A/D) and 11 (Reset, VBAT and POR) to silicon revision B2. Issue 10 is also added to silicon revision C0.

Added data sheet clarifications 18-19 (A/D), 20-21 (Memory Organization), 22-24 (Oscillator) and 25 (Power-Saving Features).

Corrected the titles of several existing silicon issues (1, 2, 3, 4, 7 and 8) for compatibility with existing errata documentation. No changes are made to the text of any issues.

Updated the title of data sheet clarification 8 (“Getting Started with 16-bit Microcontrollers”) to “Overview”.

Updated several data sheet clarification issues (3, 4, 13 and 17) to remove extraneous tables, rows and other information not relevant to the items being changed.

Other minor typographic corrections throughout.

Rev D Document (1/2013)

In silicon issue 7 (Core (Deep Sleep)), changed the maximum value for Deep Sleep at 3.3V from 2.5 μA to 6 μA.

Added data sheet clarifications 26 (Power-Saving Features, 27 (Oscillator Configuration), 28 (Packaging Information), 29 (Serial Peripheral Interface (SPI)) and 30 (I/O Ports).

Rev E Document (2/2013)

Indicated that silicon issue 7 is also applicable to silicon revision C0.

Added data sheet clarification 31 (Power-Saving Features).

Rev F Document (10/2013)

Added silicon issue 12 (LCD).

Rev G Document (6/2014)

Updated silicon issue 4 (Core, VBAT mode) with information regarding VBTBOR in Revision B2 and Revision C0. Added silicon issue 13 (Power-on Reset).

Removed all previous data sheet clarifications that have been addressed in the latest data sheet revision.

Rev H (9/2016

Added silicon issue 14 (Core).

Added data sheet clarifications 1 (Pin Diagrams) and 2 (Packaging Information).

Rev J (1/2019)

Added silicon issue 15 (Core).

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
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