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FAIRCHILD SEMICONDUCTOR®

January 2013

FMS6501A
12x9 Video Switch Matrix with Input Clamp, Input Bias Circuitry, and Output Drivers

Features

- 12 x 9 Crosspoint Matrix
- Supports SD, ED, HD (1080i, 1080p Video)
- Input Clamp / Bias Circuitry
- Dual-Load Output Drivers with Disable
- AC- or DC-Coupled Inputs
- AC- or DC-Coupled Outputs
- 1-to-1 or 1-to-Many Input-to-Output Connections
- Programmable Gain: +6, +7, +8, or +9 dB
- I^2C Compatible Digital Interface, Standard Mode
- 9 kV ESD Protection
- Supply Voltage Range: 3.3 V to 5 V
- Lead-Free 28–Lead TSSOP Package

Applications

- Cable and Satellite Set-Top Boxes
- TV and HDTV Sets
- A/V Switchers
- Personal Video Recorder (PVR)
- Security and Surveillance
- Video Distribution
- Automotive (In-Cabin Entertainment)

Description

The FMS6501A switch matrix provides flexible options for today's video applications. The device has twelve (12) inputs that can be routed to any of the nine (9) outputs. Each input can be routed to one or more outputs, but only one input may be routed to any one output. The input-to-output routing is controlled via an I^2C-compatible digital interface.

Each input supports an integrated clamp option to set the output sync-tip level of video with sync to approximately 300 mV. Alternatively, the input may be internally biased to center signals without sync (Chroma, Pb, Pr) at approximately 1.25 V. These DC output levels are for the 6 dB gain setting. Higher gain settings increase the DC output levels accordingly. The input clamp/bias mode is selected via I^2C control.

Unused outputs may be powered down to reduce power dissipation.

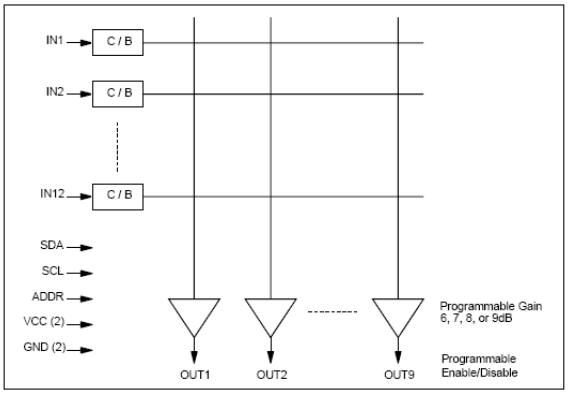

Figure 1. Block Diagram

Ordering Information

Part Number	Operating Temperature Range	Package	Packing Method	Quantity
FMS6501AMTC28X	-40°C to +85°C	28-Lead, Thin-Shrink Small-Outline Package (TSSOP), JEDEC MO-153, 4.4 mm Wide	Reel	2500

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Pin Configuration

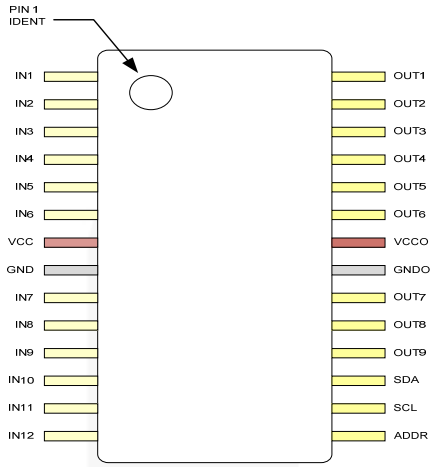

Figure 2. Pin Assignments

Pin Definitions

Pin #	Name	Type	Description
1	IN1	Input	Input, channel 1
2	IN2	Input	Input, channel 1
3	IN3	Input	Input, channel 1
4	IN4	Input	Input, channel 1
5	IN5	Input	Input, channel 1
6	IN6	Input	Input, channel 1
7	VCC	Power	Core power, must be tied to positve power supply
8	GND	Power	Core ground, must be tied to ground
9	IN7	Input	Input, channel 7
10	IN8	Input	Input, channel 8
11	IN9	Input	Input, channel 9
12	IN10	Input	Input, channel 10
13	IN11	Input	Input, channel 11
14	IN12	Input	Input, Channel 12
15	ADDR	Input	Selects I^2C address; 0=0x06 (0000 0110), 1=0x86 (1000 0110)
16	SCL	Input	Serial clock for I^2C port
17	SDA	Input	Serial data for I^2C port
18	OUT9	Output	Output, channel 9
19	OUT8	Output	Output, channel 8
20	OUT7	Output	Output, Channel 7
21	GNDO	Power	Output ground, must be tied to ground
22	VCCO	Power	Output power, must be tied to positve power supply
23	OUT6	Output	Output, channel 6
24	OUT5	Output	Output, channel 5
25	OUT4	Output	Output, channel 4
26	OUT3	Output	Output, channel 3
27	OUT2	Output	Output, channel 2
28	OUT1	Output	Output, channel 1

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Min.	Max.	Unit
V_S	DC Supply Voltage	-0.3	6.0	V
V_{IO}	Analog and Digital I/O	-0.3	V_{CC}+0.3	V
V_{OUT}	Maximum Output Current Per Channel, Do Not Exceed		40	mA

Electrostatic Discharge Information

Symbol	Parameter	Min.	Unit
ESD	Human Body Model (HBM), JESD22-A114, Pins 18,19,20,23,24,25,26,27,28	12	kV
	Human Body Model (HBM), JESD22-A114, All Input Pins and VCC	9	
	Charged Device Model(CDM), JESD22-C101, All Pins	2	

Reliability Information

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_J	Junction Temperature			150	°C
T_{STG}	Storage Temperature Range	-65		150	°C
T_L	Lead Temperature (Soldering, 10 Seconds)			300	°C
Θ_{JA}	Thermal Resistance, JEDEC Standard, Multilayer Test Boards, Still Air		50		°C/W

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_A	Operating Temperature Range	-40		+85	°C
V_{CC}	Supply Voltage Range	3.135	5.00	5.25	V

DC Electrical Characteristics

T_A=25°C, V_{CC} 5 V, V_{IN} = 1 V_{pp}, input bias mode, one-to-one routing, 6 dB gain, all inputs AC coupled with 0.1 µF, unused inputs AC-terminated through 75 Ω to GND, all outputs AC coupled with 220 ΩF into 150 Ω loads, referenced to 400 kHz, unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_{CC}	Supply Current(1)	No Load, All Outputs Enabled		80	100	mA
V_{OUT}	Video Output Range			2.8		V_{PP}
R_{OFF}	Off Channel Output Impedance	Output Disabled		3.0		kΩ
V_{CLAMP}	DC Output Level(1)	Clamp Mode		0.3	0.4	V
V_{BIAS}	DC Output Level(1)	Bias Mode	1.15	1.25	1.35	V
PSRR	Power Supply Rejection Ratio	DC (All Channels)		50		dB

Note:
1. 100% tested at T_A=25°C.

AC Electrical Characteristics

T_A=25°C, V_{CC} 5 V, V_{IN} = 1 V_{pp}, input bias mode, one-to-one routing, 6 dB gain, all inputs AC coupled with 0.1 µF, unused inputs AC-terminated through 75 Ω to GND, all outputs AC coupled with 220 ΩF into 150 Ω loads, referenced to 400 kHz, unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
AV_{SD}	Channel Gain Error(2)	All Channels, All Gain Settings, DC	-0.2	0	+0.2	dB
AV_{STEP}	Gain Step(2)	All Channels, DC	0.9	1.0	1.1	dB
f_{+1dB}	1dB Peaking Bandwidth	V_{OUT} = 1.4 V_{PP}		65		MHz
f_{-1dB}	-1dB Bandwidth	V_{OUT} = 1.4 V_{PP}		90		MHz
f_C	-3dB Bandwidth	V_{OUT} = 1.4 V_{PP}		115		MHz
dG	Differential Gain	Standard SD Signal 3.58 MHz		0.1		%
dP	Differential Phase	Standard SD Signal 3.58 MHz		0.2		°
THD_{SD}	SD Output Distortion	V_{OUT} = 1.4 V_{PP} 5 MHz		0.05		%
THD_{HD}	HD Output Distortion	V_{OUT} = 1.4 V_{PP} 22 MHz		0.6		%
X_{TALK1}	Input Crosstalk	1 MHz, V_{OUT} = 2.0 V_{PP}(3)		-72		dB
X_{TALK2}	Input Crosstalk	15 MHz, V_{OUT} = 2.0 V_{PP}(3)		-50		dB
X_{TALK3}	Output Crosstalk	1 MHz, V_{OUT} = 2.0 V_{PP}(3)		-68		dB
X_{TALK4}	Output Crosstalk	15 MHz, V_{OUT} = 2.0 V_{PP}(3)		-61		dB
X_{TALK5}	Multi-Channel Crosstalk	Standard SD Video, V_{OUT} = 2.0 V_{PP}(4)		-45		dB
SNR_{SD}	Signal-to-Noise Ratio(5)	NTC-7 Weighting, 4.2 MHz Low Pass, 100 kHz High Pass		73		dB
V_{NOISE}	Channel Noise	400 kHz to 100 MHz, Input Referred		20		nV/rtHz
AMP_{ON}	Amplifier Recovery Time	Post I^2C Programming		300		ns

Notes:
2. 100% tested at T_A=25°C.
3. Adjacent input pair to adjacent output pair. Interfering input is through an open switch.
4. Crosstalk of eight synchronous switching outputs into single, asynchronous switching output.
5. Signal-to-Noise Ratio (SNR) = 20 x log (714 mV/rms noise).

Applications Information

Digital Interface

The I^2C-compatible interface is used to program output enables, input-to-output routing, input clamp / bias, and output gain. The I^2C address is 0x06 (0000 0110) with the ability to offset it to 0x86 (1000 0110) by tying the ADDR pin HIGH.

Both data and address data, of eight bits each, are written to the I^2C address to access control functions.

There are separate internal addresses for each output. Each output's address includes bits to select an input channel, adjust the output gain, and enable or disable the output amplifier. More than one output can select the same input channel for one-to-many routing. When the outputs are disabled, they are placed in a high-impedance state. This allows multiple FMS6501A devices to be paralleled to create a larger switch matrix. Typical output power-up time is less than 500 ns.

The clamp / bias control bits are written to their own internal addresses, since they should always remain the same regardless of signal routing. They are set based on the input signal connected to the FMS6501A.

All undefined addresses may be written without effect.

Table 1. Output Control Register Contents and Defaults

Control Name	Width	Type	Default	Bit(s)	Description
Enable	1 Bit	Write	0	7	Channel Enable: 1=Enable, 0=Power Down(6)
Gain	2 Bits	Write	0	6:5	Channel Gain: 00=6dB, 01=7dB, 10=8dB, 11=9dB
Inx	5 Bits	Write	0	4:0	Input Selected to Drive this Output: 00000=OFF(7), 00001=IN1, 00010=IN2... 01100=IN12

Notes:
6. Power down places the output in a high-impedance state so multiple FMS6501 devices may be paralleled. Power down also de-selects any input routed to the specified output.
7. When all inputs are OFF, the amplifier input is tied to approximately 150 mV and the output goes to approximately 300 mV with the 6 dB gain setting.

Table 2. Output Control Register MAP

Register Name	Register Address	Bit 7	Bit 6	Bit5	Bit4(8)	Bit3	Bit2	Bit1	Bit0
OUT1	0x01	Enable	Gain1	Gain0	IN4	IN3	IN2	IN1	IN0
OUT2	0x02	Enable	Gain1	Gain0	IN4	IN3	IN2	IN1	IN0
OUT3	0x03	Enable	Gain1	Gain0	IN4	IN3	IN2	IN1	IN0
OUT4	0x04	Enable	Gain1	Gain0	IN4	IN3	IN2	IN1	IN0
OUT5	0x05	Enable	Gain1	Gain0	IN4	IN3	IN2	IN1	IN0
OUT6	0x06	Enable	Gain1	Gain0	IN4	IN3	IN2	IN1	IN0
OUT7	0x07	Enable	Gain1	Gain0	IN4	IN3	IN2	IN1	IN0
OUT8	0x08	Enable	Gain1	Gain0	IN4	IN3	IN2	IN1	IN0
OUT9	0x09	Enable	Gain1	Gain0	IN4	IN3	IN2	IN1	IN0

Notes:
8. IN4 is provided for forward compatibility and should always be written as 0.

Table 3. Clamp Control Register Contents and Defaults

Control Name	Width	Type	Default	Bit(s)	Description
CLAMP	1 bit	Write	0	7:0	Clamp / Bias selection: 1 = Clamp, 0 = Bias

Table 4. Clamp Control Register Map

Register Name	Register Address	Bit 7	Bit 6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CLAMP1	0x1D	Clmp8	Clmp7	Clmp6	Clmp5	Clmp4	Clmp3	Clmp2	Clmp1
CLAMP2	0x1E	Resv'd	Resv'd	Resv'd	Resv'd	Clmp12	Clmp11	Clmp10	Clmp9

I²C BUS Characteristics

T_A = 25°C and V_{CC} = 5 V unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{IL}	Digital Input Low[9]	SDA, SCL, ADDR	0		1.5	V
V_{IH}	Digital Input High[9]	SDA, SCL, ADDR	3.0		V_{CC}	V
f_{scl}	Clock Frequency	SCK		100		kHz
t_R	Input Rise Time	1.5 V to 3 V		1000		ns
t_F	Input Fall Time	1.5 V to 3 V		300		ns
t_{LOW}	Clock Low Period			4.7		µs
t_{HIGH}	Clock High Period			4.0		µs
$t_{SU,DAT}$	Data Set-up Time			300		ns
$t_{HD,DAT}$	Data Hold Time			0		ns
$t_{SU,STO}$	Set-up Time from Clock HIGH to Stop			4		µs
t_{BUF}	Start Set-up Time Following a Stop			4.7		µs
$t_{HD,STA}$	Start Hold Time			4		µs
$t_{SU,STA}$	Start Set-up Time Following Clock LOW to HIGH			4.7		µs

Notes:
9. 100% tested at T_A=25°C.

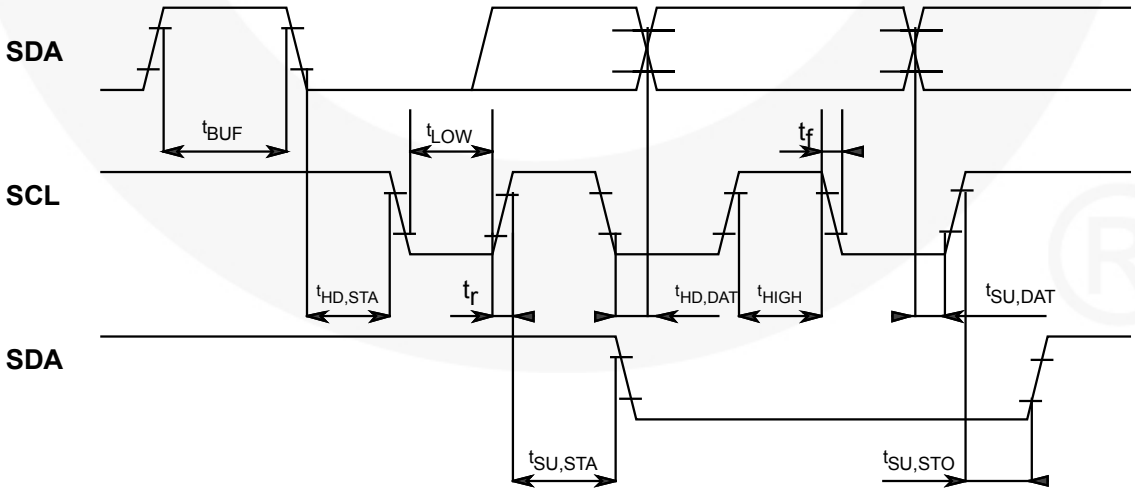

Figure 3. I²C Bus Timing

I²C Interface

Operation

The I²C-compatible interface conforms to the I²C specification for Standard Mode. Individual addresses may be written. There is no read capability. The interface consists of two lines. These is a serial data line (SDA) and a serial clock line (SCL), both of which must be connected to a positive supply through an external resistor. Data transfer may be initiated only when the bus is not busy.

Bit Transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse. Changes in the line during this time are interpreted as a control signal.

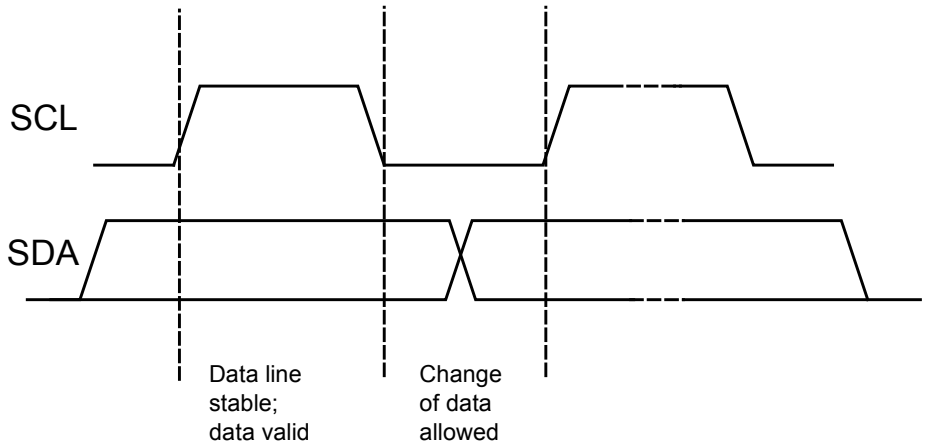

Figure 4. Bit Transfer

Start and Stop Conditions

The data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH, is defined as START condition (S). A LOW-to-HIGH transition of the data line, while the clock is HIGH, is defined as STOP condition (P).

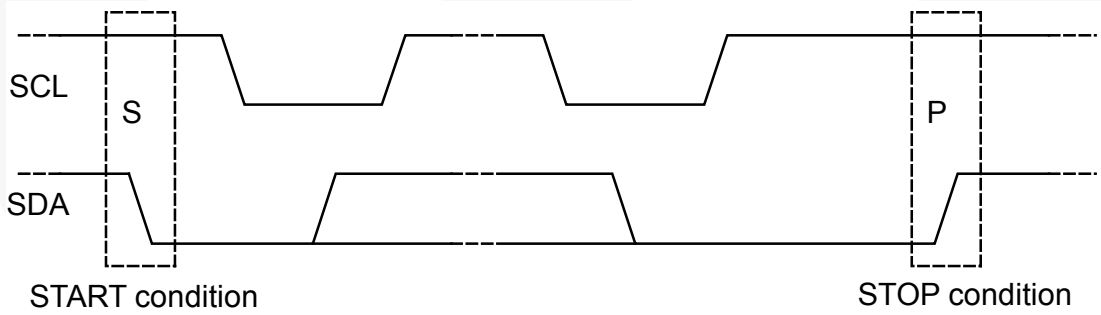

Figure 5. Definition of START and STOP conditions

Acknowledge

The number of data bytes transferred between the START and STOP conditions from transmitter to receiver is unlimited. Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a high-level signal put on the bus by the transmitter, during which the master generates an extra acknowledge-related clock pulse. A slave receiver must generate an acknowledge (ACK) after the reception of each byte. A master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledges must pull down the SDA line during the acknowledge clock pulse so the SDA line is stable LOW during the HIGH period of the acknowledge-related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

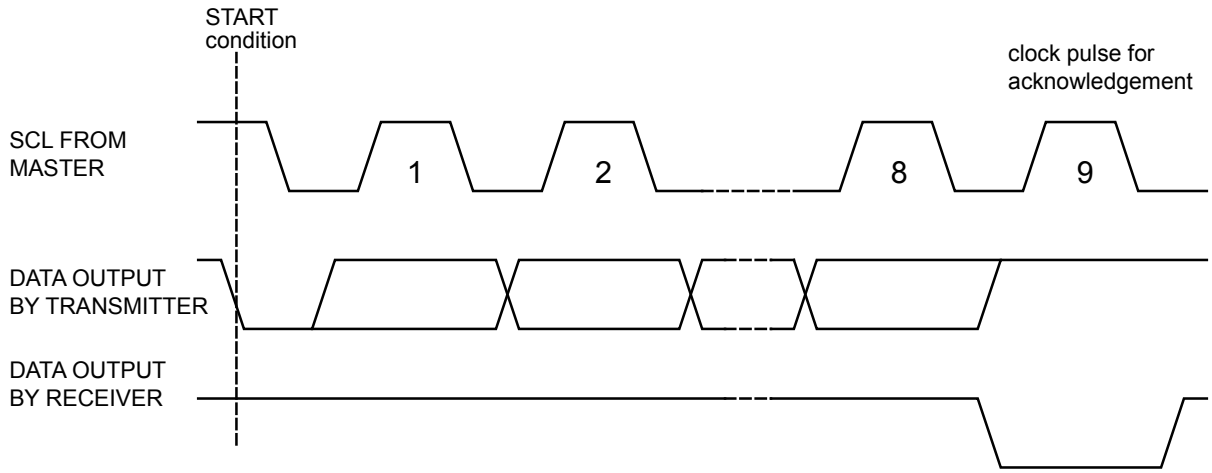

Figure 6. Acknowledgement on the I²C Bus®

I²C Bus Protocol

Before any data is transmitted on the I²C Bus, the device that should respond is addressed first. The addressing is always carried out with the first byte transmitted after the START procedure. The I²C bus configuration for a data write to the FMS6501 is shown in Figure 7.

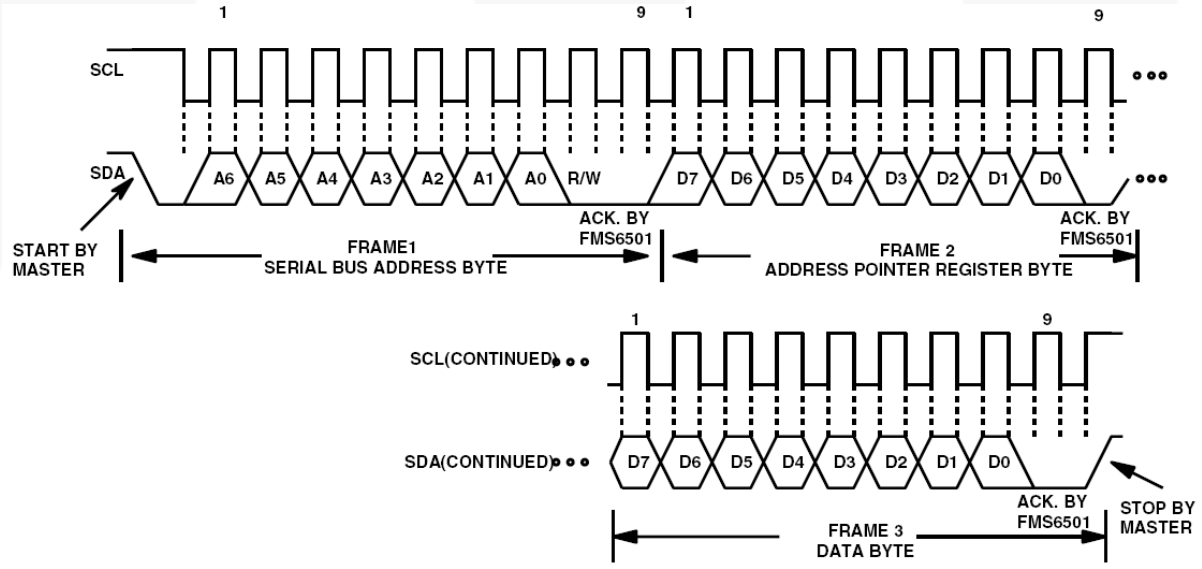

Figure 7. Write a Register Address to the Pointer Register, Then Write Data to the Selected Register

Applications Information

Input Clamp / Bias Circuitry

The FMS6501A accommodates AC- or DC-coupled inputs. Internal clamping and bias circuitry are provided to support AC-coupled inputs. These are selectable through the CLMP bits via the I^2C compatible interface.

For DC-coupled inputs, the device should be programmed to use the bias input configuration. In this configuration, the input is internally biased to 625 mV through a 100 kΩ resistor. Distortion is optimized with the output levels set between 250 mV above ground and 500 mV below the power supply. These constraints, along with the desired channel gain, need to be considered when configuring the input signal levels for input DC coupling.

With AC-coupled inputs, the FMS6501A uses a simple clamp rather than a full DC-restore circuit. For video signals with and without sync (Y, CV, R, G, B); the lowest voltage at the output pins is clamped to ~300 mV above ground when the 6dB gain setting is selected.

If symmetric AC-coupled input signals are used (Chroma, Pb, Pr, Cb, Cr), the bias circuit described above can be used to center them within the input common range. The average DC value at the output is approximately 1.27 V with a 6 dB gain setting. This value changes, depending upon the selected gain setting, as shown in Table 5.

Table 5. Common Mode Voltage

Gain Setting	Clamp Voltage	Bias Voltage
6dB	300 mV	1.27 V
7dB	330 mV	1.43 V
8dB	370 mV	1.60 V
9dB	420 mV	1.80 V

Figure 8 shows the clamp-mode input circuit and the internally controlled voltage at the input pin for AC-coupled inputs.

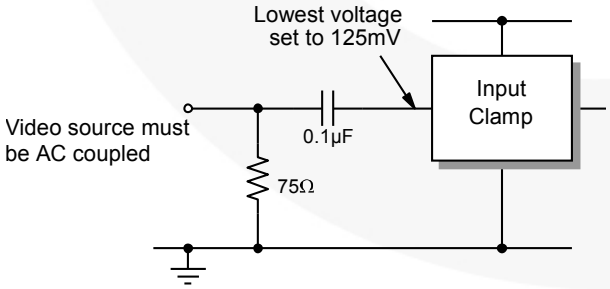

Figure 8. Clamp Mode Input Circuit

Figure 9 shows the bias mode input circuit and internally controlled voltage at the input pin for AC-coupled inputs.

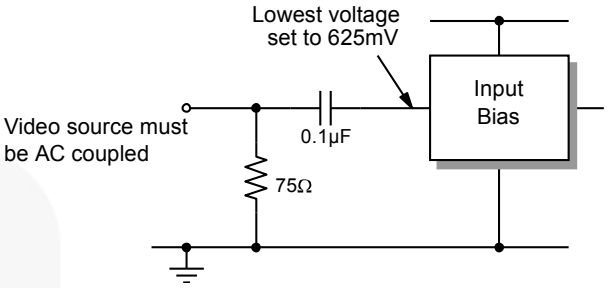

Figure 9. Bias Mode Input Circuit

Output Configuration

The FMS6501A outputs may be either AC or DC coupled. Resistive output loads can be as low as 75 Ω, representing a dual doubly terminated video load. High impedance capacitive loads of up to 20 pF can be driven without loss of signal integrity. For standard 75 Ω video loads, a 75 Ω matching resistor should be placed in series to allow for a doubly terminated load. DC-coupled outputs should be connected as shown in Figure 10.

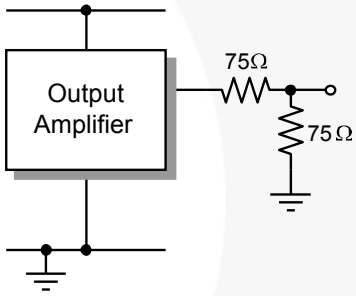

Figure 10. DC-Coupled Load Connection

If multiple low-impedance loads are DC coupled, increased power and thermal issues need to be addressed. In this case, the use of a multilayer board with a large ground plane is recommended to help dissipate heat. If a two-layer board is used under these conditions, an extended ground plane directly under the device is recommended. This plane should extend at least 12.7 mm (0.5 inches) beyond the device. PC board layout issues are discussed in the Layout Considerations section.

AC-coupled loads should be configured as in shown in Figure 11.

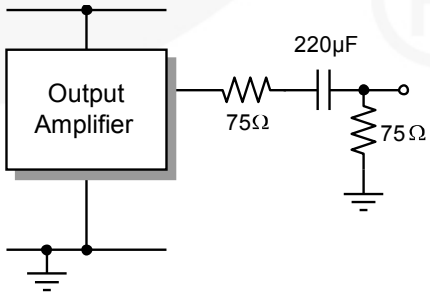

Figure 11. AC-Coupled Load Connection

Thermal issues are reduced with AC-coupled outputs, eliminating special PC layout requirements.

Each of the outputs can be independently powered down and placed in a high-impedance state with the ENABLE bit. This function can be used to mute video signals, to parallel multiple FMS6501A outputs, or to save power. When the output amplifier is disabled, the high-impedance output presents a 3 kΩ load to ground. The output amplifier typically enters and recovers from the power-down state in less than 300 ns after being programmed.

When an output channel is not connected to an input, the input to that channel's amplifier is forced to ~150mV. The output amplifier is active unless specifically disabled by the I^2C interface. Voltage output levels depend on the programmed gain for the channel.

Crosstalk

Crosstalk is an important consideration: input and output crosstalk represent the two major coupling modes in a typical application. Input crosstalk is crosstalk in the input pins and switches when the interfering signal drives an open switch. It is dominated by inductive coupling in the package lead frame between adjacent leads. It decreases rapidly as the interfering signal moves farther away from the pin adjacent to the input signal selected. Output crosstalk is coupling from one driven output to another active output. It decreases with increasing load impedance, as it is caused mainly by ground and power coupling between output amplifiers. If a signal is driving an open switch, its crosstalk is mainly input crosstalk. If it is driving a load through an active output, its crosstalk is mainly output crosstalk.

Input and output crosstalk measurements are performed with the test configuration shown in Figure 12.

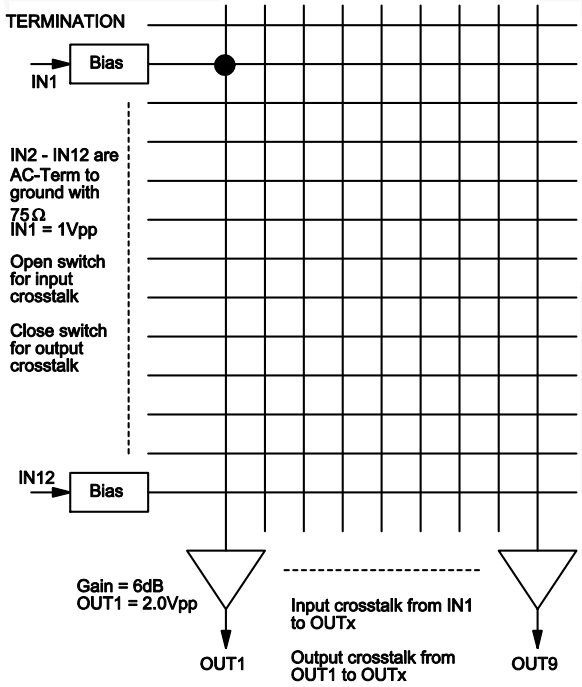

Figure 12. Test Configuration for Crosstalk

For input crosstalk, the switch is open. All inputs are in bias mode. Channel 1 input is driven with a 1 V_{PP} signal, while all other inputs are AC terminated with 75 Ω. All outputs are enabled and crosstalk is measured from IN1 to any output. For output crosstalk, the switch is closed. Crosstalk from OUT1 to any output is measured.

Crosstalk from multiple sources into a given channel has been measured with the setup shown in Figure 13. Input IN1 is driven with a 1 V_{PP} pulse source and is connected to outputs Out1 to Out8. Input In9 is driven with a secondary, asynchronous, gray-field video signal, and is connected to Out9. All other inputs are AC terminated with 75 Ω. Crosstalk effects on the gray field are measured and calculated with respect to a standard 1 V_{PP} output measured at the load.

If not all inputs and outputs are needed, avoid using adjacent channels, where possible, to reduce crosstalk. Disable all unused channels to further reduce crosstalk and power dissipation.

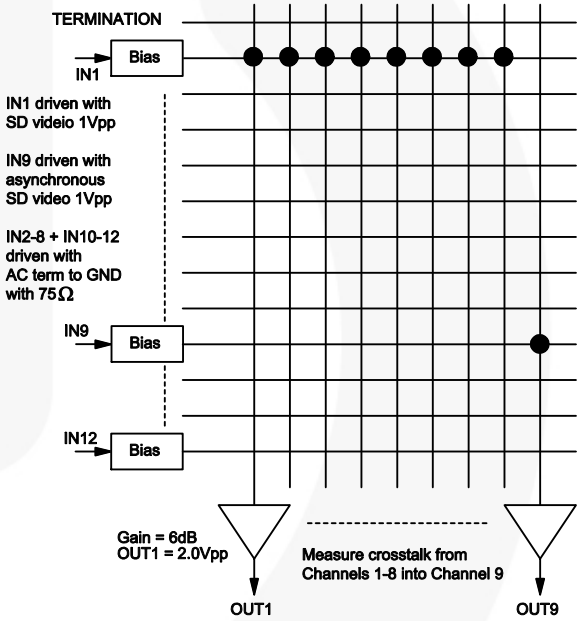

Figure 13. Test Configuration for Multi-Channel Crosstalk

Layout Considerations

General layout and supply bypassing play major roles in high-frequency performance and thermal characteristics. Fairchild offers a demonstration board, FMS6501ADEMO, to use as a guide for layout and to aid in device testing and characterization. The FMS6501ADEMO is a four-layer board with a full power and ground plane. For optimum results, follow the steps below as a basis for high frequency layout.

- Include 10 µF and 0.1 µF bypass capacitors.
- Place the 10 µF capacitor within 19.05 mm (0.75 inches) of the power pin.
- Place the 0.1 µF capacitor within 2.7 mm (0.1 inches) of the power pin.
- Connect all external ground pins as tightly as possible, preferably with a large ground plane under the package.
- Place channel connections to reduce mutual trace inductance.
- Minimize all trace lengths to reduce series inductances. If routing across a board, place device such that longer traces are at the inputs rather than the outputs.

If using multiple, low-impedance, DC-coupled outputs; special layout techniques may be employed to help dissipate heat.

If a multilayer board is used, a large ground plane directly under the device helps reduce package case temperature.

For dual-layer boards, an extended plane can be used.

Worst-case, additional die power due to DC loading can be estimated at ($V_{CC2}/4R_L$) per output channel. This assumes a constant DC output voltage of $V_{CC}/2$. For 5 V V_{CC} with a dual-DC video load, add 25 / (4x75) = 83 mW, per channel.

Video Switch Matrix Applications

The increased demand for consumer multimedia systems has created a challenge for system designers to provide cost-effective solutions to capitalize on the growth potential in graphics display technologies. These applications require cost-effective video switching and filtering solutions to deploy high-quality display technologies rapidly and effectively to the target audience. Areas of specific interest include HDTV, media centers, and automotive “infotainment” (includes navigation, in-cabin entertainment, and back-up camera). In all cases, the advantages an integrated video switch matrix provides are high-quality video switching specific to the application as well as video input clamps and on-chip low-impedance output cable drivers with switchable gain.

Generally the largest application for a video switch is for the front end of an HDTV, where it takes multiple inputs and routes them to appropriate signal paths (main picture and Picture-in-Picture (PiP)). These are normally routed into ADCs followed by decoders. There are many different technologies for HDTV; including LCD, plasma, and CRT, with similar analog switching circuitry.

An example of a HDTV application is shown in Figure 14. This system combines a video switch matrix and two three-channel switchable anti-aliasing filters. There are two three-channel signal paths in the system; one for the main picture, the other for PiP.

VIPDEMO™ Control Software

The FMS6501A is configured via an I^2C-compatible digital interface. To facilitate demonstration, Fairchild Semiconductor had developed the VIPDEMO™ GUI-based control software to write to the register map. This software is included in the FMS6501ADEMO kit. A parallel port I^2C adapter and an interface cable to connect to the board are also included. Besides using the full interface, the VIPDEMO can also be used to control single-register read and writes for I^2C.

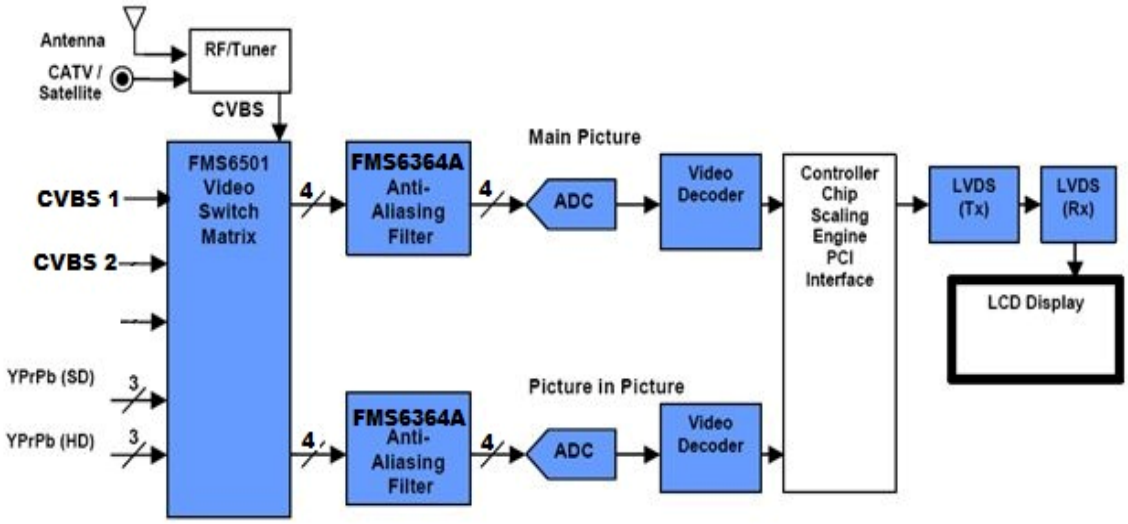

Figure 14. HDTV Application Using the FMS6501A Video Switch Matrix

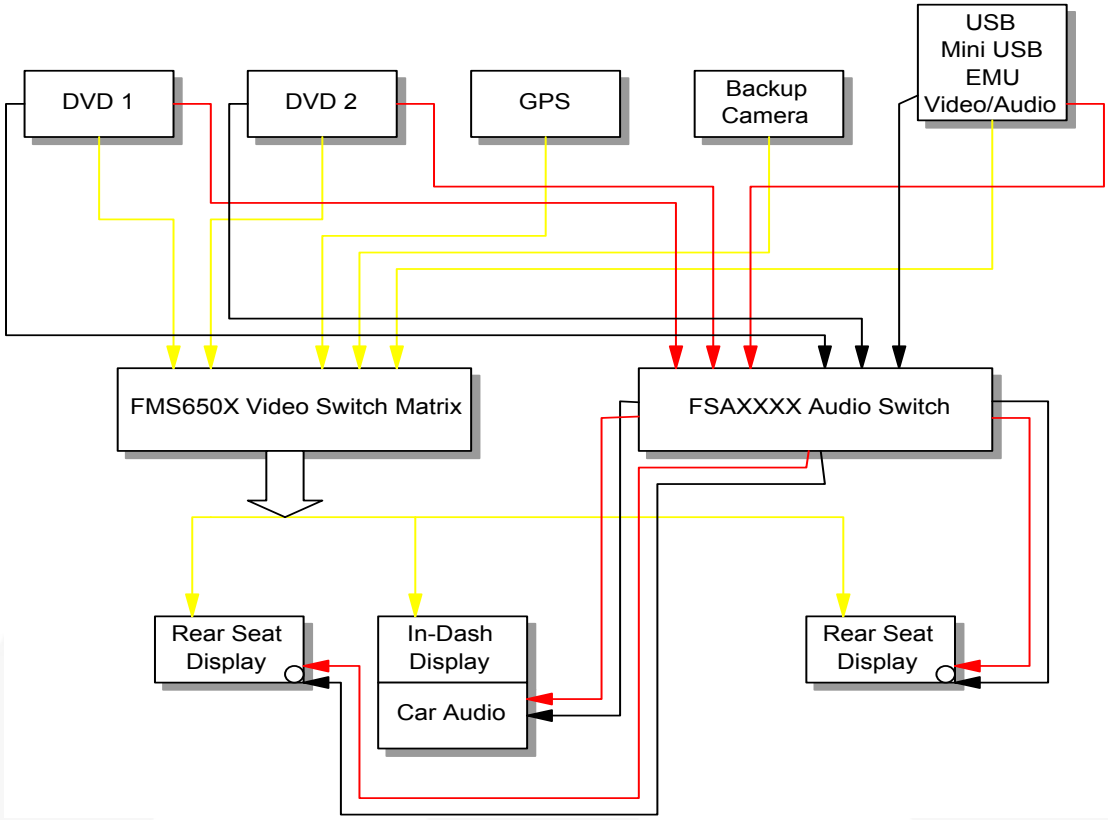

Figure 15. Example of an In-Cabin System

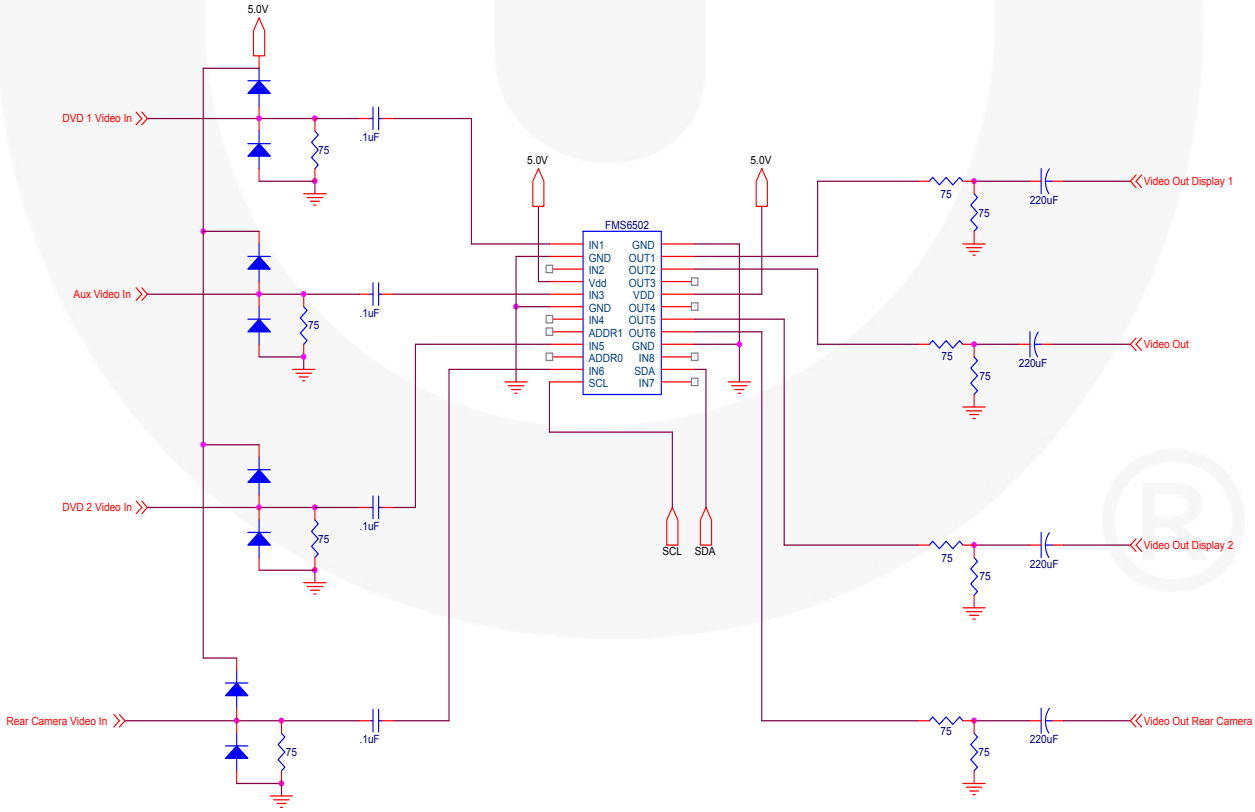

Figure 16. Schematic of an In-Cabin System

Physical Dimensions

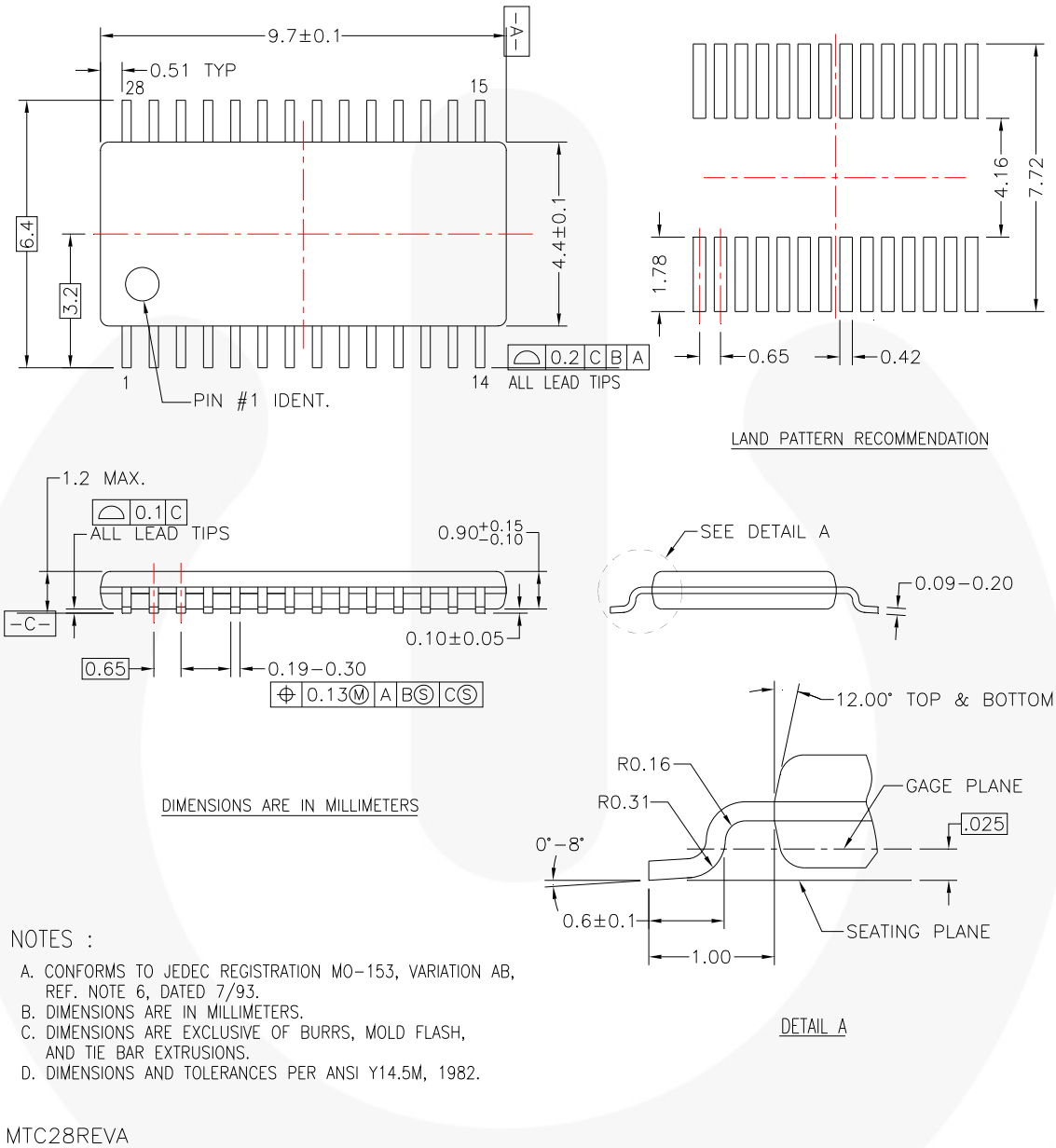

Figure 17. 28-Lead, Thin-Shrink Small-Outline Package (TSSOP), JEDEC MO-153, 4.4 mm Wide

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