UCD7201 Digital Control Compatible Dual Low-Side ±4 Amp MOSFET Drivers with Programmable Common Current Sense

1 Features

- Adjustable Current Limit Protection
- 3.3-V, 10-mA Internal Regulator
- DSP/µC Compatible Inputs
- Dual ±4-A TrueDrive™ High Current Drivers
- 10-ns Typical Rise and Fall Times with 2.2-nF Loads
- 20-ns Input-to-Output Propagation Delay
- 25-ns Current Sense-to-Output Propagation Delay
- Programmable Current Limit Threshold
- Digital Output Current Limit Flag
- 4.5-V to 15-V Supply Voltage Range
- Rated from -40°C to 105°C

2 Applications

- Digitally Controlled Power Supplies
- DC/DC Converters
- Motor Controllers
- Line Drivers

3 Description

The UCD7201 is a member of the UCD7K family of digital control compatible drivers for applications utilizing digital control techniques or applications requiring fast local peak current limit protection.

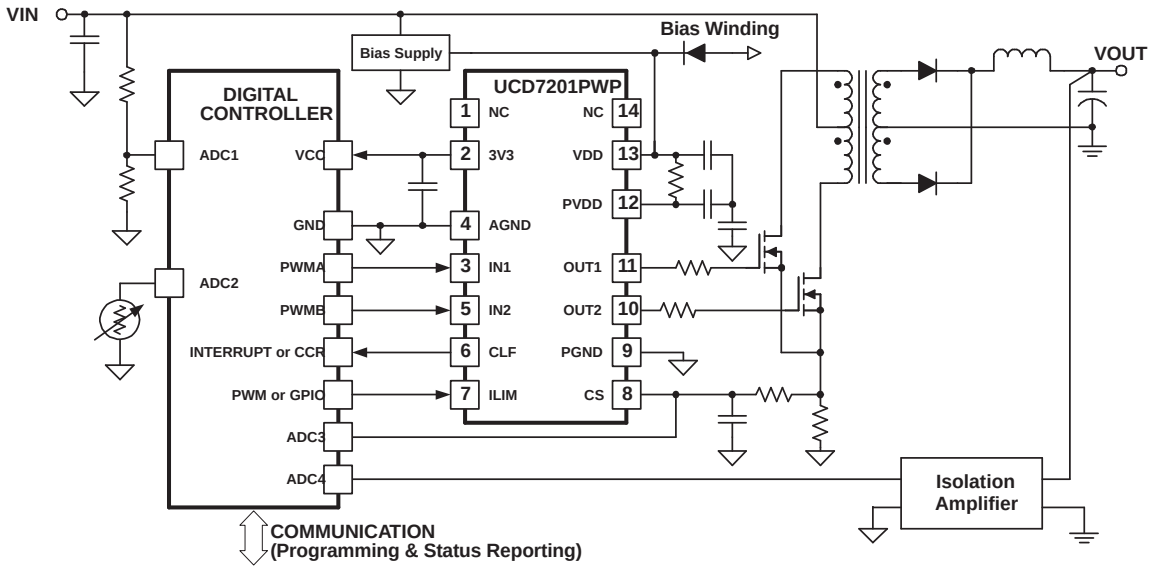
The UCD7201 includes dual low-side ±4-A high-current MOSFET gate drivers. It allows the digital power controllers such as UCD9110 or UCD9501 to interface to the power stage in double ended topologies. It provides a cycle-by-cycle current limit function for both driver channels, a programmable threshold and a digital output current limit flag which can be monitored by the host controller. With a fast cycle-by-cycle current limit protection, the driver can turn off the power stage in the event of an overcurrent condition.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
UCD7201	HTSSOP (14)	4.40 mm x 5.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Typical Application Diagram (Push-Pull Converter)



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

DATE	REVISION	CHANGE DESCRIPTION
March 2005	SLUS645	Initial release of preliminary datasheet.
April 2005	SLUS645A	Updated packaging information.
July 2005	SLUS645B	Initial release of production datasheet. Updated specification and application information.
October 2014	SLUS645F	Added Handling Rating table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section.

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5 Description (Continued)

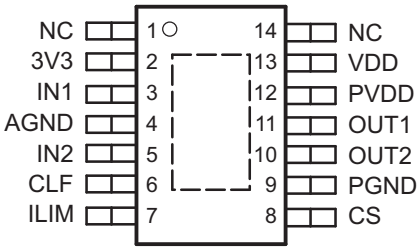
For fast switching speeds, the UCD7201 output stages use the TrueDrive™ output architecture, which delivers rated current of ±4 A into the gate of a MOSFET during the Miller plateau region of the switching transition. It also includes a 3.3-V, 10-mA linear regulator to provide power to the digital controller.

For similar applications requiring direct start-up capability from higher voltages such as the 48-V telecom input line, the UCD7601 includes a 110-V high-voltage startup circuit.

The UCD7K driver family is compatible with standard 3.3-V I/O ports of DSPs, Microcontrollers, or ASICs. UCD7201 is offered in a PowerPAD™ HTSSOP-14 package.

6 Pin Configuration and Functions

PWP
14 PIN
Top View



NC − No internal connection

Pin Functions

PIN		I/O	FUNCTION
NO.	NAME		
1	NC	-	No Connection
2	3V3	O	Regulated 3.3-V rail. The onboard linear voltage regulator is capable of sourcing up to 10 mA of current. Place 0.22 µF of ceramic capacitance from this pin to ground.
3	IN1	I	The IN pin is a high impedance digital input capable of accepting 3.3-V logic level signals up to 2 MHz. There is an internal Schmitt trigger comparator which isolates the internal circuitry from any external noise.
4	AGND	-	Analog ground return.
5	IN2	I	The IN pin is a high impedance digital input capable of accepting 3.3-V logic level signals up to 2 MHz. There is an internal Schmitt trigger comparator which isolates the internal circuitry from any external noise.
6	CLF	O	Current limit flag. When the CS level is greater than the ILIM voltage minus 25 mV, the output of the driver is forced low and the current limit flag (CLF) is set high. The CLF signal is latched high until the device receives the next rising edge on the IN pin.
7	ILIM	I	Current limit threshold set pin. The current limit threshold can be set to any value between 0.25 V and 1.0 V. The default value while open is 0.5 V.
8	CS	I	Current sense pin. Fast current limit comparator connected to the CS pin is used to protect the power stage by implementing cycle-by-cycle current limiting.
9	PGND	-	Power ground return. The pin should be connected very closely to the source of the power MOSFET.
10	OUT2	O	The high-current TrueDrive™ driver output.
11	OUT1	O	The high-current TrueDrive™ driver output.
12	PVDD	I	Supply pin provides power for the output drivers. It is not connected internally to the VDD supply rail. The bypass capacitor for this pin should be returned to PGND.
13	VDD	I	Supply input pin to power the driver. The UCD7K devices accept an input range of 4.5 V to 15 V. Bypass the pin with at least 4.7 µF of capacitance, returned to AGND.
14	NC	-	No Connection.

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7 Specifications

7.1 Absolute Maximum Ratings[(1) (2)]

			MIN	MAX	UNIT
V_{DD}	Supply Voltage			16	V
I_{DD}	Supply Current	Quiescent		20	mA
		Switching, T_A = 25°C, , T_J = 125°C, V_{DD} = 12 V		200	
V_{OUT}	Output Gate Drive Voltage	OUT	–1	PVDD	V
$I_{OUT(sink)}$	Output Gate Drive Current	OUT		4.0	A
$I_{OUT(source)}$				–4.0	
	Analog Input	ISET, CS	–0.3	3.6	V
		ILIM	–0.3	3.6	
	Digital I/O's	IN, CLF	–0.3	3.6	
	Power Dissipation	T_A = 25°C (PWP-14 package), T_J = 125°C		2.67	W
T_J	Junction Operating Temperature	UCD7201	–55	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to GND. Currents are positive into, negative out of the specified terminal.

7.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		–65	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[(1)]		2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[(2)]		500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	TYP	MAX	UNIT
Supply Voltage, VDD	4.25	12	14.5	V
Supply bypass capacitance	1			µF
Reference bypass capacitance	0.22			
Operating junction temperature	–40		105	°C

7.4 Thermal Information

THERMAL METRIC[(1)]		UCD7201 PWP 14 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	50.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	31.8	
$R_{\theta JB}$	Junction-to-board thermal resistance	27.8	
ψ_{JT}	Junction-to-top characterization parameter	1.2	
ψ_{JB}	Junction-to-board characterization parameter	27.6	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	4.1	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

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7.5 Electrical Characteristics

V_{DD} = 12 V, 4.7-µF capacitor from V_{DD} to GND, 0.22µF from 3V3 to AGND, T_A = T_J = -40°C to 105°C, (unless otherwise noted).

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY SECTION					
Supply current, OFF	V_{DD} = 4.2 V	-	200	400	µA
Supply current	Outputs not switching IN = LOW	-	1.5	2.5	mA
LOW VOLTAGE UNDERVOLTAGE LOCKOUT					
VDD UVLO ON		4.25	4.5	4.75	V
VDD UVLO OFF		4.05	4.25	4.45	
VDD UVLO hysteresis		150	250	350	mV
REFERENCE / EXTERNAL BIAS SUPPLY					
3V3 initial set point	T_A = 25°C, I_{LOAD} = 0	3.267	3.3	3.333	V
3V3 set point over temperature		3.234	3.3	3.366	
3V3 load regulation	I_{LOAD} = 1 mA to 10 mA, VDD = 5 V	-	1	6.6	mV
3V3 line regulation	VDD = 4.75 V to 12 V, I_{LOAD} = 10 mA	-	1	6.6	
Short circuit current	VDD = 4.75 to 12 V	11	20	35	mA
3V3 OK threshold, ON	3.3 V rising	2.9	3.0	3.1	V
3V3 OK threshold, OFF	3.3 V falling	2.7	2.8	2.9	
INPUT SIGNAL					
HIGH, positive-going input threshold voltage (VIT+)		1.65	-	2.08	V
LOW negative-going input threshold voltage (VIT-)		1.16	-	1.5	
Input voltage hysteresis, (VIT+ - VIT-)		0.6	-	0.8	
Frequency		-	-	2	MHz
CURRENT LIMIT (ILIM)					
ILIM internal current limit threshold	I_{LIM} = OPEN	0.51	0.55	0.58	V
ILIM maximum current limit threshold	I_{LIM} = 3.3 V	1.05	1.10	1.15	
ILIM current limit threshold	I_{LIM} = 0.75 V	0.700	0.725	0.750	
ILIM minimum current limit threshold	I_{LIM} = 0.25 V	0.21	0.23	0.25	
CLF output high level	CS > I_{LIM} , I_{LOAD} = -7 mA	2.64	-	-	
CLF output low level	CS ≤ I_{LIM}, I_{LOAD} = 7 mA	-	-	0.66	
Propagation delay from IN to CLF	IN rising to CLF falling after a current limit event	-	10	20	ns
CURRENT SENSE COMPARATOR					
Bias voltage	Includes CS comp offset	5	25	50	mV
Input bias current		-	–1	-	µA
Propagation delay from CS to OUTx	I_{LIM} = 0.5 V, measured on OUTx, CS = threshold + 60 mV	-	25	40	ns
Propagation delay from CS to CLF	I_{LIM} = 0.5 V, measured on CLF, CS = threshold + 60 mV	-	25	50	
CURRENT SENSE DISCHARGE TRANSISTOR					
Discharge resistance	IN = low, resistance from CS to AGND	10	35	75	Ω
OUTPUT DRIVERS					
Source current	VDD = 12 V, IN = high, OUTx = 5 V		4		A
Sink current	VDD = 12 V, IN = low, OUTx = 5 V		4		
Source current	VDD = 4.75 V, IN = high, OUTx = 0		2		
Sink current	VDD = 4.75 V, IN = low, OUTx = 4.75 V		3		
Rise time, t_R	C_{LOAD}= 2.2 nF, VDD = 12 V		10	20	ns
Fall time, t_F	C_{LOAD} = 2.2 nF, VDD = 12 V		10	15	
Output with VDD < UVLO	VDD =1.0 V, I_{SINK} = 10 mA		0.8	1.2	V

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Electrical Characteristics (continued)

V_{DD} = 12 V, 4.7-µF capacitor from V_{DD} to GND, 0.22µF from 3V3 to AGND, T_A = T_J = -40°C to 105°C, (unless otherwise noted).

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Propagation delay from IN to OUT1, t_{D1}	C_{LOAD} = 2.2 nF, VDD = 12 V, CLK rising		20	35	ns
Propagation delay from IN to OUT2, t_{D2}	C_{LOAD} = 2.2 nF, VDD = 12 V, CLK falling		20	35	

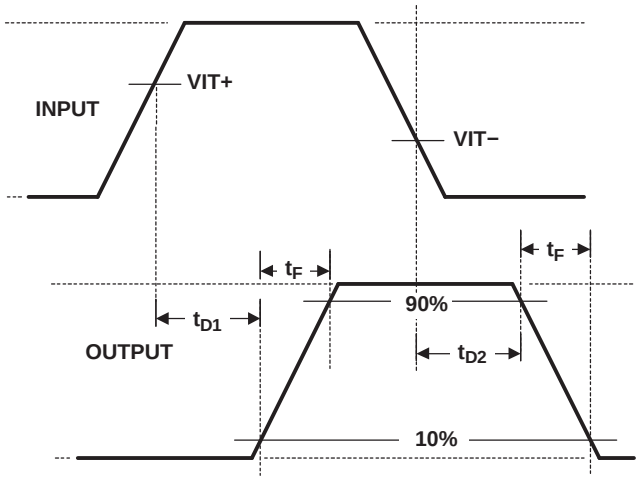

Figure 1. Timing Diagram

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7.6 Typical Characteristics

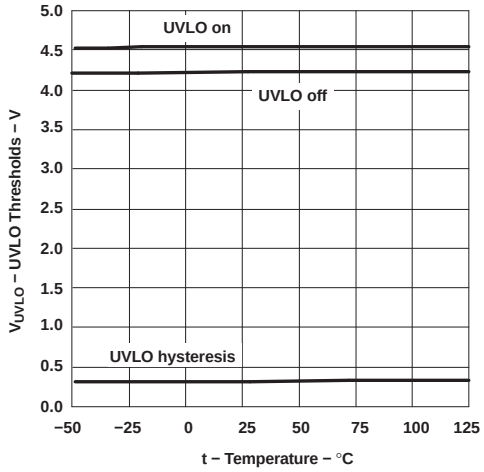

Figure 2. UVLO Thresholds vs Temperature

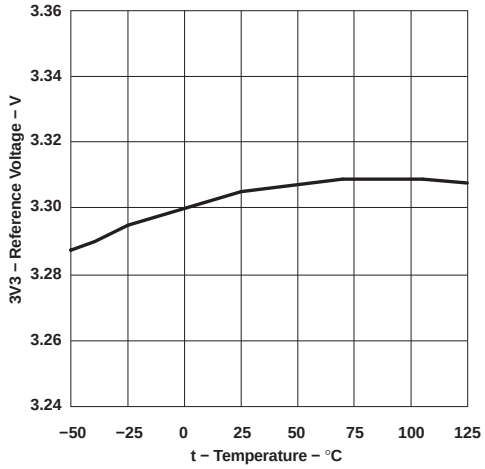

Figure 3. 3V3 Reference Voltage vs Temperature

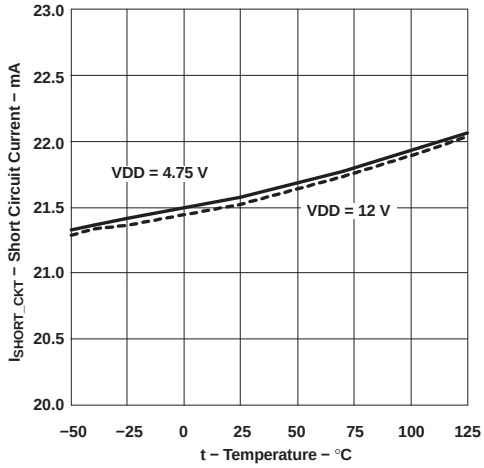

Figure 4. 3V3 Short Circuit Current vs Temperature

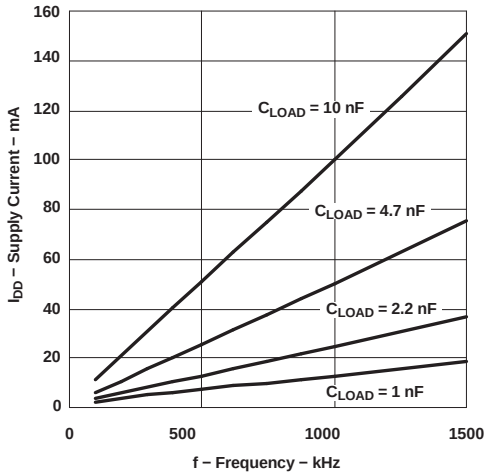

Figure 5. Supply Current vs Frequency (V_{DD} = 5 V)

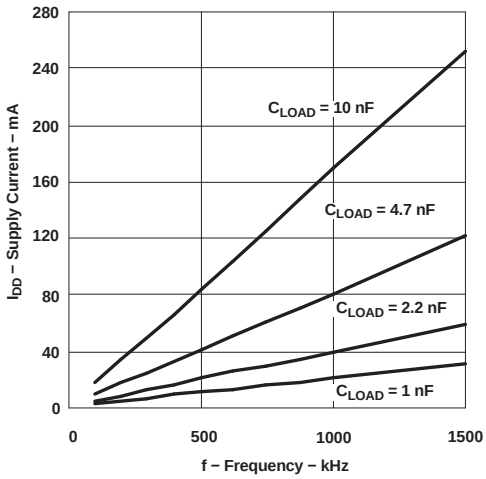

Figure 6. Supply Current vs Frequency (V_{DD} = 8 V)

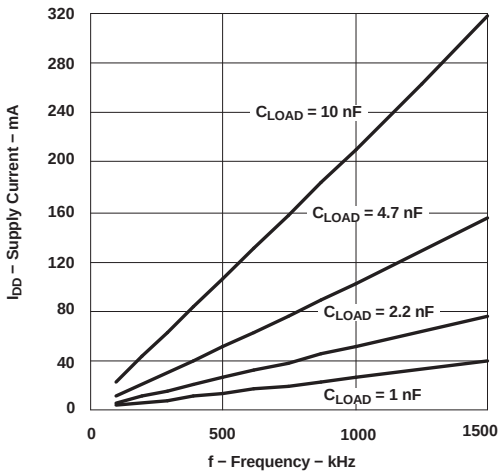

Figure 7. Supply Current vs Frequency (V_{DD} = 10 V)

Typical Characteristics (continued)

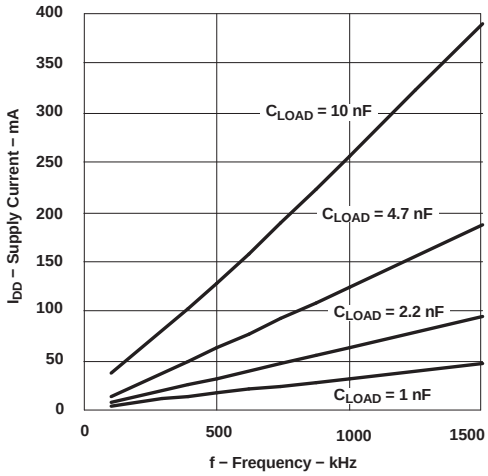

Figure 8. Supply Current vs Frequency (V_{DD} = 12V)

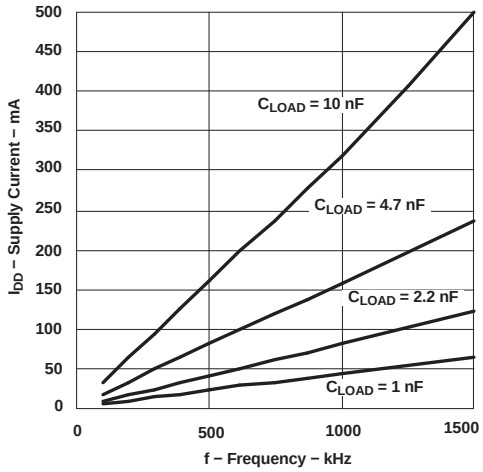

Figure 9. Supply Current vs Frequency (V_{DD} = 15 V)

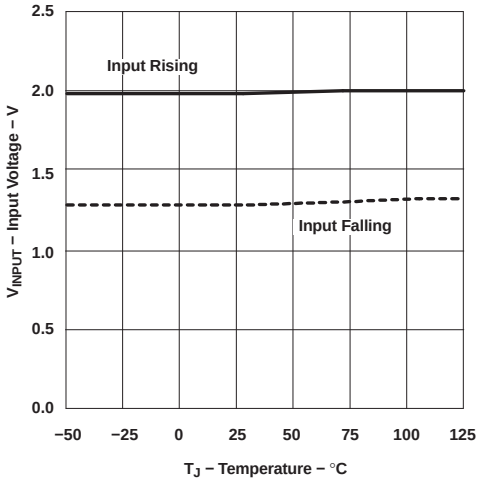

Figure 10. Input Thresholds vs Temperature

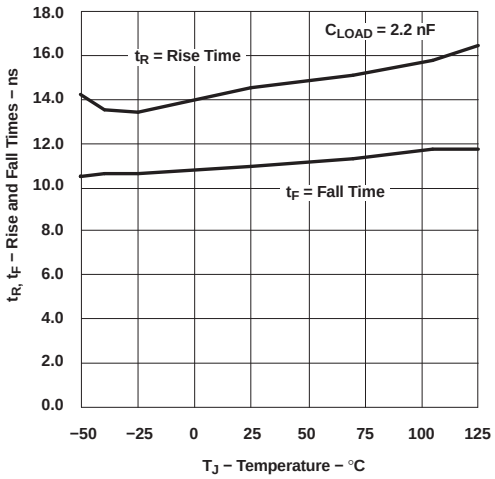

Figure 11. Output Rise Time and Fall Time vs Temperature (V_{DD} = 12 V)

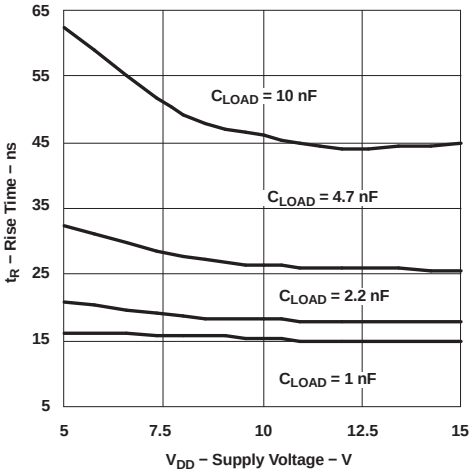

Figure 12. Rise Time vs Supply Voltage

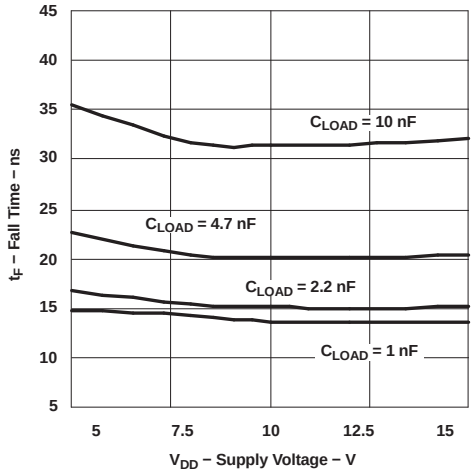

Figure 13. Fall Time vs Supply Voltage

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Typical Characteristics (continued)

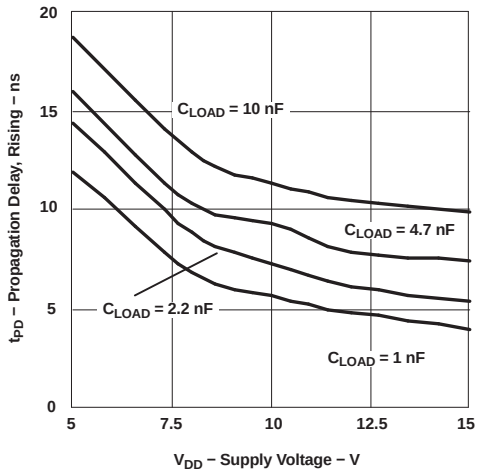

Figure 14. IN to OUTx Propagation Delay Rising vs Supply Voltage

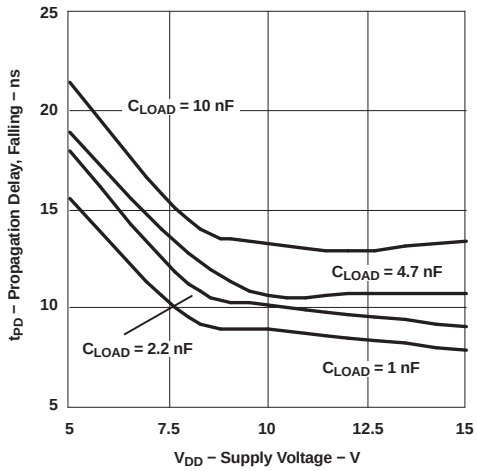

Figure 15. IN to OUTx Propagation Delay Falling vs Supply Voltage

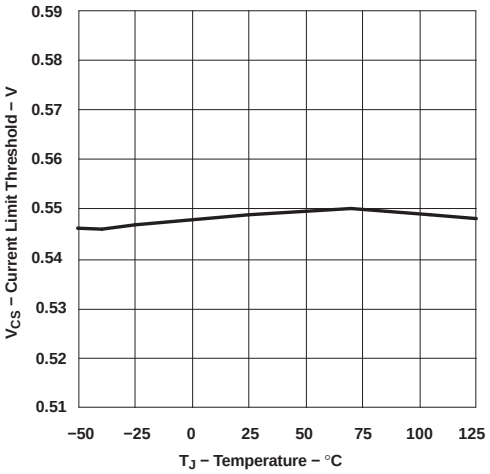

Figure 16. Default Current Limit Threshold vs Temperature

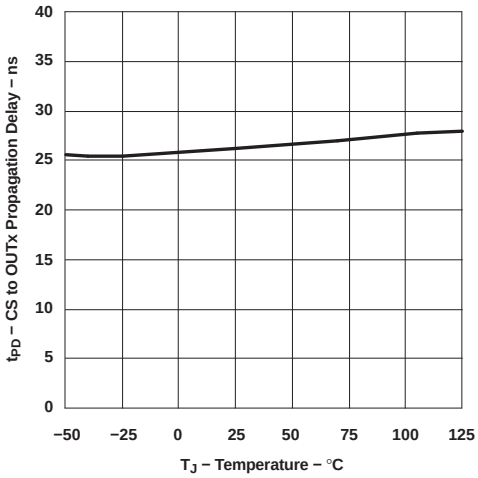

Figure 17. CS to OUTx Propagation Delay vs Temperature

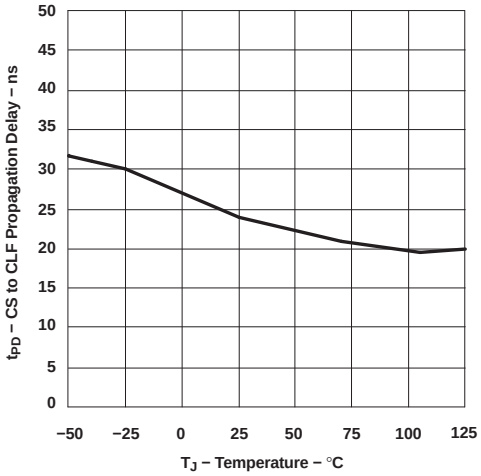

Figure 18. CS to CLF Propagation Delay vs Temperature

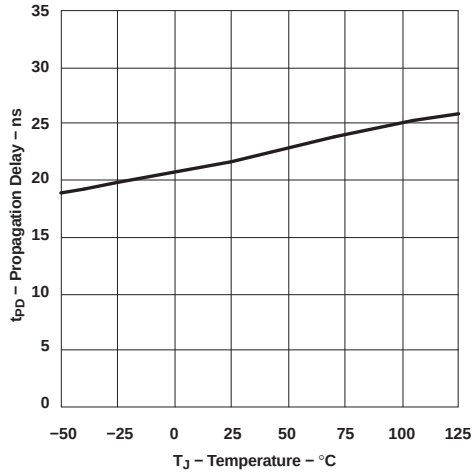

Figure 19. IN to OUT Propagation Delay vs Temperature

Typical Characteristics (continued)

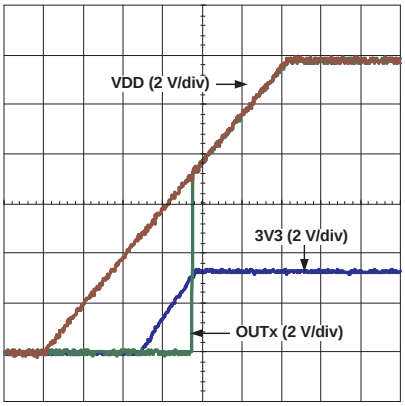

Figure 20. Start-Up Behavior at V_{DD} = 12 V (Input Tied to 3V3)

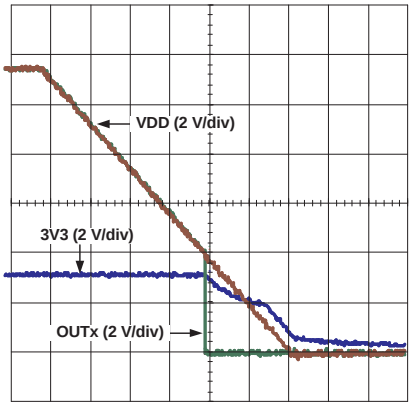

Figure 21. Shut Down Behavior at V_{DD} = 12 V (Input Tied to 3V3)

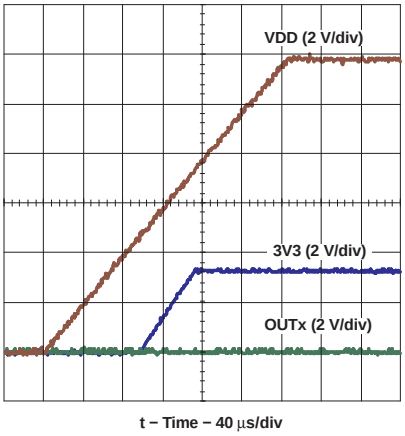

Figure 22. Start-Up Behavior at V_{DD} = 12 V (Input Shortened to GND)

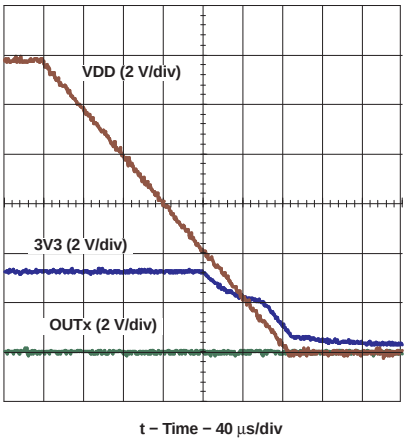

Figure 23. Shut Down Behavior at V_{DD} = 12 V (Input Shortened to GND)

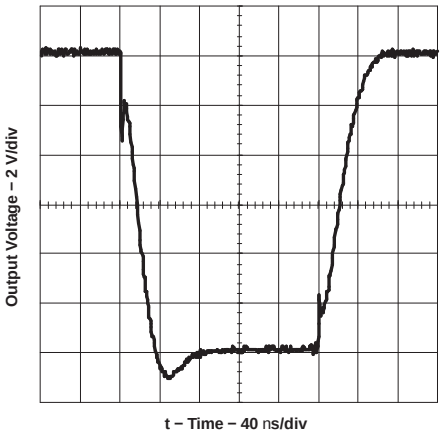

Figure 24. Output Rise and Fall Time (V_{DD} = 12 V, C_{LOAD} = 10 nF)

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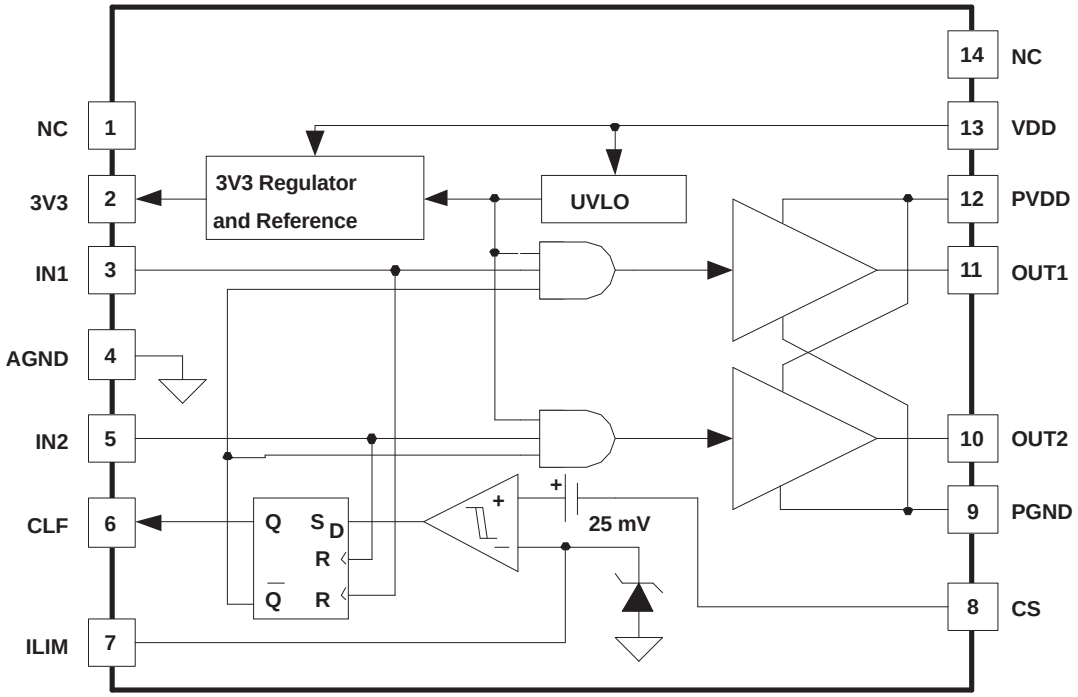
8 Detailed Description

8.1 Overview

The UCD7201 is a member of the UCD7K family of digital control compatible drivers for applications utilizing digital control techniques or applications requiring fast local peak current limit protection.

The UCD7201 is a low-side ±4-A high-current MOSFET gate driver. It allows the digital power controllers such as UCD9110 or UCD9501 to interface to the power stage in double ended topologies. It provides a cycle-by-cycle current limit function for both driver channels, a programmable threshold and a digital output current limit flag which can be monitored by the host controller. With a fast cycle-by-cycle current limit protection, the driver can turn off the power stage in the event of an overcurrent condition.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Reference / External Bias Supply

All devices in the UCD7K family are capable of supplying a regulated 3.3-V rail to power various types of external loads such as a microcontroller or an ASIC. The onboard linear voltage regulator is capable of sourcing up to 10 mA of current. For normal operation, place 0.22-µF of ceramic capacitance between the 3V3 pin to the AGND pin.

8.3.2 Input Pin

The input pins are high impedance digital inputs capable of accepting 3.3-V logic level signals up to 2 MHz. There is an internal Schmitt Trigger comparator which isolates the internal circuitry from any external noise.

If limiting the rise or fall times to the power device is desired then an external resistance may be added between the output of the driver and the load device, which is generally the gate of a power MOSFET.

8.3.3 Current Sensing and Protection

A very fast current limit comparator connected to the CS pin is used to protect the power stage by implementing cycle-by-cycle current limiting.

Feature Description (continued)

The current limit threshold may be set to any value between 0.25 V and 1.0 V by applying the desired threshold voltage to the current limit (ILIM) pin. If the ILIM pin is left floating, the internal current limit threshold will be 0.5 volts. When the CS level is greater than the I_{LIM} voltage minus 25 mV, the output of the driver is forced low and the current limit flag (CLF) is set high. The CLF signal is latched high until the device receives the next rising edge on either of the IN pins.

When the CS voltage is below I_{LIM}, the driver output follows the PWM input. The CLF digital output flag can be monitored by the host controller to determine when a current limit event occurs and to then apply the appropriate algorithm to obtain the desired current limit profile (i.e. straight time, fold back, hickup or latch-off).

A benefit of this local protection feature is that the UCD7K devices can protect the power stage if the software code in the digital controller becomes corrupted. If the controller's PWM output stays high, the local current sense circuit turns off the driver output when an over-current event occurs. The system would then likely go into retry mode because most DSP and microcontrollers have on-board watchdog, brown-out, and other supervisory peripherals to restart the device in the event that it is not operating properly. But these peripherals typically do not react fast enough to save the power stage. The UCD7K's local current limit comparator provides the required fast protection for the power stage.

The CS threshold is 25 mV below the I_{LIM} voltage. If the user attempts to command zero current while the CS pin is at ground the CLF flag will latch high until the IN pin receives a pulse. At start-up it is necessary to ensure that the ILIM pin will always be greater than the CS pin for the handshaking to work as described below. If for any reason the CS pin comes to within 25 mV of the ILIM pin during start-up, then the CLF flag will be latched high and the digital controller must poll the UCD7K device, by sending it a narrow IN pulse. If a fault condition is not present the IN pulse will reset the CLF signal to low indicating that the UCD7K device is ready to process power pulses.

8.3.4 Handshaking

The UCD7K family of devices have a built-in handshaking feature to facilitate efficient start-up of the digitally controlled power supply. At start-up the CLF flag is held high until all the internal and external supply voltages of the UCD7K device are within their operating range. Once the supply voltages are within acceptable limits, the CLF goes low and the device will process input drive signals. The micro-controller should monitor the CFL flag at start-up and wait for the CLF flag to go LOW before sending power pulses to the UCD7K device.

8.3.5 Driver Output

The high-current output stage of the UCD7K device family is capable of supplying ±4-A peak current pulses and swings to both PVDD and PGND. The driver outputs follow the state of the IN pin provided that the VDD and 3V3 voltages are above their respective under-voltage lockout threshold.

The drive output utilizes Texas Instruments' TrueDrive™ architecture, which delivers rated current into the gate of a MOSFET when it is most needed, during the Miller plateau region of the switching transition providing efficiency gains.

TrueDrive™ consists of pullup pulldown circuits with bipolar and MOSFET transistors in parallel. The peak output current rating is the combined current from the bipolar and MOSFET transistors. This hybrid output stage also allows efficient current sourcing at low supply voltages.

Each output stage also provides a very low impedance to overshoot and undershoot due to the body diode of the external MOSFET. This means that in many cases, external-schottky-clamp diodes are not required.

8.3.6 Source/Sink Capabilities During Miller Plateau

Large power MOSFETs present a large load to the control circuitry. Proper drive is required for efficient, reliable operation. The UCD7K drivers have been optimized to provide maximum drive to a power MOSFET during the Miller plateau region of the switching transition. This interval occurs while the drain voltage is swinging between the voltage levels dictated by the power topology, requiring the charging/discharging of the drain-gate capacitance with current supplied or removed by the driver device. See Reference [1]

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Feature Description (continued)

8.3.7 Drive Current and Power Requirements

The UCD7K family of drivers can deliver high current into a MOSFET gate for a period of several hundred nanoseconds. High peak current is required to turn the device ON quickly. Then, to turn the device OFF, the driver is required to sink a similar amount of current to ground. This repeats at the operating frequency of the power device.

Reference [1] discusses the current required to drive a power MOSFET and other capacitive-input switching devices.

When a driver device is tested with a discrete, capacitive load it is a fairly simple matter to calculate the power that is required from the bias supply. The energy that must be transferred from the bias supply to charge the capacitor is given by:

$$E = \frac{1}{2} \times CV^2 \tag{1}$$

where C is the load capacitor and V is the bias voltage feeding the driver.

There is an equal amount of energy transferred to ground when the capacitor is discharged. This leads to a power loss given by the following:

$$P = CV^2 \times f \tag{2}$$

where f is the switching frequency.

This power is dissipated in the resistive elements of the circuit. Thus, with no external resistor between the driver and gate, this power is dissipated inside the driver. Half of the total power is dissipated when the capacitor is charged, and the other half is dissipated when the capacitor is discharged.

With V_{DD} = 12 V, C_{LOAD} = 2.2 nF, and f = 300 kHz, the power loss can be calculated as:

$$P = 2.2\text{nF} \times 12^2 \times 300\text{kHz} = 0.095\text{W} \tag{3}$$

With a 12-V supply, this would equate to a current of:

$$I = \frac{P}{V} = \frac{0.095\text{W}}{12\text{V}} = 7.9\text{mA} \tag{4}$$

8.3.8 Operational Waveforms

Figure 22 shows the circuit performance achievable with the output driving a 10-nF load at 12-V V_{DD}. The input pulsewidth (not shown) is set to 200 ns to show both transitions in the output waveform. Note the linear rising and falling edges of the switching waveforms. This is due to the constant output current characteristic of TrueDrive™ stage as opposed to the resistive output impedance of traditional MOSFET-based gate drivers.

8.4 Device Functional Modes

8.4.1 Operation with V_{DD} < 4.25 V (Minimum V_{DD})

The devices operate with V_{DD} voltages above 4.75 V. The maximum UVLO voltage is 4.75 V and operates at V_{DD} voltages above 4.75 V. The typical UVLO voltage is 4.5 V. The minimum UVLO voltage is 4.25 V. At V_{DD} below the actual UVLO voltage, the devices do not operate, OUT1 and OUT2 remain low.

8.4.2 Operation with IN Pin Open

If the IN1 or IN2 pin is disconnected (open), a 100 kΩ internal resistor connects IN1 or IN2 to GND to prevent unpredictable operation due to a floating IN1 or IN2 pin, OUT1 or OUT2 remains low.

8.4.3 Operation with ILIM Pin Open

If the ILIM pin is disconnected (open), the current limit threshold is set at 0.55 V.

8.4.4 Operation with ILIM Pin High

If the signal on ILIM pin is higher than 1.1 V, the current limit threshold is clamped at 1.1 V.

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9 Applications and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The UCD7201 is member of the UCD7K family of digital compatible drivers targeting applications utilizing digital control techniques or applications that require local fast peak current limit protection.

9.2 Typical Applications

9.2.1 Half-Bridge Converter

Figure 25 shows the UCD7201 in a half-bridge converter design. The digital controller is performing the output voltage compensation and all supervisory functions. The isolation amplifier is made up of a linear opto-coupler configured for a gain of 1/10, so the output voltage is transformed to a level comparable with the ADC of the digital controller.

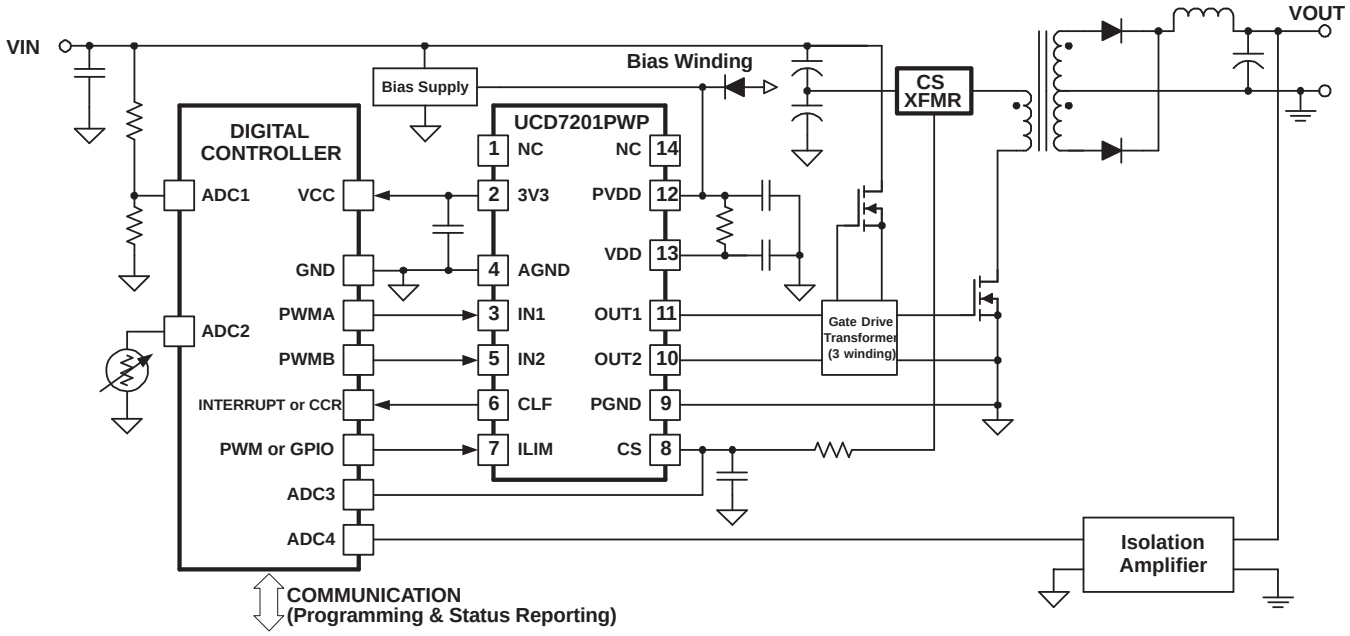

Figure 25. Half-Bridge Converter

9.2.1.1 Design Requirements

In this design example, the input current is sensed by a current transformer (CT), the cycle-by-cycle protection threshold is set at 5 A.

9.2.1.2 Detailed Design Procedure

The cycle-by-cycle current protection is implemented by connect the current sense signal to CS pin. When the CS level is greater than the ILIM voltage minus 25 mV, the output of the driver is forced low and the current limit flag (CLF) is set high. The CLF signal is latched high until the UCD7K device receives the next rising edge on the IN pin.

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Typical Applications (continued)

The current limit threshold can be set to any value between 0.25 V and 1.0 V, select the right turns ratio of the CT and right resistor at the output of CT, such that the CT output is within this range. Assuming the CT output is 0.775V when input current is 5A, if the digital controller has internal digital-to-analog converter, then it can generate 0.775 V and connect to ILIM directly. For digital controller without internal digital-to-analog converter, it can generate PWM signal, send PWM signal through a low pass filter, then connect to ILIM pin.

Assuming the magnitude of the PWM pulse is 3.3V, then the duty cycle is:

$$D = \frac{0.775}{3.3} \tag{5}$$

9.2.1.3 Application Curves

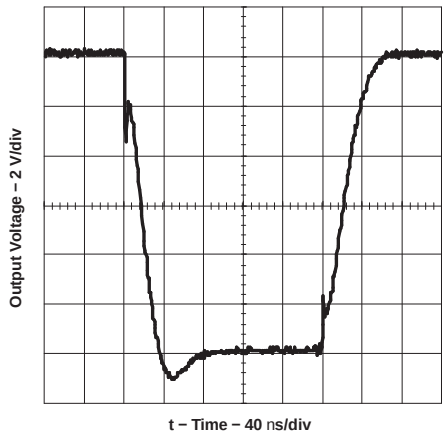

Figure 26. Output Rise and Fall Time (V_{DD} = 12 V, C_{LOAD} = 10 nF)

9.2.2 Intermediate Bus Converter

Figure 27 shows the UCD7201 in an analog only implementation of an intermediate bus converter. The ILIM pin of the UCD7201 is exponentially increased at start-up, which minimizes overshoot on the output voltage. The UCC28089 is a push-pull controller with fixed dead-time. The UCC28089 operates at a fixed duty cycle close to 100% so the circuit acts like a DC transformer linearly transforming the input voltage via the turns ratio of the transformer.

Typical Applications (continued)

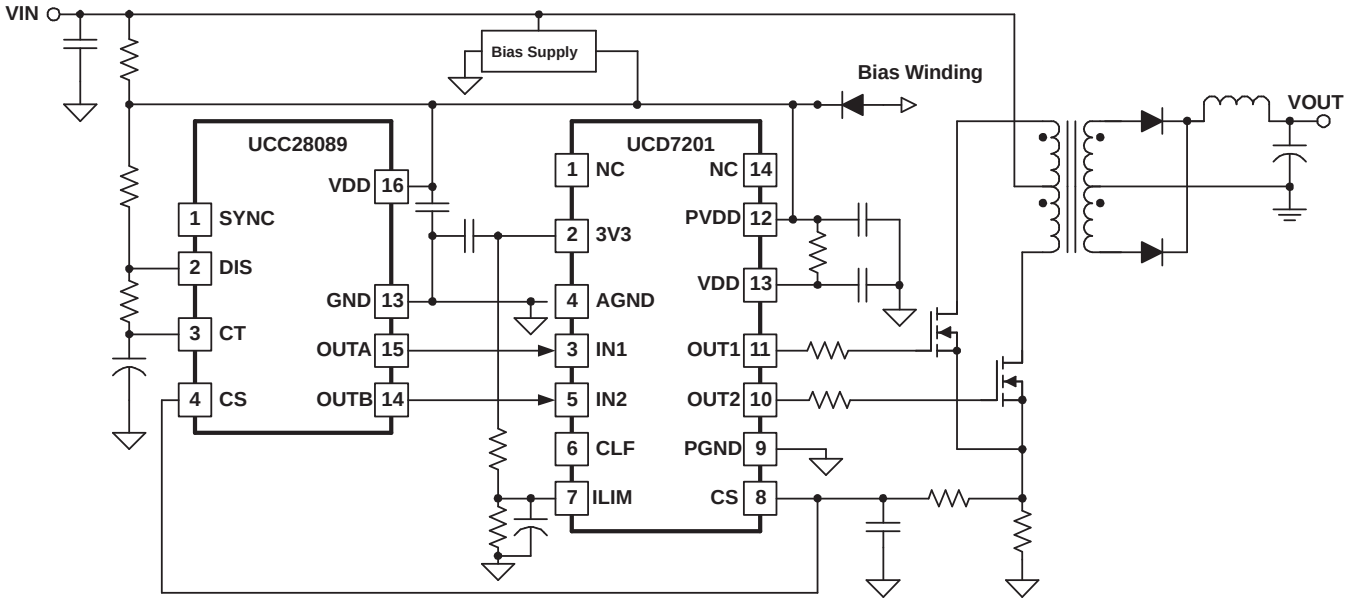

Figure 27. Intermediate Bus Converter

9.2.2.1 Design Requirements

In this design example, the input current is sensed by a current shunt, the cycle-by-cycle protection threshold is set at 5 A.

9.2.2.2 Detailed Design Procedure

$$I_{peak} \times R_{sense} = V_{ILIM} - 0.025 \tag{6}$$

$$R_{sense} = \frac{VILIM - 0.025}{I_{peak}} \tag{7}$$

The current limit threshold can be set to any value between 0.25 V and 1.0 V, so R_{sense} need to be between 0.045 Ω and 0.195 Ω. Let's choose R_{sense} as 0.15 Ω. VILIM need to be 0.775 V in order to protect input current at 5 A.

Since the controller is analog, it cannot program the V_{ILIM}, however, V_{ILIM} can be implemented by a voltage divider connect the pin 2 of UCD7201. Since the voltage on pin 2 is 3.3 V, so the voltage divider needs to be:

$$\frac{R_{bottom}}{R_{bottom} + R_{top}} \times 3.3 = 0.775 \tag{8}$$

9.2.3 Application Curves

See Figure 26.

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10 Power Supply Recommendations

The UCD7K devices accept a supply range of 4.5 V to 15 V. The device has an internal precision linear regulator that produces the 3V3 output from this VDD input. A separate pin, PVDD, not connected internally to the VDD supply rail provides power for the output drivers. In all applications the same bus voltage supplies the two pins. It is recommended that a low value of resistance be placed between the two pins so that the local capacitance on each pin forms low pass filters to attenuate any switching noise that may be on the bus.

Although quiescent VDD current is low, total supply current depends on the gate drive output current required for capacitive load and switching frequency. Total VDD current is the sum of quiescent VDD current and the average OUT current. Knowing the operating frequency and the MOSFET gate charge (Q_G), average OUT current can be calculated from:

$I_{OUT} = Q_G \times f$, where f is frequency.

For the best high-speed circuit performance, VDD bypass capacitors are recommended to prevent noise problems. A 4.7-µF ceramic capacitor should be located closest to the VDD and the AGND connection. In addition, a larger capacitor with relatively low ESR should be connected to the PVDD and PGND pin, to help deliver the high current peaks to the load. The capacitors should present a low impedance characteristic for the expected current levels in the driver application. The use of surface mount components for all bypass capacitors is highly recommended.

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11 Layout

11.1 Layout Guidelines

In a power driver operating at high frequency, it is critical to minimize stray inductance to minimize overshoot/undershoots and ringing. The low output impedance of these drivers produces waveforms with high di/dt. This tends to induce ringing in the parasitic inductances. It is advantageous to connect the driver device close to the MOSFETs. It is recommended that the PGND and the AGND pins be connected to the PowerPad™ of the package with a thin trace. It is critical to ensure that the voltage potential between these two pins does not exceed 0.3 V. The use of schottky diodes on the outputs to PGND and PVDD is recommended when driving gate transformers.

11.2 Layout Example

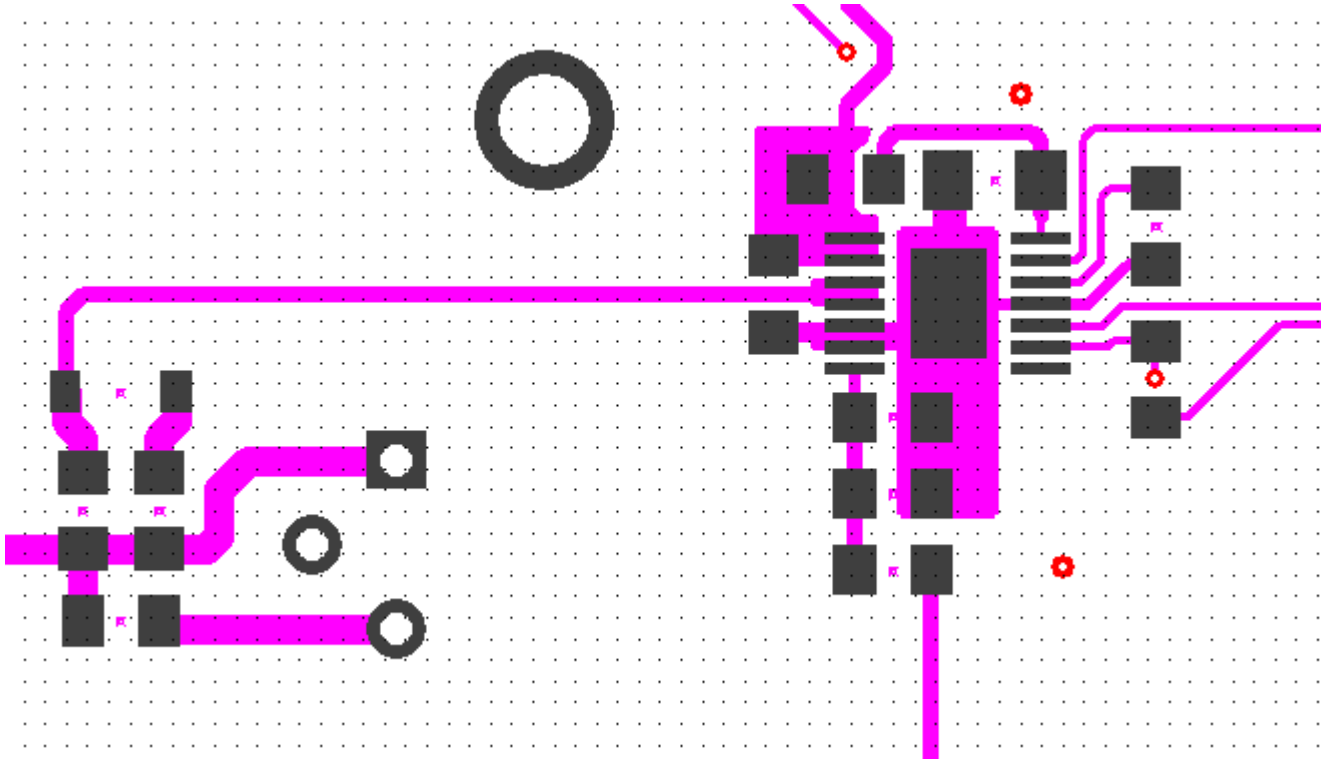

Figure 28. UCD7100 Layout Example

11.3 Thermal Considerations

The useful range of a driver is greatly affected by the drive power requirements of the load and the thermal characteristics of the device package. In order for a power driver to be useful over a particular temperature range the package must allow for the efficient removal of the heat produced while keeping the junction temperature within rated limits. The UCD7K family of drivers is available in PowerPAD™ TSSOP and QFN/DFN packages to cover a range of application requirements. Both have an exposed pad to enhance thermal conductivity from the semiconductor junction.

As illustrated in Reference [2], the PowerPAD™ packages offer a leadframe die pad that is exposed at the base of the package. This pad is soldered to the copper on the PC board (PCB) directly underneath the device package, reducing the T_{JC} down to 2.07°C/W. The PC board must be designed with thermal lands and thermal vias to complete the heat removal subsystem, as summarized in Reference [3].

Note that the PowerPAD™ is not directly connected to any leads of the package. However, it is electrically and thermally connected to the substrate which is the ground of the device. The PowerPad™ should be connected to the quiet ground of the circuit.

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12 Device and Documentation Support

12.1 Device Support

12.1.1 Development Support

TEMPERATURE RANGE	CURRENT SENSE LIMIT PER CHANNEL	FEATURES
UCD7100	Single Low Side ±4-A Driver with Independent CS	3V3, CS(1) (2)
UCD7200	Dual Low Side ±4-A Drivers with Independent CS	3V3, CS(1) (2)
UCD7230	±4-A Synchronous Buck Driver with CS	3V3, CS(1) (2)
UCD7500	Single Low Side ±4-A Driver with CS and 110-V High Voltage Startup	3v3, CS, HVS110 (1) (2) (3)
UCD7600	Dual Low Side ±4-A Drivers with Independent CS and 110-V High Voltage Startup	3V3, CS, HVS110 (1) (2) (3)
UCD7601	Dual Low Side ±4-A Drivers with Common CS and 110-V High Voltage Startup	3V3, CCS, HVS110 (1) (4) (3)
UCD9110	Digital Power Controller for High Performance Single-loop Applications	
UCD9501	Digital Power Controller for High Performance Multi-Loop Applications	

(1) 3V3 = 3.3-V linear regulator.
(2) CS = current sense and current limit function.
(3) HVS110 = 110-V high voltage startup circuit.
(4) CCS = Common current sense and current limit function.

12.2 Documentation Support

12.2.1 Related Documentation

1. *Power Supply Seminar SEM-1400 Topic 2: Design And Application Guide For High Speed MOSFET Gate Drive Circuits*, by Laszlo Balogh, SLUP133.
2. Technical Brief, *PowerPad Thermally Enhanced Package*, SLMA002
3. Application Brief, *PowerPAD Made Easy*, SLMA004

12.3 Trademarks

TrueDrive, PowerPAD are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCD7201PWP	ACTIVE	HTSSOP	PWP	14	90	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	UCD7201	Samples
UCD7201PWPG4	ACTIVE	HTSSOP	PWP	14	90	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	UCD7201	Samples
UCD7201PWPR	ACTIVE	HTSSOP	PWP	14	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	UCD7201	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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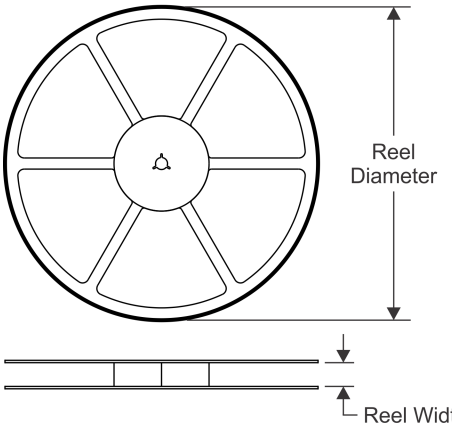
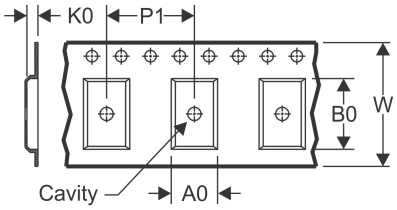
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

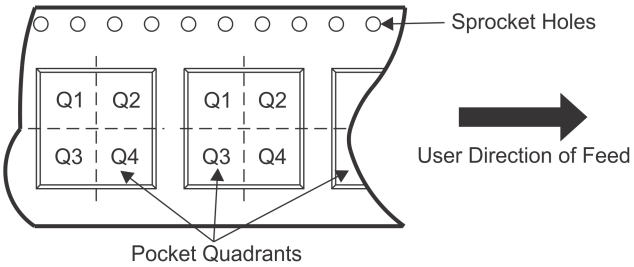


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

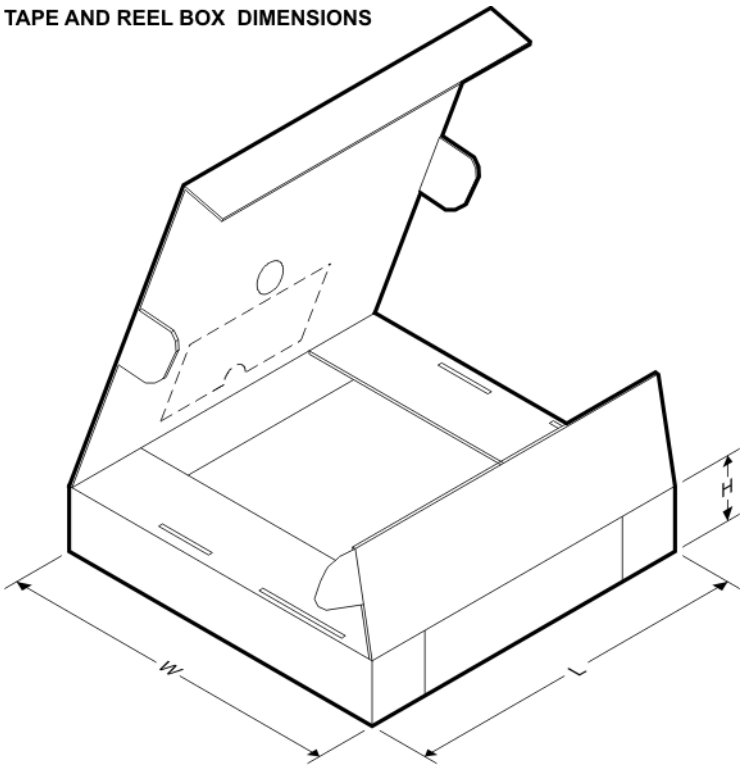
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCD7201PWPR	HTSSOP	PWP	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

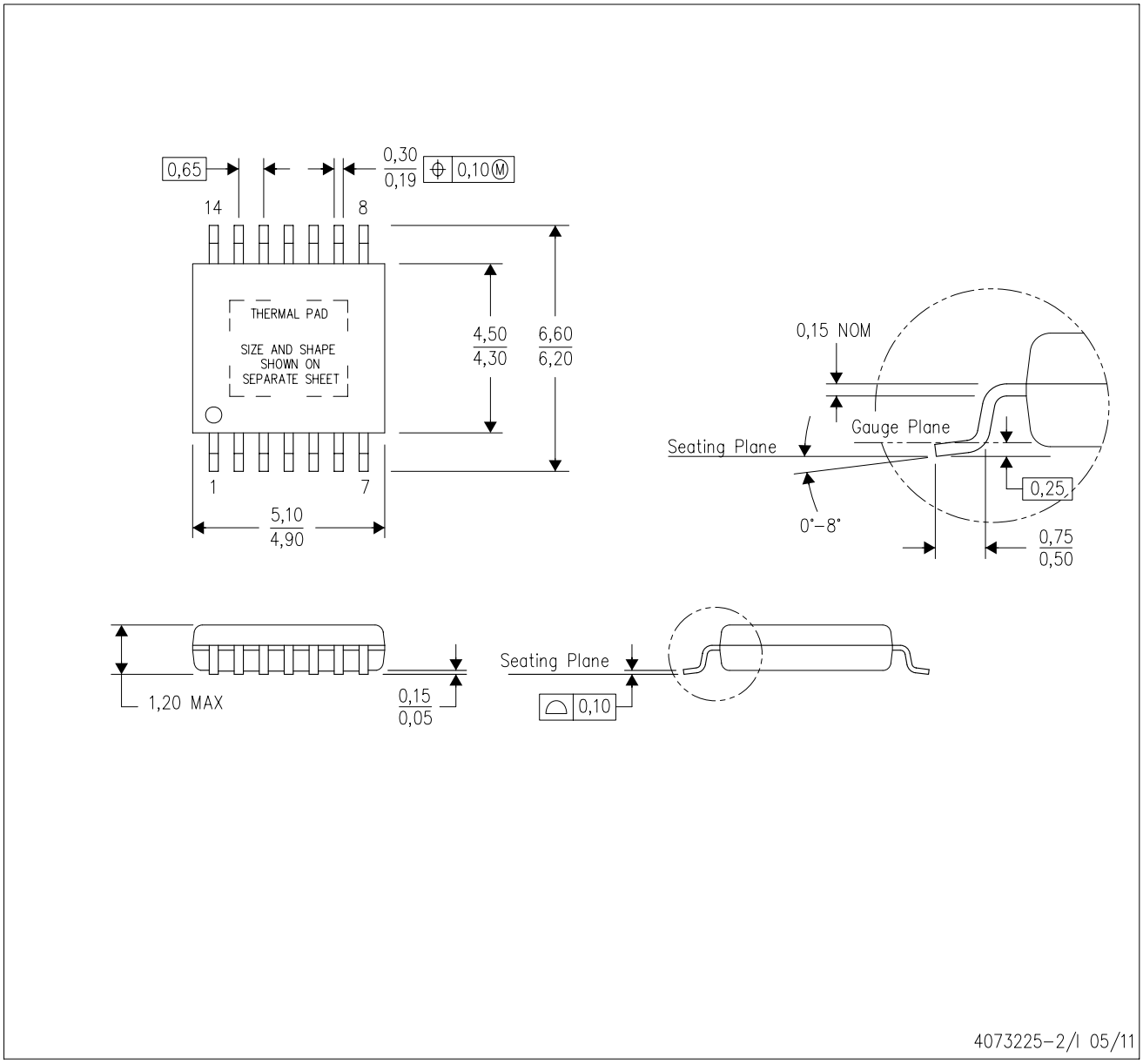
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCD7201PWPR	HTSSOP	PWP	14	2000	350.0	350.0	43.0

PWP (R-PDSO-G14) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO-153

PowerPAD is a trademark of Texas Instruments.

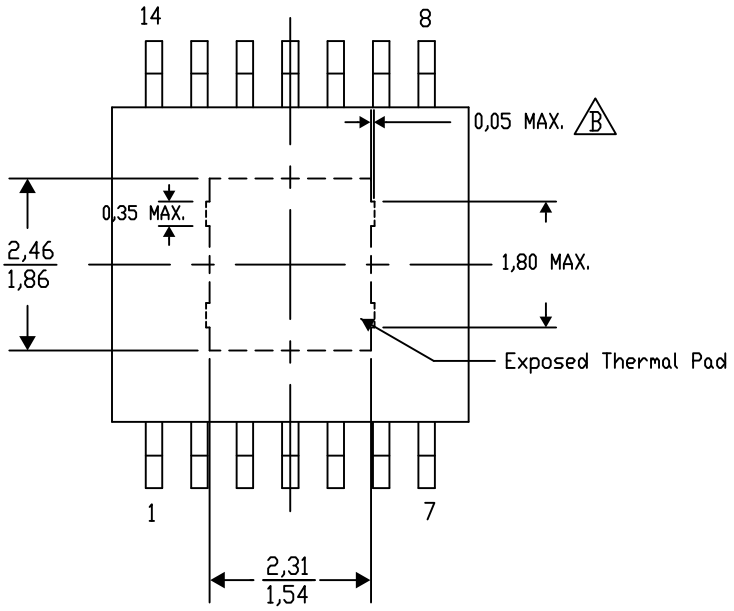
PWP (R-PDSO-G14) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

4206332-44/AO 01/16

NOTE: A. All linear dimensions are in millimeters

B. Exposed tie strap features may not be present.

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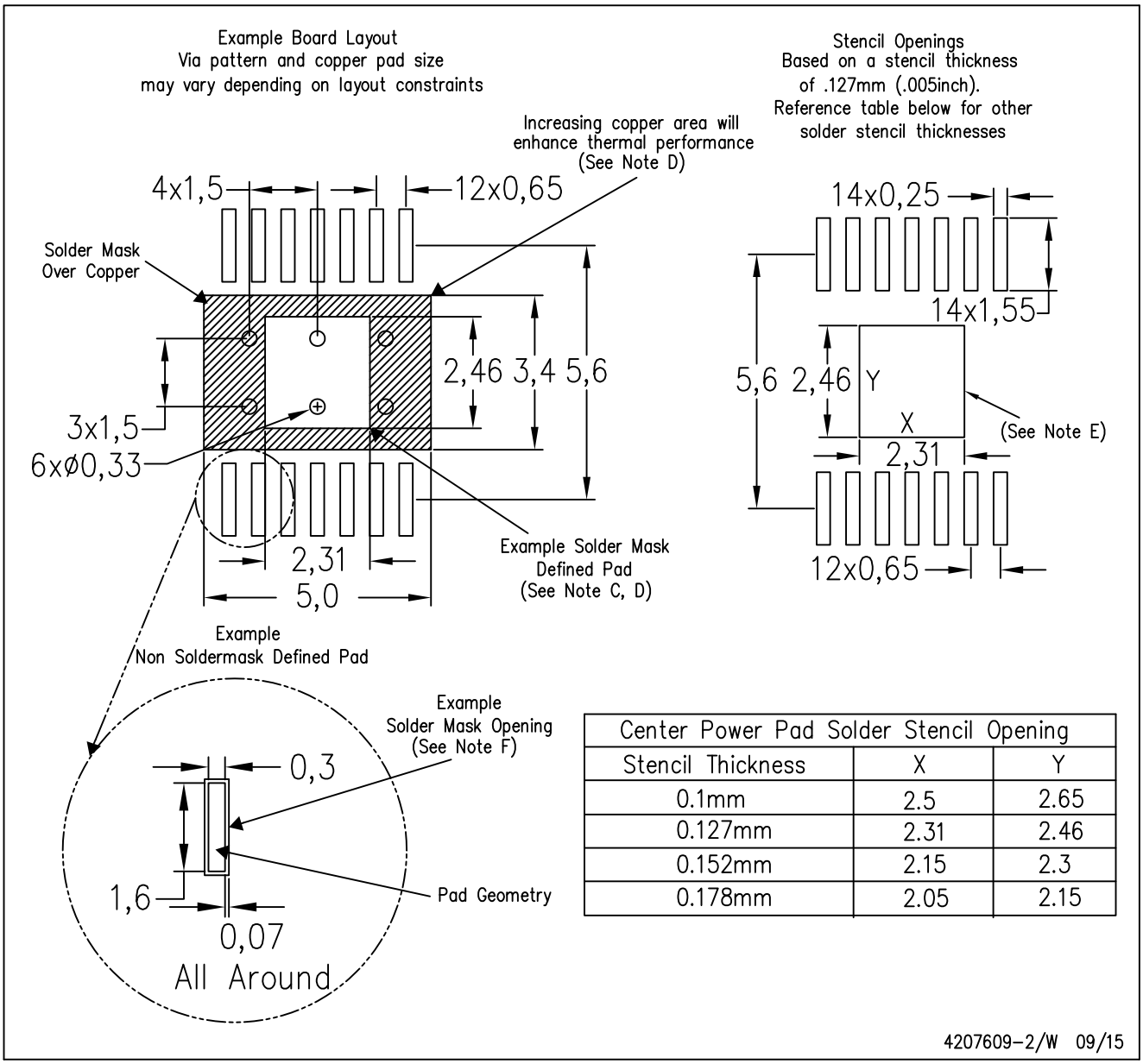
PWP (R–PDSO–G14) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	2.5	2.65
0.127mm	2.31	2.46
0.152mm	2.15	2.3
0.178mm	2.05	2.15

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
- F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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