19-5653; Rev 0; 12/10

EVALUATION KIT AVAILABLE

Dual-Output DC/DC Power Supply for AMOLED

MAX17116

General Description

The MAX17116 includes two current-mode 1.4MHz switch mode power-supply (SMPS) regulators for active-matrix organic light-emitting diode (AMOLED) displays. The positive supply is provided by a step-up regulator with a synchronous rectifier. The negative supply is provided by an inverting regulator with a synchronous rectifier.

The step-up DC-DC converter is a high-accuracy 250mA regulator with an integrated power MOSFET switch and synchronous rectifier. The synchronous rectifier improves efficiency and also provides True Shutdown™. Its 4.6V (fixed) output efficiency exceeds 85% at 150mA from a 3.7V input. A built-in, 7-bit, digital soft-start function controls startup inrush currents.

The inverting DC-DC converter is a high-accuracy 250mA regulator with a built-in power MOSFET switch and synchronous rectifier. Its -5.4V to -1.5V output efficiency exceeds 80% at 150mA from a 3.7V input. A built-in, 7-bit, digital soft-start function controls startup inrush currents. The internally set output voltage is adjusted through a unique communication protocol through the single EN pin.

The IC is available in a 12-pin, 3mm x 3mm x 0.5mm, ultra-thin DFN package with exposed pad and 0.5mm lead spacing to facilitate placement on extremely narrow circuit boards and a 24-pin, 4mm x 4mm, thin QFN package with exposed pad.

Applications

OLED Displays

Phone, DSC Displays

Automobile Navigation

Features

- **2.3V to 4.2V Input Operating Voltage Range**
- **High-Performance PWM Step-Up Regulator**
  - **Fixed 4.6V, 250mA Output**
  - **High Accuracy (±1%)**
  - **1.4MHz Switching Frequency**
  - **Built-In 6V/0.25Ω n-Channel MOSFET with Lossless Current Sensing**
  - **Built-In 6V/0.5Ω p-Channel MOSFET Synchronous Rectifier**
  - **Cycle-by-Cycle Current Limit**
  - **More than 85% Efficiency at 150mA**
  - **Good Low-Duty Factor Operation**
- **High-Performance PWM Inverting Regulator**
  - **Programmable 250mA Output**
  - **High Accuracy (±1%)**
  - **Adjustable Controlled-Output-Voltage Slew Rate**
  - **1.4MHz Switching Frequency**
  - **Built-In 14V/0.25Ω p-Channel Power MOSFET with Lossless Current Sensing**
  - **Built-In 14V/0.25Ω n-Channel Power MOSFET Synchronous Rectifier**
  - **Cycle-by-Cycle Current Limit**
  - **More than 80% Efficiency at 150mA**
- **True Shutdown for Both Outputs**
- **Timer-Delayed Output Undervoltage Shutdown for Both Outputs**
- **Thermal-Overload Protection**
- **12-Pin, 3mm x 3mm Ultra-Thin DFN Package and 24-Pin, 4mm x 4mm TQFN Package**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX17116EVC+	-40°C to +85°C	12 UTDFN**
MAX17116ETG+*	-40°C to +85°C	24 TQFN**

+Denotes a lead(Pb)-free/RoHS-compliant package.
**Future product—contact factory for availability.*
***Exposed pad.*

True Shutdown is a trademark of Maxim Integrated Products, Inc.

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

Dual-Output DC/DC Power Supply for AMOLED

ABSOLUTE MAXIMUM RATINGS

IN, EN, IC, OUTP, LXP to AGND .....-0.3V to +6V
LXN to IN .....-14V to +0.3V
STEP to AGND .....-0.3V to (V_{IN} + 0.3V)
PGND to AGND .....-0.3V to +0.3V
OUTN to AGND .....-7V to +0.3V
LXN to OUTN .....-0.3V to +14V
LXP, LXN, OUTP, OUTN, IN RMS Current Rating 1.6A

Continuous Power Dissipation (T_A = +70°C)
12-Pin UTDFN (derate 15.1mW/°C above +70°C) 1206.6W
24-Pin TQFN (derate 19mW/°C above +70°C).....1520.9mW
Operating Temperature Range ..... -40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range..... -65°C to +160°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow) .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = +3.7V, Circuit of Figure 2, V_{OUTP} = +4.9V, V_{OUTN} = -4.9V, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
IN Input Supply Range		2.3		4.2	V
IN Undervoltage-Lockout Threshold	V_{IN} rising, hysteresis = 200mV	1.8	2.0	2.2	V
IN Quiescent Current	EN = IN, no load, not switching		50	90	µA
OUTP Quiescent Current	EN = IN, no load, not switching		0.8	1.1	mA
V_{IN} Quiescent Current	EN = IN, no load		1.6	2.5	mA
IN Shutdown Current	EN = AGND, T_A = +25°C			1	µA
STEP-UP REGULATOR					
OUTP Regulation Voltage	I_{LOAD} = 10mA to 200mA, V_{IN} = 2.3V to 4.2V	4.554	4.60	4.646	V
OUTP Fault Trip Level	Falling edge, no hysteresis	3.496	3.68	3.864	V
	Falling edge, no hysteresis, no timer	2.116	2.3	2.484	
OUTP Load Regulation	0 < I_{LOAD} < 200mA, DC regulation		0.1		%
Oscillator Frequency		1190	1400	1610	kHz
Maximum Load Current	V_{IN} = 2.9V to 4.2V (Note 2)	250			mA
LXP/OUTP Peak Current Limit	Duty cycle = 35%	850	1100	1350	mA
LXP nMOS N1 On-Resistance	I_{LXP1} = 200mA, Figure 3		0.2	0.4	Ω
LXP pMOS1 P1 On-Resistance	I_{LXP1} = 200mA, Figure 3		0.15	0.3	Ω
LXP pMOS2 P2 On-Resistance	I_{LXP2} = 200mA, Figure 3		0.15	0.3	Ω
LXP Damping Switch On-Resistance			20		Ω
OUTP Discharge Resistance	OUTP to PGND		330		Ω
Soft-Start Period	7-bit voltage ramp with filtering to prevent high peak currents		2		ms
INVERTING REGULATOR					
OUTN Default Regulation Voltage	At startup: I_{LOAD} 10mA to 200mA; V_{IN} = 2.3V to 4.2V	-4.949	-4.9	-4.851	V
OUTN Minimum Regulation Voltage	Lowest DAC code: I_{LOAD} 10mA to 200mA; V_{IN} = 2.3V to 4.2V	-5.454	-5.4	-5.346	V

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = +3.7V, Circuit of Figure 2, V_{OUTP} = +4.9V, V_{OUTN} = -4.9V, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
OUTN Maximum Regulation Voltage	Highest DAC code: I_{LOAD} 10mA to 200mA; V_{IN} = 2.3V to 4.2V	-1.530	-1.5	-1.470	V
OUTN Fault Trip Level	Rising edge, no hysteresis, relative to current DAC step	73	80	87	%
	Rising edge, no hysteresis, relative to current DAC step, no timer	43	50	57	
Oscillator Frequency		1190	1400	1610	kHz
Maximum Load Current	V_{IN} = 2.9V to 4.2V (Note 2)	250			mA
OUTN/LXN Peak Current Limit	Duty cycle = 65%	1000	1200	1400	mA
LXN-to-IN pMOS On-Resistance	I_{LXN} = 200mA		0.25	0.50	Ω
LXN-to-OUTN nMOS On-Resistance	I_{LXN} = 200mA		0.25	0.50	Ω
LXN Damping Switch On-Resistance			70		Ω
OUTN Discharge Resistance	OUTN to PGND		330		Ω
Soft-Start Period	7-bit voltage ramp with filtering to prevent high peak currents		2		ms
DAC Step Voltage		0.01	0.025	0.04	V
Number of DAC Steps Between Levels			4		
STEP Period	STEP = AGND	3.5	4	4.5	ms
	R_{STEP} = 50kΩ	1.5	2	2.5	
	R_{STEP} = 150kΩ	5	6	7	
SEQUENCE CONTROL					
EN Input Low Voltage				0.6	V
EN Input High Voltage		1.2			V
EN Input Resistance	To AGND		140		kΩ
FAULT DETECTION					
Duration-to-Trigger Fault Condition	OUTP or OUTN below threshold		50		ms
Thermal-Shutdown Threshold	Latched fault		+160		°C
TIMING SPECIFICATIONS					
Enable Start Delay	t_{EN_DLY} (Note 3)		300	400	µs
EN Pulse Stop Time	t_{STOP} (Note 3)	250	300		µs
EN Turn-Off Delay	t_{OFF_DLY} (Note 3)	50	60	70	µs
OUTN Initial Start Ramp Time	OUTN transition from -4.9V to -1.5V (Note 4)		2		ms
EN Pulse Frequency	50% duty factor	12	50	250	kHz

Dual-Output DC/DC Power Supply for AMOLED

ELECTRICAL CHARACTERISTICS

(V_{IN} = +3.7V, Circuit of Figure 2, V_{OUTP} = +4.9V, V_{OUTN} = -4.9V, **T_A = -40°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
IN Input Supply Range		2.3		4.2	V
IN Undervoltage-Lockout Threshold	V_{IN} rising, hysteresis = 200mV	1.8		2.2	V
IN Quiescent Current	EN = IN, no load			90	µA
				2.5	mA
OUTP Quiescent Current	EN = IN, no load			1.1	mA
STEP-UP REGULATOR					
OUTP Regulation Voltage	I_{LOAD} = 10mA to 200mA, V_{IN} = 2.3V to 4.2V	4.554		4.646	V
OUTP Fault Trip Level	Falling edge, no hysteresis	3.496		3.864	V
	Falling edge, no hysteresis, no timer	2.116		2.484	
Oscillator Frequency		1190		1610	kHz
LXP/OUTP Peak Current Limit	Duty cycle = 35%	800		1400	mA
LXP nMOS N1 On-Resistance	I_{LXP1} = 200mA, Figure 3			0.4	Ω
LXP pMOS1 P1 On-Resistance	I_{LXP1} = 200mA, Figure 3			0.3	Ω
LXP pMOS2 P2 On-Resistance	I_{LXP2} = 200mA, Figure 3			0.3	Ω
INVERTING REGULATOR					
OUTN Default Regulation Voltage	At startup: I_{LOAD} 10mA to 200mA; V_{IN} = 2.3V to 4.2V	-4.949		-4.851	V
OUTN Minimum Regulation Voltage	Lowest DAC code: I_{LOAD} 10mA to 200mA; V_{IN} = 2.3V to 4.2V	-5.454		-5.366	V
OUTN Maximum Regulation Voltage	Highest DAC code: I_{LOAD} 10mA to 200mA; V_{IN} = 2.3V to 4.2V	-1.530		-1.470	V
OUTN Fault Trip Level	Rising edge, no hysteresis, relative to current DAC step	73		87	%
	Rising edge, no hysteresis, relative to current DAC step, no timer	43		57	
Oscillator Frequency		1190		1610	kHz
OUTN/LXN Peak Current Limit	Duty cycle = 65%	1000		1400	mA
LXN to IN pMOS On-Resistance	I_{LXN} = 200mA			0.50	Ω
LXN to OUTN nMOS On-Resistance	I_{LXN} = 200mA			0.50	Ω
DAC Step Voltage		0.01		0.04	V
STEP Period	STEP = AGND	3.5		4.5	ms
	R_{STEP} = 50kΩ	1.5		2.5	
	R_{STEP} = 150kΩ	5		7	
SEQUENCE CONTROL					
EN Input Low Voltage				0.6	V
EN Input High Voltage		1.2			V

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = +3.7V, Circuit of Figure 2, V_{OUTP} = +4.9V, V_{OUTN} = -4.9V, **T_A = -40°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
TIMING SPECIFICATIONS					
Enable Start Delay	t_{EN_DLY} (Note 3)			400	µs
EN Pulse Stop Time	t_{STOP} (Note 3)	250			µs
EN Turn-Off Delay	t_{OFF_DLY} (Note 3)	50		70	µs
EN Pulse Frequency	50% duty factor	12		250	kHz

Note 1: Limits are 100% production tested at T_A = +25°C. Maximum and minimum limits over temperature are guaranteed by design and characterization.

Note 2: Guaranteed by design, not production tested.

Note 3: The timing definitions are illustrated in Figure 1.

Note 4: The initial start ramp time depends on load conditions and is correct only when the discharge time due to load on the output capacitance is shorter than ramp time.

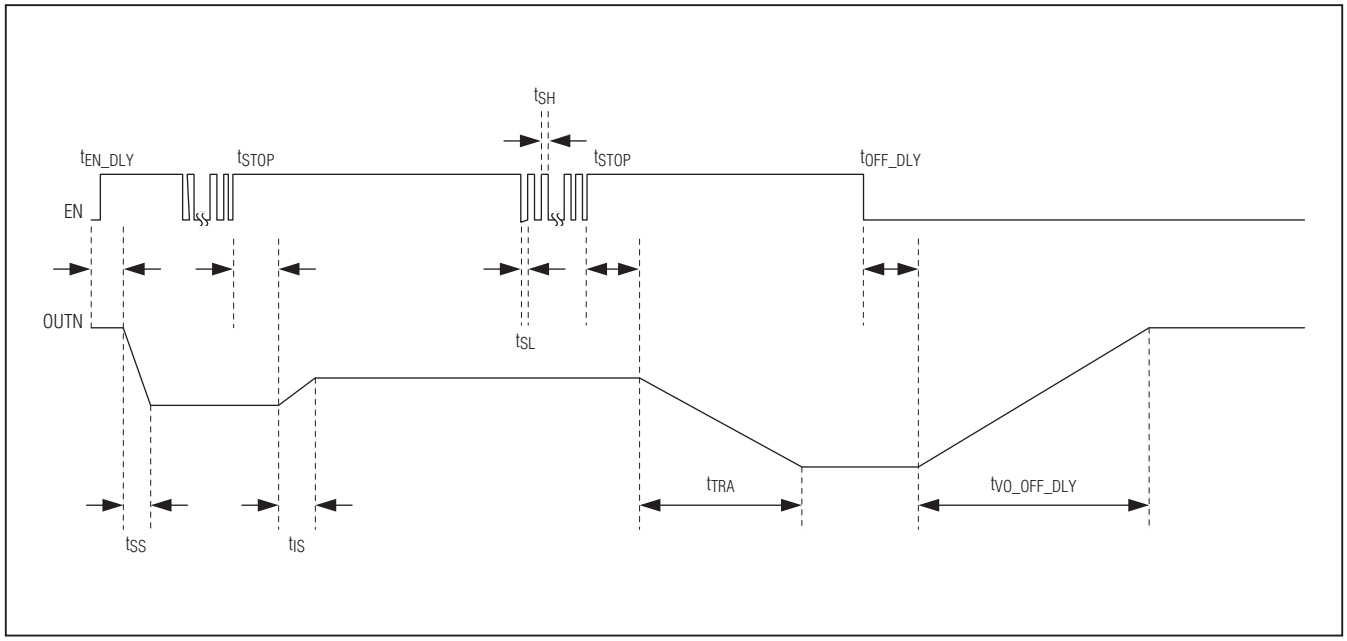


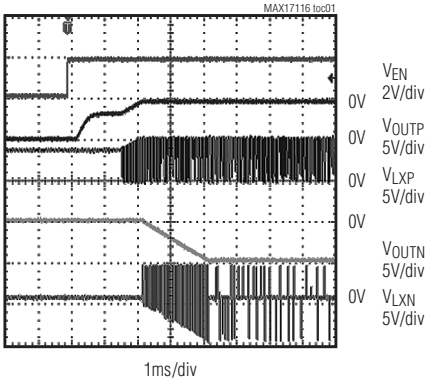
Figure 1. EN Serial Interface Timing Diagram

Dual-Output DC/DC Power Supply for AMOLED

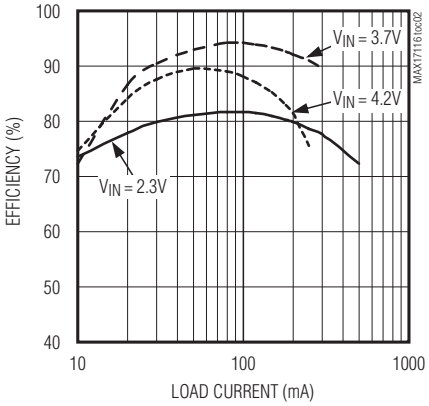
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

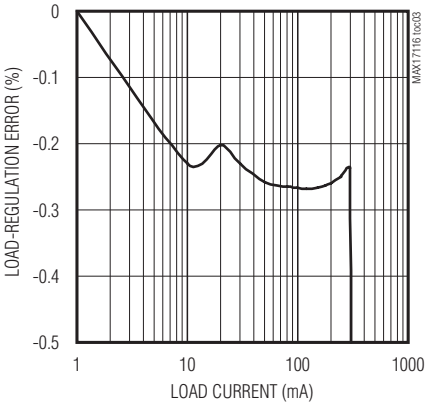
STARTUP WAVEFORMS



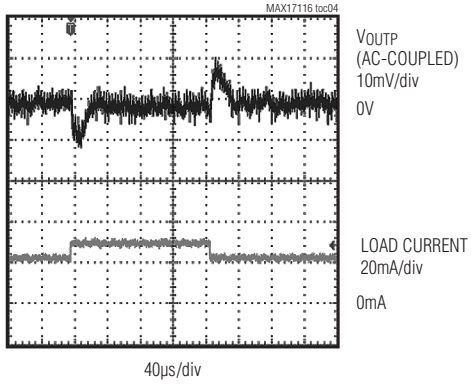
STEP-UP REGULATOR EFFICIENCY vs. LOAD CURRENT



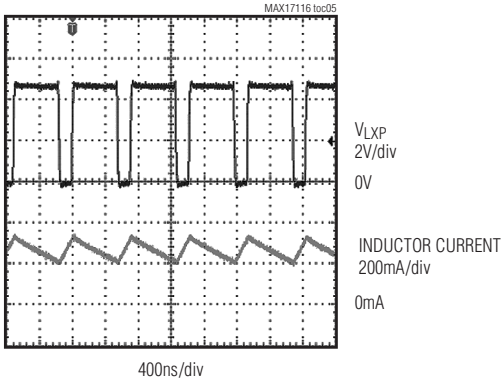
STEP-UP REGULATOR OUTPUT LOAD REGULATION vs. LOAD CURRENT



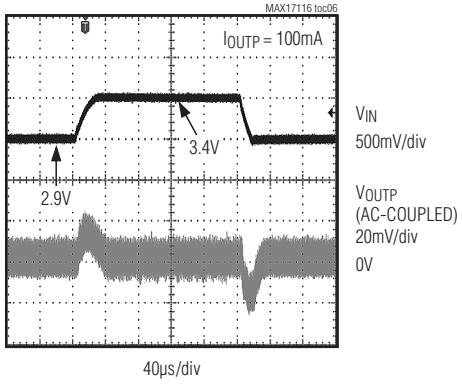
STEP-UP REGULATOR LOAD TRANSIENT (20mA ◄► 30mA)



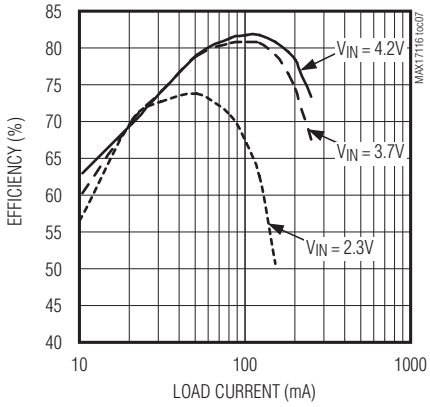
STEP-UP REGULATOR SWITCHING WAVEFORMS



STEP-UP REGULATOR LINE TRANSIENT



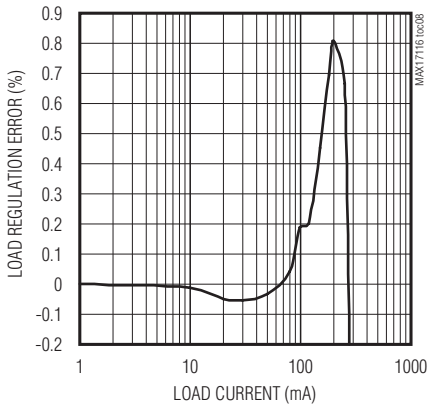
BUCK-BOOST REGULATOR EFFICIENCY vs. LOAD CURRENT



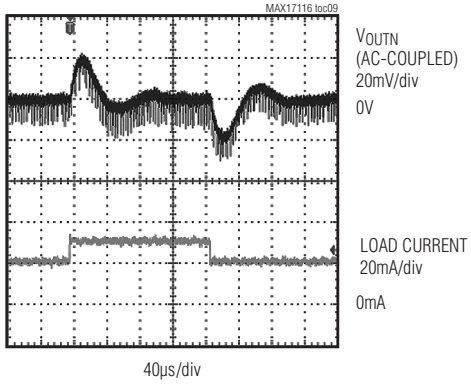
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

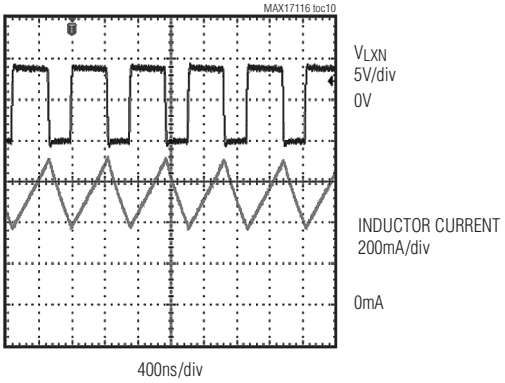
BUCK-BOOST REGULATOR OUTPUT LOAD REGULATION vs. LOAD CURRENT



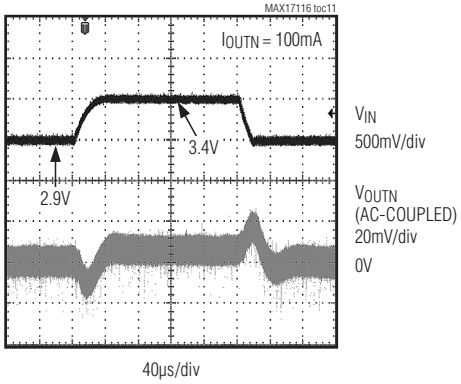
BUCK-BOOST REGULATOR LOAD TRANSIENT (20mA ◄► 30mA)



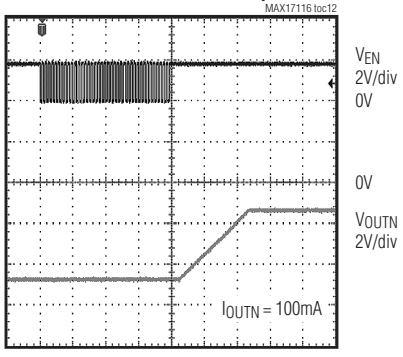
BUCK-BOOST REGULATOR SWITCHING WAVEFORMS



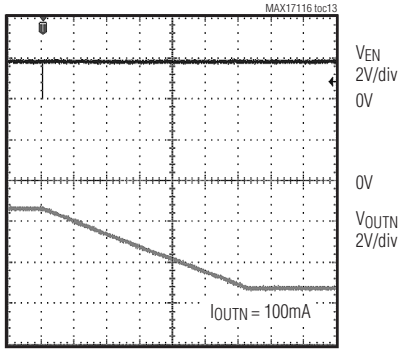
BUCK-BOOST REGULATOR LINE TRANSIENT



BUCK-BOOST REGULATOR TRANSITION BEHAVIOR (FIRST TRANSITION FROM -4.9V TO -1.5V)

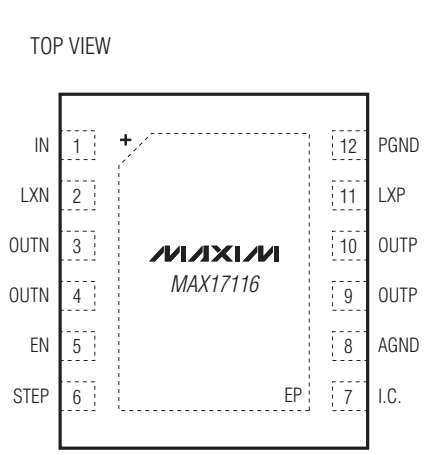


BUCK-BOOST REGULATOR TRANSITION BEHAVIOR (LATER TRANSITION FROM -1.5V TO -5.4V)

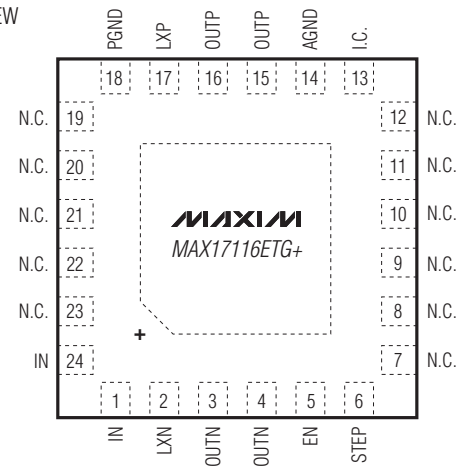


Dual-Output DC/DC Power Supply for AMOLED

Pin Configurations



UTDFN (3mm x 3mm)



TQFN (4mm x 4mm)

Pin Description

PIN		NAME	FUNCTION
UTDFN	TQFN		
1	1, 24	IN	Input Supply. Source of the internal inverting regulator p-channel MOSFET switch. Connect both IN pins to the input voltage and bypass IN to PGND with a 4.7µF ceramic capacitor.
2	2	LXN	Inverting Regulator Switching Node. Connect the inverting regulator's inductor here and minimize the trace area to reduce EMI.
3, 4	3, 4	OUTN	Inverting Regulator Output Connection
5	5	EN	Active-High Enable Input and Serial Interface Input. See the *EN Serial Interface* section for more details.
6	6	STEP	DAC Step-Rate Adjustment. Connect STEP to AGND to select the default 250Hz (4ms) step rate. Connect a resistor from STEP to AGND to select a different step rate. Since there are four DAC steps between each EN code setting, the time between single EN step settings is 4/250Hz = 16ms default or an adjustable time. See the *EN Serial Interface* section for more details.
7	13	I.C.	Internal Connection. Connect I.C. to AGND.
—	7–12, 19–23	N.C.	Not Connected
8	14	AGND	Analog Ground for Step-Up Regulator and Inverting Regulator. Connect AGND to the power ground (PGND) pin.
9, 10	15, 16	OUTP	Step-Up Regulator Output Connection
11	17	LXP	Step-Up Regulator Switching Node. Drain of the internal step-up regulator's n-channel MOSFET switch. Connect the step-up regulator's inductor here and minimize the trace area to reduce EMI.
12	18	PGND	Power Ground
—	—	EP	Exposed Pad. Connect to AGND and PGND with a large copper area for power dissipation.

Typical Operating Circuit

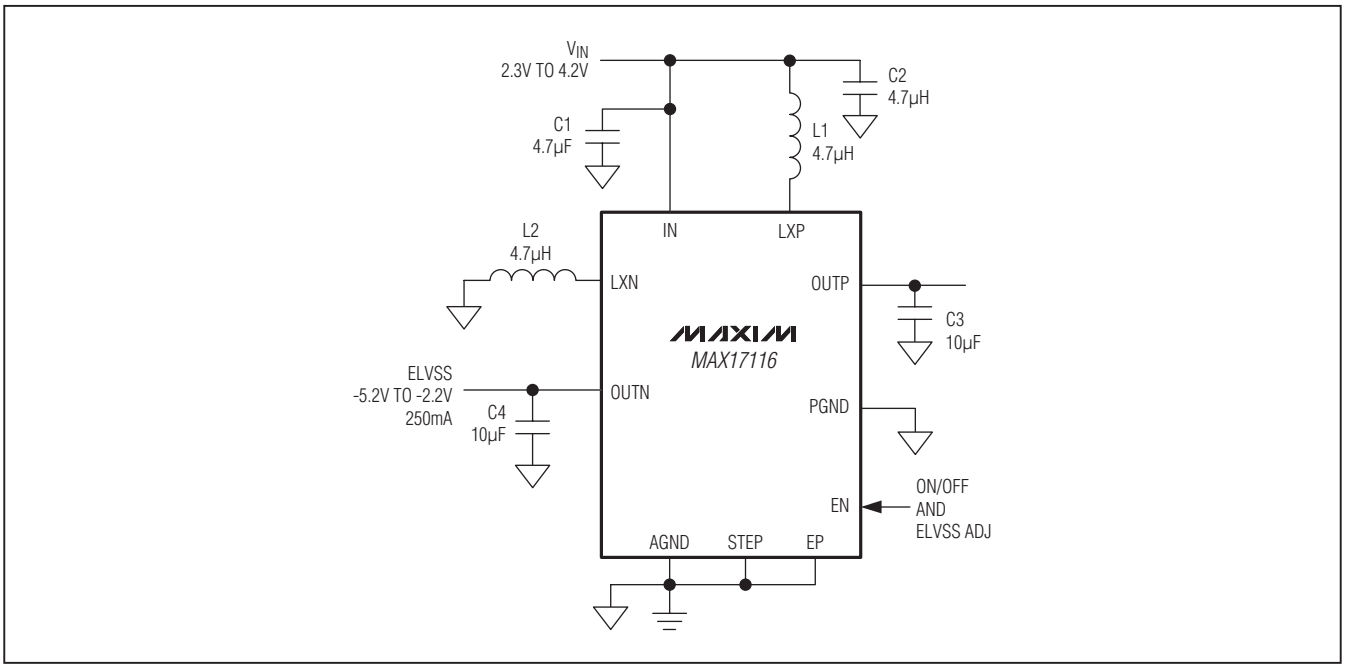


Figure 2. MAX17116 Typical Operating Circuit

The device's typical operating circuit is shown as Figure 2. The input supply voltage range is from 2.3V to 4.2V. The output voltage ELVDD is a fixed voltage of 4.6V (typ) and the ELVSS voltage is adjustable from -5.4V to -1.5V through the EN serial interface. Table 1 lists some recommended components, and Table 2 lists the contact information for component suppliers.

Table 1. Component List

DESIGNATION	DESCRIPTION
C1, C2	4.7µF ±10%, 10V X5R ceramic capacitors (0603) TDK C1608X5R1A475K
C3, C4	10µF ±10%, 10V X7R ceramic capacitors (0805) Murata GRM21BR71A106K
L1, L2	Low-profile 4.7µH, 0.9A inductors Würth TPC2807 Sumida CDH36D07NP-4R7

Table 2. Component Suppliers

SUPPLIER	PHONE	FAX	WEBSITE
Sumida Corp.	847-545-6700	847-545-6720	www.sumida.com
TDK Corp.	847-803-610	847-390-4405	www.component.tdk.com
Würth Electronik GmbH & Co. KG	408-262-4400	408-262-4410	www.we-online.com

Dual-Output DC/DC Power Supply for AMOLED

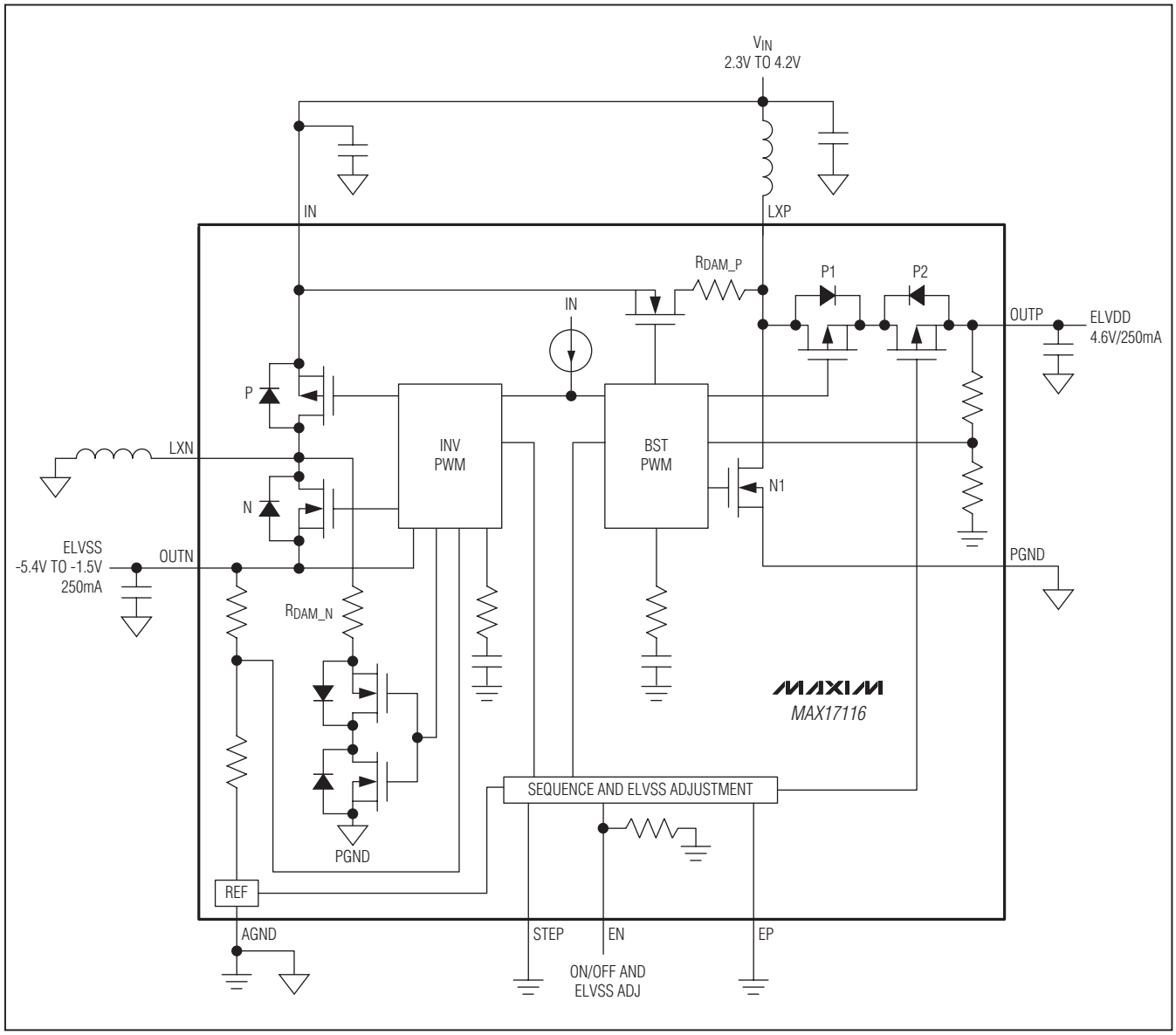


Figure 3. MAX17116 Functional Diagram

Detailed Description

The MAX17116 includes two current-mode 1.4MHz SMPS regulators for AMOLED displays. The positive supply is provided by a step-up regulator with a synchronous rectifier. The negative supply is provided by an inverting regulator with a synchronous rectifier. The step-up regulator output is a fixed voltage of 4.6V and the inverting regulator output is adjustable from -5.4V to -1.5V through the single-wire EN serial interface. The input voltage range is 2.3V to 4.2V and both regulators provide an output current of 250mA from an input voltage of at least 2.9V. Figure 3 shows the MAX17116 functional diagram.

Step-Up Regulator

The step-up regulator is a constant-frequency current-mode type. It operates at a 1.4MHz switching frequency to allow the use of tiny 0.6mm thin inductors. The IC's internal digital soft-start, internal MOSFET switch, and synchronous rectifier reduce the number of external components for a very compact application circuit.

The regulator controls the output voltage and the power delivered to the output by modulating duty cycle D of the internal power MOSFET in each switching cycle. An error amplifier compares the feedback signal with an internal reference voltage and changes its output internal compensation node with its pole/zero series resistor and capacitor to set the peak inductor current. As the load varies, the error amplifier sources or sinks current to the compensation node accordingly to produce the inductor peak current necessary to service the load. To maintain stability at high duty cycles, a slope compensation signal is added.

On the rising edge of the internal clock, the controller sets a flip-flop, turning on the n-channel MOSFET and applying the input voltage across the inductor. The current through the inductor ramps up linearly, storing energy in its magnetic field. Once the sum of the current-feedback signal and the slope compensation exceed the compensation voltage, the controller resets the flip-flop, turning off the MOSFET and turning on the synchronous rectifier. Since the inductor current is continuous, a transverse potential develops across the inductor and the inductor sources current to the output. The voltage across the inductor then becomes the difference between the output voltage and the input voltage. This discharge condition forces the current through the inductor to ramp back down, transferring the energy stored in the magnetic field to the output capacitor and the load. The MOSFET remains off for the rest of the clock cycle.

The converter operates in skip mode only at very light loads (typically it is less than 4mA) and includes a damping switch that turns on when the synchronous rectifier turns off at zero or negative current to control LXP ringing.

Inverting Converter

The inverting converter is also a constant-frequency (1.4MHz) current-mode type and includes synchronous rectification to lower application of BOM cost and improve efficiency. The inverter operates in skip mode only at light loads and includes a damping switch that turns on when the synchronous rectifier turns off at zero or negative current. The switch prevents ringing in the inductor in discontinuous conduction and the resulting RF noise.

The inverting converter operates similarly to the step-up converter, except that the main switch is a p-channel MOSFET between LXN and IN. Energy is stored in the inductor during the switch on-time and the continuous inductor current pulls current from the output to ground when the flip-flop resets, the main switch turns off, and the synchronous rectifier turns on.

The internally set output voltage for the inverting converter is adjustable between -5.4V and -1.5V in 100mV steps. Adjustment is accomplished though a unique control interface using the EN pin as shown in the *EN Serial Interface* section. The step rate while programming V_{OUTN} is also adjustable through STEP pin settings shown in the *Electrical Characteristics* table.

EN Serial Interface

The enable pin (EN) is used as an on/off pin, as well as a serial interface input. When EN goes high, the IC starts operation only after a 300µs delay. Similarly, when EN falls, the IC enters the shutdown state only after a 60µs delay. This makes the EN pin available for serial-data input as long as the pin state keeps changing fast enough to avoid entering shutdown (12kHz or greater).

The interface protocol is a simple correspondence between the number of pulses to ground on EN (1 to 40) and the desired output voltage (-5.4V to -1.5V). Table 3 shows the relationship between the number of pulses and the desired output voltage for the driver IC.

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Table 3. Inverting Regulator Output Voltage with EN Pulses

EN PULSES	V_{OUTN} (V)	EN PULSES	V_{OUTN} (V)
1	-5.4	22	-3.3
2	-5.3	23	-3.2
3	-5.2	24	-3.1
4	-5.1	25	-3.0
5	-5.0	26	-2.9
6	-4.9	27	-2.8
7	-4.8	28	-2.7
8	-4.7	29	-2.6
9	-4.6	30	-2.5
10	-4.5	31	-2.4
11	-4.4	32	-2.3
12	-4.3	33	-2.2
13	-4.2	34	-2.1
14	-4.1	35	-2.0
15	-4.0	36	-1.9
16	-3.9	37	-1.8
17	-3.8	38	-1.7
18	-3.7	39	-1.6
19	-3.6	40	-1.5
20	-3.5	—	—
21	-3.4	—	—

During serial pulses, EN must remain in the high state or in the low state for between 2µs and 45µs. Pulses are counted until EN remains high at least 200µs. After EN stays high for that length of time, the count of pulses is latched and decoded to the desired DAC code.

The output voltage normally changes very slowly, over a long time period. This is accomplished by dividing each 100mV DAC step in 4 x 25mV substeps lasting approximately 4ms each. The timing is controlled by an internal oscillator with a default timing of 4ms, which can also be adjusted by an external resistor from STEP to AGND. For example, when STEP is connected to AGND, a default timing of 4ms per substep is selected and when R_{STEP} varies from 50kΩ to 150kΩ, the step rate varies from 2ms to 6ms.

For most output-voltage transitions, V_{OUTN} changes slowly in this strictly controlled manner. The exceptions to this include startup to the standard startup voltage of -5.4V, the first commanded transition from the startup voltage, and shutdown.

For startup, the DAC is set to the standard startup voltage of -4.9V, with no DAC stepping, and a 2ms voltage-ramping soft-start is used. After startup, the first transition to a programmed value uses DAC stepping with a step-rate that is 128 times the normal rate to accomplish the largest possible transition in less than 3ms. Note that transitions to less negative output voltages depend on the output load, as much as the DAC stepping, to determine that transition rate.

For shutdown, the DAC stepping is not used and the internal discharge resistor, along with the output load, determines the output discharge rate. The internal discharge resistor (330Ω, typ) is available on both OUTP and OUTN.

Figure 4 shows the timing sequence for the output-voltage transitions for these three exceptional cases.

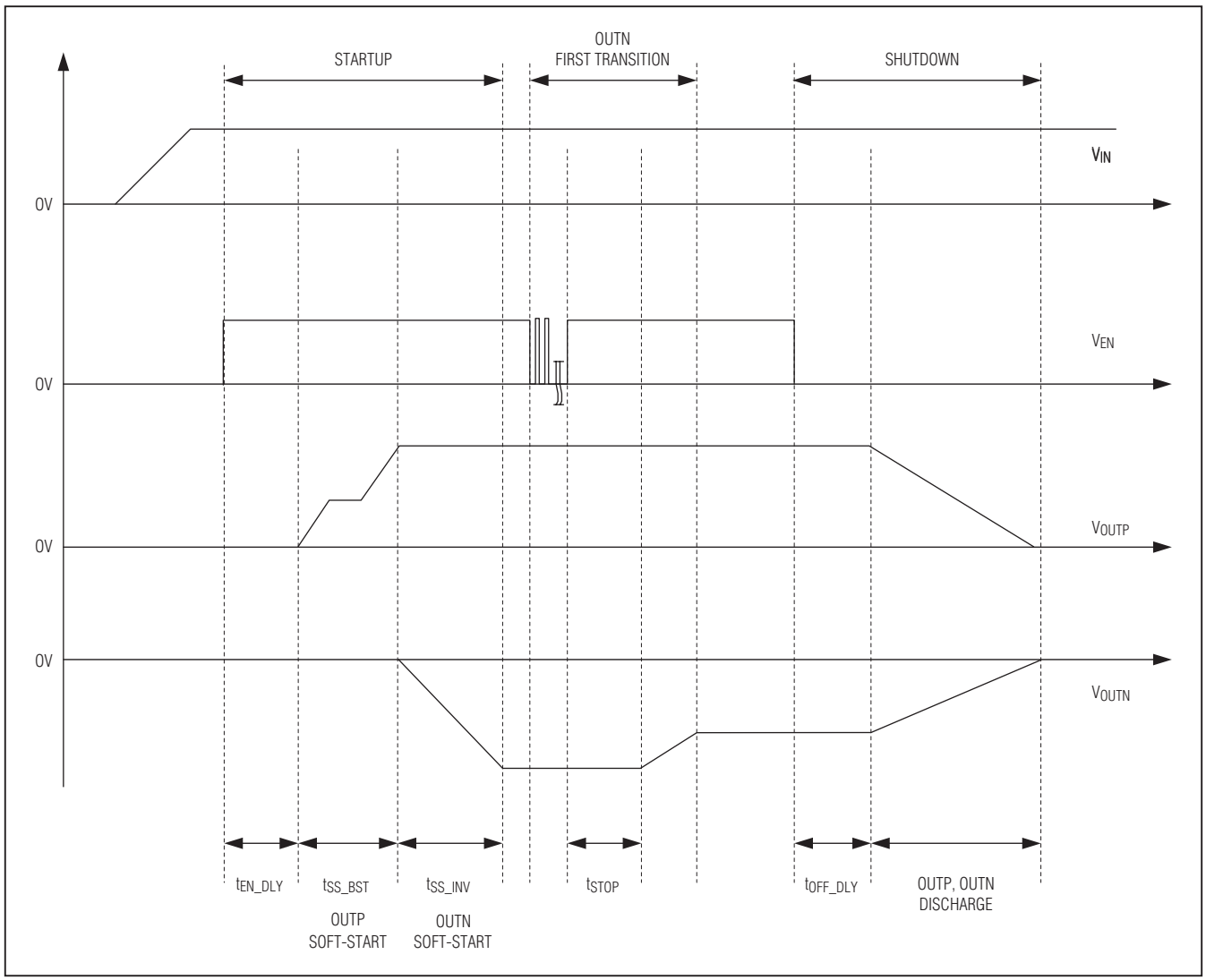


Figure 4. MAX17116 Power-On/-Off Timing Sequence

Undervoltage Lockout (UVLO)

The UVLO circuit compares the input voltage at IN with the UVLO threshold (2.0V, typ) to ensure the input voltage is high enough for reliable operation. The wide 200mV (typ) hysteresis prevents supply transients from causing a restart. The startup procedure begins when input voltage exceeds the UVLO rising threshold and EN goes above its logic-high threshold. During normal operation, if the input voltage falls below the UVLO falling threshold, the device enters its shutdown state.

Output Undervoltage Protection

During steady-state operation, if the output of the step-up converter or inverting regulator output does not exceed certain fault-detection thresholds, protection circuitry is activated and the outputs may shut down. Each regulator has an output-short threshold (typically 50% of regulation) that triggers immediate shutdown of all outputs. Further, for simple overload conditions, each regulator has an undervoltage threshold (typically 80% of regulation) that activates an internal fault timer (50ms, typ); if the overload condition continues for the fault-timer duration, then the IC shuts down all its outputs.

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Thermal Protection

The MAX17116 includes a thermal-protection circuit. Thermal-overload protection prevents excessive power dissipation from overheating the device. When the junction temperature exceeds T_J = +160°C (typ), the device shuts down. Cycling the input voltage (below the UVLO falling threshold) or bringing EN low for more than 70µs clears the fault latch and reactivates the device. The thermal-overload protection protects the controller in the event of fault conditions. For continuous operation, do not exceed the absolute maximum junction temperature rating of T_J = +150°C.

Design Procedure

Inductor Selections

The inductance value, peak current rating, and series resistance are factors to consider when selecting the inductors for the step-up and inverting converters. These factors influence the converters' efficiencies, maximum output load capabilities, transient response times, and output ripple voltages. Physical size and cost are also important factors to be considered.

The maximum output currents, input voltages, output voltages, and switching frequencies determine the inductor values. Very high inductance values minimize the current ripple, and therefore, reduce the peak current, which decreases core losses in the inductor and I^2R losses in the entire power path. However, large inductor values also require more energy storage and more turns of wire, which increase physical size and can increase I^2R losses in the inductor. Low inductance values decrease the physical size but increase the current ripple and peak current. Finding the best inductor involves choosing the best compromise between circuit efficiency, inductor size, and cost.

The equations used here include a constant, LIR, which is the ratio of the inductor peak-to-peak ripple current to the average DC inductor current at the full load current. The best trade-off between inductor size and circuit efficiency for step-up and inverting regulators generally has an LIR between 0.3 and 0.5. However, depending on the AC characteristics of the inductor core material and ratio of inductor resistance to other power-path resistances, the best LIR can shift up or down. If the inductor resistance is relatively high, more current ripple can be accepted to reduce the number of turns required and increase the wire diameter. If the inductor resistance is relatively low, increasing inductance to lower the peak current can decrease losses throughout the power path. If extremely thin high-resistance inductors are used, the best LIR can increase to between 0.5 and 1.0.

Once a physical inductor is chosen, higher and lower values of the inductor should be evaluated for efficiency improvements in typical operating regions.

Calculate the required inductance, the maximum DC current, the inductor ripple current, and the peak inductor current using the equations below to choose an inductor value from an appropriate inductor family. The inductor's saturation current rating and the LXP and LXN current limits should exceed the peak currents calculated above. The inductor's DC current rating should exceed the maximum expected DC current. For good efficiency, choose an inductor with less than 0.5Ω series resistance.

Step-Up Converter Inductor L_P

Use the following procedure to choose the inductor for the step-up converter. An example is provided below using typical operating conditions of:

$V_{IN(TYP)}$ = 3.7V Typical operating input voltage

$V_{IN(MIN)}$ = 2.3V Minimum operating input voltage

$I_{OUTP1(MAX)}$ = 250mA Maximum output current (V_{IN} > 2.9V)

$I_{OUTP2(MAX)}$ = 200mA Maximum output current (V_{IN} = 2.3V)

$\eta_{P(TYP)}$ = 0.90 Expected efficiency at the typical operating condition

$\eta_{P(MIN)}$ = 0.81 Worst-case efficiency expected at the minimum operating input voltage and maximum output current

f_{SW} = 1.4MHz Switching frequency

LIR = 0.5 Ratio of the inductor peak-to-peak ripple current to the average DC inductor current

1) Calculate the required inductance:

$$L_P = \left(\frac{V_{IN(TYP)}}{V_{OUTP}}\right)^2 \times \left(\frac{V_{OUTP} - V_{IN(TYP)}}{I_{OUTP(MAX)} \times f_{SW}}\right) \times \left(\frac{\eta_{P(TYP)}}{LIR}\right)$$

$$= \left(\frac{3.7V}{4.6V}\right)^2 \times \left(\frac{4.6V - 3.7V}{250mA \times 1.4MHz}\right) \times \left(\frac{0.9}{0.5}\right)$$

$$= 2.99\mu H$$

Choose L_P = 4.7µH since actual inductance of these small inductors is much less at significant current.

2) Calculate the maximum DC current in the inductor and select an inductor whose DC current rating is greater than the maximum DC current calculated:

$$I_{LP(DC_MAX)} = \frac{I_{OUTP2(MAX)} \times V_{OUTP}}{V_{IN(MIN)} \times \eta_{P(MIN)}} = \frac{200mA \times 4.6V}{2.3V \times 0.81} = 493mA$$

3) Calculate the peak amplitude of the inductor current and choose an inductor with a saturation current rating greater than the peak inductor current calculated. Also, verify that the peak inductor current amplitude is below the minimum current rating of LXP. Use the formulas below to calculate the inductor current ripple and peak inductor current:

$$\Delta I_{LP_RIPPLE} = \frac{V_{IN(MIN)} \times (V_{OUTP} - V_{IN(MIN)})}{L_P \times V_{OUTP} \times f_{SW}}$$

$$I_{P(PEAK)} = I_{LP(DC,MAX)} + \frac{\Delta I_{LP_RIPPLE}}{2} = 493mA + \frac{2.3V \times (4.6V - 2.3V)}{2 \times 4.7\mu H \times 4.6V \times 1.4MHz} = 580mA$$

Inverting Converter Inductor L_N

Use the following procedure to choose the inductor for the inverting converter. An example is provided below using typical operating conditions of:

$V_{IN(TYP)}$ = 3.7V Typical operating input voltage

$V_{IN(MIN)}$ = 2.3V Minimum operating input voltage

V_{OUTN} = -4.9V Output voltage

$I_{OUTN1(MAX)}$ = 250mA Maximum output current (V_{IN} > 2.9V)

$I_{OUTN2(MAX)}$ = 130mA Maximum output current (V_{IN} = 2.3V)

$\eta_{P(TYP)}$ = 0.70 Expected efficiency at the typical operating condition

$\eta_{N(MIN)}$ = 0.60 Worst-case efficiency expected at the minimum operating input voltage and maximum output current

f_{SW} = 1.4MHz Switching frequency

LIR = 0.6 Ratio of the inductor peak-to-peak ripple current to the average DC inductor current

1) Calculate the required inductance:

$$L_N = \left(\frac{V_{IN(TYP)}}{(V_{IN(TYP)}) + |V_{OUTN}|}\right)^2 \left(\frac{|V_{OUTN}| \times \eta_{N(TYP)}}{f_{SW} \times I_{OUTN1(MAX)} \times LIR}\right) = \left(\frac{3.7V}{3.7V + |-4.9V|}\right)^2 \left(\frac{|-4.9V| \times 0.70}{1.4MHz \times 250mA \times 0.6}\right) = 3.6A$$

Choose L_N = 4.7µH since inductance of these small inductors decreases with high current.

2) Calculate the maximum DC current in the inductor to select an inductor whose DC current rating is greater than the maximum DC current calculated:

$$I_{LN(DC,MAX)} = I_{OUTN2(MAX)} \times \left[\frac{|V_{OUTN}| + V_{IN(MIN)}}{\eta_{N(MIN)} \times V_{IN(MIN)}}\right] = 130mA \times \left[\frac{|-4.9V| + 2.3V}{0.60 \times 2.3V}\right]$$

3) Calculate the peak amplitude of the inductor current to choose an inductor with a saturation current rating less than the peak inductor current calculated. Also, with this result, verify that the peak inductor current amplitude is below the minimum current rating of LXN. Formulas to calculate the inductor current ripple and peak inductor current follow:

$$\Delta I_{LN_RIPPLE} = \left(\frac{V_{IN(MIN)}}{L_N \times f_{SW}}\right) \times \left(\frac{|V_{OUTN}|}{V_{IN(MIN)} + |V_{OUTN}|}\right)$$

$$I_{LN(PEAK)} = I_{LN(DC,MAX)} + \frac{\Delta I_{LN_RIPPLE}}{2} = 680mA + \left(\frac{2.3V}{4.7\mu H \times 1.4MHz}\right)\left(\frac{|-4.9V|}{2.3 + |-4.9V|}\right)$$

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OUTP and OUTN Output Capacitor Selection

The total output voltage ripple has two components: the capacitive ripple caused by the charging and discharging of the output capacitance, and the ohmic ripple due to the capacitor's equivalent series resistance (ESR):

For the step-up converter:

$$V_{OUTP_RIPPLE} = V_{OUTP_RIPPLE(C)} + V_{OUTP_RIPPLE(ESR)}$$

$$V_{OUTP_RIPPLE(C)} \approx \left(\frac{I_{OUTP}}{C_{OUTP} \times f_{SW}}\right)\left(\frac{V_{OUTP} - V_{IN}}{V_{OUTP}}\right)$$

and:

$$V_{OUTP_RIPPLE(ESR)} \approx I_{LP(PEAK)} \times R_{ESR_COUTP}$$

where:

C_{OUTP} is the step-up converter's output capacitance.

$I_{LP(PEAK)}$ is the step-up converter's peak inductor current from the inductor selection.

R_{ESR_COUTP} is the capacitor's ESR.

For the inverting converter:

$$V_{OUTN_RIPPLE} = V_{OUTN_RIPPLE(C)} + V_{OUTN_RIPPLE(ESR)}$$

$$V_{OUTN_RIPPLE(C)} \approx \left(\frac{I_{OUTN}}{C_{OUTN} \times f_{SW}}\right)\left(\frac{|V_{OUTN}|}{V_{IN} + |V_{OUTN}|}\right)$$

and:

$$V_{OUTN_RIPPLE(ESR)} \approx I_{LN(PEAK)} \times R_{ESR_COUTN}$$

where:

C_{OUTN} is the inverting converter's output capacitance

$I_{LN(PEAK)}$ is the inverting converter's peak inductor current from the inductor selection

R_{ESR_COUTN} is the capacitor's ESR

For ceramic capacitors, the output-voltage ripple is typically dominated by the capacitive term. The voltage rating and temperature characteristics of the output capacitor must also be considered.

Input Capacitor Selection

The input capacitor reduces the current peaks drawn from the input supply and reduces noise injection into the IC. Two 4.7µF ceramic capacitors are used in Figure 2.

Applications Information

Power Dissipation

An IC's maximum power dissipation depends on the thermal resistance from the die to the ambient environment and the ambient temperature. The thermal resistance depends on the IC package, PCB copper area, other thermal mass, and airflow. More PCB copper, cooler ambient air, and more airflow increase the possible dissipation, while less copper or warmer air decreases the IC's dissipation capability. The major components of power dissipation are the power dissipated in the step-up regulator and inverting converter.

Step-Up Regulator

The largest portions of power dissipation in the step-up regulator are the internal MOSFET, the inductor, and the synchronous rectifier. If the step-up regulator has 90% efficiency, approximately 4% to 6% of the power is lost in the internal MOSFET and synchronous rectifier, approximately 3% to 4% in the inductor. The remaining 1% to 3% is distributed among the input and output capacitors and the PCB traces. This gives a good estimate of the power dissipated in the IC by the step-up regulator. The following formulas can also be used to estimate the power loss in the internal power MOSFET and the synchronous rectifier (excluding switching losses). The conduction power loss in the internal power MOSFET is:

$$P_{LXP_ON} = I^2_{SW1(RMS)} \times R_{DSON_LXP}$$

where:

$$I_{SW1(RMS)} = I_{LP(DC_MAX)} \times \sqrt{D_1 \times [1 + \frac{1}{3} \times (\frac{\Delta I_{LP_RIPPLE}}{I_{LP(DC_MAX)}})^2]}$$

R_{DSON_LXP} is the on-resistance for the internal power MOSFET.

D_1 is the duty cycle on the step-up regulator.

The conduction power loss in the synchronous rectifier is:

$$P_{SYN1} = I^2_{SYN1(RMS)} \times R_{DSON_SYN1}$$

where:

$$I_{SYN1(RMS)} = I_{LP(DC_MAX)} \times \sqrt{(1-D_1) \times [1+\frac{1}{3} \times (\frac{\Delta I_{LP_RIPPLE}}{I_{LP(DC_MAX)}})^2]}$$

R_{DSON_SYN1} is the on-resistance for the synchronous rectifier.

D_1 is the duty cycle on the step-up regulator.

In general, at full power, if the switch sizes have been chosen well, the switching losses in the main switch are approximately equal to the conduction losses in that switch. The synchronous rectifier switching losses are small since switching occurs with zero voltage across the switch.

Inverting Converter

The largest portions of power dissipation in the inverting regulator are the internal MOSFET, the inductor, and the synchronous rectifier. If the inverting regulator has 85% efficiency, approximately 7% to 10% of the power is lost in the internal MOSFET and synchronous rectifier, approximately 4% to 5% in the inductor. The remaining 1% to 4% is distributed among the input and output capacitors and the PCB traces. This gives a good estimate of the power dissipated in the IC by the inverting regulator. Like the step-up converter, the following formulas can be used to estimate the power loss in the internal power MOSFET and the synchronous rectifier (excluding switching losses):

The conduction power loss in the internal power MOSFET is:

$$P_{LXN_ON} = I^2_{SW2(RMS)} \times R_{DSON_LXN}$$

where:

$$I_{SYN2(RMS)} = I_{LN(DC_MAX)} \times \sqrt{(1-D_2) \times [1+\frac{1}{3} \times (\frac{\Delta I_{LN_RIPPLE}}{I_{LN(DC_MAX)}})^2]}$$

R_{DSON_LXN} is the on-resistance for the internal power MOSFET.

D_2 is the duty cycle on the inverting converter.

The conduction power loss in the synchronous rectifier is:

$$P_{SYN2} = I^2_{SYN2(RMS)} \times R_{DSON_SYN2}$$

where:

$$I_{SYN2(RMS)} = I_{LN(DC_MAX)} \times \sqrt{(1-D_2) \times [1+\frac{1}{3} \times (\frac{\Delta I_{LN_RIPPLE}}{I_{LN(DC_MAX)}})^2]}$$

R_{DSON_SYN2} is the on-resistance for the synchronous rectifier.

D_2 is the duty cycle on the inverting converter.

In general, at full power, if the switch sizes have been chosen well, the switching losses in the main switch are approximately equal to the conduction losses in that switch. The synchronous rectifier switching losses are small since switching occurs with zero voltage across the switch.

PCB Layout and Grounding

Careful PCB layout is important for proper operation. Use the following guidelines for good PCB layout:

1) Place the input capacitors as close as possible to the IN pin so the trace connecting one end of the capacitors to the IN pin and the trace connecting the other end of the capacitors to the PGND pin is as short as possible.
2) Place the step-up converter inductor so the traces connecting the inductor to the LXP pin and the input capacitors are as short as possible.
3) Connect the output capacitors of OUTP and OUTN as close as possible to their respective pins.
4) Create a power ground plane (PGND) so the other end of these capacitors and the PGND pin can connect to this plane directly.
5) Create an analog ground plane (AGND) so the other end of these capacitors and the AGND pin can connect to this plane directly. Place the inverting converter inductor so the trace connecting the inductor to the LXN pin and the distance the inductor current has to travel through the PGND plane to the PGND pin are as short as possible.

6) Make a single connection between the AGND and PGND planes together at a point closest to the PGND pin only. Connect the entire backside pad to PGND with a larger plane for good thermal performance. Make no other connections between these two ground planes. If vias are needed to make this connection, use multiple vias instead of a single via to help reduce the resistance and the inductance attributed by the vias and place the vias close to the PGND pin so the AGND plane can connect to the PGND plane at a point closest to the PGND pin.
7) Care should be taken to avoid running traces that carry any noise-sensitive signals near LXP or LXN or high-current traces.
8) Minimize the length and maximize the width of the traces between the output capacitors and the load for best transient responses.
9) Avoid using vias in the high-current paths. If vias are unavoidable, use multiple vias instead of single vias to help reduce the resistance and the inductance attributed by the vias. Avoid using vias in connection with switched current. Use vias, if necessary, in connections with continuous currents. For the step-up regulator, the continuous-current connections are between the input capacitor and the inductor and between the inductor and LXP. For the inverting regulator, the continuous current paths are between the inductor and PGND and between the inductor and LXN. Avoid vias in all other high-current connections including ground connections.
10 Refer to the MAX17116 Evaluation Kit for an example of a proper board layout.

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
12 UTDFN-EP	V1233N+1	21-0451	90-0339
24 TQFN-EP	T2444N+4	21-0139	90-0035

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	12/10	Initial release	—

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