LM20136 6A, Synchronous Buck Regulator with Input Synchronization

Check for Samples: LM20136

FEATURES

- **Input Voltage Range 2.95V to 5.5V**
- **Accurate Current Limit Minimizes Inductor Size**
- **97% Peak Efficiency**
- **Frequency Synchronization Pin**
- **16mΩ and 20mΩ Integrated FET Switches**
- **Starts up Into Pre-biased Loads**
- **Output Voltage Tracking**
- **Peak Current Mode Control**
- **Adjustable Output Voltage Down to 0.8V**
- **Adjustable Soft-Start with External Capacitor**
- **Precision Enable Pin with Hysteresis**
- **Integrated OVP, UVLO, Power Good and Thermal Shutdown**
- **16-Pin HTSSOP exposed Pad Package**

APPLICATIONS

- **Simple to Design, High Efficiency Point of Load Regulation from a 5V or 3.3V Bus**
- **High Performance DSPs, FPGAs, ASICs and Microprocessors**
- **Broadband, Networking and Optical Communications Infrastructure**

DESCRIPTION

The LM20136 is a full featured synchronous buck regulator capable of delivering up to 6A of continuous output current. The current mode control loop can be compensated to be stable with virtually any type of output capacitor. For most cases, compensating the device only requires two external components, providing maximum flexibility and ease of use. The device is optimized to work over the input voltage range of 2.95V to 5.5V making it suitable for a wide variety of low voltage systems.

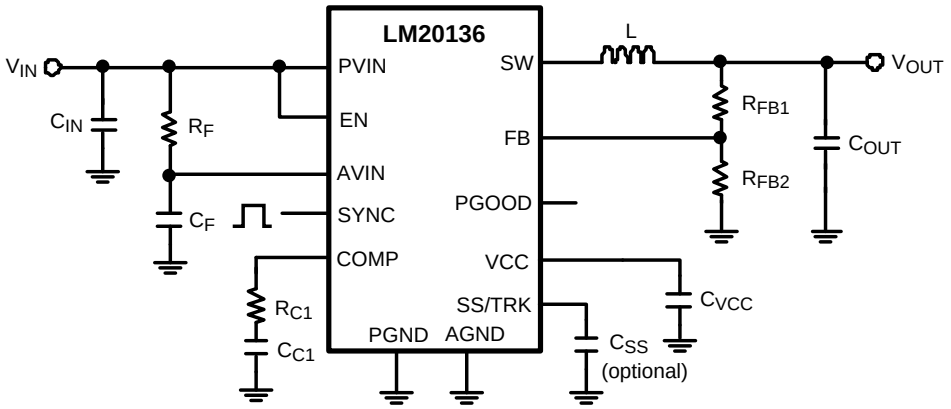
The device features internal over voltage protection (OVP) and over current protection (OCP) circuits for increased system reliability. A precision enable pin and integrated UVLO allows the turn on of the device to be tightly controlled and sequenced. Start-up inrush currents are limited by both an internally fixed and externally adjustable Soft-Start circuit. Fault detection and supply sequencing are possible with the integrated power good circuit.

The switching frequency of the LM20136 can be synchronized to an external clock by use of the SYNC pin. The SYNC pin is capable of synchronizing to input signals ranging from 500 kHz to 1.5 MHz

The LM20136 is designed to work well in multi-rail power supply architectures. The output voltage of the device can be configured to track a higher voltage rail using the SS/TRK pin. If the output of the LM20136 is pre-biased at startup it will not pull the ouput low.

The LM20136 is offered in a 16-pin HTSSOP package with an exposed pad that can be soldered to the PCB, eliminating the need for bulky heatsinks.

Typical Application Circuit



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Connection Diagram

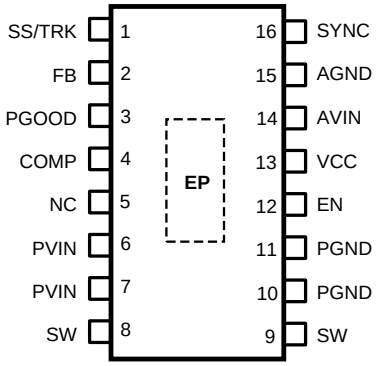


Figure 1. Top View
16-Pin HTSSOP
See PWP Package

PIN DESCRIPTIONS

Pin #	Name	Description
1	SS/TRK	Soft-Start or Tracking control input. An internal 5 µA current source charges an external capacitor to set the Soft-Start ramp rate. If driven by a external source less than 800 mV, this pin overrides the internal reference that sets the output voltage. If left open, an internal 1ms Soft-Start ramp is activated.
2	FB	Feedback input to the error amplifier from the regulated output. This pin is connected to the inverting input of the internal transconductance error amplifier. An 800 mV reference connected to the non-inverting input of the error amplifier sets the closed loop regulation voltage at the FB pin.
3	PGOOD	Power good output signal. Open drain output indicating the output voltage is regulating within tolerance. A pull-up resistor of 10 to 100 kΩ is recommend for most applications.
4	COMP	External compensation pin. Connect a resistor and capacitor to this pin to compensate the device.
5	NC	Connect this pin to GND to ensure proper operation
6,7	PVIN	Input voltage to the power switches inside the device. These pins should be connected together at the device. A low ESR capacitor should be placed near these pins to stabilize the input voltage.
8,9	SW	Switch pin. The PWM output of the internal power switches.
10,11	PGND	Power ground pin for the internal power switches.
12	EN	Precision enable input for the device. An external voltage divider can be used to set the device turn-on threshold. If not used the EN pin should be connected to PVIN.
13	VCC	Internal 2.7V sub-regulator. This pin should be bypassed with a 1 µF ceramic capacitor.
14	AVIN	Analog input supply that generates the internal bias. Must be connected to PVIN through a low pass RC filter.
15	AGND	Quiet analog ground for the internal bias circuitry.
16	SYNC	Frequency synchronization pin. An external clock connected to this pin will set the switching frequency. If grounded the device will operate at approximately 410 kHz.
EP	Exposed Pad	Exposed metal pad on the underside of the package with a weak electrical connection to ground. It is recommended to connect this pad to the PC board ground plane in order to improve heat dissipation.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

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Absolute Maximum Ratings[1][2]

Voltages from the indicated pins to GND	
AVIN, PVIN, EN, PGOOD, SS/TRK, COMP, FB, SW, SYNC	-0.3V to +6V
Storage Temperature	-65°C to 150°C
Junction Temperature	150°C
Power Dissipation[3]	2.6W
Lead Temperature (Soldering, 10 sec)	260°C
Minimum ESD Rating[4]	±2kV

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) The maximum allowable power dissipation is a function of the maximum junction temperature, T_{J_MAX}, the junctions-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation at any ambient temperature is calculated using: $P_{D_MAX} = (T_{J_MAX} – T_A)/\theta_{JA}$. The maximum power dissipations of 2.6W is determined using T_A = 25°C, θ_{JA} = 25°C/W, and T_{J_MAX} = 125°C. The θ_{JA} specification of 25°C/W listed in the electrical characteristics table is measured with the part surface mounted to a 2" x 2" FR4 4 layer board. See Figure 37 for more detailed θ_{JA} information.
(4) The human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor to each pin.

Operating Ratings

PVIN, AVIN to GND	2.95V to 5.5V
Junction Temperature	−40°C to + 125°C

Electrical Characteristics

Unless otherwise stated, the following conditions apply: AVIN = PVIN = VIN = 5V. Limits in standard type are for T_J = 25°C only, limits in bold face type apply over the junction temperature (T_J) range of -40°C to +125°C. Minimum and Maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{FB}	Feedback pin voltage	V_{IN} = 2.95V to 5.5V	**0.788**	0.8	**0.812**	V
$\Delta V_{OUT}/\Delta I_{OUT}$	Load Regulation	I_{OUT} = 100 mA to 6A		0.04		%/A
I_{CL}	Switch Current Limit Threshold	V_{IN} = 3.3V	**7.65**	8.5	**9.35**	A
R_{DS_ON}	High-Side Switch On Resistance	I_{SW} = 3.5A		20	**27**	mΩ
R_{DS_ON}	Low-Side Switch On Resistance	I_{SW} = 3.5A		16	**23**	mΩ
I_Q	Operating Quiescent Current	Non-switching, $V_{FB} = V_{COMP}$		3.5	**6**	mA
I_{SD}	Shutdown Quiescent current	V_{EN} = 0V		75	**180**	µA
V_{UVLO}	VIN Under Voltage Lockout	Rising V_{IN}	**2.45**	2.7	**2.95**	V
V_{UVLO_HYS}	VIN Under Voltage Lockout Hysteresis	Falling V_{IN}		45	**100**	mV
V_{VCC}	VCC Voltage	I_{VCC} = 0 µA	**2.45**	2.7	**2.95**	V
I_{SS}	Soft-Start Pin Source Current	$V_{SS/TRK}$ = 0V	**2**	4.5	**7**	µA
V_{TRACK}	SS/TRK Accuracy, V_{SS} - V_{FB}	$V_{SS/TRK}$ = 0.4V	**-10**	3	**15**	mV
Oscillator and Clock Synchronization						
F_{OSC}	Oscillator Frequency	V_{SYNC} = Static	**360**	410	**460**	kHz
F_{OSCH}	Maximum SYNC Frequency			1500		kHz
F_{OSCL}	Minimum SYNC Frequency		**460**			kHz
V_{IH_SYNC}	SYNC pin Logic High		**2**			V
V_{IL_SYNC}	SYNC pin Logic Low				**0.8**	V
I_{SYNC}	SYNC pin input leakage	V_{SYNC} = 5V		10		nA
DC_{MAX}	Maximum Duty Cycle	I_{LOAD} = 0A		85		%
T_{ON_TIME}	Minimum On Time			100		ns
T_{CL_BLANK}	Current Sense Blanking Time	After Rising V_{SW}		80		ns
Error Amplifier and Modulator						

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Electrical Characteristics (continued)

Unless otherwise stated, the following conditions apply: AVIN = PVIN = VIN = 5V. Limits in standard type are for T_J = 25°C only, limits in bold face type apply over the junction temperature (T_J) range of -40°C to +125°C. Minimum and Maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{FB}	Feedback pin bias current	V_{FB} = 0.8V		1	**100**	nA
I_{COMP_SRC}	COMP Output Source Current	V_{FB} = 0.6V, V_{COMP} = 0.5V	**80**	100		µA
I_{COMP_SNK}	COMP Output Sink Current	V_{FB} = 1.0V, V_{COMP} = 0.6V	**80**	100		µA
g_m	Error Amplifier Transconductance	I_{COMP} = ± 50 µA	**450**	510	**600**	µmho
A_{VOL}	Error Amplifier Voltage Gain			2000		V/V
Power Good						
V_{OVP}	Over Voltage Protection Rising Threshold	With respect to V_{FB}	**105**	108	**111**	%
V_{OVP_HYS}	Over Voltage Protection Hysteresis			2	**3**	%
V_{PGTH}	PGOOD Rising Threshold	With respect to V_{FB}	**92**	94	**96**	%
V_{PGHYS}	PGOOD Falling Hysteresis			2	**3**	%
T_{PGOOD}	PGOOD deglitch time			16		µs
I_{OL}	PGOOD Low Sink Current	V_{PGOOD} = 0.4V	**0.6**	1		mA
I_{OH}	PGOOD High Leakage Current	V_{PGOOD} = 5V		5	**100**	nA
Enable						
V_{IH_EN}	EN Pin Turn on Threshold	V_{EN} Rising	**1.08**	1.18	**1.28**	V
V_{EN_HYS}	EN Pin Hysteresis			66		mV
Thermal Shutdown						
T_{SD}	Thermal Shutdown			160		°C
T_{SD_HYS}	Thermal Shutdown Hysteresis			10		°C
Thermal Resistance						
θ_{JA}	Junction to Ambient	See(1)		25		°C/W

(1) The maximum allowable power dissipation is a function of the maximum junction temperature, T_{J_MAX}, the junctions-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation at any ambient temperature is calculated using: $P_{D_MAX} = (T_{J_MAX} - T_A)/\theta_{JA}$. The maximum power dissipations of 2.6W is determined using T_A = 25°C, θ_{JA} = 25°C/W, and T_{J_MAX} = 125°C. The θ_{JA} specification of 25°C/W listed in the electrical characteristics table is measured with the part surface mounted to a 2" x 2" FR4 4 layer board. See Figure 37 for more detailed θ_{JA} information.

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Typical Performance Characteristics

Unless otherwise specified: C_{IN} = C_{OUT} = 100µF, L = 1.0µH (TDK SPM6530T-1R0M120), V_{IN} = 5V, V_{OUT} = 1.2V, R_{LOAD} = 1.2Ω, f_{SW} = 1 MHz, T_A = 25°C for efficiency curves, loop gain plots and waveforms, and T_J = 25°C for all others.

Efficiency vs. Load Current (V_{IN} = 5V, f_{SW} = 1 MHz)

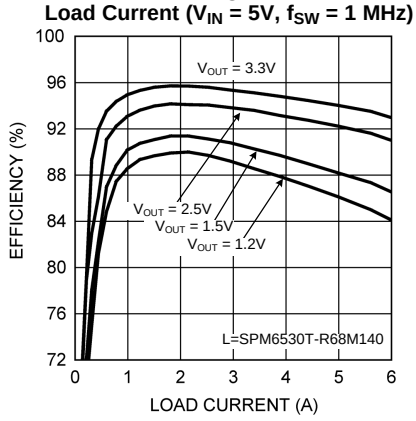


Figure 2.

Efficiency vs. Load Current (V_{IN} = 3.3V, f_{SW} = 1 MHz)

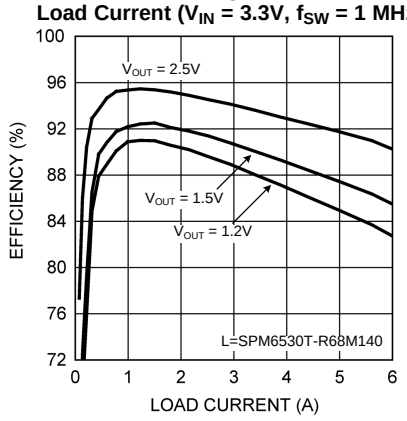


Figure 3.

Efficiency vs. Load Current (V_{IN} = 5V, f_{SW} = 500 kHz)

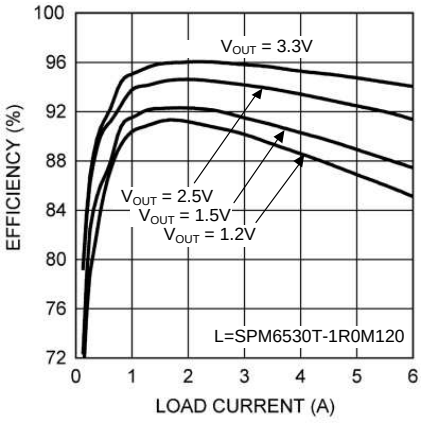


Figure 4.

Efficiency vs. Load Current (V_{IN} = 3.3V, f_{SW} = 500 kHz)

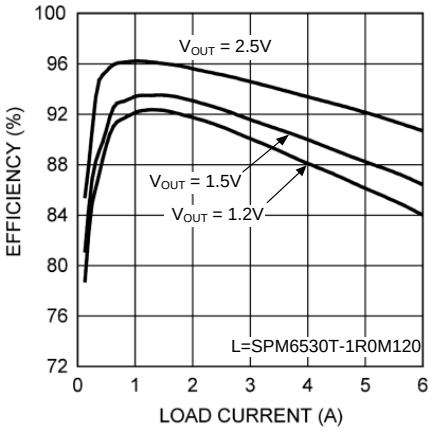


Figure 5.

High-Side FET resistance vs. Temperature (T_J)

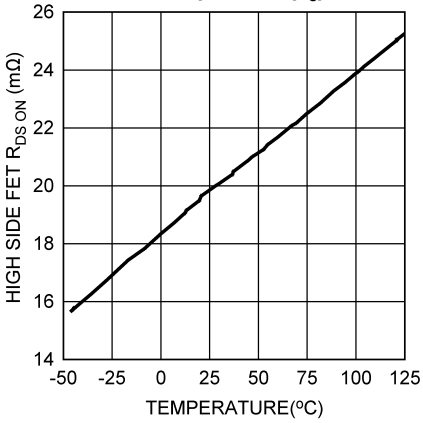


Figure 6.

Low-Side FET resistance vs. Temperature (T_J)

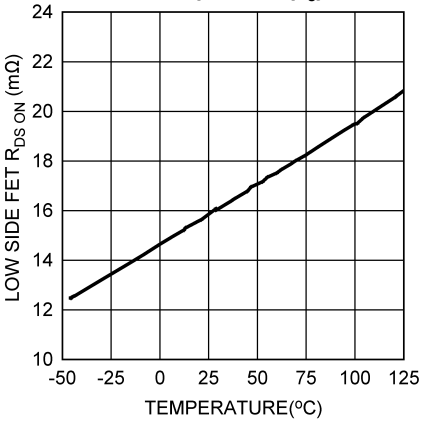


Figure 7.

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Typical Performance Characteristics (continued)

Unless otherwise specified: $C_{IN} = C_{OUT} = 100\mu F$, L = 1.0µH (TDK SPM6530T-1R0M120), $V_{IN} = 5V$, $V_{OUT} = 1.2V$, $R_{LOAD} = 1.2\Omega$, $f_{SW} = 1$ MHz, $T_A = 25°C$ for efficiency curves, loop gain plots and waveforms, and $T_J = 25°C$ for all others.

Error Amplifier Gain vs. Frequency

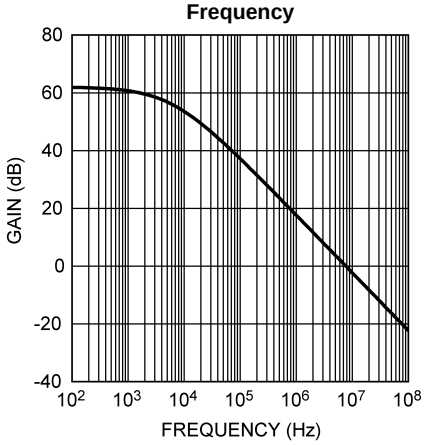


Figure 8.

Line Regulation

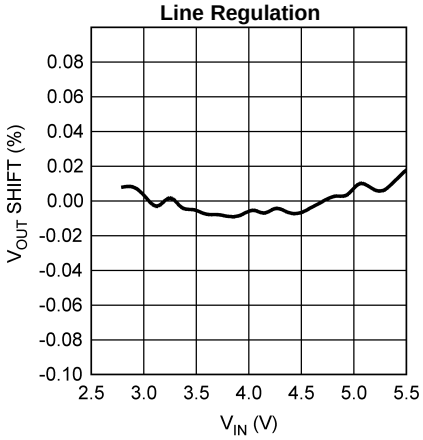


Figure 9.

Load Regulation

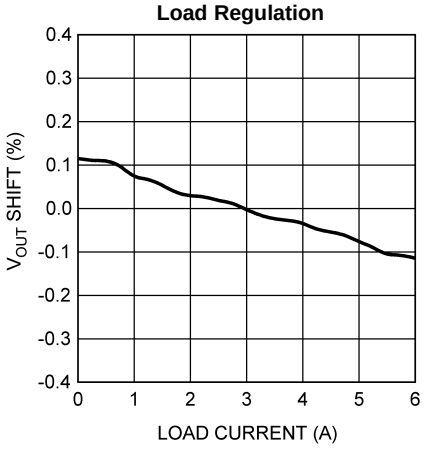


Figure 10.

Feedback Pin Voltage vs. Temperature (T_J)

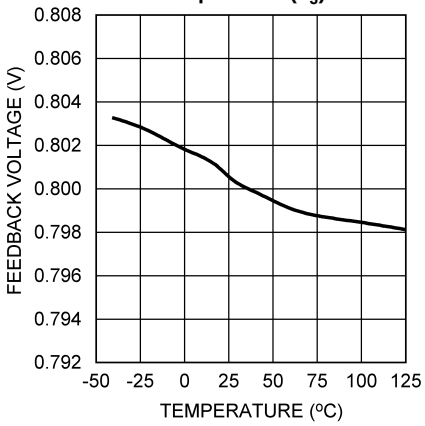


Figure 11.

Switching Frequency vs. Temperature (T_J)

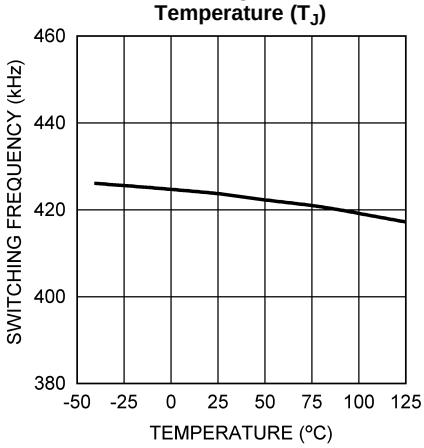


Figure 12.

Switch Synchronization

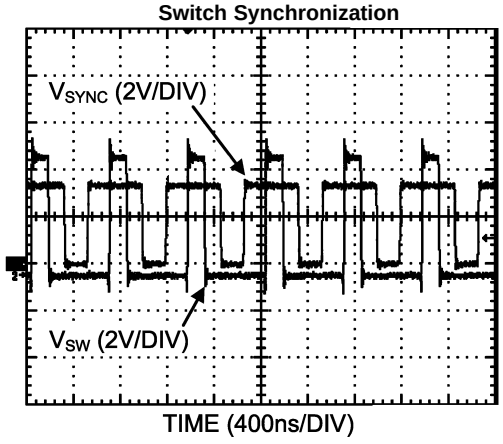


Figure 13.

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Typical Performance Characteristics (continued)

Unless otherwise specified: $C_{IN} = C_{OUT} = 100\mu F$, $L = 1.0\mu H$ (TDK SPM6530T-1R0M120), $V_{IN} = 5V$, $V_{OUT} = 1.2V$, $R_{LOAD} = 1.2\Omega$, $f_{SW} = 1$ MHz, $T_A = 25°C$ for efficiency curves, loop gain plots and waveforms, and $T_J = 25°C$ for all others.

Quiescent Current vs. Temperature (Not Switching)

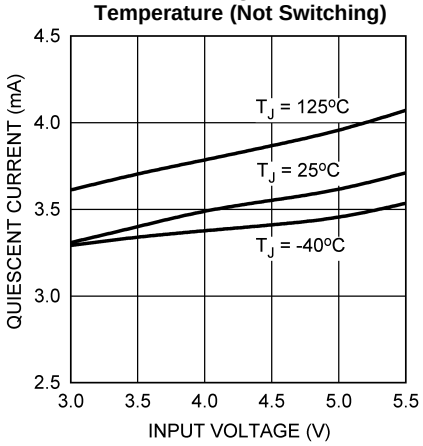


Figure 14.

Shutdown Current vs. V_{IN}

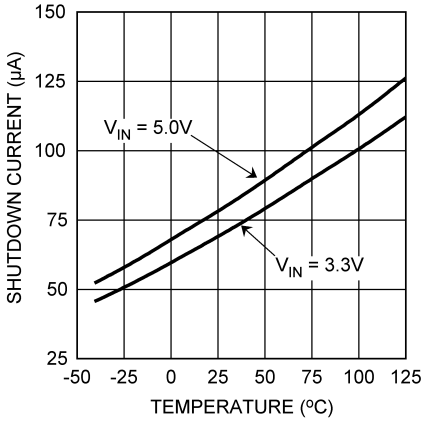


Figure 15.

Enable Threshold vs. Temperature (T_J)

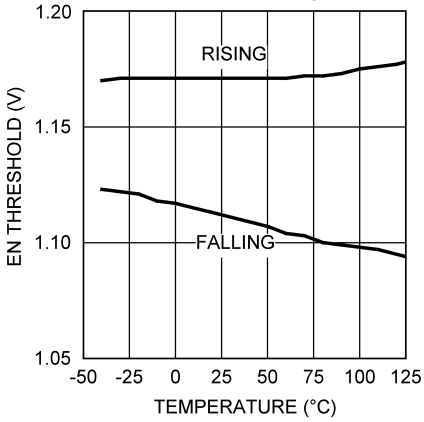


Figure 16.

UVLO Threshold vs. Temperature (T_J)

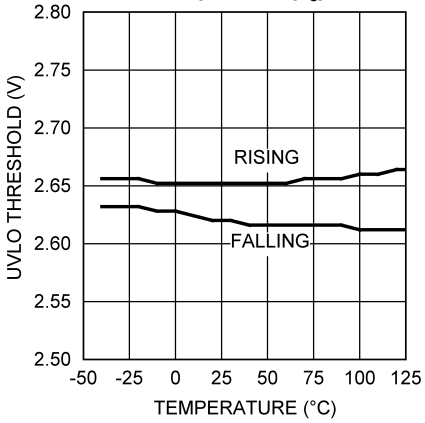


Figure 17.

Peak Current Limit vs. Temperature (T_J)

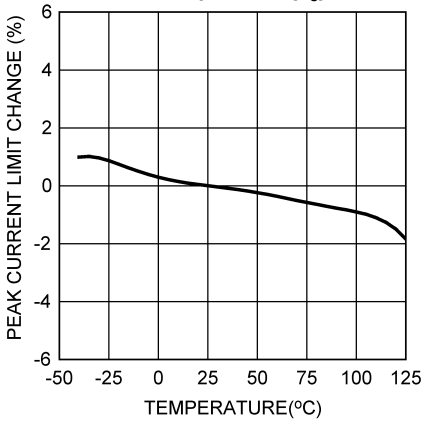


Figure 18.

Peak Current Limit vs. V_{OUT}

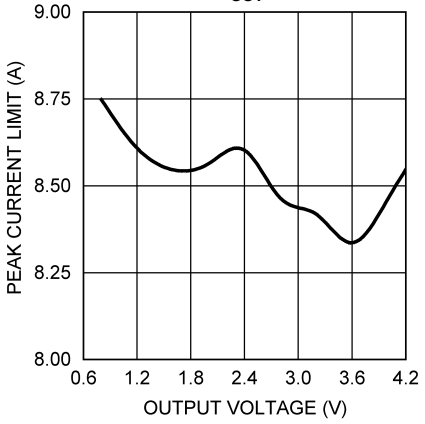


Figure 19.

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Typical Performance Characteristics (continued)

Unless otherwise specified: $C_{IN} = C_{OUT} = 100\mu F$, L = 1.0µH (TDK SPM6530T-1R0M120), V_{IN} = 5V, V_{OUT} = 1.2V, R_{LOAD} = 1.2Ω, f_{SW} = 1 MHz, T_A = 25°C for efficiency curves, loop gain plots and waveforms, and T_J = 25°C for all others.

Peak Current Limit vs. V_{IN}

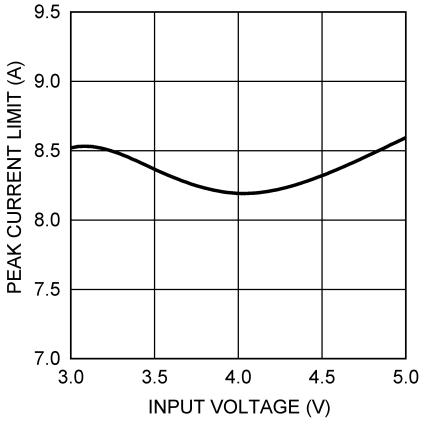


Figure 20.

Load Transient Response

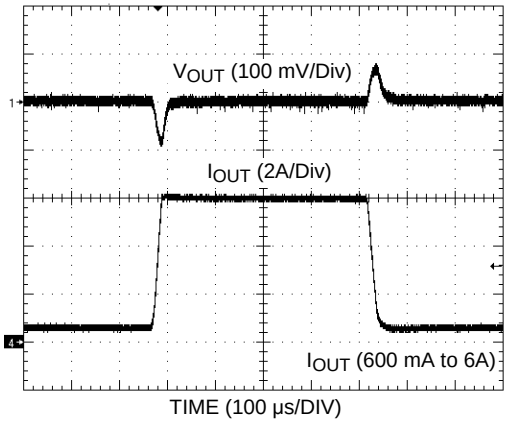


Figure 21.

Line Transient Response

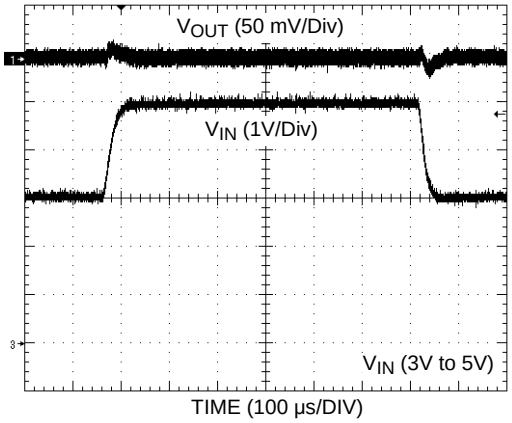


Figure 22.

Start-Up (Soft-Start)

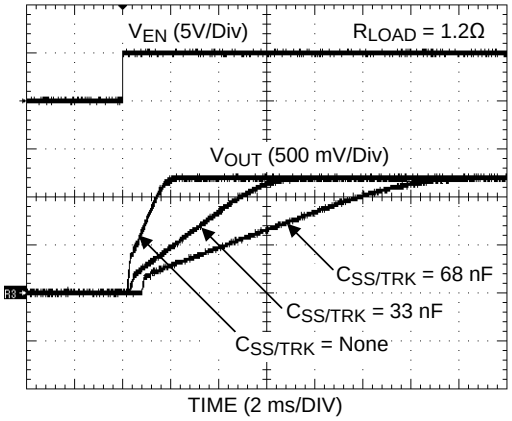


Figure 23.

Start-Up (Tracking)

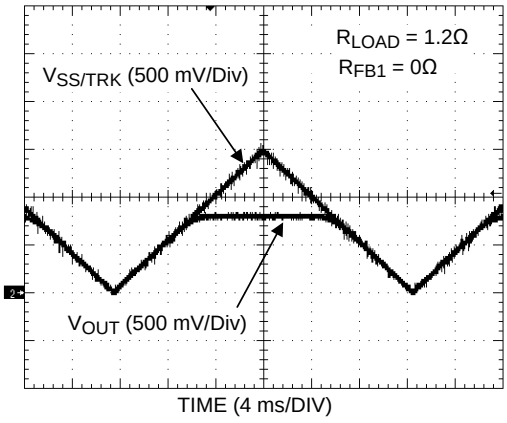


Figure 24.

Power Down

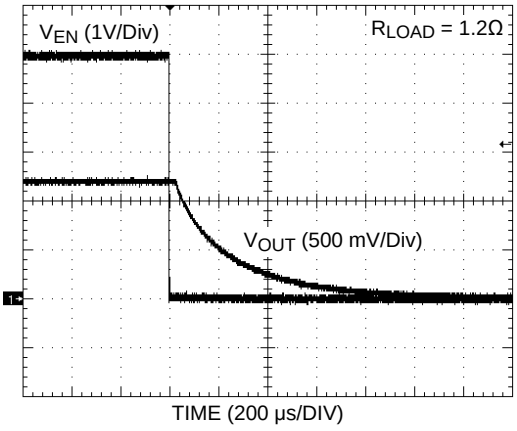


Figure 25.

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Typical Performance Characteristics (continued)

Unless otherwise specified: C_{IN} = C_{OUT} = 100µF, L = 1.0µH (TDK SPM6530T-1R0M120), V_{IN} = 5V, V_{OUT} = 1.2V, R_{LOAD} = 1.2Ω, f_{SW} = 1 MHz, T_A = 25°C for efficiency curves, loop gain plots and waveforms, and T_J = 25°C for all others.

Short Circuit Input Current vs. V_{IN}

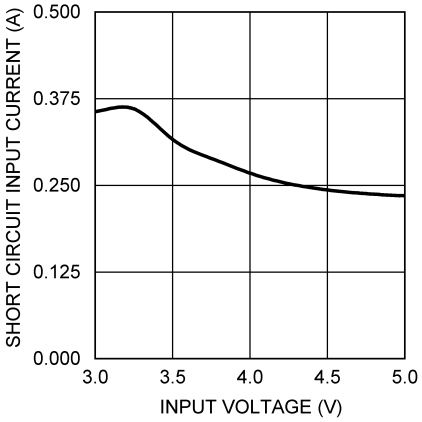


Figure 26.

P_{GOOD} vs. I_{PGOOD}

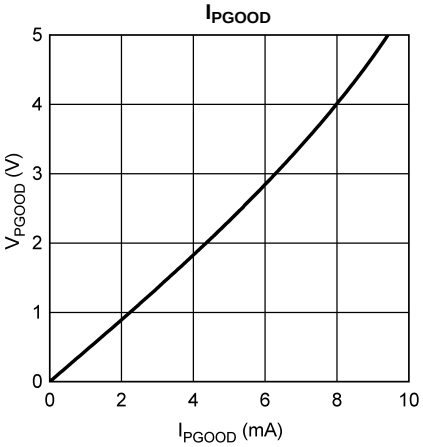
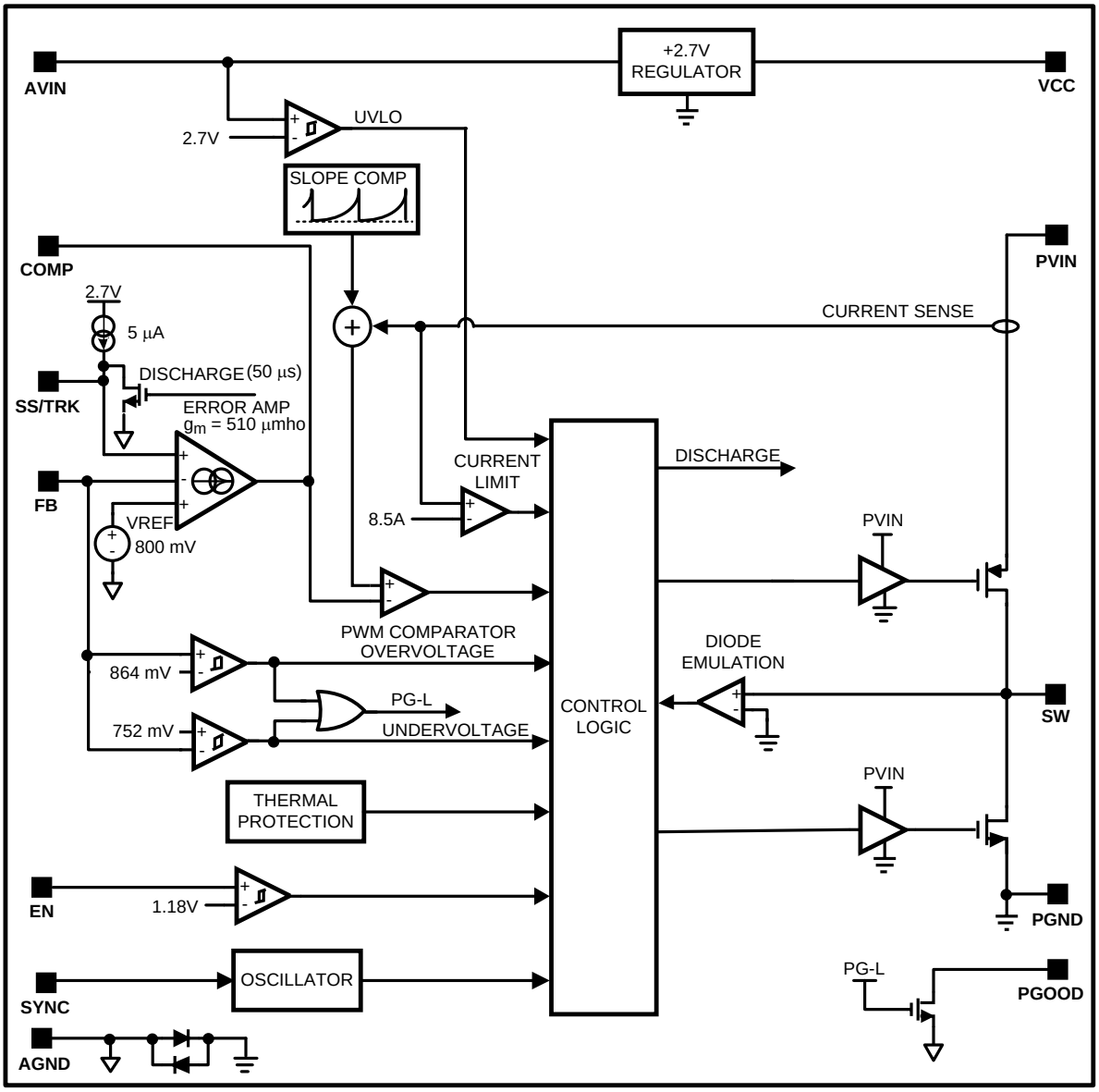


Figure 27.

Block Diagram



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OPERATION DESCRIPTION

General

The LM20136 switching regulator features all of the functions necessary to implement an efficient low voltage buck regulator using a minimum number of external components. This easy to use regulator features two integrated switches and is capable of supplying up to 6A of continuous output current. The regulator utilizes peak current mode control with nonlinear slope compensation to optimize stability and transient response over the entire output voltage range. Peak current mode control also provides inherent line feed-forward, cycle-by-cycle current limiting and easy loop compensation. The internal oscillator can synchronize up to 1.5 MHz minimizing the inductor size while still achieving efficiencies up to 96%. The precision internal voltage reference allows the output to be set as low as 0.8V. Fault protection features include: current limiting, thermal shutdown, over voltage protection, and shutdown capability. The device is available in the HTSSOP package featuring an exposed pad to aid thermal dissipation. The LM20136 can be used in numerous applications to efficiently step-down from a 5V or 3.3V bus. The typical application circuit for the LM20136 is shown in Figure 30 in the design guide.

Precision Enable

The enable (EN) pin allows the output of the device to be enabled or disabled with an external control signal. This pin is a precision analog input that enables the device when the voltage exceeds 1.18V (typical). The EN pin has 66 mV of hysteresis and will disable the output when the enable voltage falls below 1.11V (typical). If the EN pin is not used, it should be connected to V_{IN}. Since the enable pin has a precise turn on threshold it can be used along with an external resistor divider network from V_{IN} to configure the device to turn on at a precise input voltage. The precision enable circuitry will remain active even when the device is disabled.

Frequency Synchronization

The frequency synchronization pin (SYNC) allows the switching frequency of the device to be controlled with an external clock signal. This feature allows the user to synchronize multiple converters, avoiding undesirable frequency bands of operation. Multiple devices can be configured to switch out of phase reducing input capacitor requirements and EMI of the power supply system.

The turn on of the high-side switch will lock-on to the rising edge of the SYNC pin input. The logic low level for the input clock must be below 0.8V and the logic high level must exceed 2.0V to ensure proper operation. The device will synchronize to frequencies from 500 kHz to 1.5 MHz. If the synchronization clock is removed or not present during startup, the oscillator of the device will run at approximately 410 kHz. If the SYNC pin is not used it should be connected to ground.

Peak Current Mode Control

In most cases, the peak current mode control architecture used in the LM20136 only requires two external components to achieve a stable design. The compensation can be selected to accommodate any capacitor type or value. The external compensation also allows the user to set the crossover frequency and optimize the transient performance of the device.

For duty cycles above 50% all current mode control buck converters require the addition of an artificial ramp to avoid sub-harmonic oscillation. This artificial linear ramp is commonly referred to as slope compensation. What makes the LM20136 unique is the amount of slope compensation will change depending on the output voltage. When operating at high output voltages the device will have more slope compensation than when operating at lower output voltages. This is accomplished in the LM20136 by using a non-linear parabolic ramp for the slope compensation. The parabolic slope compensation of the LM20136 is much better than the traditional linear slope compensation because it optimizes the stability of the device over the entire output voltage range.

Current Limit

The precise current limit of the LM20136 is set at the factory to be within 10% over the entire operating temperature range. This enables the device to operate with smaller inductors that have lower saturation currents. When the peak inductor current reaches the current limit threshold, an over current event is triggered and the internal high-side FET turns off and the low-side FET turns on allowing the inductor current to ramp down until the next switching cycle. For each sequential over-current event, the reference voltage is decremented and PWM pulses are skipped resulting in a current limit that does not aggressively fold back for brief over-current events, while at the same time providing frequency and voltage foldback protection during hard short circuit conditions.

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Soft-Start and Voltage Tracking

The SS/TRK pin is a dual function pin that can be used to set the start up time or track an external voltage source. The start up or Soft-Start time can be adjusted by connecting a capacitor from the SS/TRK pin to ground. The Soft-Start feature allows the regulator output to gradually reach the steady state operating point, thus reducing stresses on the input supply and controlling start up current. If no Soft-Start capacitor is used the device defaults to the internal Soft-Start circuitry resulting in a start up time of approximately 1ms. For applications that require a monotonic start up or utilize the PGOOD pin, an external Soft-Start capacitor is recommended. The SS/TRK pin can also be set to track an external voltage source. The tracking behavior can be adjusted by two external resistors connected to the SS/TRK pin as shown in Figure 35 in the design guide.

Pre-Bias Start up Capability

The LM20136 is in a pre-biased state when the device starts up with an output voltage greater than zero. This often occurs in many multi-rail applications such as when powering an FPGA, ASIC, or DSP. In these applications the output can be pre-biased through parasitic conduction paths from one supply rail to another. Even though the LM20136 is a synchronous converter it will not pull the output low when a pre-bias condition exists. During start up the LM20136 will not sink current until the Soft-Start voltage exceeds the voltage on the FB pin. Since the device can not sink current it protects the load from damage that might otherwise occur if current is conducted through the parasitic paths of the load.

Power Good and Over Voltage Fault Handling

The LM20136 has built in under and over voltage comparators that control the power switches. Whenever there is an excursion in output voltage above the set OVP threshold, the part will terminate the present on-pulse, turn on the low-side FET, and pull the PGOOD pin low. The low-side FET will remain on until either the FB voltage falls back into regulation or the zero cross detection is triggered which in turn tri-states the FETs. If the output reaches the UVP threshold the part will continue switching and the PGOOD pin will be asserted and go low. Typical values for the PGOOD resistor are on the order of 100 kΩ or less. To avoid false tripping during transient glitches the PGOOD pin has 16 µs of built in deglitch time to both rising and falling edges.The powergood behavior for fault conditions is illustrated in Figure 28

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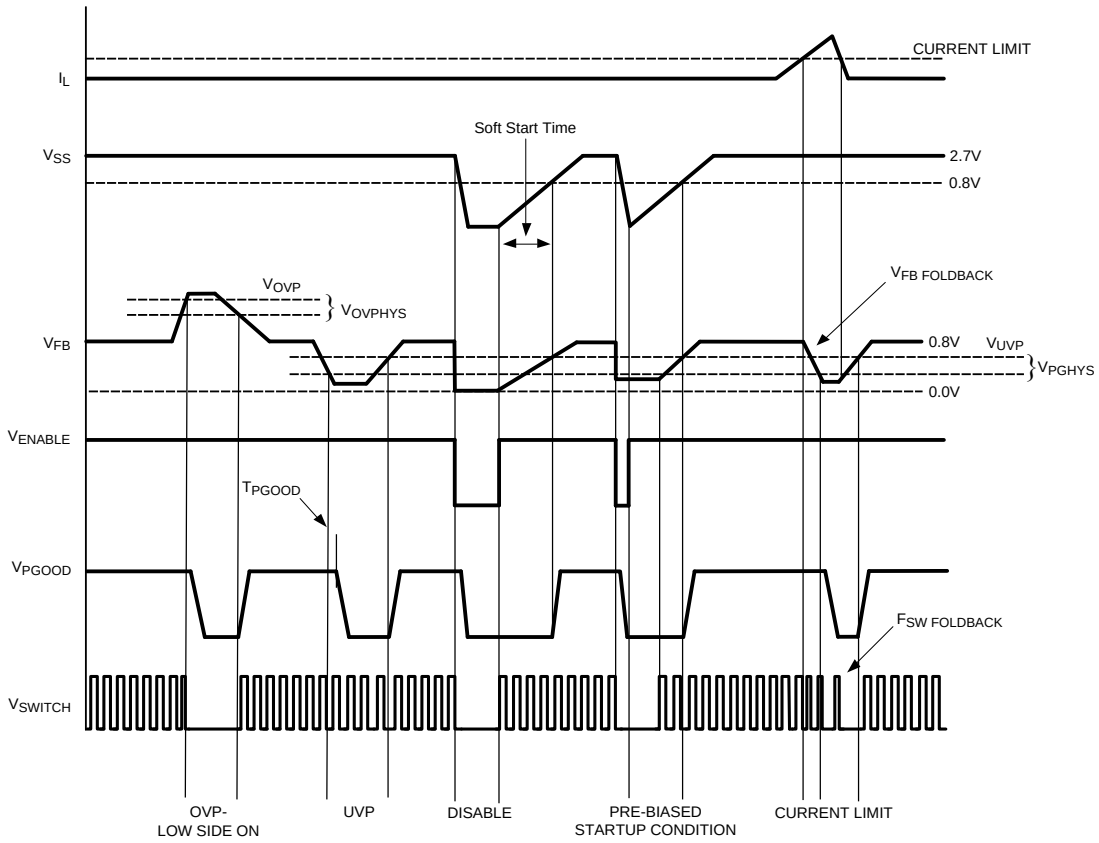


Figure 28. Powergood Behavior

UVLO

The LM20136 has a built-in under-voltage lockout protection circuit that keeps the device from switching until the input voltage reaches 2.7V (typical). The UVLO threshold has 45 mV of hysteresis that keeps the device from responding to power-on glitches during start up. If desired the turn-on point of the supply can be changed by using the precision enable pin and a resistor divider network connected to V_{IN} as shown in Figure 34 in the design guide.

Thermal Protection

Internal thermal shutdown circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. When activated, typically at 160°C, the LM20136 tri-states the power FETs and resets soft start. After the junction cools to approximately 150°C, the part starts up using the normal start up routine. This feature is provided to prevent catastrophic failures from accidental device overheating.

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Light Load Operation

The LM20136 offers increased efficiency when operating at light loads. Whenever the load current is reduced to a point where the peak to peak inductor ripple current is greater than two times the load current, the part will enter the diode emulation mode preventing significant negative inductor current. The point at which this occurs is the critical conduction boundary and can be calculated by the following equation:

$$I_{BOUNDARY} = \frac{(V_{IN} - V_{OUT}) \times D}{2 \times L \times f_{SW}} \quad (1)$$

Several diagrams are shown in Figure 29 illustrating continuous conduction mode (CCM), discontinuous conduction mode, and the boundary condition.

It can be seen that in diode emulation mode, whenever the inductor current reaches zero the SW node will become high impedance. Ringing will occur on this pin as a result of the LC tank circuit formed by the inductor and the parasitic capacitance at the node. If this ringing is of concern an additional RC snubber circuit can be added from the switch node to ground.

At very light loads, usually below 100mA, several pulses may be skipped in between switching cycles, effectively reducing the switching frequency and further improving light-load efficiency.

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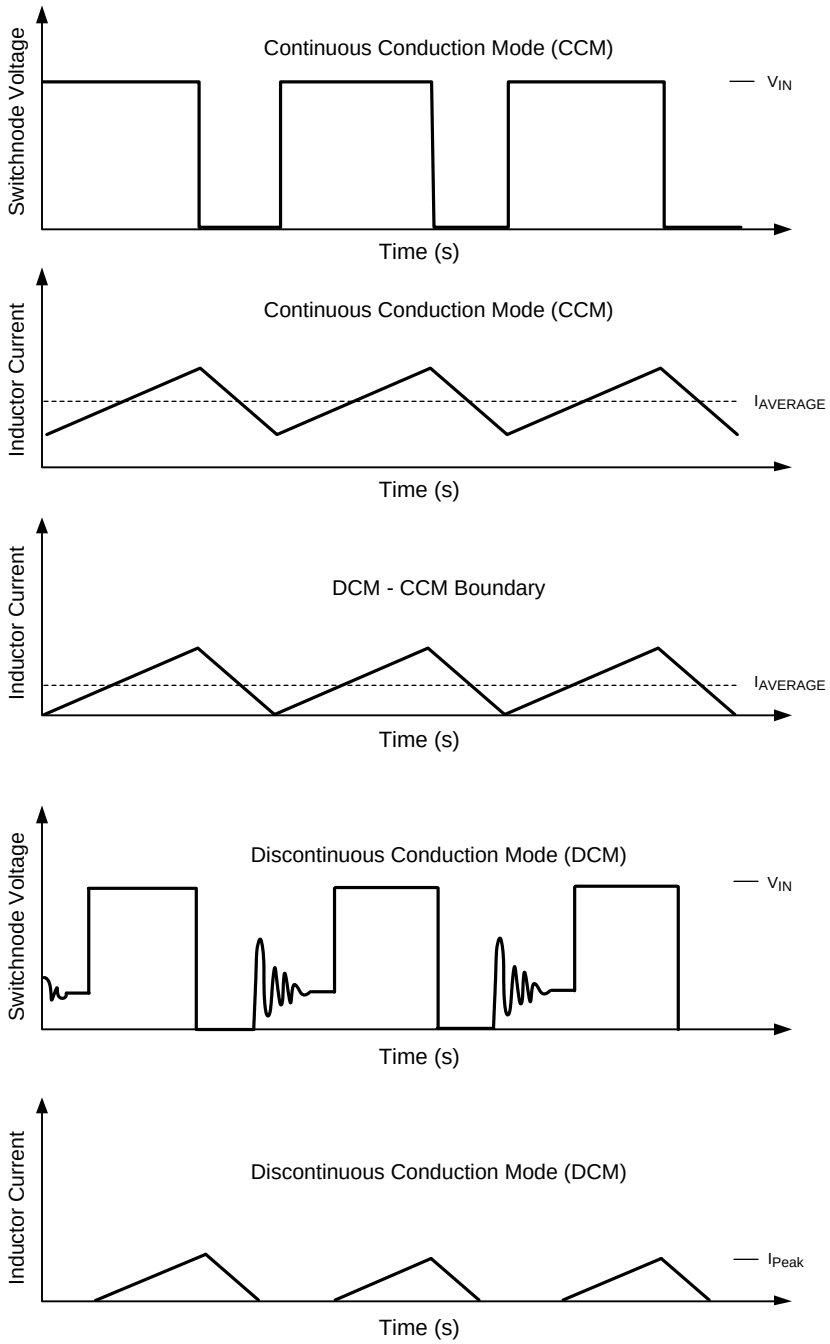


Figure 29. Modes of Operation for LM20136

Design Guide

This section walks the designer through the steps necessary to select the external components to build a fully functional power supply. As with any DC-DC converter numerous trade-offs are possible to optimize the design for efficiency, size, or performance. These will be taken into account and highlighted throughout this discussion. To facilitate component selection discussions the circuit shown in Figure 30 below may be used as a reference. Unless otherwise indicated all formulas assume units of Amps (A) for current, Farads (F) for capacitance, Henries (H) for inductance and Volts (V) for voltage.

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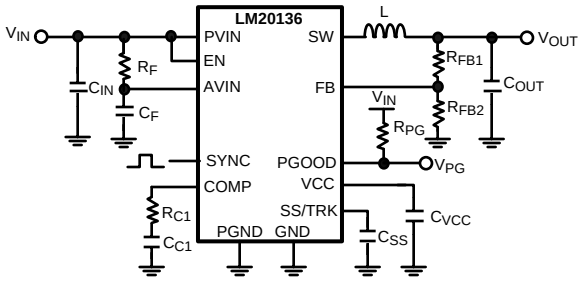


Figure 30. Typical Application Circuit

The first equation to calculate for any buck converter is duty-cycle. Ignoring conduction losses associated with the FETs and parasitic resistances it can be approximated by:

$$D = \frac{V_{OUT}}{V_{IN}} \tag{2}$$

Inductor Selection (L)

The inductor value is determined based on the operating frequency, load current, ripple current, and duty cycle.

The inductor selected should have a saturation current rating greater than the peak current limit of the device. Keep in mind the specified current limit does not account for delay of the current limit comparator, therefore the current limit in the application may be higher than the specified value. To optimize the performance and prevent the device from entering current limit at maximum load, the inductance is typically selected such that the ripple current, Δi_L, is less than 30% of the rated output current. Figure 31, shown below illustrates the switch and inductor ripple current waveforms. Once the input voltage, output voltage, operating frequency, and desired ripple current are known, the minimum value for the inductor can be calculated by the formula shown below:

$$L_{MIN} = \frac{(V_{IN} - V_{OUT}) \times D}{\Delta i_L \times f_{SW}} \tag{3}$$

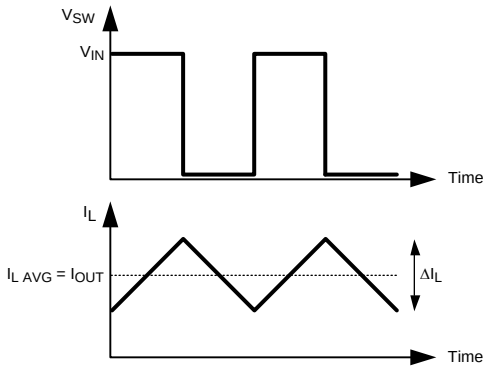


Figure 31. Switch and Inductor Current Waveforms

If needed, slightly smaller value inductors can be used, however, the peak inductor current, $I_{OUT} + \Delta i_L/2$, should be kept below the peak current limit of the device. In general, the inductor ripple current, Δi_L, should be greater than 10% of the rated output current to provide adequate current sense information for the current mode control loop. If the ripple current in the inductor is too low, the control loop will not have sufficient current sense information and can be prone to instability.

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Output Capacitor Selection (C_{OUT})

The output capacitor, C_{OUT}, filters the inductor ripple current and provides a source of charge for transient load conditions. A wide range of output capacitors may be used with the LM20136 that provide excellent performance. The best performance is typically obtained using ceramic, SP, or OSCON type chemistries. Typical trade-offs are that the ceramic capacitor provides extremely low ESR to reduce the output ripple voltage and noise spikes, while the SP and OSCON capacitors provide a large bulk capacitance in a small volume for transient loading conditions.

When selecting the value for the output capacitor the two performance characteristics to consider are the output voltage ripple and transient response. The output voltage ripple can be approximated by using the formula shown below.

$$\Delta V_{OUT} = \Delta i_L \times \left[ESR + \frac{1}{8 \times f_{SW} \times C_{OUT}} \right]$$

where

- ΔV_{OUT} (V) is the amount of peak to peak voltage ripple at the power supply output
- R_{ESR} (Ω) is the series resistance of the output capacitor
- f_{SW}(Hz) is the switching frequency
- C_{OUT} (F) is the output capacitance used in the design (4)

The amount of output ripple that can be tolerated is application specific; however a general recommendation is to keep the output ripple less than 1% of the rated output voltage. Keep in mind ceramic capacitors are sometimes preferred because they have very low ESR; however, depending on package and voltage rating of the capacitor the value of the capacitance can drop significantly with applied voltage. The output capacitor selection will also affect the output voltage droop during a load transient. The peak droop on the output voltage during a load transient is dependent on many factors; however, an approximation of the transient droop ignoring loop bandwidth can be obtained using the following equation.

$$V_{DROOP} = \Delta I_{OUTSTEP} \times R_{ESR} + \frac{L \times \Delta I_{OUTSTEP}^2}{C_{OUT} \times (V_{IN} - V_{OUT})}$$

where

- C_{OUT} (F) is the minimum required output capacitance
- L (H) is the value of the inductor, V_{DROOP} (V) is the output voltage drop ignoring loop bandwidth considerations
- $\Delta I_{OUTSTEP}$ (A) is the load step change
- R_{ESR} (Ω) is the output capacitor ESR
- V_{IN} (V) is the input voltage
- V_{OUT} (V) is the set regulator output voltage (5)

Both the tolerance and voltage coefficient of the capacitor needs to be examined when designing for a specific output ripple or transient drop target.

Input Capacitor Selection (C_{IN})

Good quality input capacitors are necessary to limit the ripple voltage at the V_{IN} pin while supplying most of the switch current during the on-time. In general it is recommended to use a ceramic capacitor for the input as they provide both a low impedance and small footprint. One important note is to use a good dielectric for the ceramic capacitor such as X5R or X7R. These provide better over temperature performance and also minimize the DC voltage derating that occurs on Y5V capacitors. For most applications, a 22 µF, X5R, 6.3V input capacitor is sufficient; however, additional capacitance may be required if the connection to the input supply is far from the PVIN pins. The input capacitor should be placed as close as possible PVIN and PGND pins of the device.

Non-ceramic input capacitors should be selected for RMS current rating and minimum ripple voltage. A good approximation for the required ripple current rating is given by the relationship:

$$I_{IN\text{-}RMS} = I_{OUT} \sqrt{D(1 - D)} \quad (6)$$

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As indicated by the RMS ripple current equation, highest requirement for RMS current rating occurs at 50% duty cycle. For this case, the RMS ripple current rating of the input capacitor should be greater than half the output current. For best performance, low ESR ceramic capacitors should be placed in parallel with higher capacitance capacitors to provide the best input filtering for the device.

Setting the Output Voltage (R_{FB1}, R_{FB2})

The resistors R_{FB1} and R_{FB2} are selected to set the output voltage for the device. Table 1, shown below, provides suggestions for R_{FB1} and R_{FB2} for common output voltages.

Table 1. Suggested Values for R_{FB1} and R_{FB2}

R_{FB1}(kΩ)	R_{FB2}(kΩ)	V_{OUT}
short	open	0.8
4.99	10	1.2
8.87	10.2	1.5
12.7	10.2	1.8
21.5	10.2	2.5
31.6	10.2	3.3

If different output voltages are required, R_{FB2} should be selected to be between 4.99 kΩ to 49.9 kΩ and R_{FB1} can be calculated using the equation below.

$$R_{FB1} = \left(\frac{V_{OUT}}{0.8} - 1 \right) \times R_{FB2} \tag{7}$$

Loop Compensation (R_{C1}, C_{C1})

The purpose of loop compensation is to meet static and dynamic performance requirements while maintaining adequate stability. Optimal loop compensation depends on the output capacitor, inductor, load, and the device itself. Table 2 below gives values for the compensation network that will result in a stable system when using a 100 µF, 6.3V ceramic X5R output capacitor and 1 µH inductor.

Table 2. Recommended Compensation for C_{OUT} = 100 µF, L = 1.5 µH & f_{SW} = 500 kHz

V_{IN}	V_{OUT}	C_{C1} (nF)	R_{C1} (kΩ)
5.00	3.30	2.2	15.4
5.00	2.50	2.2	13.3
5.00	1.80	2.2	10.7
5.00	1.50	2.2	9.31
5.00	1.20	2.2	7.87
5.00	0.80	2.7	4.42
3.30	2.50	2.7	8.45
3.30	1.80	2.7	7.5
3.30	1.50	2.7	6.81
3.30	1.20	2.7	5.9
3.30	0.80	2.7	4.32

If the desired solution differs from the table above the loop transfer function should be analyzed to optimize the loop compensation. The overall loop transfer function is the product of the power stage and the feedback network transfer functions. For stability purposes, the objective is to have a loop gain slope that is -20db/decade from a very low frequency to beyond the crossover frequency. Figure 32, shown below, shows the transfer functions for power stage, feedback/compensation network, and the resulting closed loop system for the LM20136.

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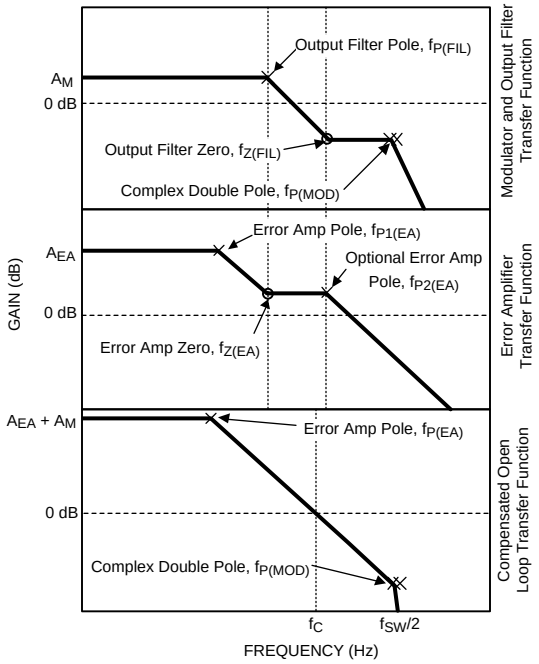


Figure 32. LM20136 Loop Compensation

The power stage transfer function is dictated by the modulator, output LC filter, and load; while the feedback transfer function is set by the feedback resistor ratio, error amp gain, and external compensation network.

To achieve a -20dB/decade slope, the error amplifier zero, located at $f_{Z(EA)}$, should positioned to cancel the output filter pole ($f_{P(FIL)}$). An additional error amp pole, located at $f_{P2(EA)}$, can be added to cancel the output filter zero at ($f_{Z(FIL)}$). Cancellation of the output filter zero is recommended if larger value, non-ceramic output capacitors are used.

Compensation of the LM20136 is achieved by adding an RC network as shown in Figure 33 below.

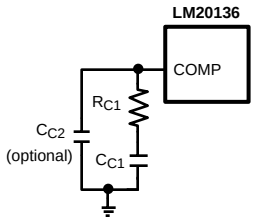


Figure 33. Compensation Network for LM20136

A good starting value for C_{C1} for most applications is 3.3nF. Once the value of C_{C1} is chosen the value of RC should be calculated using the equation below to cancel the output filter pole ($f_{P(FIL)}$) as shown in Figure 32.

$$R_{C1} = \left[\frac{C_{C1}}{C_{OUT}} \times \left[\frac{I_{OUT}}{V_{OUT}} + \frac{1\text{-}D}{f_{SW} \times L} + \frac{D \times f_{SW}}{48750 * V_{IN}} - \frac{1}{2 \times f_{SW} \times L} \right] \right]^{-1} \quad (8)$$

A higher crossover frequency can be obtained, usually at the expense of phase margin, by lowering the value of C_{C1} and recalculating the value of R_{C1}. Likewise, increasing C_{C1} and recalculating R_{C1} will provide additional phase margin at a lower crossover frequency. As with any attempt to compensate the LM20136 the stability of the system should be verified for desired transient droop and settling time.

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If the output filter zero, ($f_{Z(FIL)}$) approaches the crossover frequency (F_C), an additional capacitor (C_{C2}) should be placed at the COMP pin to ground. This capacitor adds a pole to cancel the output filter zero assuring the crossover frequency will occur before the double pole at $f_{SW}/2$ degrades the phase margin. The output filter zero is set by the output capacitor value and ESR as shown in the equation below.

$$f_{Z(FIL)} = \frac{1}{2 \times \pi \times C_{OUT} \times R_{ESR}} \quad (9)$$

If needed, the value for C_{C2} should be calculated using the equation shown below.

$$C_{C2} = \frac{C_{OUT} \times R_{ESR}}{R_{C1}}$$

where

- R_{ESR} is the output capacitor series resistance
- R_{C1} is the calculated compensation resistance (10)

AVIN Filtering Components (C_F and R_F)

To prevent high frequency noise spikes from disturbing the sensitive analog circuitry connected to the AVIN and AGND pins, a high frequency RC filter is required between PVIN and AVIN. These components are shown in Figure 30 as C_F and R_F. The required value for R_F is 1Ω. C_F must be used. Recommended value of C_F is 1.0 µF. The filter capacitor, C_F should be placed as close to the IC as possible with a direct connection from AVIN to AGND. A good quality X5R or X7R ceramic capacitor should be used for C_F.

Sub-Regulator Bypass Capacitor (C_{VCC})

The capacitor at the VCC pin provides noise filtering and stability for the internal sub-regulator. The recommended value of C_{VCC} should be no smaller than 1 µF and no greater than 10 µF. The capacitor should be a good quality ceramic X5R or X7R capacitor. In general, a 1 µF ceramic capacitor is recommended for most applications.

Setting the Start up Time (C_{SS})

The addition of a capacitor connected from the SS pin to ground sets the time at which the output voltage will reach the final regulated value. Larger values for C_{SS} will result in longer start up times. Table 3, shown below provides a list of soft start capacitors and the corresponding typical start up times.

Table 3. Start Up Times for Different Soft-Start Capacitors

Start Up Time (ms)	C_{SS} (nF)
1	none
5	33
10	68
15	100
20	120

If different start up times are needed the equation shown below can be used to calculate the start up time.

$$t_{SS} = \frac{0.8V \times C_{SS}}{I_{SS}} \quad (11)$$

As shown above, the start up time is influenced by the value of the Soft-Start capacitor C_{SS}(F) and the 5 µA Soft-Start pin current I_{SS}(A). that may be found in the Electrical Characteristics table.

While the Soft-Start capacitor can be sized to meet many start up requirements, there are limitations to its size. The Soft-Start time can never be faster than 1ms due to the internal default 1ms start up time. When the device is enabled there is an approximate time interval of 50 µs when the Soft-Start capacitor will be discharged just prior to the Soft-Start ramp. If the enable pin is rapidly pulsed or the Soft-Start capacitor is large there may not be enough time for C_{SS} to completely discharge resulting in start up times less than predicted. To aid in discharging the Soft-Start capacitor during long disable periods an external 1 MΩ resistor from SS/TRK to ground can be used without greatly affecting the start-up time.

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Using Precision Enable and Power Good

The precision enable(EN) and power good(PGOOD) pins of the LM20136 can be used to address many sequencing requirements. The turn-on of the LM20136 can be controlled with the precision enable pin by using two external resistors as shown in Figure 34

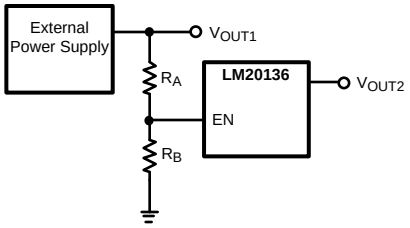


Figure 34. Sequencing LM20136 with Precision Enable

The value for resistor R_B can be selected by the user to control the current through the divider. Typically this resistor will be selected to be between 10 kΩ and 1 MΩ. Once the value for R_B is chosen the resistor R_A can be solved using the equation below to set the desired turn-on voltage.

$$R_A = \left(\frac{V_{TO}}{V_{IH_EN}} - 1 \right) \times R_B \tag{12}$$

When designing for a specific turn-on threshold (V_{TO}) the tolerance on the input supply, enable threshold (V_{IH_EN}), and external resistors needs to be considered to insure proper turn-on of the device.

The LM20136 features an open drain power good (PGOOD) pin to sequence external supplies or loads and to provide fault detection. This pin requires an external resistor (R_{PG}) to pull PGOOD high while when the output is within the PGOOD tolerance window. Typical values for this resistor range from 10 kΩ to 100 kΩ.

Tracking an External Supply

By using a properly chosen resistor divider network connected to the SS/TRK pin, as shown in Figure 35, the output of the LM20136 can be configured to track an external voltage source to obtain a simultaneous or ratiometric start up.

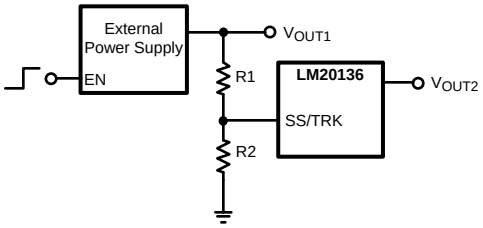


Figure 35. Tracking an External Supply

Since the Soft-Start charging current I_{SS} is always present on the SS/TRK pin, the size of R2 should be less than 10 kΩ to minimize the errors in the tracking output. Once a value for R2 is selected the value for R1 can be calculated using appropriate equation in Figure 36, to give the desired start up. Figure 36 shows two common start up sequences; the top waveform shows a simultaneous start up while the waveform at the bottom illustrates a ratiometric start up.

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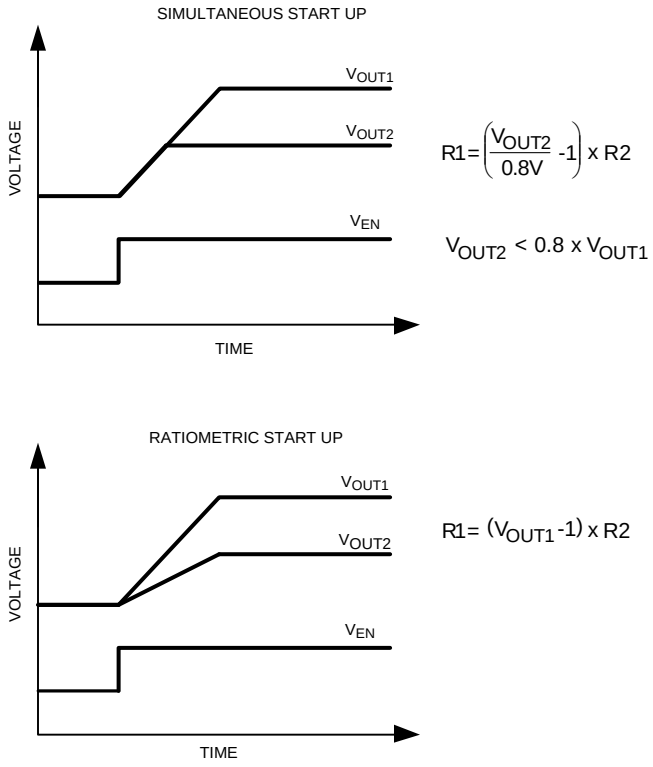


Figure 36. Common Start Up Sequences

A simultaneous start up is preferred when powering most FPGAs, DSPs, or other microprocessors. In these systems the higher voltage, V_{OUT1}, usually powers the I/O, and the lower voltage, V_{OUT2}, powers the core. A simultaneous start up provides a more robust power up for these applications since it avoids turning on any parasitic conduction paths that may exist between the core and the I/O pins of the processor..

The second most common power on behavior is known as a ratiometric start up. This start up is preferred in applications where both supplies need to be at the final value at the same time.

Similar to the Soft-Start function, the fastest start up possible is 1ms regardless of the rise time of the tracking voltage. When using the track feature the final voltage seen by the SS/TRACK pin should exceed 1V to provide sufficient overdrive and transient immunity.

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Thermal Considerations

The thermal characteristics of the LM20136 are specified using the parameter θ_{JA}, which relates the junction temperature to the ambient temperature. Although the value of θ_{JA} is dependant on many variables, it still can be used to approximate the operating junction temperature of the device.

To obtain an estimate of the device junction temperature, one may use the following relationship:

$$T_J = P_D \theta_{JA} + T_A \quad (13)$$

and

$$P_D = P_{IN} \times (1 - \text{Efficiency}) - 1.1 \times I_{OUT}2 \times DCR$$

where

- T_J is the junction temperature in °C
- P_{IN} is the input power in Watts ($P_{IN} = V_{IN} \times I_{IN}$)
- θ_{JA} is the junction to ambient thermal resistance for the LM20136
- T_A is the ambient temperature in °C
- I_{OUT} is the output load current
- DCR is the inductor series resistance (14)

It is important to always keep the operating junction temperature (T_J) below 125°C for reliable operation. If the junction temperature exceeds 160°C the device will cycle in and out of thermal shutdown. If thermal shutdown occurs it is a sign of inadequate heatsinking or excessive power dissipation in the device.

Figure 37, shown below, provides a better approximation of the θ_{JA} for a given PCB copper area. The PCB heatsink area consists of 2oz. copper located on the bottom layer of the PCB directly under the HTSSOP exposed pad. The bottom copper area is connected to the HTSSOP exposed pad by means of a 4 x 4 array of 12 mil thermal vias.

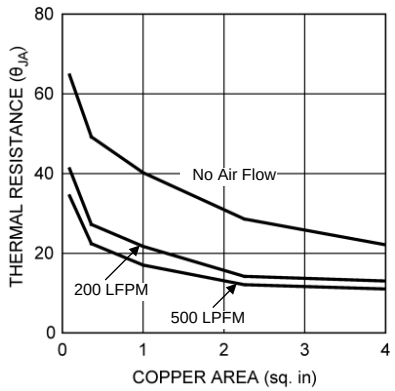


Figure 37. Thermal Resistance vs PCB Area

PCB Layout Considerations

PC board layout is an important part of DC-DC converter design. Poor board layout can disrupt the performance of a DC-DC converter and surrounding circuitry by contributing to EMI, ground bounce, and resistive voltage loss in the traces. These can send erroneous signals to the DC-DC converter resulting in poor regulation or instability.

Good layout can be implemented by following a few simple design rules.

1. Minimize area of switched current loops. In a buck regulator there are two loops where currents are switched rapidly. The first loop starts from the input capacitor, to the regulator VIN pin, to the regulator SW pin, to the inductor then out to the output capacitor and load. The second loop starts from the output capacitor ground, to the regulator PGND pins, to the inductor and then out to the load (see Figure 38). To minimize both loop areas the input capacitor should be placed as close as possible to the PVIN pin. Grounding for both the input and output capacitor should consist of a small localized top side plane that connects to PGND and the die attach pad (DAP). The inductor should be placed as close as possible to the SW pin and output capacitor.

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2. Minimize the copper area of the switch node. Since the LM20136 has the SW pins on opposite sides of the package it is recommended to via these pins down to the bottom or internal layer with 2 to 4 vias on each SW pin. The SW pins should be directly connected with a trace that runs across the bottom of the package. To minimize IR losses this trace should be no smaller that 50 mils wide, but no larger than 100 mils wide to keep the copper area to a minimum. In general the SW pins should not be connected on the top layer since it could block the ground return path for the power ground. The inductor should be placed as close as possible to one of the SW pins to further minimize the copper area of the switch node.

3. Have a single point ground for all device analog grounds located under the DAP. The ground connections for the compensation, feedback, and Soft-Start components should be connected together then routed to the AGND pin of the device. The AGND pin should connect to PGND under the DAP. This prevents any switched or load currents from flowing in the analog ground plane. If not properly handled poor grounding can result in degraded load regulation or erratic switching behavior.

4. Minimize trace length to the FB pin. Since the feedback node can be high impedance the trace from the output resistor divider to FB pin should be as short as possible. This is most important when high value resistors are used to set the output voltage. The feedback trace should be routed away from the SW pin and inductor to avoid contaminating the feedback signal with switch noise.

5. Make input and output bus connections as wide as possible. This reduces any voltage drops on the input or output of the converter and can improve efficiency. If voltage accuracy at the load is important make sure feedback voltage sense is made at the load. Doing so will correct for voltage drops at the load and provide the best output accuracy.

6. Provide adequate device heatsinking. Use as many vias as is possible to connect the DAP to the power plane heatsink. For best results use a 4x4 via array with a minimum via diameter of 12 mils. See the Thermal Considerations section to insure enough copper heatsinking area is used to keep the junction temperature below 125°C.

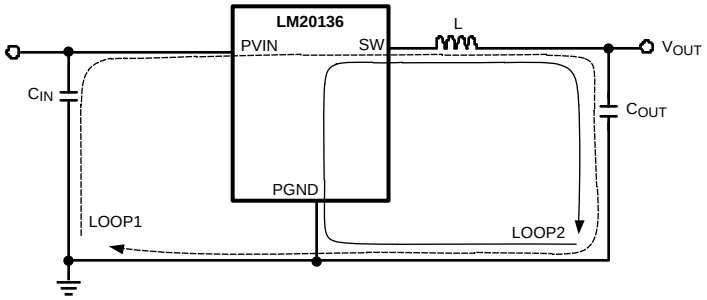


Figure 38. Schematic of LM20136 Highlighting Layout Sensitive Nodes

Typical Application Circuits

This section provides several application solutions with a bill of materials. All bill of materials reference the below figure. The compensation for these solutions were optimized to work over a wide range of input and output voltages; if a faster transient response is needed reduce the value of C_{C1} and calculate the new value for R_{C1} as outlined in the design guide.

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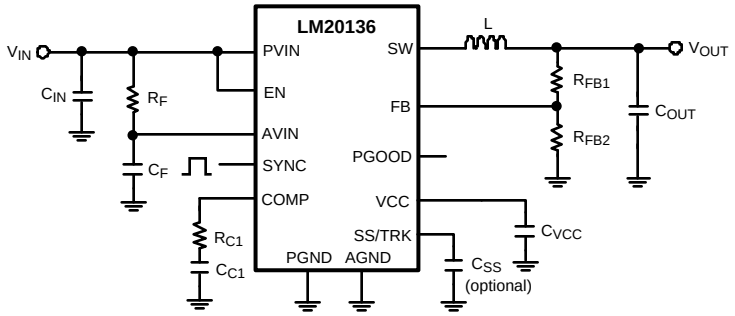


Figure 39.

Bill of Materials (V_{IN} = 5V, V_{OUT} = 3.3V, I_{OUTMAX} = 6A, F_{SYNC} = 500kHz)

Designator	Description	Part Number	Manufacturer	Qty
U1	Synchronous Buck Regulator	LM20136	Texas Instruments	1
C_{IN}	100µF, 1210, X5R, 6.3V	C3225X5R0J107M	TDK	1
C_{OUT}	100µF, 1210, X5R, 6.3V	C3225X5R0J107M	TDK	1
L	1.0 µH, 7.8 mΩ	SPM6530T-1R0M120	TDK	1
R_F	1Ω, 0603	CRCW06031R0J-e3	Vishay-Dale	1
C_F	100nF, 0603, X7R, 16V	GRM188R71C104KA01	Murata	1
C_{VCC}	1µF, 0603, X5R, 6.3V	GRM188R60J105KA01	Murata	1
R_{C1}	14.3 kΩ, 0603	CRCW06031432F-e3	Vishay-Dale	1
C_{C1}	1nF, 0603, COG, 50V	GRM1885C1H102JA01	Murata	1
C_{SS}	33nF, 0603, X7R, 25V	VJ0603Y333KXXA	Vishay-Vitramon	1
R_{FB1}	31.6kΩ, 0603	CRCW06033162F-e3	Vishay-Dale	1
R_{FB2}	10.2kΩ, 0603	CRCW06031022F-e3	Vishay-Dale	1

Bill of Materials (V_{IN} = 3.3V or 5V, V_{OUT} = 1.2V, I_{OUTMAX} = 6A, F_{SYNC} = 1000kHz)

Designator	Description	Part Number	Manufacturer	Qty
U1	Synchronous Buck Regulator	LM20136	Texas Instruments	1
C_{IN}	100µF, 1210, X5R, 6.3V	C3225X5R0J107M	TDK	1
C_{OUT}	100µF, 1210, X5R, 6.3V	C3225X5R0J107M	TDK	1
L	0.68µH, 5.39 mΩ	SPM6530T-R68M140	TDK	1
R_F	1Ω, 0603	CRCW06031R0J-e3	Vishay-Dale	1
C_F	100nF, 0603, X7R, 16V	GRM188R71C104KA01	Murata	1
C_{VCC}	1µF, 0603, X5R, 6.3V	GRM188R60J105KA01	Murata	1
R_{C1}	4.99 kΩ, 0603	CRCW06034992F-e3	Vishay-Dale	1
C_{C1}	1.8nF, 0603, X7R, 25V	VJ0603Y182KXXA	Vishay-Vitramon	1
C_{SS}	33nF, 0603, X7R, 25V	VJ0603Y333KXXA	Vishay-Vitramon	1
R_{FB1}	4.99kΩ, 0603	CRCW06034991F-e3	Vishay-Dale	1
R_{FB2}	10kΩ, 0603	CRCW06031002F-e3	Vishay-Dale	1

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REVISION HISTORY

Changes from Revision A (April 2013) to Revision B	Page
• Changed layout of National Data Sheet to TI format	25

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM20136MH/NOPB	ACTIVE	HTSSOP	PWP	16	92	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	L20136 MH	Samples
LM20136MHE/NOPB	ACTIVE	HTSSOP	PWP	16	250	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	L20136 MH	Samples
LM20136MHX/NOPB	ACTIVE	HTSSOP	PWP	16	2500	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	L20136 MH	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

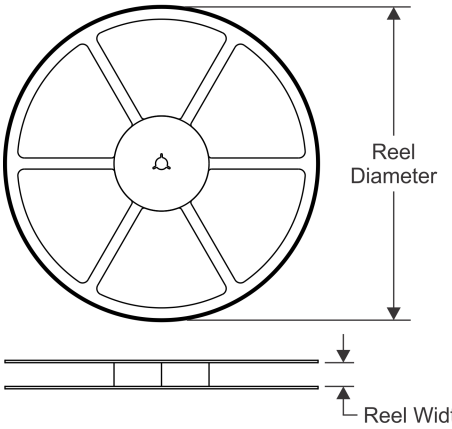
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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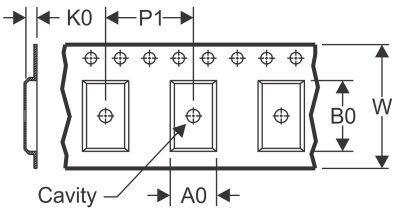
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

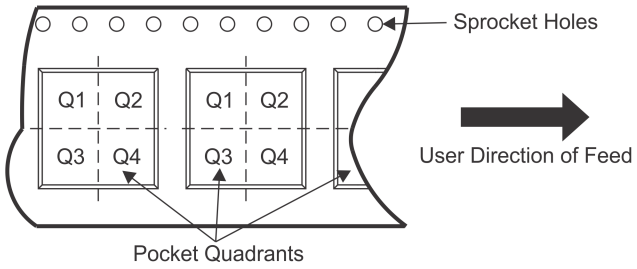


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

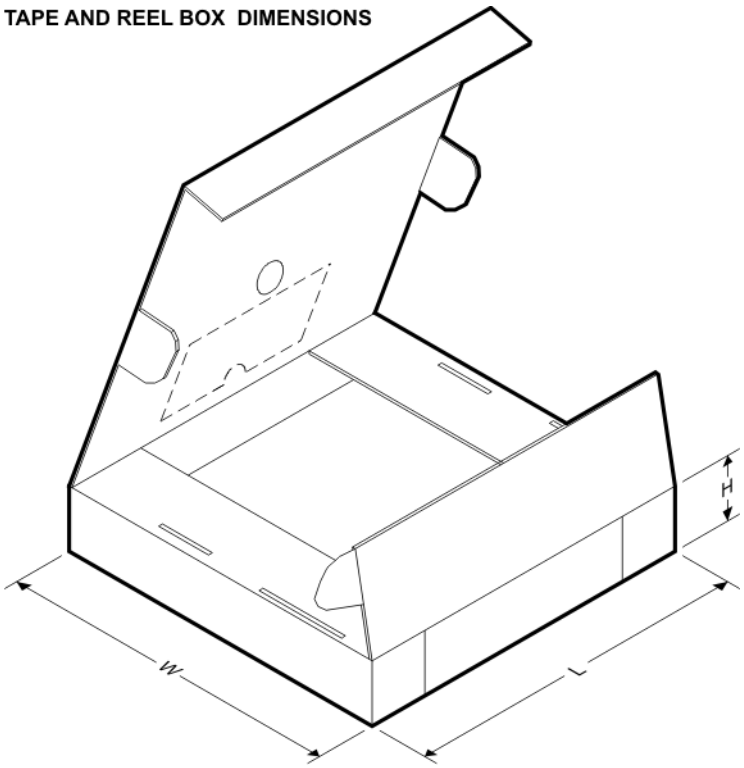
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

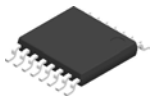
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM20136MHE/NOPB	HTSSOP	PWP	16	250	178.0	12.4	6.95	5.6	1.6	8.0	12.0	Q1
LM20136MHX/NOPB	HTSSOP	PWP	16	2500	330.0	12.4	6.95	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM20136MHE/NOPB	HTSSOP	PWP	16	250	210.0	185.0	35.0
LM20136MHX/NOPB	HTSSOP	PWP	16	2500	367.0	367.0	35.0

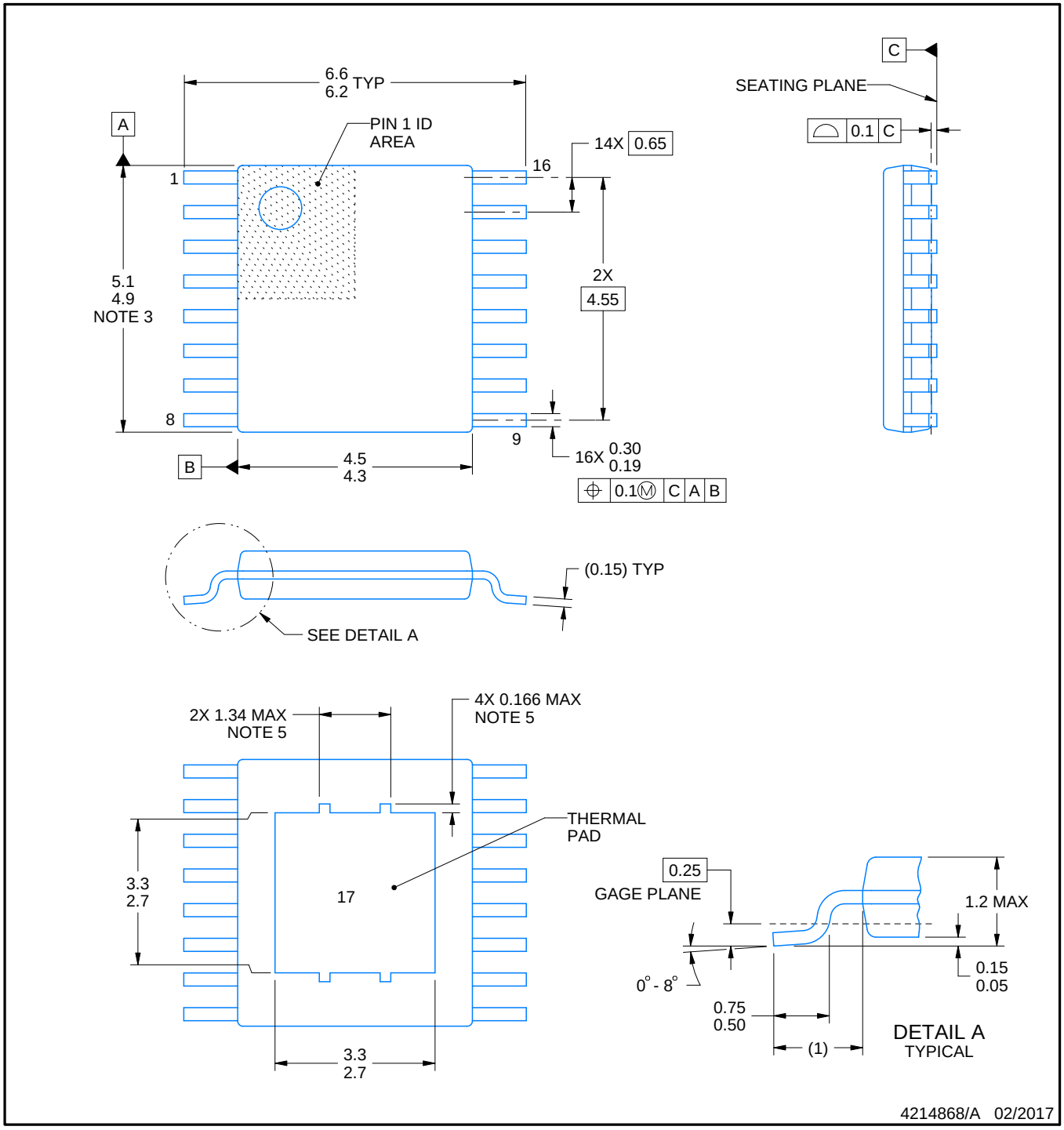


PACKAGE OUTLINE

PWP0016A

PowerPAD ™ HTSSOP - 1.2 mm max height

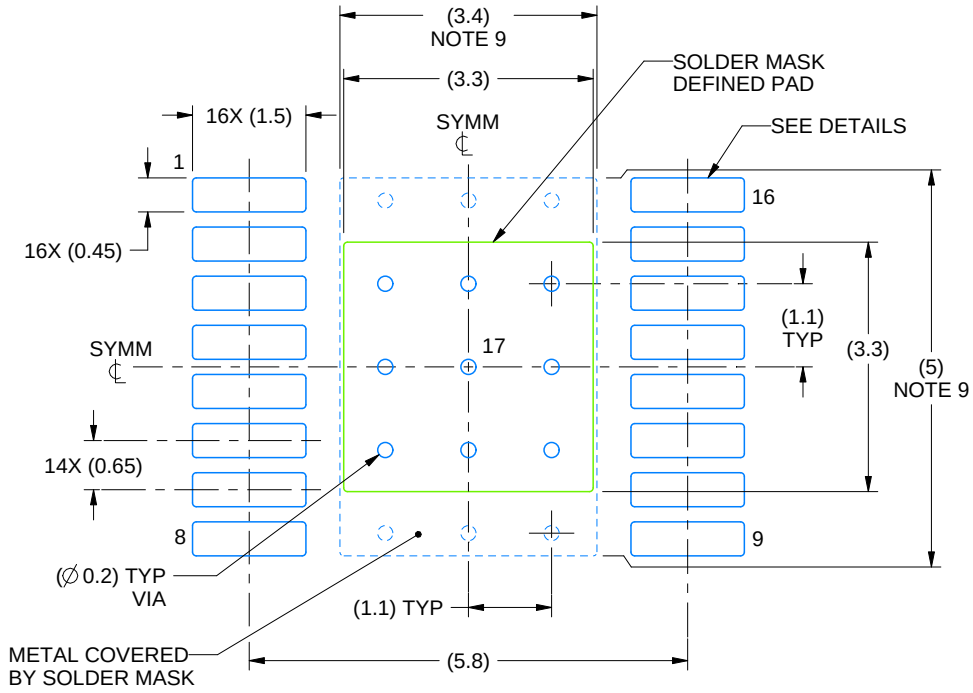
PLASTIC SMALL OUTLINE



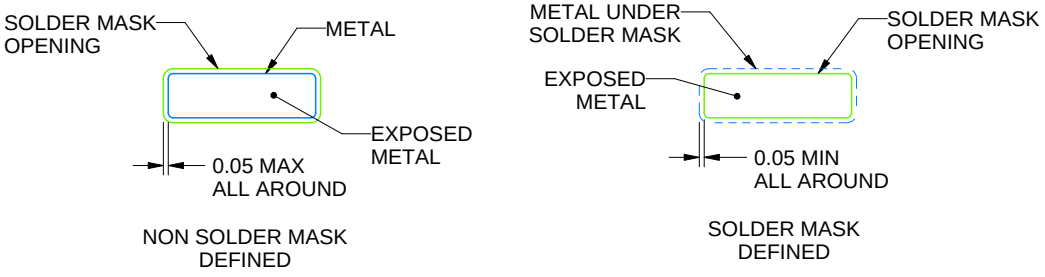
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:10X

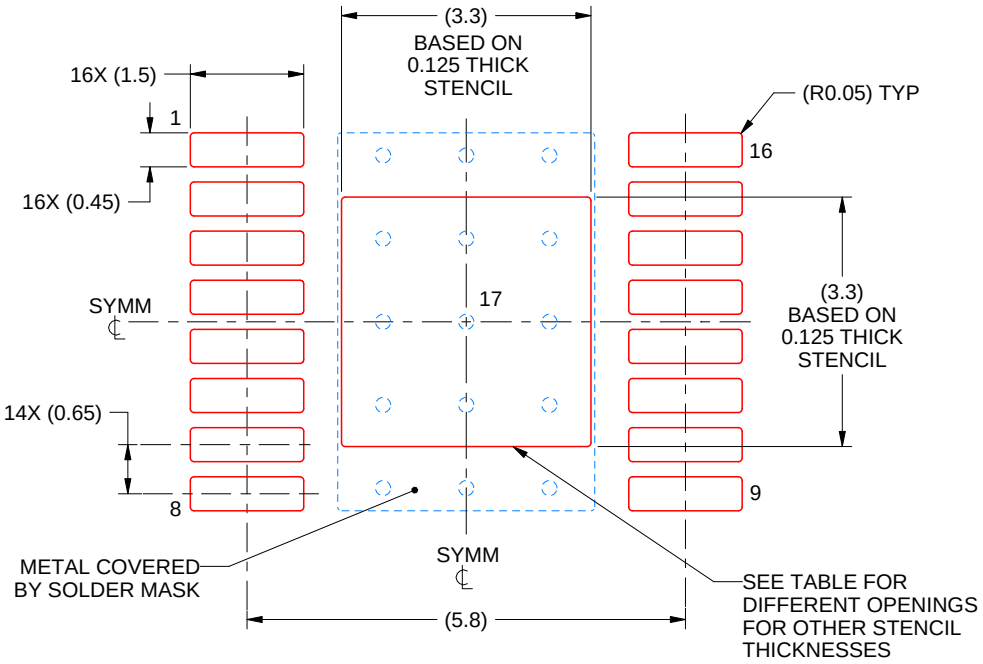


SOLDER MASK DETAILS
PADS 1-16

4214868/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.69 X 3.69
0.125	3.3 X 3.3 (SHOWN)
0.15	3.01 X 3.01
0.175	2.79 X 2.79

4214868/A 02/2017

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

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