19-4538; Rev 0; 4/09

EVALUATION KIT AVAILABLE

Internal-Switch Boost Regulator with Scan Driver, Op Amp, LDO, and VCOM Calibrator

MAX17102

General Description

The MAX17102 includes a high-performance step-up regulator with integrated switch, a multichannel high-voltage level-shifting scan driver with a dedicated discharge channel, and an op amp for VCOM with integrated programmable VCOM calibrator. The VCOM calibrator also features temperature-compensation. The VCOM output can be adjusted by an external temperature-sensing element. The device is optimized for thin-film transistor (TFT) liquid-crystal display (LCD) applications.

The step-up DC-DC converter provides the regulated supply voltage for the panel source driver ICs. The converter is a 450kHz to 1.2MHz frequency-adjustable current-mode regulator with an integrated 20V n-channel power MOSFET. The high switching frequency allows the use of ultra-small inductors and ceramic capacitors. The current-mode control architecture provides fast-transient response to pulsed loads. The step-up regulator features adjustable soft-start and cycle-by-cycle current limit.

The high-voltage level-shifting scan driver is designed to drive the TFT panel gate logic. It has eight outputs that can swing from +35V to -10V and swiftly drive capacitive loads.

The op amp features high output short-circuit current (150mA typ), fast slew rate (45V/µs), and wide bandwidth (20MHz). Its rail-to-rail inputs and outputs maximize application flexibility.

The programmable VCOM calibrator adjusts VCOM level through its serial interface. Nonvolatile memory is used to store the desired VCOM voltage level.

The MAX17102 is available in a 48-pin, 7mm x 7mm, thin QFN package with a maximum thickness of 0.8mm for thin LCD panels.

Applications

LCD Monitor Panels

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX17102ETM+	-40°C to +85°C	48 Thin QFN-EP*

+Denotes a lead(Pb)-free and RoHS-compliant package.

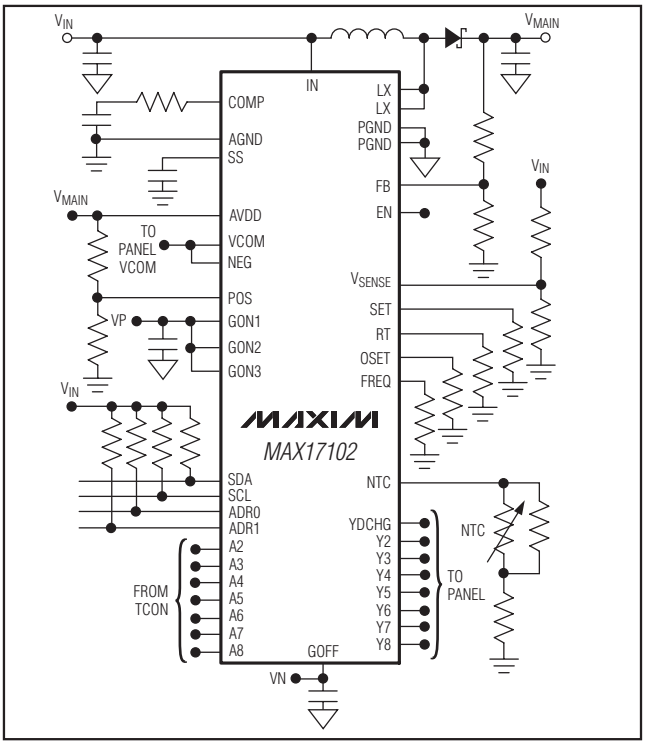
**EP = Exposed pad.*

Pin Configuration appears at end of data sheet.

Features

- **2.5V to 6V IN Supply Voltage Range**
- **1.2MHz Current-Mode Step-Up Regulator**
  - **Fast-Transient Response**
  - **High-Accuracy Reference (1.5%)**
  - **Integrated 20V, 3.5A, 120mΩ MOSFET**
  - **High Efficiency (> 85%)**
  - **Adjustable Soft-Start**
  - **Adjustable Constant Switching Frequency**
- **High-Current 18V Output Buffer**
  - **150mA (typ) Output Short-Circuit Current**
  - **45V/µs Slew Rate**
  - **20MHz, -3dB Bandwidth**
  - **Rail-to-Rail Inputs and Outputs**
- **High-Voltage Scan Drivers**
  - **+35V to -10V Outputs**
- **Programmable VCOM Calibrator**
  - **7-Bit Adjustable Current-Sink Output**
  - **Serial Interface**
  - **Nonvolatile Adjustment Memory**
- **VCOM Output Temperature Compensation**
  - **Programmable Compensation Slope**
  - **Programmable Offset**
  - **Programmable Compensation Starting Point**
- **Thermal-Overload Protection**
- **48-Pin, 7mm x 7mm, Thin QFN Package**

Simplified Operating Circuit



For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

Internal-Switch Boost Regulator with Scan Driver, Op Amp, LDO, and VCOM Calibrator

ABSOLUTE MAXIMUM RATINGS

SCL, SDA, IN, EN, A2–A8 to AGND .....-0.3V to +7.5V
V_{SENSE}, COMP, FB, FREQ, SS to AGND .....-0.3V to (V_{IN} + 0.3V)
ADR0, ADR1 to AGND.....-0.3V to (V_{IN} + 0.3V)
SET, NTC, RT, OSET to AGND .....-0.3V to (V_{IN} + 0.3V)
LX to PGND .....-0.3V to +20V
AVDD to BGND .....-0.3V to +20V
POS, NEG, VCOM to BGND.....-0.3V to (V_{AVDD} to +0.3V)
POS to NEG.....-6V to +6V
PGND, BGND to AGND.....-0.3V to +0.3V
GON1, GON2, GON3 to AGND.....-0.3V to +40V
GOFF to AGND.....-14V to +0.3V
Y2, Y3, Y4, YDCHG to AGND..(V_{GOFF} - 0.3V) to (V_{GON1} + 0.3V)
Y5, Y6 to AGND.....(V_{GOFF} - 0.3V) to (V_{GON2} + 0.3V)
Y7, Y8 to AGND..... (V_{GOFF} - 0.3V) to (V_{GON3} + 0.3V)
LX, PGND RMS Current Rating.....2.4A
Y1–Y7, YDCHG Load RMS Current 95mA
GON1, GON2, GON3 RMS Current 110mA
GOFF RMS Current 250mA
Continuous Power Dissipation (T_A = +70°C)
48-Pin, 7mm x 7mm, Thin QFN
(derate 31.9mW/°C above +70°C) 2548mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = V_{EN} = +3V, Circuit of Figure 2, $V_{GON_}$ = 35V, V_{GOFF} = -10V, V_{AVDD} = 14V, **T_A = 0°C to +85°C**. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
GENERAL						
IN Input Voltage Range	(Note 1)		2.5		6.0	V
IN Shutdown Current	EN = 0			0.5	1	mA
IN Quiescent Current	V_{FB} = 1.5V, not switching			1.0	1.5	mA
	V_{FB} = 1.1V, continuous switching			2.5	4	
IN Undervoltage Lockout	IN rising, typical hysteresis 200mV		2.05	2.25	2.45	V
MAIN DC-DC CONVERTER						
Output-Voltage Range			6		18	V
SMPS Operating Frequency	f (kHz) = 15 x R_{FREQ} (kΩ)	R_{FREQ} = 80kΩ	1000	1200	1400	kHz
		R_{FREQ} = 30kΩ	370	450	530	
		FREQ = unconnected	510	600	690	
Oscillator Maximum Duty Cycle			88	92	96	%
FB Regulation Voltage			1.216	1.235	1.254	V
FB Load Regulation	0 < I_{MAIN} < 200mA, transient only			0.01		%
FB Line Regulation	V_{IN} = 2.5V to 6.0V		-0.25	-0.08	+0.25	%/V
FB Input Bias Current	V_{FB} = 1.3V, T_A = +25°C		25	80	125	nA
FB Transconductance	ΔI = 5µA at COMP		75	160	280	µS
FB Voltage Gain	FB to COMP			2000		V/V
LX On-Resistance	I_{LX} = 200mA			120	200	mΩ
LX Input Bias Current	V_{LX} = 18V			10	20	µA
LX Current Limit	Duty cycle = 65%		2.8	3.5	4.2	A
Current-Sense Transresistance			0.1	0.2	0.3	V/A
SS Output Current			3.5	5	6.5	µA

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = V_{EN} = +3V, Circuit of Figure 2, $V_{GON_}$ = 35V, V_{GOFF} = -10V, V_{AVDD} = 14V, **T_A = 0°C to +85°C**. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
HIGH-VOLTAGE DRIVER BLOCK					
GON_ Input-Voltage Range		12		35	V
GOFF Input-Voltage Range		-10		-4	V
GOFF Supply Current	A1–A8 = AGND, no load		120	250	µA
GON_ Total Supply Current	A1–A8 = AGND, no load		265	450	µA
Output-Voltage Low (Y1–Y8)	I_{OUT} = 10mA		GOFF + 0.035	GOFF + 0.06	V
Output-Voltage High (Y1–Y8)	I_{OUT} = 10mA	GON - 0.26	GON - 0.16		V
Rise Time (Y1)	T_A = +25°C, V_{GON} = 30V and V_{GOFF} = -6.2V (Note 2)		310	450	ns
Fall Time (Y1)	T_A = +25°C, V_{GON} = 30V and V_{GOFF} = -6.2V		60	120	ns
Rise Time (Y2)	T_A = +25°C, V_{GON} = 30V and V_{GOFF} = -6.2V (Note 2)		10	200	ns
Fall Time (Y2)	T_A = +25°C, V_{GON} = 30V and V_{GOFF} = -6.2V (Note 2)		10	200	ns
Rise Time (Y3–Y6)	T_A = +25°C, V_{GON} = 30V and V_{GOFF} = -6.2V (Note 2)		310	450	ns
Fall Time (Y3–Y6)	T_A = +25°C, V_{GON} = 30V and V_{GOFF} = -6.2V (Note 2)		60	120	ns
Rise Time (Y7, Y8)	T_A = +25°C, V_{GON} = 30V and V_{GOFF} = -6.2V (Note 2)		345	1600	ns
Fall Time (Y7, Y8)	T_A = +25°C, V_{GON} = 30V and V_{GOFF} = -6.2V (Note 2)		345	700	ns
Propagation Delay High-to-Low Transition (Y1–Y8)	T_A = +25°C, V_{GON} = 30V and V_{GOFF} = -6.2V (Note 2)		65		ns
Propagation Delay Low-to-High Transition (Y1–Y8)	T_A = +25°C, V_{GON} = 30V and V_{GOFF} = -6.2V (Note 2)		50		ns
OP AMP					
AVDD Supply Range		6		18	V
AVDD Overvoltage-Fault Threshold		18.1	19.0	19.90	V
AVDD Supply Current	Buffer configuration, V_{POS} = V_{AVDD}/2, no load		3.5	5	mA
Input Offset Voltage	V_{NEG}, V_{POS} = V_{AVDD}/2, T_A = +25°C	-14		+14	mV
	V_{NEG}, V_{POS} = V_{AVDD} - 0.1V	-14		+14	
	V_{NEG}, V_{POS} = 0.1V	-14		+14	
Input Bias Current	V_{NEG}, V_{POS} = V_{AVDD}/2, T_A = +25°C	-50		+50	nA
Input Common-Mode Voltage Range		0		V_{AVDD}	V
Input Common-Mode Rejection Ratio			80		dB
Output-Voltage Swing High	I_{OUT} = 50mA	V_{SUP} - 300			mV
Output-Voltage Swing Low	I_{OUT} = -50mA			300	mV
Large-Signal Voltage Gain	V_{OUT} = 1V to V_{AVDD} - 1V		80		dB
Slew Rate			45		V/µs
-3dB Bandwidth			20		MHz
Short-Circuit Current	Short to V_{AVDD} - 1.5V, sourcing	150	350		mA
	Short to V_{AVDD} - 1.5V, sinking	150	500		

Internal-Switch Boost Regulator with Scan Driver, Op Amp, LDO, and VCOM Calibrator

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = V_{EN} = +3V, Circuit of Figure 2, $V_{GON_}$ = 35V, V_{GOFF} = -10V, V_{AVDD} = 14V, **T_A = 0°C to +85°C**. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CONTROL INPUTS					
Logic Input-Voltage Low (A2–A8, EN)	2.5V < V_{IN} < 6V			0.8	V
Logic Input-Voltage High (A2–A8, EN)	2.5V < V_{IN} < 6V	2			V
Logic Input Bias Current (A2–A8)	0 < A_ < V_{IN}, T_A = +25°C	-1		+1	µA
Logic Input Bias Current (EN)	0 < V_{EN} < V_{IN}, T_A = +25°C	-1		+1	µA
VOLTAGE DETECTOR					
V_{SENSE} Voltage Range				V_{IN}	V
V_{SENSE} Bias Current	T_A = +25°C	-1		+1	µA
V_{SENSE} Threshold Voltage	Falling edge	1.200	1.235	1.270	V
FAULT DETECTION					
Thermal Shutdown	Rising edge, typical hysteresis = 15°C		160		°C
Thermal-Shutdown Trial Times	Before latchup		3		Times
PROGRAMMABLE VCOM CALIBRATOR					
AVDD Input Range	For nonvolatile memory writing	7.5		18	V
SET Voltage Resolution		7			Bits
SET Differential Nonlinearity	Monotonic overtemperature	-1		+1	LSB
SET Zero-Scale Error		-1	+1	+3	LSB
SET Full-Scale Error		-4		+4	LSB
SET Current				120	µA
SET External Resistance (Note 5)	To GND, V_{AVDD} = 18V	8.5		170	kΩ
	To GND, V_{AVDD} = 7.5V	3.1		62	kΩ
V_{SET}/V_{AVDD} Voltage Ratio	DAC zero scale		0.05		V/V
POS Settling Time	To ±0.5 LSB error band		20		µs
Memory Write Cycles	Guaranteed by design, not production tested	30			Times
Memory Write Time				150	ms
VCOM TEMPERATURE COMPENSATION					
OSET Voltage	Improve to ±1% without design change if supported by characterization	0.585	0.6	0.615	V
OSET Current	V_{AVDD} = 7.5V to 18V, V_{OSET} in regulation	14	55		µA
Compensation Current Ratio	$I_{TCOMP}/\Delta R$, ΔR = 5kΩ		2		µA/kΩ
Compensation Current-Ratio Tolerance		-8		+8	%
Compensation Current	V_{RTC} - V_{NTC} = 0.2V	14	21		µA
Temperature Compensation Trip Hysteresis	R_{RT} = R_{NTC} = 29.4kΩ	3	6	9	°C
NTC, RT Current		17	20	23	µA
Compensation Threshold	V_{RT} - V_{NTC}	-7	0	+7	mV

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = V_{EN} = +3V, Circuit of Figure 2, $V_{GON_}$ = 35V, V_{GOFF} = -10V, V_{AVDD} = 14V, **T_A = 0°C to +85°C**. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
SERIAL INTERFACE					
Logic Input Low Voltage	SDA, SCL, ADR0, ADR1			0.8	V
Logic Input High Voltage	SDA, SCL, ADR0, ADR1	2.0			V
Logic Input Current	SDA, SCL, ADR0, ADR1, T_A = +25°C	-1		+1	µA
Logic Output Low Voltage (SDA)	SDA sink, 3mA			0.4	V
SDA and SCL Capacitive Loading				400	pF
SCL Frequency		DC		400	kHz
SCL High Time		600			ns
SCL Low Time		1300			ns
SDA and SCL Rise Time/Fall Time	C_b = total capacitance of bus line in pF (Note 3)	20 + 0.1 x Cb		300	ns
START Condition Hold Time	10% of SDA to 90% of SCL	600			ns
START Condition Setup Time		600			ns
Data Input Hold Time		50			ns
Data Input Setup Time		100			ns
STOP Condition Setup Time		600			ns
Bus Free Time		1300			ns
Input Filter Spike Suppression	SDA, SCL, not tested			50	ns
ADR0, ADR1 Setup Time	Before START	600			ns
ADR0, ADR1 Hold Time	After STOP	600			ns

ELECTRICAL CHARACTERISTICS

(V_{IN} = V_{EN} = +3V, Circuit of Figure 1, $V_{GON_}$ = 35V, V_{GOFF} = -10V, V_{AVDD} = 14V, **T_A = -40°C to +85°C**.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
GENERAL						
IN Input Voltage Range	(Note 1)		2.5		6.0	V
IN Shutdown Current	EN = 0				1	mA
IN Quiescent Current	V_{IN} = 3V, V_{FB} = 1.5V, not switching				1.5	mA
	V_{IN} = 3V, V_{FB} = 1.1V, continuous switching				4	
IN Undervoltage Lockout	IN rising		2.05		2.45	V
MAIN DC-DC CONVERTER						
Output-Voltage Range			6		18	V
Switching Frequency	f (MHz) = 0.015 x R_{FREQ} (kΩ)	R_{FREQ} = 80kΩ	1000		1400	kHz
		R_{FREQ} = 30kΩ	360		540	
		FREQ = unconnected	490		710	
Oscillator Maximum Duty Cycle			88		96	%
FB Regulation Voltage			1.216		1.254	V
FB Transconductance	ΔI = 5µA at COMP		75		300	µS

Internal-Switch Boost Regulator with Scan Driver, Op Amp, LDO, and VCOM Calibrator

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = V_{EN} = +3V, Circuit of Figure 1, GON_ = 35V, GOFF = -10V, V_{AVDD} = 14V, **T_A = -40°C to +85°C**.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
LX On-Resistance	I_{LX} = 200mA			200	mΩ
LX Input Bias Current	V_{LX} = 18V			20	µA
LX Current Limit	Duty cycle = 65%	2.8		4.2	A
Current-Sense Transresistance		0.1		0.3	V/A
SS Output Current		3.5		6.5	µA
HIGH-VOLTAGE DRIVER BLOCK					
GON_ Input-Voltage Range		12		35	V
GOFF Input-Voltage Range		-10		-4	V
GOFF Supply Current	A2–A8 = AGND, no load			250	µA
GON_ Total Supply Current	A2–A8 = AGND, no load			450	µA
Output-Voltage Low (Y1–Y8)	I_{OUT} = 10mA			GOFF + 0.06	V
Output-Voltage High (Y1–Y8)	I_{OUT} = 10mA	GON - 0.26			V
OPERATIONAL AMPLIFIER					
AVDD Supply Range		6		18	V
AVDD Overvoltage-Fault Threshold		18.1		19.90	V
AVDD Supply Current	Buffer configuration, V_{POS} = V_{AVDD}/2, no load			5	mA
Input Offset Voltage	V_{NEG}, V_{POS} = V_{AVDD}/2, T_A = +25°C	-14		+14	mV
	V_{NEG}, V_{POS} = V_{AVDD} - 0.1V	-14		+14	
	V_{NEG}, V_{POS} = 0.1V	-14		+14	
Input Common-Mode Voltage Range		0		V_{AVDD}	V
Output-Voltage Swing High	I_{OUT} = 50mA	V_{SUP} - 300			mV
Output-Voltage Swing Low	I_{OUT} = -50mA			300	mV
Short-Circuit Current	Short to V_{AVDD} - 1.5V, sourcing	150			mA
	Short to 1.5V, sinking	150			
CONTROL INPUTS					
Logic Input Voltage Low (A2–A8, EN)	2.5V < V_{IN} < 6V			0.8	V
Logic Input Voltage High (A2–A8, EN)	2.5V < V_{IN} < 6V	2			V
VOLTAGE DETECTOR					
VSENSE Voltage Range				V_{IN}	V
VSENSE Threshold Voltage	Falling edge	1.200		1.270	V

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = V_{EN} = +3V, Circuit of Figure 1, GON_ = 35V, GOFF = -10V, V_{AVDD} = 14V, **T_A = -40°C to +85°C**.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
PROGRAMMABLE VCOM CALIBRATOR					
AVDD Threshold to Program Enable	Rising edge, 800mV hysteresis typical	7.05		7.45	V
AVDD Input Range	For EEPROM writing	7.5		18	V
SET Voltage Resolution		7			Bits
SET Differential Nonlinearity	Monotonic overtemperature	-2		+2	LSB
SET Zero-Scale Error		-1		+3	LSB
SET Full-Scale Error		-4		+4	LSB
SET Current				120	µA
SET External Resistance (Note 3)	To GND, V_{AVDD} = 18V	8.5		170	kΩ
	To GND, V_{AVDD} = 7.5V	3.1		62	kΩ
VCOM TEMPERATURE COMPENSATION					
OSET Voltage		0.585		0.615	V
OSET Current	AVDD = 7.5V to AVDD = 18V; 0.585V < V_{OSET} < 0.615	14			µA
Compensation Current-Ratio Tolerance	$I_{TCOMP}/\Delta R$, ΔR = 5kΩ	1.76		2.24	µA/kΩ
Compensation Current	V_{TRC} - V_{NTC} = 0.2V	12			µA
Temperature Compensation Trip Hysteresis	R_{RT} = R_{NTC} = 29.4kΩ	3		9	°C
NTC, RT Voltage	With 29.4kΩ resistor to AGND	500		676	mV
NTC, RT Current		17		32	µA
Compensation Threshold	V_{RT} - V_{NTC}	-7		+7	mV
SERIAL INTERFACE					
Logic Input Low Voltage	SDA, SCL, ADR0, ADR1			0.8	V
Logic Input High Voltage	SDA, SCL, ADR0, ADR1	2.0			V
Logic Output Low Voltage (SDA)	SDA, I_{SDA} = 3mA	0		0.4	V
Logic Input Current	SDA, SCL, ADR0, ADR1, T_A = +25°C	-1		+1	µA
SDA and SCL Capacitive Loading				400	pF
SCL Frequency		DC		400	kHz
SCL High Time		600			ns
SCL Low Time		1300			ns
SDA and SCL Rise and Fall Time	C_b = total capacitance of bus line in pF	20 + 10 x Cb		300	ns
START Condition Hold Time	10% of SDA to 90% of SCL	600			ns
START Condition Setup Time		600			ns
Data Input Hold Time		50			ns
Data Input Setup Time		100			ns

Internal-Switch Boost Regulator with Scan Driver, Op Amp, LDO, and VCOM Calibrator

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = V_{EN} = +3V, Circuit of Figure 1, GON_ = 35V, GOFF = -10V, V_{AVDD} = 14V, **T_A = -40°C to +85°C**.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
STOP Condition Setup Time		600			ns
Bus Free Time		1300			ns
Input Filter Spike Suppression	SDA, SCL, not tested			50	ns

Note 1: For 5.5V< V_{IN} < 6.0V, use IC for no longer than 1% of IC lifetime. For continuous operation, input voltage should not exceed 5.5V.
Note 2: The panel models for different channels are illustrated in Figure 13.
Note 3: Maximum amount of capacitance allowed on the SDA bus line.
Note 4: T_A = -40°C specifications are guaranteed by design, not production tested.
Note 5: SET external resistor range is verified at DAC full scale.

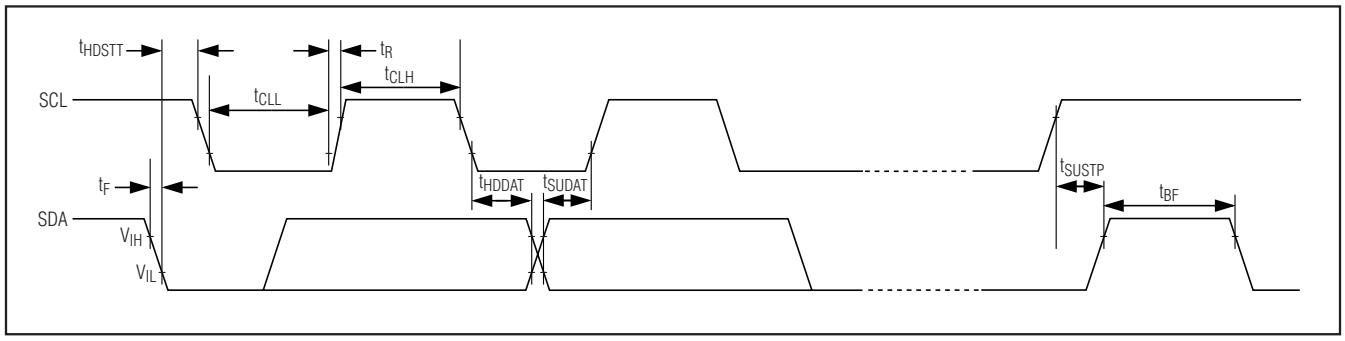
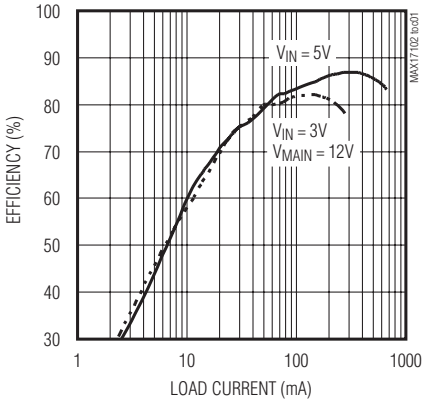


Figure 1. Timing Definitions Used in the Electrical Characteristics

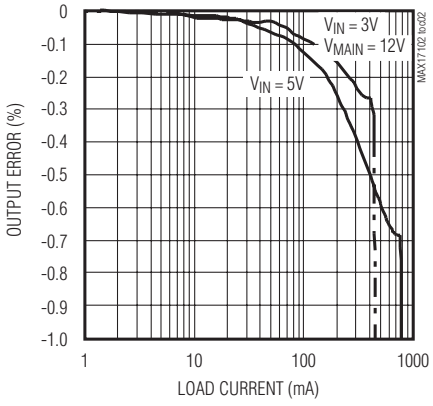
Typical Operating Characteristics

(Circuit of Figure 2, V_{IN} = 5V, V_{MAIN} = 16V, T_A = +25°C, unless otherwise noted.)

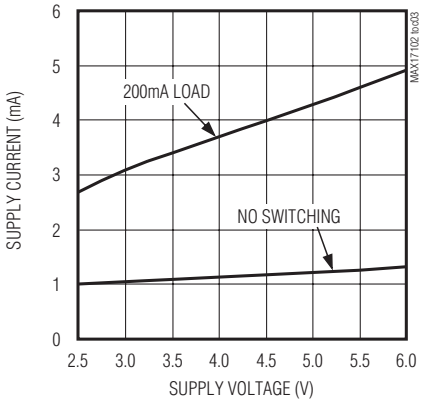
STEP-UP REGULATOR EFFICIENCY vs. LOAD CURRENT



STEP-UP REGULATOR OUTPUT LOAD REGULATION vs. LOAD CURRENT



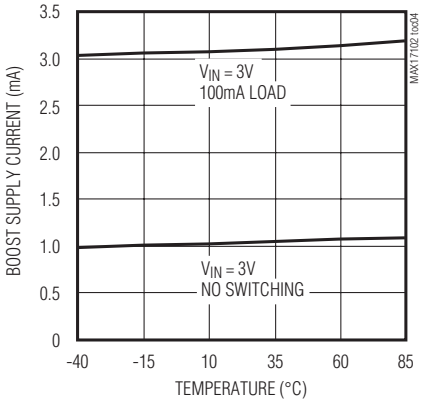
IN SUPPLY QUIESCENT CURRENT vs. IN SUPPLY VOLTAGE



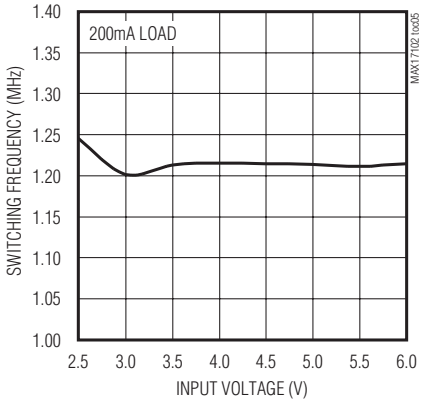
Typical Operating Characteristics (continued)

(Circuit of Figure 2, V_{IN} = 5V, V_{MAIN} = 16V, T_A = +25°C, unless otherwise noted.)

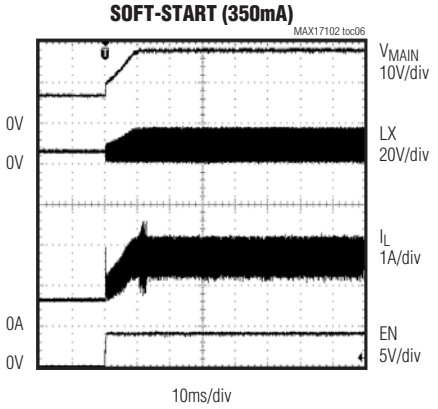
STEP-UP REGULATOR SUPPLY CURRENT vs. TEMPERATURE



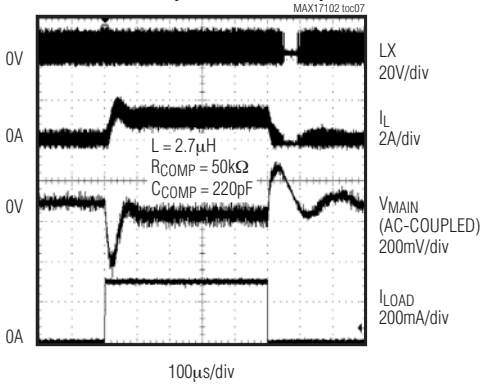
STEP-UP CONVERTER SWITCHING FREQUENCY vs. INPUT VOLTAGE



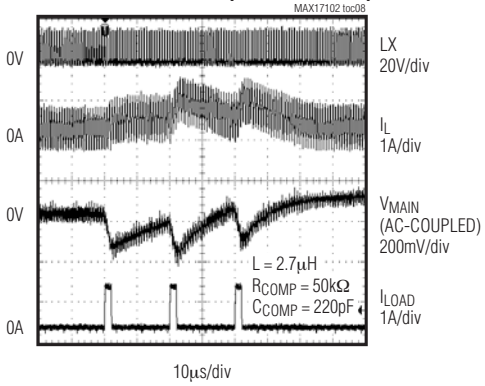
STEP-UP REGULATOR HEAVY-LOAD SOFT-START (350mA)



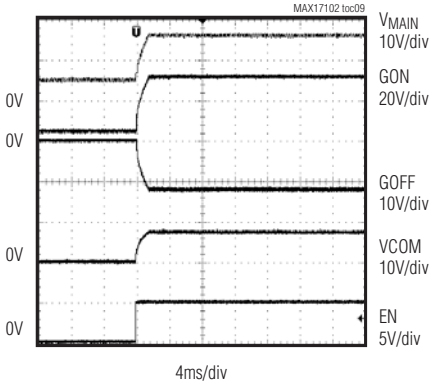
STEP-UP REGULATOR LOAD-TRANSIENT RESPONSE (40mA TO 340mA)



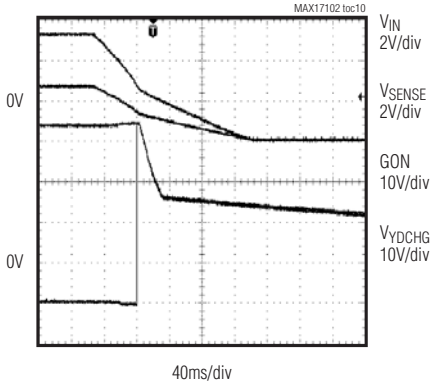
STEP-UP REGULATOR PULSED LOAD-TRANSIENT RESPONSE (40mA TO 1.04A)



POWER-UP SEQUENCE OF ALL SUPPLY OUTPUTS



DISCHARGE FUNCTION

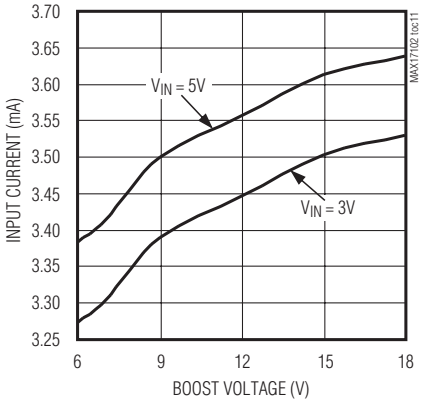


Internal-Switch Boost Regulator with Scan Driver, Op Amp, LDO, and VCOM Calibrator

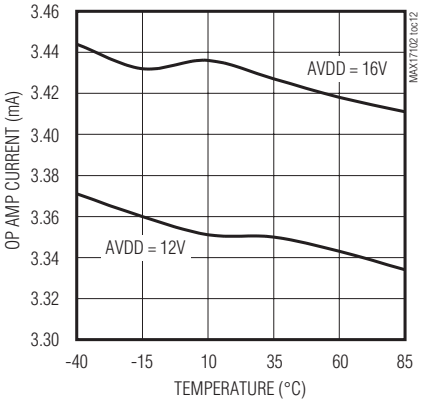
Typical Operating Characteristics (continued)

(Circuit of Figure 2, V_{IN} = 5V, V_{MAIN} = 16V, T_A = +25°C, unless otherwise noted.)

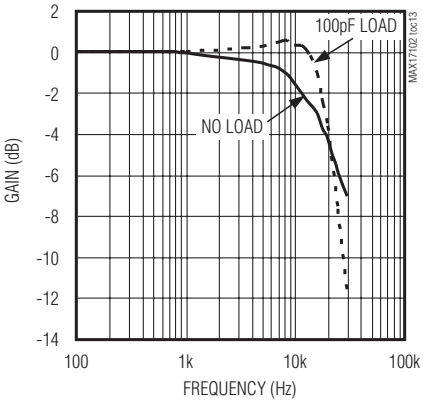
OP AMP SUPPLY CURRENT vs. AVDD SUPPLY VOLTAGE



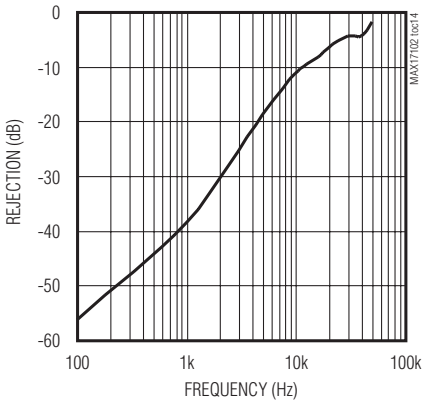
OP AMP SUPPLY CURRENT vs. TEMPERATURE



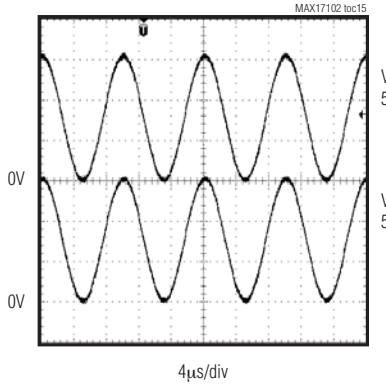
OPERATIONAL AMPLIFIER FREQUENCY RESPONSE



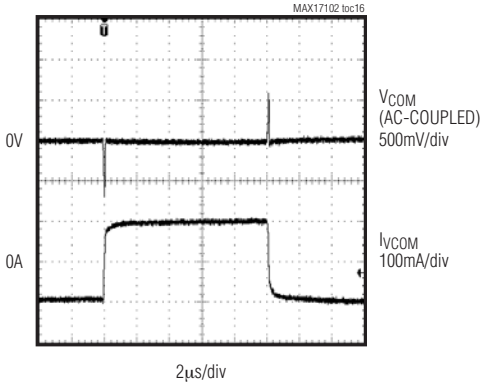
OPERATIONAL AMPLIFIER PSSR vs. FREQUENCY



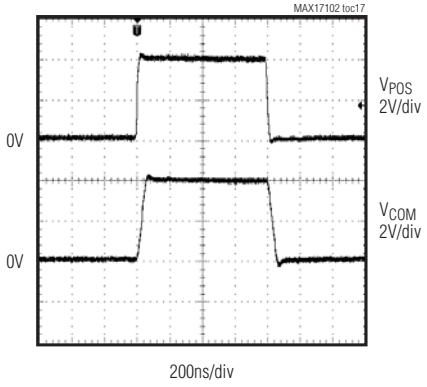
OPERATIONAL AMPLIFIER RAIL-TO-RAIL INPUT/OUTPUT WAVEFORMS



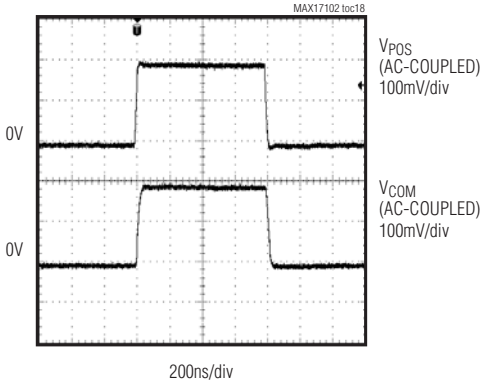
OPERATIONAL AMPLIFIER LOAD-TRANSIENT RESPONSE



OPERATIONAL AMPLIFIER LARGE-SIGNAL STEP RESPONSE



OPERATIONAL AMPLIFIER SMALL-SIGNAL STEP RESPONSE

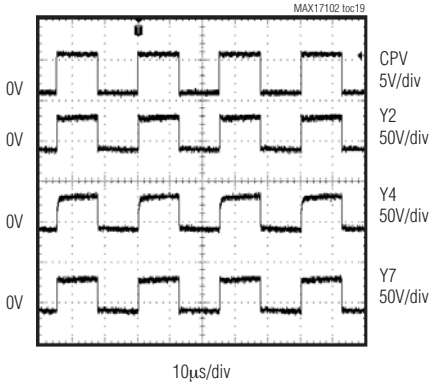


Internal-Switch Boost Regulator with Scan Driver, Op Amp, LDO, and VCOM Calibrator

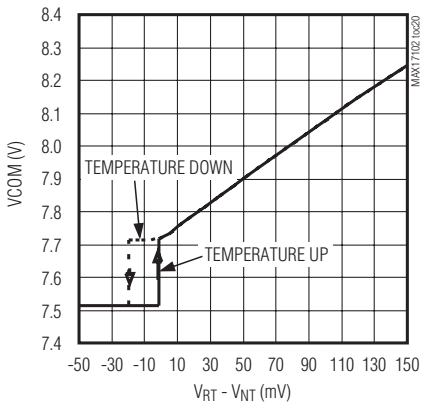
Typical Operating Characteristics

(Circuit of Figure 2, V_{IN} = 5V, V_{MAIN} = 16V, T_A = +25°C, unless otherwise noted.)

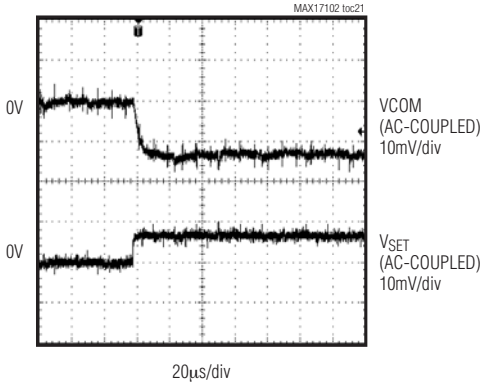
SCAN DRIVER INPUT/OUTPUT WAVEFORMS



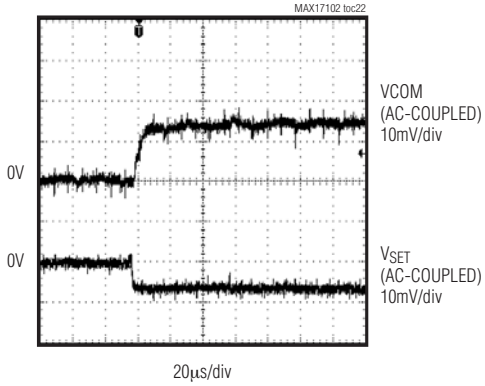
VCOM TEMPERATURE COMPENSATION



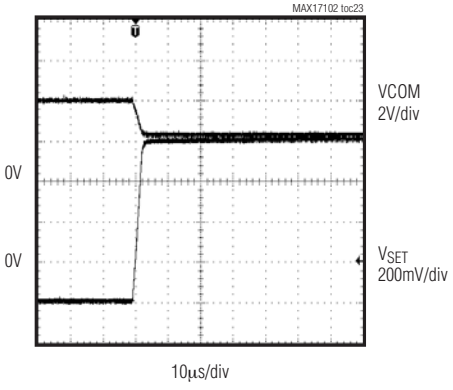
CALIBRATOR SIGNAL DOWNWARD LSB STEP RESPONSE



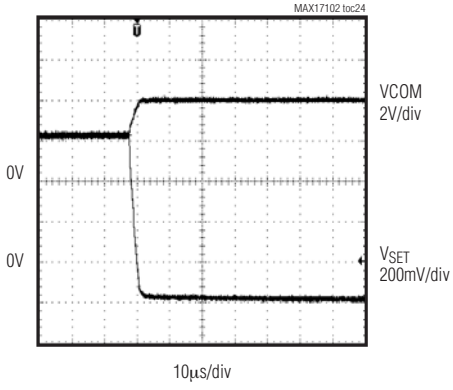
CALIBRATOR SIGNAL UPWARD LSB STEP RESPONSE



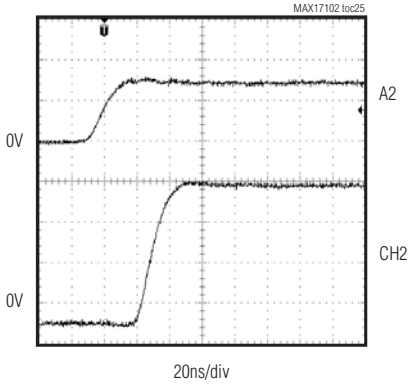
CALIBRATOR FULL-SCALE DOWNWARD STEP RESPONSE



CALIBRATOR FULL-SCALE UPWARD STEP RESPONSE



SCAN DRIVER A2-TO-CH2 RISING DELAY AND SLEW RATE

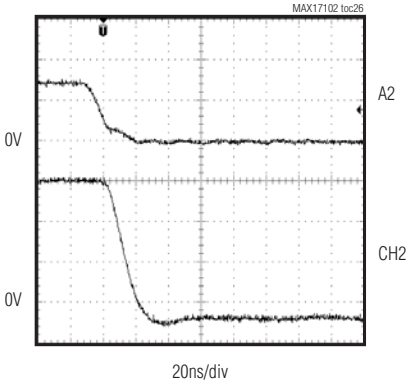


Internal-Switch Boost Regulator with Scan Driver, Op Amp, LDO, and VCOM Calibrator

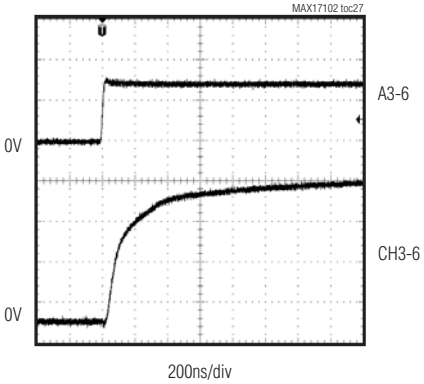
Typical Operating Characteristics (continued)

(Circuit of Figure 2, V_{IN} = 5V, V_{MAIN} = 16V, T_A = +25°C, unless otherwise noted.)

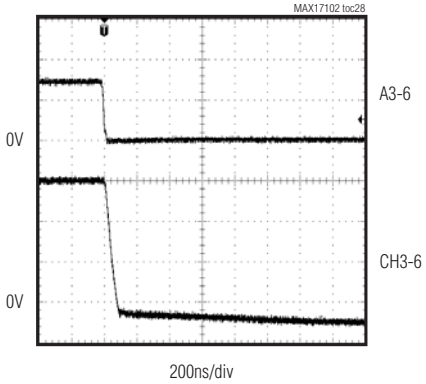
SCAN DRIVER A2-TO-CH2 FALLING DELAY AND SLEW RATE



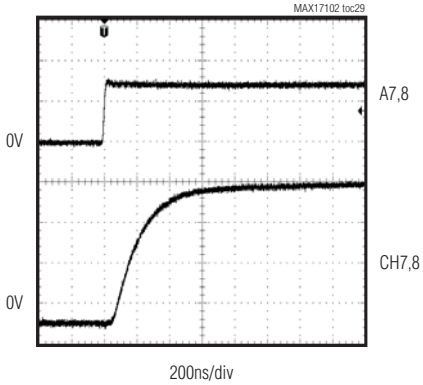
SCAN DRIVER A3-6-TO-CH3-6 RISING DELAY AND SLEW RATE



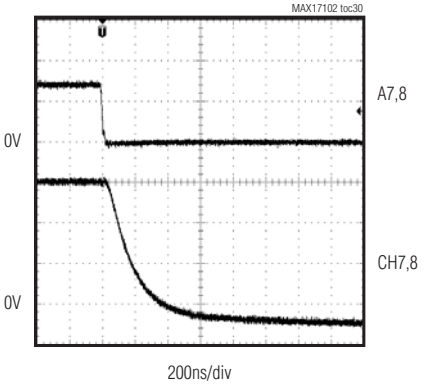
SCAN DRIVER A3-6-TO-CH3-6 FALLING DELAY AND SLEW RATE



SCAN DRIVER A7,8-TO-CH7,8 RISING DELAY AND SLEW RATE



SCAN DRIVER A7,8-TO-CH7,8 FALLING DELAY AND SLEW RATE



Pin Description

PIN	NAME	FUNCTION
1, 15, 28	N.C.	No Connection. Not used.
2	FREQ	Frequency Pin. Connect FREQ to AGND to set the switching frequency. Use 80kΩ for 1.2MHz operation or 30kΩ for 450kHz operation. For other frequency settings, F = 15 x R (kHz) with R in kΩ. Frequency-adjustable range is 400kHz to 1.2MHz.
3	OSET	VCOM Temperature-Compensation Offset Input. Connect a resistor R_{OSET} to AGND creates a current I_{OSET}, which flows into the VCOM setting resistor-divider and generates the offset voltage. $I_{OSET} = V_{OSET}/R_{OSET}$. Leave the pin high impedance if temperature compensation is unused.
4, 5	ADR0, ADR1	Address Select Pins to Set the Slave Address for Serial Interface
6	SCL	Serial Interface Clock Input
7	SDA	Serial Interface Data I/O.
8–14	A8–A2	Level-Shifter Logic-Level Inputs

Pin Description (continued)

PIN	NAME	FUNCTION
16	YDCHG	Level-Shifter Output. Discharging channel.
17–23	Y2–Y8	Level-Shifter Logic-Level Outputs
24	GOFF	Gate-Off Supply Input. GOFF is the negative supply for the Y2, Y8 and YDCHG channel level-shifter outputs. Bypass to PGND with a minimum 0.33µF ceramic capacitor.
25	GON3	Gate-On Supply Input 3. GON3 is the positive supply for the Y7, Y8 level-shifter outputs. Bypass to PGND with a minimum 0.1µF ceramic capacitor.
26	GON2	Gate-On Supply Input 2. GON2 is the positive supply for the Y5, Y6 level-shifter outputs. Bypass to PGND with a minimum 0.1µF ceramic capacitor.
27	GON1	Gate-On Supply Input 1. GON1 is the positive supply for the Y2, Y3, Y4, and YDCHG channel level-shifter outputs. Bypass to PGND with a minimum 0.1µF ceramic capacitor.
29	AGND	Analog Ground
30	RT	Temperature Setting for VCOM Compensation. A resistor from RT to ground sets the starting temperature point for VCOM temperature compensation. The threshold is $R_{NTC} < R_{RT}$. Select $R_{RT} = R_{NTC}$ at the chosen temperature. Leave the pin high impedance if temperature compensation is unused.
31	NTC	Temperature Sense and Compensation Slope Set Input. Use one parallel and one series resistor to linearize the NTC's resistance. A current source proportional to the resistance difference between the NTC pin and RT pin sets the slope of VCOM compensation. The sourcing current is $2 \times 10^{-6} \times \Delta R$ (mA), where $\Delta R = R_{RT} - R_{NTC}$ (ohm). Leave this pin high impedance if temperature compensation is unused.
32	SET	Set Current Adjustment Input. Connect a resistor, R_{SET}, from SET to GND to set sink current range.
33	VCOM	Op-Amp Output
34	NEG	Op-Amp Negative Input
35	POS	Op-Amp Positive Input
36	AVDD	Op-Amp Supply Voltage. Connect to step-up converter output.
37	BGND	Analog Ground for VCOM Op Amp
38	FB	Step-Up Regulator Feedback Pin. Set the step-up regulator output voltage with an external resistive voltage-divider with its center tap at FB.
39, 40	PGND	Power Ground
41, 42	LX	Switching Node
43	EN	Shutdown Control Input. Pull EN low to turn off the DC-DC converter. The level shifters remain active if sufficient AVDD voltage is available for operation.
44	IN	Supply Pin. Bypass IN to AGND with a minimum 0.1µF ceramic capacitor.
45	V_{SENSE}	Input Voltage Sense for Voltage Detector. Connect this pin to V_{IN} through a resistor-divider. When V_{SENSE} is below 1.235V, discharge channel of level-shifter channel I is turned on.
46	COMP	Compensation Pin. Connect a series RC from this pin to AGND. Typical values are 50kΩ and 220pF.
47	SS	Step-Up Regulator Soft-Start Control Pin. Connect a capacitor between SS and AGND to set the step-up regulator soft-start timing. SS is connected to AGND when $\overline{SHDN}$ is low. When $\overline{SHDN}$ goes high, the capacitor at SS is charged by an internal 5µA current source, slowly raising the internal current limit. The full LX current limit is available when V_{SS} = 1.235V.
48	AGND	Analog Ground
—	EP	Exposed Backside Pad. Connect to AGND. Copper area should be maximized for better thermal performance.

Internal-Switch Boost Regulator with Scan Driver, Op Amp, LDO, and VCOM Calibrator

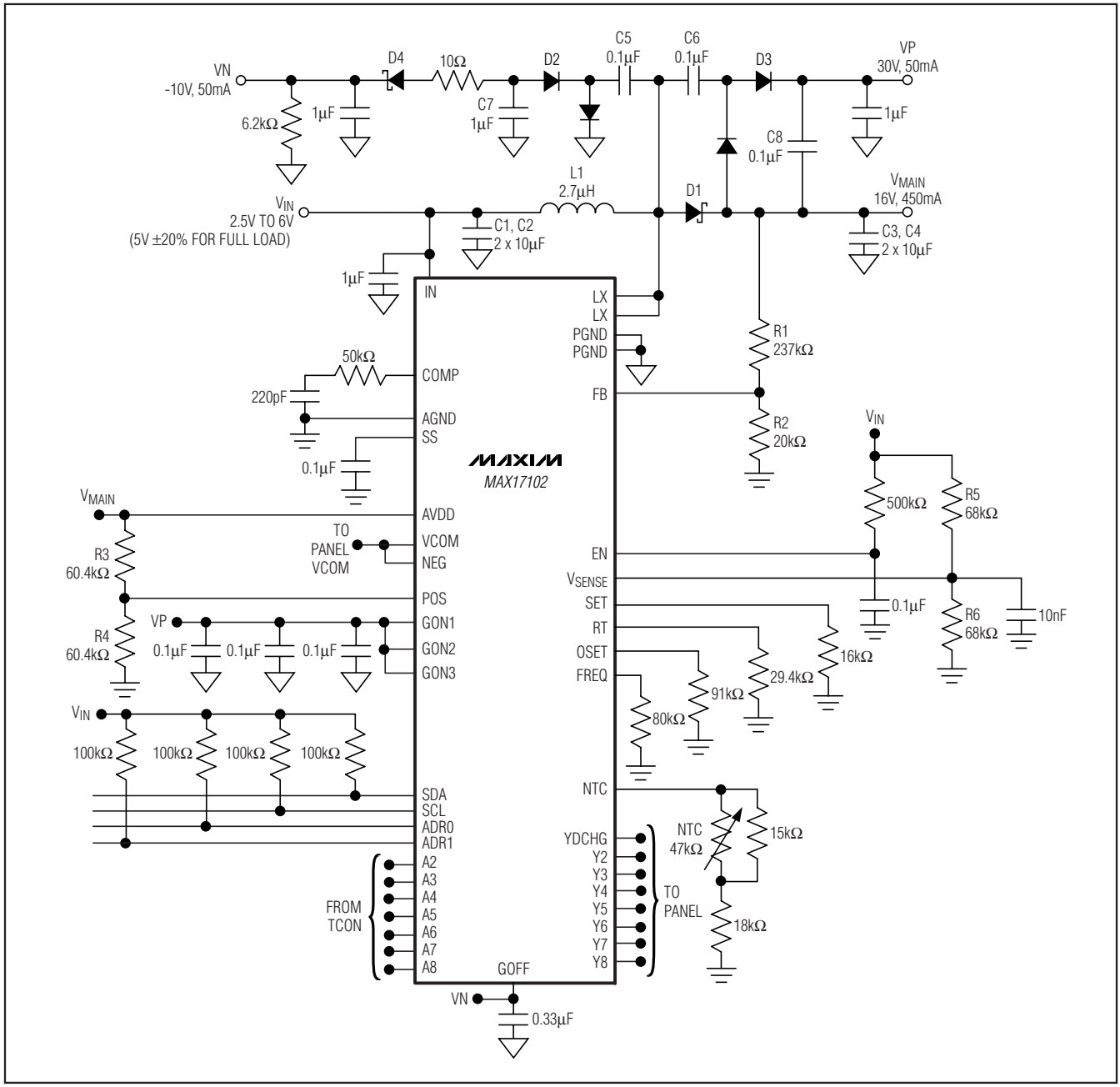


Figure 2. Typical Operating Circuit

Typical Operating Circuit

The typical operating circuit (Figure 2) of the MAX17102 is a complete power-supply system for TFT LCD panels in monitors and TVs. The circuit generates a +16V source driver supply from a +2.5V to +6.0V input. A +30V positive gate-driver supply and a -12V negative gate-driver supply can also be easily derived using discrete components. Table 1 lists some selected components and Table 2 lists the contact information for component suppliers.

Table 1. Component List

DESIGNATION	DESCRIPTION
C1, C2	10µF ±20%, 6.3V X5R ceramic capacitors (0805) Murata GRM188R60J106M TDK C1608X5R0J106M
C3, C4	10µF ±20%, 25V X5R ceramic capacitors (1210) Murata GRM31CR61E106M TDK C3216X5R1E106M
C5–C8	0.1µF ±10%, 50V X7R ceramic capacitors (0603) Murata GRM188R71H104K TDK C1608X7R1H104K

DESIGNATION	DESCRIPTION
D1	3A, 30V Schottky diode (M-Flat) Toshiba CMS02(TE12L,Q)
D2, D3	30V, 200mA dual diodes (3 SOT23) Zetex BAT54S Fairchild BAT54S
D4	2.7V, 500mW zener diode, (SOD-123) Diodes, Inc. BZT52C2V7-7-F
L1	2.7µH, 3ADC inductor Sumida CDR6D23MNNP-2R7NC

Table 2. Component Suppliers

SUPPLIER	PHONE	FAX	WEBSITE
Diodes Inc.	805-446-4800	805-446-4850	www.diodes.com
Fairchild Semiconductor	888-522-5372	408-822-2102	www.fairchildsemi.com
Murata Electronics North America, Inc.	770-436-1300	770-436-3030	www.murata-northamerica.com
Sumida Corp.	847-545-6700	847-545-6720	www.sumida.com
TDK Corp.	847-803-6100	847-390-4405	www.component.tdk.com
Toshiba America Electronic Components, Inc.	949-623-2900	949-859-3963	www.toshiba.com/taec
Zetex Semiconductors	631-543-7100	631-360-8222	www.zetex.com

Detailed Description

The MAX17102 contains an adjustable constant-frequency current-mode control step-up switching regulator to generate the source driver supply. Gate driver supplies can be easily derived using discrete components and the switching node (LX pin). The MAX17102 also includes one high-performance op amp designed to drive the LCD back plane (VCOM). Besides the features of high output current (150mA typ), fast slew rate (45V/µs), wide bandwidth (20MHz), and rail-to-rail inputs and outputs, the amplifier has a programmable VCOM calibrator that can adjust VCOM through serial interface with 7-bit resolution. It can also be temperature compensated by connecting an external temperature-sensing element and resistors that set the compensation enabling threshold and compensation slope. The high-voltage level-shifting scan drivers are designed to drive the TFT panel gate lines. All eight outputs can swing from +35V (max) to -10V and swiftly drive capacitive loads. Figure 3 shows the MAX17102 functional diagram.

Internal-Switch Boost Regulator with Scan Driver, Op Amp, LDO, and VCOM Calibrator

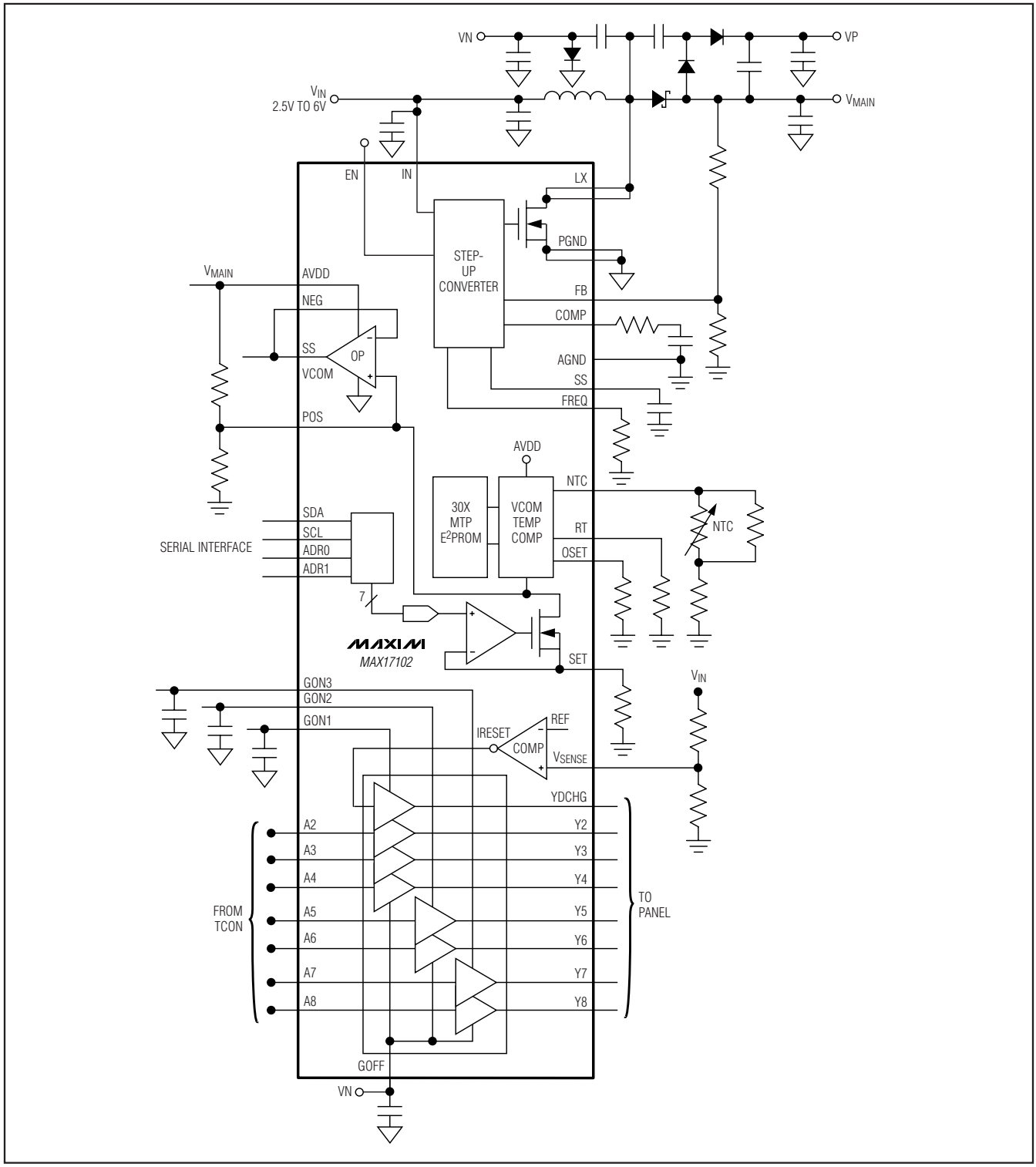


Figure 3. MAX17102 Functional Diagram

Internal-Switch Boost Regulator with Scan Driver, Op Amp, LDO, and VCOM Calibrator

Main Step-Up Regulator

The step-up regulator employs peak current-mode control architecture with an adjustable (450kHz to 1.2MHz), constant-switching frequency that maximizes loop bandwidth and provides a fast-transient response to pulsed loads found in source drivers of TFT-LCD panels. The high switching frequency is programmable from 450Hz to 1.2MHz by selecting an appropriate external resistor connected between the FREQ input and AGND.

The regulator controls the output voltage and the power delivered to the output by modulating the duty cycle (D) of the internal power MOSFET in each switching cycle. The duty cycle of the MOSFET is approximated by:

$$D \approx \frac{V_{MAIN} - V_{IN}}{V_{MAIN}}$$

where V_{MAIN} is the output voltage of the step-up regulator.

Figure 4 shows the step-up regulator functional diagram. An error amplifier compares the signal at FB to 1.235V and changes the COMP output. The voltage at COMP sets the peak inductor current. As the load varies, the error amplifier sources or sinks current to the COMP output accordingly to produce the inductor peak current necessary to service the load. To maintain stability at high duty cycles, a slope compensation signal is summed with the current-sense signal.

On the rising edge of the internal clock, the controller sets a flip-flop, turning on the n-channel MOSFET and applying the input voltage across the inductor. The current through the inductor ramps up linearly, storing energy in its magnetic field. Once the sum of the current-feedback signal and the slope-compensation exceed the COMP voltage, the controller resets the flip-flop and turns off the MOSFET. Since the inductor current is continuous, a transverse potential develops across the inductor that turns on the diode (D1). The voltage across the inductor then becomes the difference between the output voltage and the input voltage. This discharge condition forces the current through the inductor to ramp back down, transferring the energy stored in the magnetic field to the output capacitor and the load. The MOSFET remains off for the rest of the clock cycle.

Power-Up Sequence and Soft-Start

During startup, an internal reference is enabled when the input voltage is higher than the UVLO. Once the internal reference reaches regulation, the step-up regulator also enters its soft-start period simultaneously if EN is set to high.

Soft-start limits the peak switch current, allowing from zero up to full current limit in the time duration set by the capacitor at the SS pin. The current-charging SS capacitor is 5µA. The full current limit is available when the voltage at SS reaches 1.235V (typ). This soft-start routine minimizes the inrush current and voltage overshoot, and ensures a well-defined startup behavior. Figure 5 shows the power-up sequence.

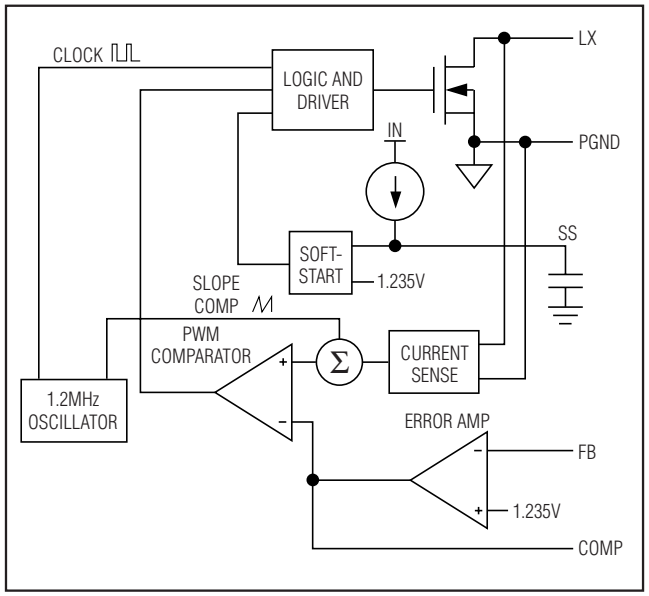


Figure 4. Step-Up Regulator Block Diagram

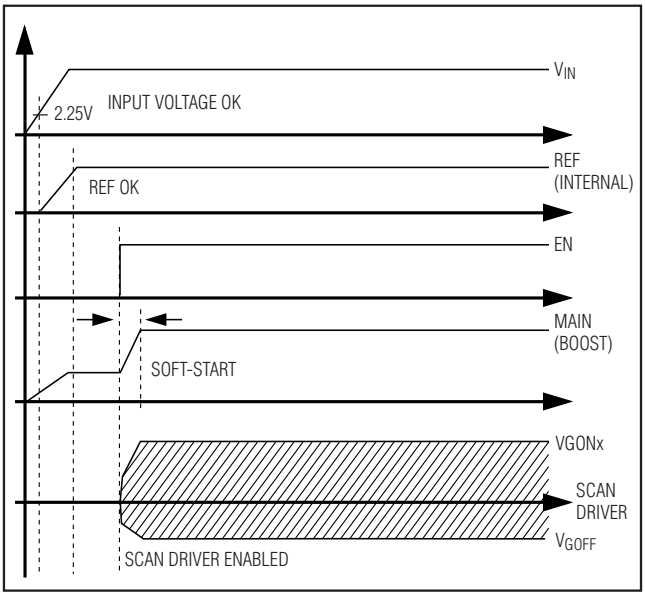


Figure 5. Power-Up Sequence

Internal-Switch Boost Regulator with Scan Driver, Op Amp, LDO, and VCOM Calibrator

Undervoltage Lockout (UVLO)

The undervoltage lockout (UVLO) circuit compares the input voltage at IN with the UVLO threshold (2.25V rising and 2.05V falling (typ)) to ensure that the input voltage is high enough for reliable operation. The 200mV (typ) hysteresis prevents supply transients from causing a restart. Once the input voltage exceeds the UVLO rising threshold, startup begins. When the input voltage falls below the UVLO falling threshold, the controller turns off the main step-up regulator and the op-amp outputs are high impedance.

Op Amp

The MAX17102 has one op amp. The op amp is typically used to drive the LCD backplane (VCOM) or the gamma-correction divider string. It features ±350mA output short-circuit current, 45V/µs slew rate, and 20MHz, 3dB bandwidth. The rail-to-rail input and output capability maximizes system flexibility.

Short-Circuit Current Limit and Input Clamp

The op amp delivers minimum short-circuit current of ±150mA if the output is directly shorted to V_{IN} or to GND. If the short-circuit condition persists, the junction temperature of the IC rises until it reaches the thermal-shutdown threshold (+160°C typ). Once the junction temperature reaches the thermal-shutdown threshold, an internal thermal sensor temporarily shuts off all the IC's outputs. See the *Thermal-Overload Protection* section for details.

Driving Pure Capacitive Load

The op amp is typically used to drive the LCD backplane (VCOM) or the gamma-correction divider string. The LCD backplane consists of a distributed series capacitance and resistance, a load that can be easily driven by the op amp. However, if the op amp is used in an application with a pure capacitive load, steps must be taken to ensure stable operation. As the op amp's capacitive load increases, the amplifier's bandwidth decreases and gain peaking increases. A 5Ω to 50Ω small resistor placed between OUT and the capacitive load reduces peaking, but also reduces the gain. An alternative method of reducing peaking is to place a series RC network (snubber) in parallel with the capacitive load. The RC network does not continuously load the output or reduce the gain. Typical values of the resistor are between 100Ω and 200Ω, and the typical value of the capacitor is 10nF.

VCOM Calibrator

The VCOM calibrator is a solid-state alternative to mechanical potentiometers used for adjusting the LCD backplane voltage (VCOM) in TFT LCD displays. A digitally controlled current source attaches to the external resistive voltage-divider at the POS terminals of the op amp and sinks a programmable current (I_{CAL}), which sets the VCOM levels (Figure 6). An internal 7-bit digital-to-analog converter (DAC) controls the sink current and allows the user to increase or decrease the VCOM levels. The DAC is ratiometric (1/20) relative to V_{MAIN} and is monotonic over all operating conditions. The user can store the DAC setting in the internal **nonvolatile** memory cells—multiple one-time programmable (MTP). On power-up, the MTP presets the DAC to the last stored setting. The 2-wire serial interface between the system controller and the programming circuit is used to adjust the DAC and program the MTP.

The resistive voltage-divider and AVDD supply set the maximum value of VCOM. I_{CAL} sink current reduces the POS voltage level and VCOM output. The external resistor at SET (R_{SET}) sets the full-scale sink current and the minimum value of VCOM.

The AVDD input provides the high voltage required to program the MTP. AVDD should be between 7.5V and 18V. MTP programming is disabled when AVDD is below 7.25V (typ).

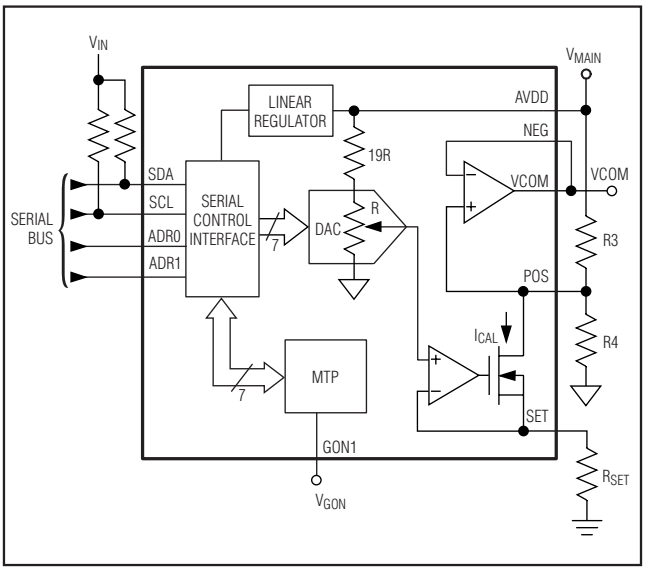


Figure 6. VCOM Calibrator Functional Diagram

VCOM Temperature Compensation

VCOM temperature compensation utilizes external temperature-sensing element (NTC) and resistors to set the enabling threshold and compensation slope; see Figure 7. The exact same amount of current sources from the RT and the NTC pins. Once the RT pin voltage is larger than the NTC pin voltage, this temperature compensation circuit is activated. An offset voltage set by R_{OSET} is added immediately to VCOM after the compensation circuit starts to work. The compensation slope largely depends on the characteristic of NTC. Resistors R_P and R_S are added to NTC to make the effective resistance-temperature characteristic more linear. See Figure 8 for VCOM temperature compensation characteristics.

Hysteresis is necessary to avoid VCOM jump back and force one offset voltage apart. Typical hysteresis is 6°C. If NTC is left open, the temperature compensation is disabled.

High-Voltage Level-Shifting Scan Driver

The MAX17102 includes eight logic-level to high-voltage level-shifting scan drivers. The driver outputs, Y1–Y8, swing between their power-supply rails according to the input logic level on A1–A8. The driver output ties to GOFF when its input is logic-low, and to GON when its input is logic-high. They can swiftly drive capacitive loads.

These eight driver channels are grouped for different high-level supplies. A1–A4 are supplied from GON1, A5 and A6 are supplied from GON2, and A7 and A8 are supplied from GON3.

Working with the input voltage falling detector, the channel 1 (A1–Y1) scan driver is dedicated to be a discharge channel.

Input-Voltage Detector

The function of the voltage detector is to sense the input-voltage amplitude and to activate the level shifter's discharging channel (YDCHG) once the input voltage falls below a user-defined threshold, (V_{IN_TH}). A comparator senses the input voltage through an external resistor-divider from V_{IN}. See Figure 3. Once the voltage at the positive terminal of the comparator (V_{SENSE}) falls below the voltage at the negative terminal of the comparator (1.235V), the comparator output goes high to activate the level shifter. Once the level shifter receives the signal, the YDCHG output is tied to GON1 to discharge the panel.

During power-down, the comparator output is high if V_{SENSE} < 1.235V or if V_{IN} < V_{IN_UVLO}. After the discharge function is triggered, the comparator output remains high even when the input voltage disappears, thus providing longer discharge time.

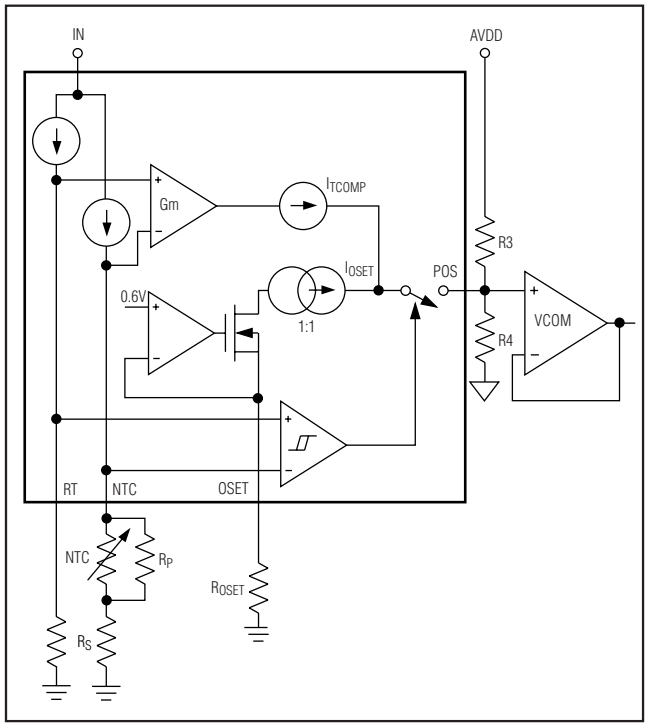


Figure 7. VCOM Temperature Compensation Functional Diagram

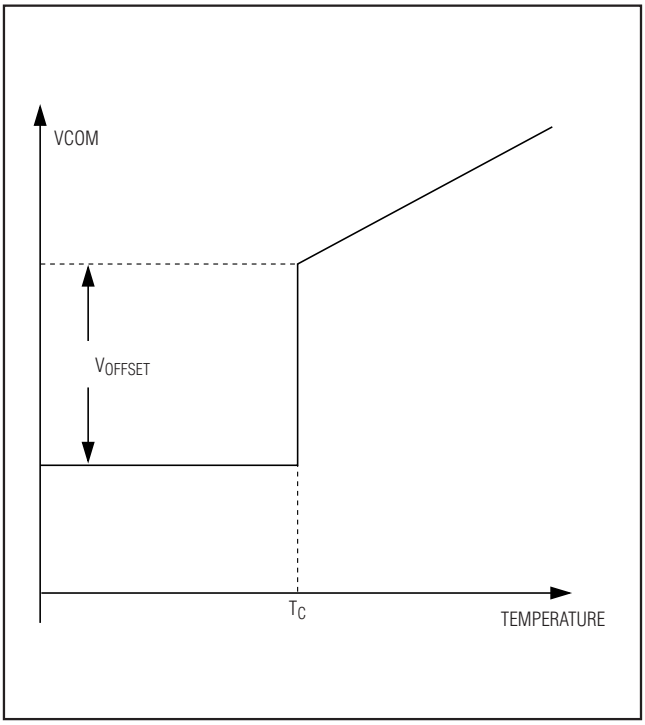


Figure 8. VCOM Temperature Compensation Characteristics

Internal-Switch Boost Regulator with Scan Driver, Op Amp, LDO, and VCOM Calibrator

Thermal-Overload Protection

The thermal-overload protection prevents excessive power dissipation from overheating the device. When junction temperature exceeds T_J = +160°C, a thermal sensor temporarily activates the fault protection, shuts down all outputs, allowing the device to cool down. Once the device cools down by approximately 15°C, it is reactivated. The MAX17102 tries this three times. After the third time, the fault latch is set and the MAX17102 does not restart until the power is recycled.

Design Procedure

Main Step-Up Regulator

Inductor Selection

The minimum inductance value, peak current rating, and series resistance are factors to consider when selecting the inductor. These factors influence the converter's efficiency, maximum output load capability, transient response time, and output-voltage ripple. Physical size and cost are also important factors to be considered.

The maximum output current, input voltage, output voltage, and switching frequency determine the inductor value. Very high inductance values minimize the current ripple and therefore reduce the peak current, which decreases core losses in the inductor and I^2R losses in the entire power path. However, large inductor values also require more energy storage and more turns of wire, which increase physical size and can increase I^2R losses in the inductor. Low inductance values decrease the physical size but increase the current ripple and peak current. Finding the best inductor involves choosing the best compromise between circuit efficiency, inductor size, and cost.

The equations used here include a constant called LIR, which is the ratio of the inductor peak-to-peak ripple current to the average DC inductor current at the full load current. The best trade-off between inductor size and circuit efficiency for step-up regulators generally has an LIR between 0.3 and 0.5. However, depending on the AC characteristics of the inductor core material and ratio of inductor resistance to other power-path resistances, the best LIR can shift up or down. If the inductor resistance is relatively high, more ripples can be accepted to reduce the number of turns required and increase the wire diameter. If the inductor resistance is relatively low, increasing inductance to lower the peak current can decrease losses throughout the power path. If extremely thin high-resistance inductors are used, as is common for LCD panel applications, the best LIR can increase to between 0.5 and 1.0.

Once a physical inductor is chosen, higher and lower values of the inductor should be evaluated for efficiency improvements in typical operating regions.

In Figure 2's typical operating circuit, the LCD's gate-on and gate-off supply voltages are generated from two unregulated charge pumps driven by the step-up regulator's LX node. The additional load on LX must therefore be considered in the inductance and current calculations. The effective maximum output current, $I_{MAIN(EFF)}$, becomes the sum of the maximum load current of the step-up regulator's output plus the contributions from the positive and negative charge pumps:

$$I_{MAIN(EFF)} = I_{MAIN(MAX)} + n_{NEG} \times I_{NEG} + (n_{POS} + 1) \times I_{POS}$$

where $I_{MAIN(MAX)}$ is the maximum step-up output current, n_{NEG} is the number of negative charge-pump stages, n_{POS} is the number of positive charge-pump stages, I_{NEG} is the negative charge-pump output current, and I_{POS} is the positive charge-pump output current, assuming the initial pump source for I_{POS} is V_{MAIN}.

Calculate the approximate inductor value using the typical input voltage (V_{IN}), the maximum output current ($I_{MAIN(EFF)}$), the expected efficiency (η_{TYP}) taken from an appropriate curve in the *Typical Operating Characteristics*, and an estimate of LIR based on the above discussion:

$$L = \left(\frac{V_{IN}}{V_{MAIN}}\right)^2 \left(\frac{V_{MAIN} - V_{IN}}{I_{MAIN(EFF)} \times f_{OSC}}\right)\left(\frac{\eta_{TYP}}{LIR}\right)$$

Choose an available inductor value from an appropriate inductor family. Calculate the maximum DC input current at the minimum input voltage $V_{IN(MIN)}$ using conservation of energy and the expected efficiency at that operating point (η_{MIN}) taken from an appropriate curve in the *Typical Operating Characteristics*:

$$I_{IN(DC,MAX)} = \frac{I_{MAIN(EFF)} \times V_{MAIN}}{V_{IN(MIN)} \times \eta_{MIN}}$$

Calculate the ripple current at that operating point and the peak current required for the inductor:

$$I_{RIPPLE} = \frac{V_{IN(MIN)} \times \left(V_{MAIN} - V_{IN(MIN)}\right)}{L \times V_{MAIN} \times f_{OSC}}$$

$$I_{PEAK} = I_{IN(DC,MAX)} + \frac{I_{RIPPLE}}{2}$$

The inductor's saturation current rating and the MAX17102's LX current limit (I_{LIM}) should exceed I_{PEAK} and the inductor's DC current rating should exceed $I_{IN(DC,MAX)}$. For good efficiency, choose an inductor with less than 0.1Ω series resistance.

Considering the typical operating circuit, the maximum load current ($I_{MAIN(MAX)}$) is 450mA, with a 16V output and a typical input voltage of 5V. The effective full-load step-up current is:

$$I_{MAIN(EFF)} = 450mA + 1 \times 50mA + (1+1) \times 50mA = 600mA$$

Choosing an LIR of 0.25 and estimating efficiency of 87% at this operating point:

$$L = \left(\frac{5V}{16V}\right)^2 \left(\frac{16V - 5V}{0.6A \times 1.2MHz}\right)\left(\frac{0.87}{0.25}\right) \approx 1.7\mu H$$

A 2.7µH inductor is chosen. Then, using the circuit's minimum input voltage (3V) and estimating efficiency of 80% at that operating point:

$$I_{IN(DC,MAX)} = \frac{0.6A \times 16V}{3V \times 0.8} \approx 4A$$

The ripple current and the peak current at that input voltage are:

$$I_{RIPPLE} = \frac{3V \times (16V - 3V)}{2.7\mu H \times 16V \times 1.2MHz} \approx 0.75A$$

$$I_{PEAK} = 4A + \frac{0.75A}{2} = 4.375A$$

Note that this is an illustration only. The inductor peak current limit is less than 4A maximum; therefore, at V_{IN} = 3V, part does not deliver a full 600mA current.

Output Capacitor Selection

The total output-voltage ripple has two components: the capacitive ripple caused by the charging and discharging of the output capacitance, and the ohmic ripple due to the capacitor's equivalent series resistance (ESR):

$$V_{RIPPLE} = V_{RIPPLE(C)} + V_{RIPPLE(ESR)}$$

$$V_{RIPPLE(C)} \approx \frac{I_{MAIN}}{C_{OUT}}\left(\frac{V_{MAIN} - V_{IN}}{V_{MAIN} f_{OSC}}\right)$$

and:

$$V_{RIPPLE(ESR)} \approx I_{PEAK} R_{ESR(COUT)}$$

where I_{PEAK} is the peak inductor current (see the *Inductor Selection* section). For ceramic capacitors, the output-voltage ripple is typically dominated by $V_{RIPPLE(C)}$. The voltage rating and temperature characteristics of the output capacitor must also be considered.

Input Capacitor Selection

The input capacitor ($C_{1,2}$) reduces the current peaks drawn from the input supply and reduces noise injection into the IC. Two 10µF ceramic capacitors are used in the typical operating circuit (Figure 2) because of the high source impedance seen in typical lab setups. Actual applications usually have much lower source impedance since the step-up regulator often runs directly from the output of another regulated supply. Typically, $C_{1,2}$ can be reduced below the values used in the typical operating circuit. Ensure a low-noise supply at IN by using adequate C_{IN}.

Rectifier Diode

The MAX17102's high switching frequency demands a high-speed rectifier. Schottky diodes are recommended for most applications because of their fast recovery time and low forward voltage. In general, a 3A Schottky diode complements the internal MOSFET well.

Output-Voltage Selection

The output voltage of the main step-up regulator is adjusted by connecting a resistive voltage-divider from the output (V_{MAIN}) to AGND with the center tap connected to FB (see Figure 2). Select R2 in the 10kΩ to 50kΩ range. Calculate R1 with the following equation:

$$R1 = R2 \times \left(\frac{V_{MAIN}}{V_{REF}} - 1\right)$$

where V_{REF}, the step-up regulator's feedback set point, is 1.235V (typ). Place R1 and R2 close to the IC.

Loop Compensation

Choose R_{COMP} to set the high-frequency integrator gain for fast-transient response. Choose C_{COMP} to set the integrator zero to maintain loop stability.

For low-ESR output capacitors, use the following equations to obtain stable performance and good transient response:

$$R_{COMP} \approx \frac{69 \times V_{IN} \times V_{OUT} \times C_{OUT}}{L \times I_{MAIN(MAX)}}$$

$$C_{COMP} \approx \frac{10 \times V_{MAIN} \times L \times I_{MAIN(MAX)}}{(V_{IN})^2 \times (R_{COMP})}$$

To further optimize transient response, vary R_{COMP} in 20% steps and C_{COMP} in 50% steps while observing transient-response waveforms.

Internal-Switch Boost Regulator with Scan Driver, Op Amp, LDO, and VCOM Calibrator

Setting the VCOM Adjustment Range

The external resistive voltage-divider sets the maximum value of the VCOM adjustment range. R_{SET} sets the full-scale sink current, I_{OUT}, which determines the minimum value of the VCOM adjustment range. Large R_{SET} values increase resolution but decrease the VCOM adjustment range. Calculate R3, R4, and R_{SET} using the following procedure:

1) Choose the maximum VCOM level (V_{MAX}), the minimum VCOM level (V_{MIN}), and the AVDD supply voltage (V_{AVDD}).
2) Select R3 between 10kΩ and 500kΩ based on the acceptable power loss from the V_{MAIN} supply rail connected to AVDD:
3) Calculate R4:

$$R4 \cong \frac{V_{MAX}}{(V_{AVDD} - V_{MAX})} \times R3$$

4) Calculate R_{SET}:

$$R_{SET} = \frac{V_{MAX}}{20 \times (V_{MAX} - V_{MIN})} \times R3$$

5) Verify that I_{SET} does not exceed 120µA:

$$I_{SET} = \frac{V_{AVDD}}{20 \times R_{SET}}$$

If I_{SET} exceeds 120µA, return to step 2 and choose a larger value for R3.

The resulting resolution is:

$$\frac{(V_{MAX} - V_{MIN})}{127}$$

A complete design example is given below:

V_{MAX} = 8V, V_{MIN} = 6.3V, V_{MAIN} = 16V

If:

R3 = 68kΩ, then R4 = 68kΩ and R_{SET} = 16kΩ

Resolution = 13.4mV.

VCOM Temperature Compensation

Setting Threshold and Slope

1) Choose the temperature threshold T_C at which the compensation circuit is activated.
2) Choose the voltage amount at the maximum temperature T_{MAX} that needs to be compensated ΔV_{COM}. This in turn determines the compensation slope.
3) Calculate:

$$\Delta R = \frac{\Delta V_{COM}}{(R3//R4) \times K}$$

where K = 2µA/kΩ is the compensation current ratio.

Compensation current cannot exceed 14µA. Properly select R3//R4 to make sure that ΔR x 2µA/kΩ or ≤ 14µA. Iterations of R3//R4 calculations may be needed to satisfy both VCOM temperature compensation and VCOM calibrator adjustment range.

4) Calculate parallel resistor R_P based on:

$$R_{NTC}(T_C)//R_P - R_{NTC}(T_{MAX})//R_P = \Delta R.$$

R_P linearizes the NTC characteristic between T_C and T_{MAX}. The recommended NTC is Murata NCP18WB473J03RB. There is not too much restriction for choosing R_S as long as it does not move V_{NTC} close to IN to saturate the circuit, nor close to GND to reduce the sensitivity of the comparator.

5) Finally, calculate $R_T = R_{NTC}(T_C)//R_P + R_S$.

A complete design example is given below:

1) T_C = +40°C.
2) T_{MAX} = +85°C, ΔV_{COM} = 0.39V.
3)

$$\Delta R = \frac{0.39V}{(68k\Omega//68k\Omega) \times 2\mu A\, k\Omega} = 5.7k\Omega$$

4) R_{NTC}(+40°C) = 24.3kΩ, R_{NTC}(+85°C) = 4.7kΩ; therefore, R_P = 15kΩ.
5) Put $V_{NTC}(T_C)$ = 0.5V; that gives R_S = 18kΩ.
6) R_T = 24.3kΩ//15kΩ +18kΩ = 27.3kΩ.

Setting Offset Voltage

Offset voltage is set according to the following formula:

$$V_{OFFSET} = \frac{V_{OSET}}{R_{OSET}} \times (R3//R4)$$

where V_{OSET} = 0.6V.

Setting Input-Voltage-Detector Threshold

The input-voltage-detector threshold is adjusted by a resistive voltage-divider from the input (V_{IN}) to AGND with the center tap connected to V_{SENSE} (see Figure 2). Select R5 in the 50kΩ to 100kΩ range. Calculate R6 with the following equation:

$$R5 = (\frac{V_{IN_TH}}{V_{REF}} - 1) \times R6$$

where V_{REF} is 1.235V (typ). Place R5 and R6 close to the IC.

Internal-Switch Boost Regulator with Scan Driver, Op Amp, LDO, and VCOM Calibrator

Applications Information

Power Dissipation

An IC's maximum power dissipation depends on the thermal resistance from the die to the ambient environment and the ambient temperature. The thermal resistance depends on the IC package, PCB copper area, other thermal mass, and airflow.

The MAX17102, with its exposed backside pad soldered to 1in^2 of PCB copper, can dissipate approximately 2548W into +70°C still air. More PCB copper, cooler ambient air, and more airflow increase the possible dissipation, while less copper or warmer air decreases the IC's dissipation capability. The major components of power dissipation are the power dissipated in the step-up regulator, the operational amplifiers, and the high-voltage scan driver outputs.

Step-Up Regulator

The largest portions of the power dissipated by the step-up regulator are the internal MOSFET, the inductor, and the output diode. If the step-up regulator with 3.3V input and 300mA output has approximately 85% efficiency, approximately 5% of the power is lost in the internal MOSFET, approximately 3% in the inductor, and approximately 5% in the output diode. The remaining few percent are distributed among the input and output capacitors and the PCB traces. If the input power is approximately 3W, the power lost in the internal MOSFET is approximately 150mW.

Op Amps

The power dissipated in the op amps depends on the output current, the output voltage, and the supply voltage:

$$PD_{SOURCE} = I_{VCOM_SOURCE} \times (V_{BOOST} - V_{VCOM})$$

$$PD_{SINK} = I_{VCOM_SINK} \times V_{VCOM}$$

where I_{VCOM_SOURCE} is the output current sourced by one op amp, and I_{VCOM_SINK} is the output current that the op amp sinks.

In a typical case where the supply voltage is 16V and the output voltage is 8V with an output source current of 30mA, the power dissipated is 240mW.

Scan Driver Outputs

The power dissipated by the scan driver outputs (Y2–Y8) depends on the scan frequency, the capacitive load, and the difference between the GON and GOFF supply voltages:

$$PD_{SCAN} = \sum_{Y2}^{Y8} f_{SCAN_} \times C_{PANEL_} \times (V_{GON_} - V_{GOFF})^2$$

If all scan drivers operate at a frequency of 50kHz, the total loads are 20nF, and the supply voltage difference is 40V, then the power dissipated will be 1.6W.

VCOM Calibrator Interface

The MAX17102 is a slave-only device. The 2-wire serial interface (pins SCL and SDA) is designed to attach to a 1.8V to 6V serial bus. Calculate the maximum value of the pullup resistors using:

$$R_{PULLUP} \le \frac{t_R}{C_{BUS}}$$

where t_R is the rise time in the *Electrical Characteristics*, and C_{BUS} is the total capacitance on the bus.

Bus Not Busy

Both data and clock lines remain high. Data transfers can be initiated only when the bus is not busy (Figure 9).

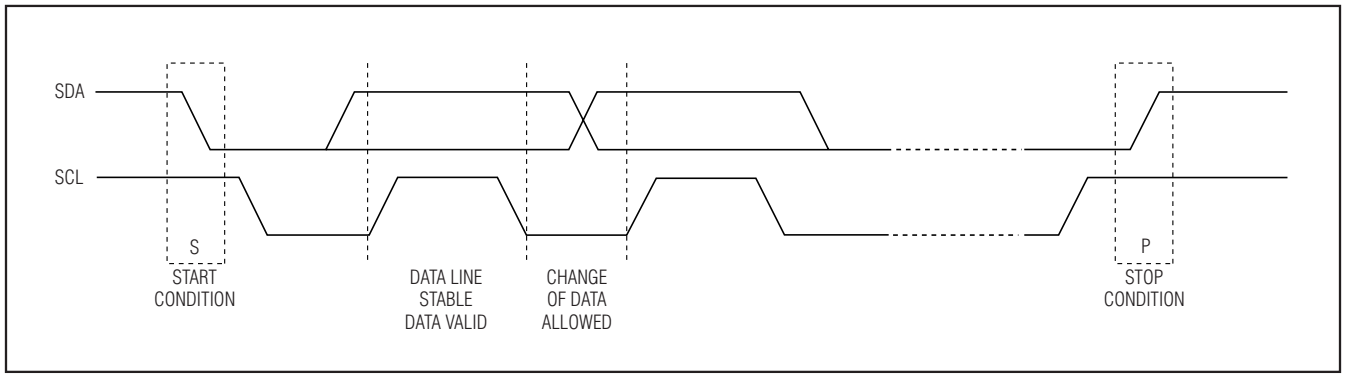


Figure 9. Serial Bus START and Data Change Conditions

Internal-Switch Boost Regulator with Scan Driver, Op Amp, LDO, and VCOM Calibrator

Start Data Transfer (S)

Starting from an idle bus state (both SDA and SCL are high), a high-to-low transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition from a master device on the bus.

Stop Data Transfer (P)

A low-to-high transition of the SDA line while the clock (SCL) is high determines a STOP condition. All operations must be ended with a STOP condition from the master device.

Data Valid

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal. The data on the line must be changed during the LOW period of the clock signal. The master generates one clock pulse per bit of data during write operations and the slave device outputs 1 data bit per clock pulse during read operations. Each data transfer is initiated with a START condition and terminated with a STOP condition. Two bytes are transferred between the START and STOP conditions.

Slave Address

The standard I^2C slave address byte consists of a 7-bit slave address plus a R/$\overline{W}$ bit (see Figure 10). For a read operation the R/$\overline{W}$ bit is 1 and for write operations it is 0. The MAX17102 slave address has to be determined by the state of the A0 and A1 address pins. These pins allow up to four devices to reside on the same serial bus. Address pins tied to GND result in a 0 in the corresponding bit position in the slave address. Conversely, address pins tied to V_{CC} result in a 1 in the corresponding bit positions. For example, if both A1 and A0 are tied to GND, the result slave address is 51h for write and 50h for read.

After generating a START condition, the bus master transmits the slave address for the MAX17102. The MAX17102 monitors the bus for its corresponding slave address continuously. It generates an acknowledge bit if it recognizes its slave address and it is not in busy programming the MTP.

An address byte is shown in Figure 10.

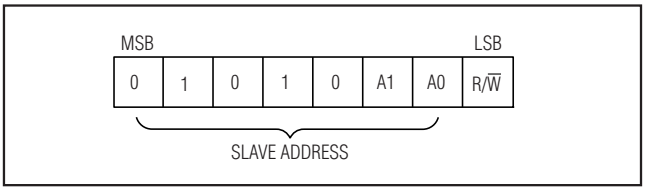


Figure 10. Address Byte

Data Register

Upon power-up of the MAX17102, the value stored in the nonvolatile initial value register (IVR) is recalled into the volatile VCOM register (VR). The VCOM value can then be changed any time after by writing the desired value to the VR/IVR register. The VR/IVR register is located at memory address 00h and is implemented as MTP volatile register.

The data byte is composed of a dummy MSB and 7 bits for the register. Reading 00h leads to VR on data bus. See Figure 11.

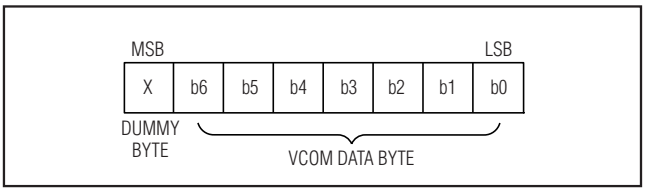


Figure 11. Data Byte Composition

Access Control Register

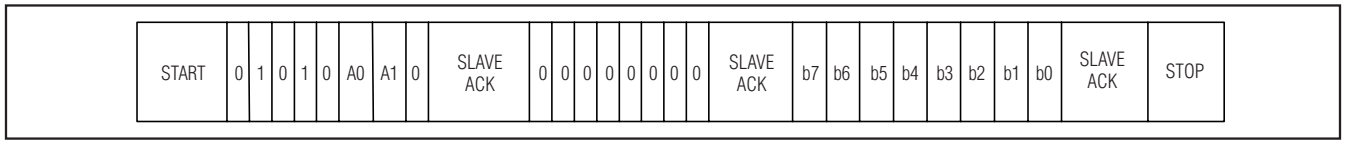
The access control register is volatile and at address 02h. It has 8 bits. Its MSB determines whether data is written to MTP. The remaining 7 bits are reserved. The customer can write either 00h or 80h to determine the access of VR or IVR memory. The default value is 00h. To program IVR MTP, 80h needs to be used. In addition, AVDD must exceed its programming threshold. Otherwise, programming does not occur and the MAX17102 does not acknowledge the programming command.

Write a Byte

A data byte has 8 bits of information (only the last 7 bits are used) transferred from master to slave with MSB first.

To write a byte, master generates a START condition, write the slave address byte (R/$\overline{W}$ = 0), write the memory address, write the byte of data, and generate a STOP condition.

To write a byte to address 00h:

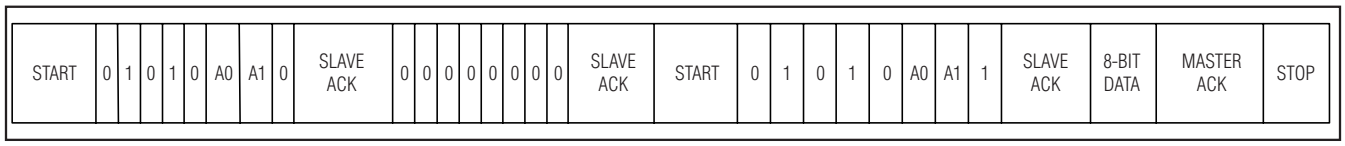


Read a Byte

Unlike writing a byte that uses the specified memory address byte to define where the data is to be written, the read operation reads the memory at the present address. To read a byte from the slave, the master needs to use a dummy write operation to fix the address, and then read from that byte.

Both 00h and 02h registers can be read in user mode.

To read a byte from 00h:



DAC Values

Table 3 lists the DAC values and the corresponding I_{SET}, V_{SET}, and V_{OUT} values.

Table 3. DAC Settings

7-BIT DATA BYTE	I_{SET}	V_{SET} (V)	V_{OUT} (V)
00000000	$I_{SET(MAX)}$	$V_{SET(MAX)}$	V_{MIN}
00000001	$I_{SET(MAX)}$ - 1 LSB	$V_{SET(MAX)}$ - 1 LSB	V_{MIN} + 1 LSB
. . .	. . .	. . .	. . .
1111110	$I_{SET(MIN)}$ + 1 LSB	$V_{SET(MIN)}$ + 1 LSB	V_{MAX} - 1 LSB
1111111	$I_{SET(MIN)}$	$V_{SET(MIN)}$	V_{MAX}

Acknowledge/Polling

The MAX17102, when addressed, generates an acknowledge pulse after the reception of each byte. The master device must generate an extra clock pulse, which is associated with this acknowledge bit. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable low during the high period of the acknowledge-related clock pulse. Of course, setup and hold times must be taken into account. The master signals an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line high to enable the master to generate the STOP condition.

The MAX17102 does not generate an acknowledge while an internal programming cycle is in progress. Once the internally timed write cycle has started and the MTP inputs are disabled, acknowledge polling can be initiated. This involves sending a START condition followed by the device address byte. Only if the internal write cycle has completed does the MAX17102 respond with an acknowledge pulse, allowing the read or write sequence to continue.

The MAX17102 does not acknowledge a command to program the MTP if AVDD is not high enough (see the *VCOM Calibrator* section) to properly program the device. Also, a program command must be preceded by a write command. The MAX17102 does not acknowledge a program command or program the MTP unless the DAC data has been modified since the most recent program command. Figure 12 shows the serial bus acknowledge, and Figure 13 shows the load model.

Internal-Switch Boost Regulator with Scan Driver, Op Amp, LDO, and VCOM Calibrator

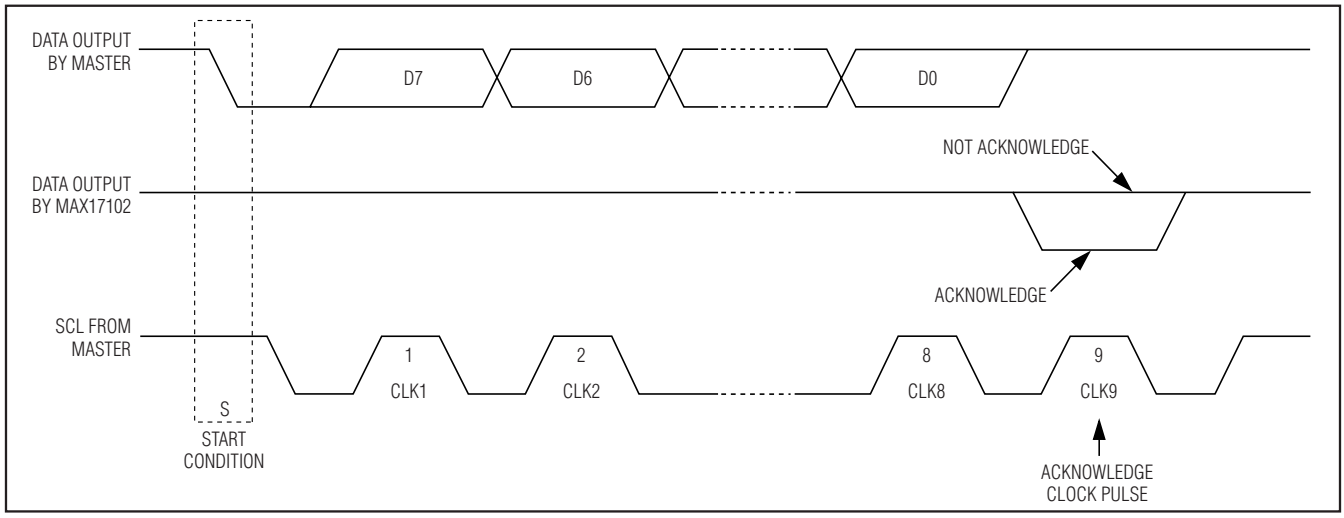


Figure 12. Serial Bus Acknowledge

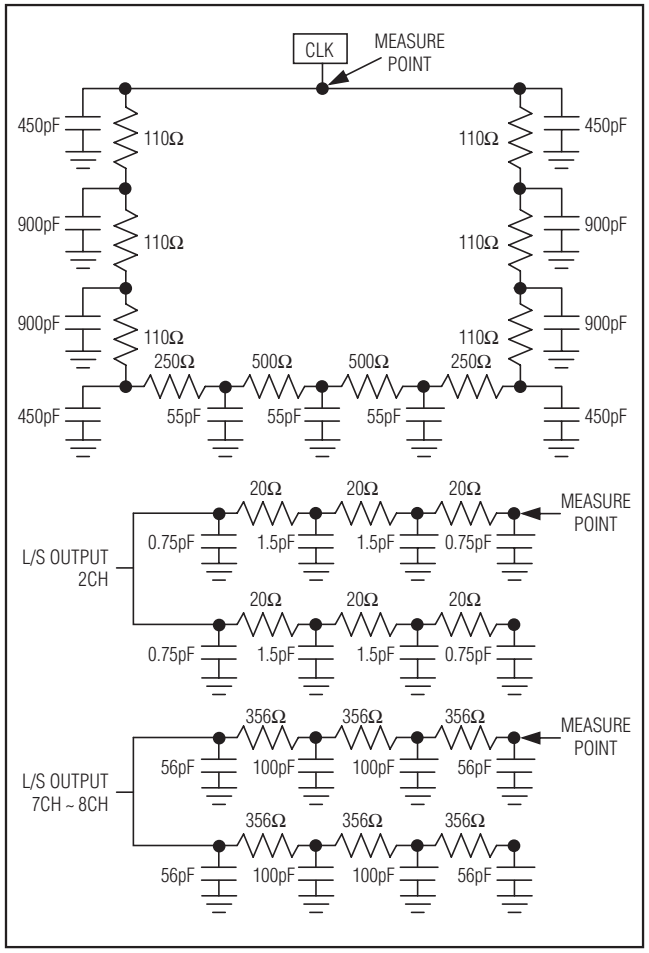


Figure 13. Load Model

PCB Layout and Grounding

Careful PCB layout is important for proper operation. Use the following guidelines for good PCB layout:

1) Minimize the area of high-current loops by placing the inductor, output diode, and output capacitors near the input capacitors and near the LX and PGND pins. The high-current input loop goes from the positive terminal of the input capacitor to the inductor, to the IC's LX pin, out of PGND, and to the input capacitor's negative terminal. The high-current output loop is from the positive terminal of the input capacitor to the inductor, to the output diode (D1), to the positive terminal of the output capacitors, reconnecting between the output capacitor and input capacitor ground terminals. Connect these loop components with short, wide connections. Avoid using vias in the high-current paths. If vias are unavoidable, use many vias in parallel to reduce resistance and inductance.

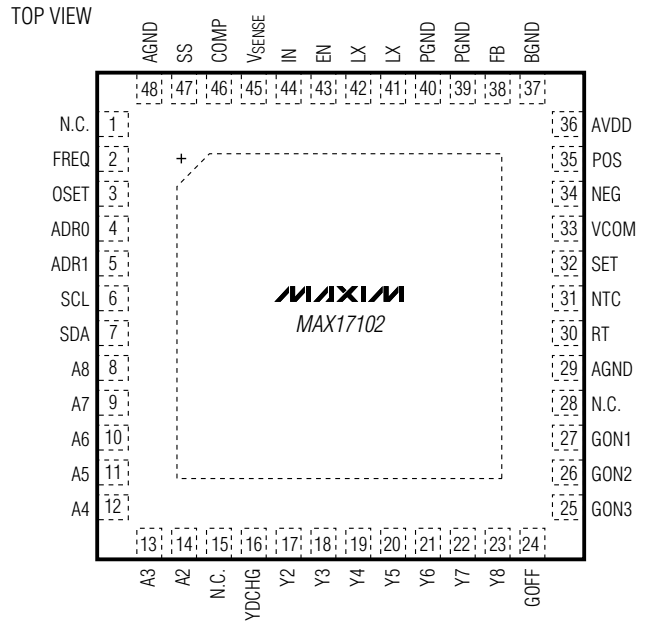
2) Create a power ground island (PGND) consisting of the input and output capacitor grounds, PGND pin, and any charge-pump components. Connect all these together with short, wide traces or a small ground plane. Maximizing the width of the power ground traces improves efficiency and reduces output-voltage ripple and noise spikes. Create an analog ground plane (AGND) consisting of the AGND pin, all the feedback-divider ground connections, the operational-amplifier-divider ground connections, the COMP capacitor ground connection, the AVDD capacitor ground connection, and the device's exposed backside pad. Connect the AGND and PGND islands by connecting the PGND pin

directly to the exposed backside pad. Make no other connections between these separate ground planes.

3) Place the feedback-voltage-divider resistors as close as possible to the feedback pin . The divider's center trace should be kept short. Placing the resistors far away causes the FB trace to become an antenna that can pick up switching noise. Care should be taken to avoid running the feedback trace near LX or the switching nodes in the charge pumps.
4) Place IN pin bypass capacitors as close as possible to the device. The ground connections of the IN bypass capacitor should be connected directly to the AGND pin with a wide trace.
5) Minimize the length and maximize the width of the traces between the output capacitors and the load for best transient responses.
6) Minimize the size of the LX node while keeping it wide and short. Keep the LX node away from the feedback node and analog ground. Use DC traces as shield, if necessary.

Refer to the MAX17102 Evaluation Kit for an example of proper board layout.

Pin Configuration



Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
48 TQFN	T4877N-8	21-0144

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