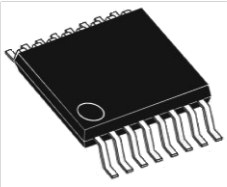
61 V, 3 A asynchronous step-down switching regulator with adjustable current limitation for automotive



HTSSOP 16

Features

- 3 A DC output current
- 4.5 V to 61 V operating input voltage
- $R_{DS(on)}$ = 250 mΩ typ.
- Adjustable f_{sw} (250 kHz to 1.5 MHz)
- Low IQ-SHD (11 µA typ. from VIN)
- Low IQ (1 mA typ. - VIN 24 V - VOUT 3.3 V)
- Output voltage adjustable from 0.8 V to VIN
- Synchronization
- Adjustable soft-start time
- Adjustable current limitation
- Low-dropout operation
- VBIAS improves efficiency at light load
- PGOOD open collector output
- Output voltage sequencing
- Digital frequency fold-back in short-circuit
- Auto recovery thermal shutdown
- Qualified following AEC-Q100 requirements

Product status link
A7987

Applications

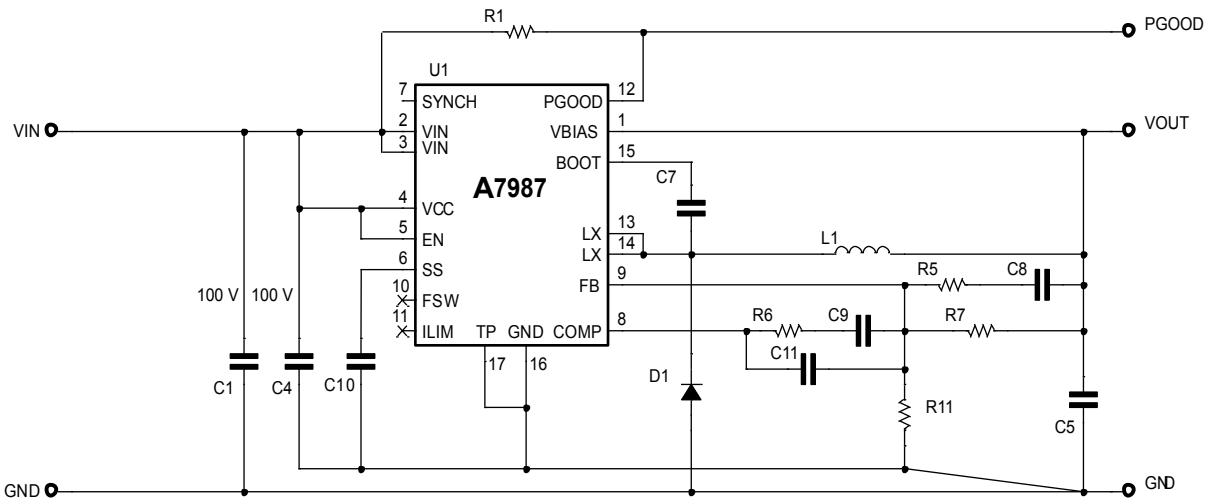
- Designed for 24 V automotive battery systems
- Industrial and commercial vehicles

Description

The A7987 is a step-down monolithic switching regulator that can deliver up to 3 A DC. The adjustable output voltage ranges from 0.8 V to VIN. The wide input voltage range and the almost 100% duty cycle capability meet the fail-safe specifications for industrial systems. The embedded switch-over feature on the VBIAS pin maximizes the efficiency at light load. The adjustable current limitation, designed to select the inductor RMS current in accordance with the nominal output current, and the high switching frequency capability make the size of the application compact. Pulse-by-pulse current sensing with digital frequency fold-back implements an effective constant current protection over the different application conditions. The peak current fold-back decreases the stress of the power components in heavy short-circuit conditions. The PGOOD open collector output can also implement the output voltage sequencing during the power-up phase. Multiple devices can be synchronized sharing the SYNCH pin to prevent beating noise for low noise requirements such as in infotainment applications.

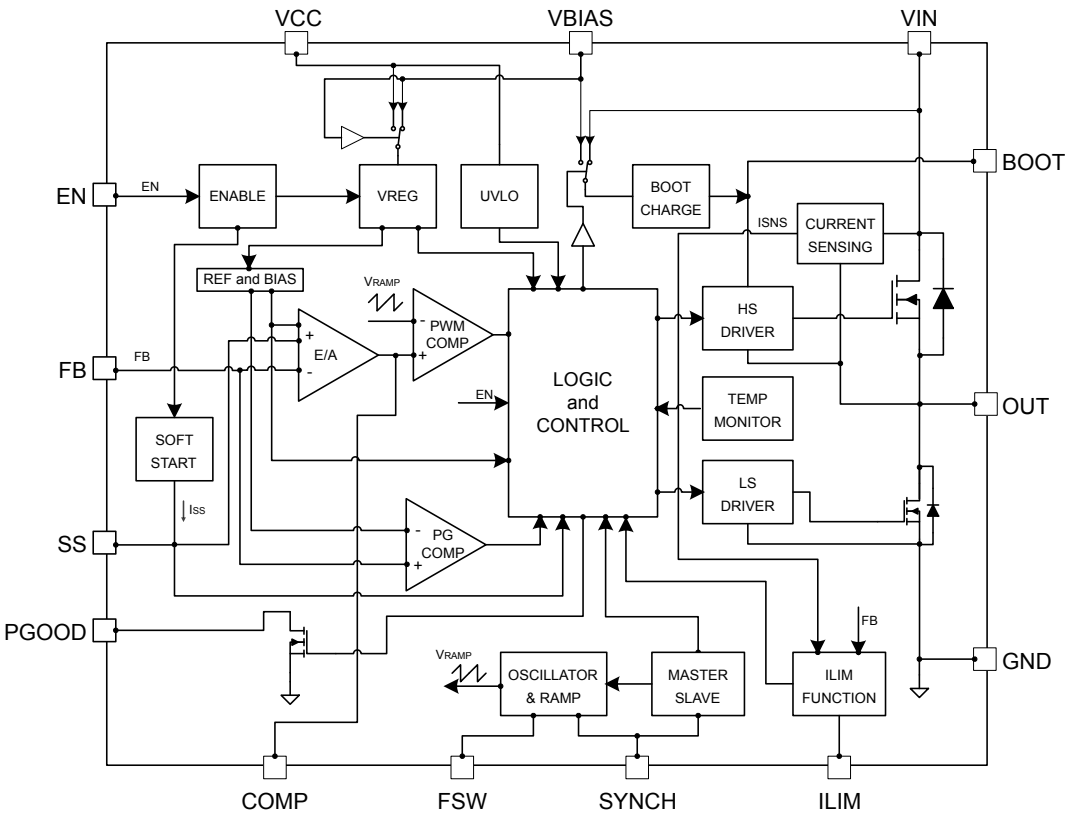
1 Application schematic

Figure 1. Application schematic



2 Block diagram

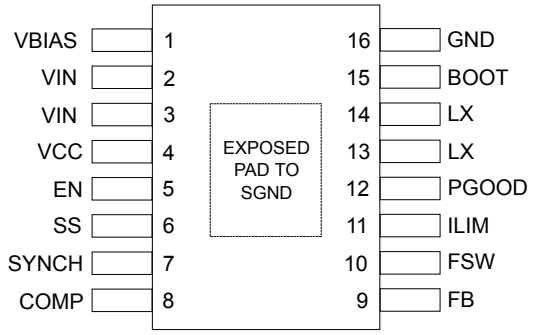
Figure 2. Block diagram



3 Pin settings

3.1 Pin connection

Figure 3. Pin connection (top view)



3.2 Pin description

Table 1. Pin description

#	Pin	Description
1	VBIAS	The auxiliary input can be used to supply part of the analog circuitry to increase the efficiency at light load. It is typically connected to the regulated output voltage or to an external voltage rail higher than 3 V. Connect to GND if it is not used or bypass with a 1 µF ceramic capacitor if supplied by the output voltage or by an auxiliary rail
2	VIN	DC input voltage
3	VIN	DC input voltage
4	VCC	Filtered DC input voltage to the internal circuitry. Bypass to GND with a 1 µF ceramic capacitor
5	EN	Active high enable pin. Connect to VCC pin if it is not used
6	SS	Soft-start programming pin. An internal current generator (5 µA typ.) charges the external capacitor to implement the soft-start
7	SYNCH	Master / slave synchronization
8	COMP	Output of the error amplifier. The designed compensation network is connected on this pin.
9	FB	Inverting input of the error amplifier
10	FSW	A pull-down resistor to GND selects the switching frequency
11	ILIM	A pull-down resistor to GND selects the peak current limitation
12	PGOOD	The PGOOD open collector output is driven low when the output voltage, sensed on the FB pin, is out of regulation
13	LX	Switching node
14	LX	Switching node
15	BOOT	Connect an external capacitor (100 nF typ.) between BOOT and LX pins. The gate charge required to drive the internal n-DMOS is recovered by an internal regulator during the off-time
16	GND	Signal GND

#	Pin	Description
--	E.P.	Exposed pad must be connected to signal GND

3.3 Maximum ratings

Table 2. Absolute maximum ratings

Symbol	Description	Min.	Max.	Unit
VIN		-0.3	61	V
VCC		-0.3	61	V
BOOT	VBOOT - GND	-0.3	65	V
	VBOOT – VLX	-0.3	4	V
VBIAS		-0.3	VCC	V
EN		-0.3	VCC	V
PGOOD		-0.3	VCC	V
LX		-0.3	VIN+0.3	V
SYNCH		-0.3	5.5	V
SS		-0.3	3.6	V
FSW		-0.3	3.6	V
COMP		-0.3	3.6	V
ILIM		-0.3	3.6	V
FB		-0.3	3.6	V
T_J	Operating temperature range	-40	150	°C
T_{STG}	Storage temperature range	-65	150	°C
T_{LEAD}	Lead temperature (soldering 10 s)		260	°C
I_{HS}	High-side RMS current		3	A

3.4 Thermal data

Table 3. Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}	Thermal resistance junction-ambient (device soldered on the STMicroelectronics evaluation board)	40	°C/W

3.5 ESD protection

Table 4. ESD protection

Symbol	Test conditions	Value	Unit
ESD	HBM	2	kV
	CDM	500	V

4 Electrical characteristics

T_J = -40 °C to +125 °C, V_{IN} = V_{CC} = 24 V and V_{EN} =3 V unless otherwise specified.

Table 5. Electrical characteristics

Symbol	Parameter	Test conditions		Min.	Typ.	Max.	Unit
V_{IN}	Operating input voltage range			4.5		61	V
$R_{DSON\ HS}$	High- side $R_{DS(on)}$	I_{SW}=0.5 A; T_j = 25 °C			0.25	0.32	Ω
		I_{SW}=0.5 A			0.25	0.46	Ω
f_{SW}	Switching frequency	FSW floating; T_j = 25 °C		233	250	267	kHz
		FSW floating		225	250	275	kHz
	Selected switching frequency	R_{FSW}=10 kΩ		1350	1500	1650	kHz
I_{PK}	Peak current limit	R_{LIM} 20 kΩ; V_{FB} = 0.6 V; T_J = 125 °C	(1)	3.2	3.7	4.4	A
		R_{LIM} 100 kΩ; V_{FB} = 0.6 V	(1)	0.69	0.84	1.0	A
		Ratio I_{PK_20k}/I_{PK_100k}	(2)		4.7		
I_{SKIP}	Pulse skipping peak current		(2)		0.5		A
V_{FOLD}	Feedback fold-back level		(2)		400		mV
T_{ONMAX}	Maximum on-time				12		µs
T_{ONMIN}	Minimum on-time				120	150	ns
T_{OFFMIN}	Minimum off-time		(2)		360		ns
VCC / VBIAS							
V_{CCH}	V_{CC} UVLO rising threshold			3.85	4.10	4.30	V
V_{CCHYST}	V_{CC} UVLO hysteresis			150	250	380	mV
SWO	V_{BIAS} threshold	Switch internal supply from V_{CC} to V_{BIAS}. VBIAS ramping up from 0 V		2.84	2.90	3.03	V
		Hysteresis			80		mV
	$V_{CC\ -VBIAS}$ threshold	Switch internal supply from V_{CC} to V_{BIAS}. V_{IN}=V_{CC}=24 V, V_{BIAS} falling from 24 V to GND		3.35	4.05	4.90	V
		Hysteresis			900		mV
Power consumption							
I_{SHTDWN}	Shutdown current from V_{IN}	VEN = GND; T_J = 25 °C			11	16	µA
		VEN = GND			23	45	
I_{QUIESC}	Quiescent current from V_{IN} and V_{CC}	LX floating, VFB=1 V, V_{BIAS}=GND, FSW floating			2.5	3.0	mA
I_{QOPVIN}	Quiescent current from V_{IN} and V_{CC}	LX floating, V_{FB}=1 V, V_{BIAS}=3.3 V, FSW floating			1.0	1.3	mA
$I_{QOPVBIAS}$	Quiescent current from V_{BIAS}				1.6	2.2	mA
Enable							
V_{EN}	Device OFF level			0.06		0.30	V
	Device ON level			0.35		0.90	V
Soft-start							

Symbol	Parameter	Test conditions		Min.	Typ.	Max.	Unit
T_{SSETUP}	Soft-start set-up time	Delay from UVLO rising to switching activity	(2)		640		µs
$I_{SS\ CH}$	CSS charging current	VSS=0		4.3	5.0	5.7	mA
Error amplifier							
V_{FB}	Voltage feedback	T_j = 25 °C		0.792	0.800	0.808	V
V_{FB}	Voltage feedback			0.788	0.800	0.812	V
V_{COMPH}		VFB=GND; V_{SS}=3.2 V		3.00	3.35	3.65	V
V_{COMPL}		VFB=1 V; V_{SS}=3.2 V				0.1	V
I_{FB}	FB biasing current	V_{FB}=3.6 V			5	50	nA
$I_{OSOURCE}$		V_{FB}=GND; SS pin floating; V_{COMP}=2 V	(2)		3.1		mA
I_{OSINK}	Output stage sinking capability	Unity gain buffer configuration (FB connected to COMP).COMP voltage variation due to I_{OSINK} injection lower than ± 0.1·V_{FB}	(2)		5		mA
A_{V0}	Error amplifier gain		(2)		100		dB
GBWP		Unity gain buffer configuration (FB connected to COMP). No load on COMP pin	(2)		23		MHz
Synchronization (fan out: 5 slave devices max.)							
$f_{SYN\ MIN}$	Synchronization frequency	FSW floating		280			kHz
V_{SYNOUT}	Master output amplitude	I_{LOAD}=4 mA		2.45			V
		I_{LOAD}=0 A; pin SYNCH floating				4.0	
V_{SYNOW}	Output pulse width	I_{LOAD}=0 A; pin SYNCH floating		150	225	275	ns
V_{SYNIH}	SYNCH slave high level input threshold			2.0			V
V_{SYNIL}	SYNCH slave low level input threshold					1.0	V
I_{SYN}	Slave SYNCH pull-down current	VSYNCH = 5 V		400	650	900	µA
V_{SYNIW}	Input pulse width			150			ns
PGOOD							
V_{PGDTH}	PGOOD rising threshold	VFB rising		0.67	0.70	0.74	V
$V_{PGDHYST}$	PGOOD hysteresis	VFB falling	(2)		30		mV
V_{PGDLOW}	PGOOD low level	I_{PGOOD}=1 mA, V_{FB}=GND			30		mV
I_{PGDLKG}	PGOOD leakage current	V_{PGOOD}=61 V;V_{FB}=0.8 V; T_j = 25 °C				0.1	µA
		V_{PGOOD}=61 V;V_{FB}=0.8 V				20	
Thermal shutdown							
T_{SHDWN}	Thermal shutdown temperature		(2)		170		°C
T_{HYS}	Thermal shutdown hysteresis		(2)		15		°C

1. *Parameter tested in a static condition during the testing phase. The parameter value may change over dynamic application conditions.*
2. *Not tested in production.*

5 Functional description

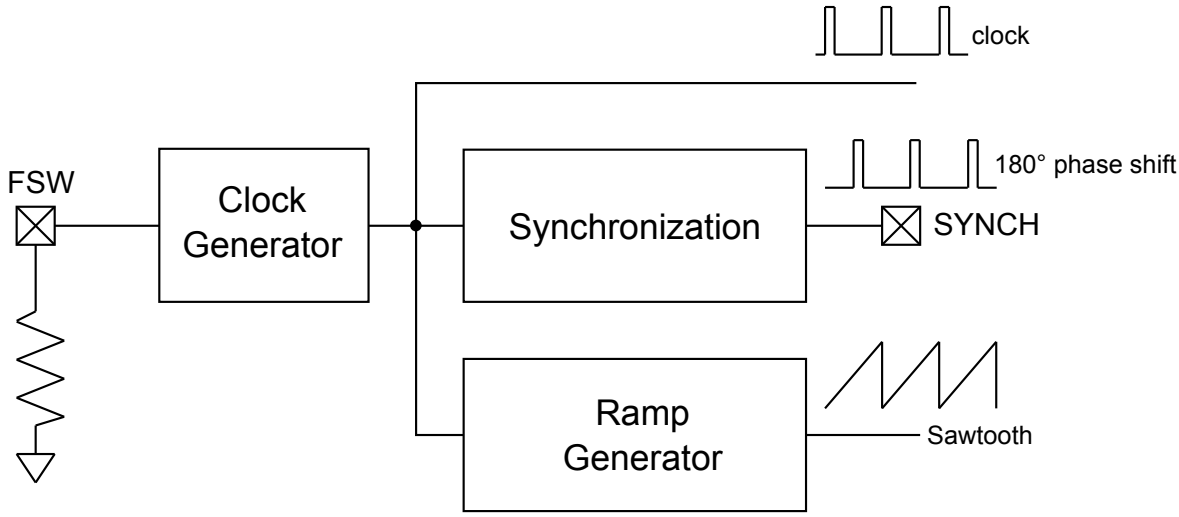
The A7987 device is based on a voltage mode, constant frequency control loop. The output voltage VOUT, sensed by the feedback pin (FB), is compared to an internal reference (0.8 V) providing an error signal on the COMP pin. The COMP voltage level is then compared to a fixed frequency sawtooth ramp, which finally controls the on- and off-time of the power switch. The main internal blocks are shown in the block diagram in Figure 2. Block diagram and can be summarized as follows:

- The fully integrated oscillator provides the sawtooth ramp to modulate the duty cycle and the synchronization signal. Its switching frequency can be adjusted by an external resistor. The input voltage feed-forward is implemented
- The soft-start circuitry to limit the inrush current during the start-up phase
- The voltage mode error amplifier
- The pulse width modulator and the relative logic circuitry necessary to drive the internal power switch
- The high-side driver for embedded N-channel power MOSFET switch and bootstrap circuitry. A dedicated high-resistance low-side MOSFET, for anti-boot discharge management purposes, is also present
- The peak current limit sensing block, with programmable threshold, to handle overload and short-circuit conditions including current fold-back and a thermal shutdown block, to prevent thermal runaway
- The voltage regulator and the internal reference to supply the internal circuitry and provide a fixed internal reference. The switchover function from VCC to VBIAS can be implemented for higher efficiency. This block also implements a voltage monitor circuitry (UVLO) that checks the input and internal voltages
- The output voltage monitor circuitry releases the PGOOD signal if the sensed output voltage is above 87% of the target value

5.1 Oscillator and synchronization

Figure 4. Oscillator and synchronization shows the block diagram of the oscillator circuit. The internal oscillator provides a constant frequency clock, whose frequency depends on the resistor externally connected between the FSW pin and ground.

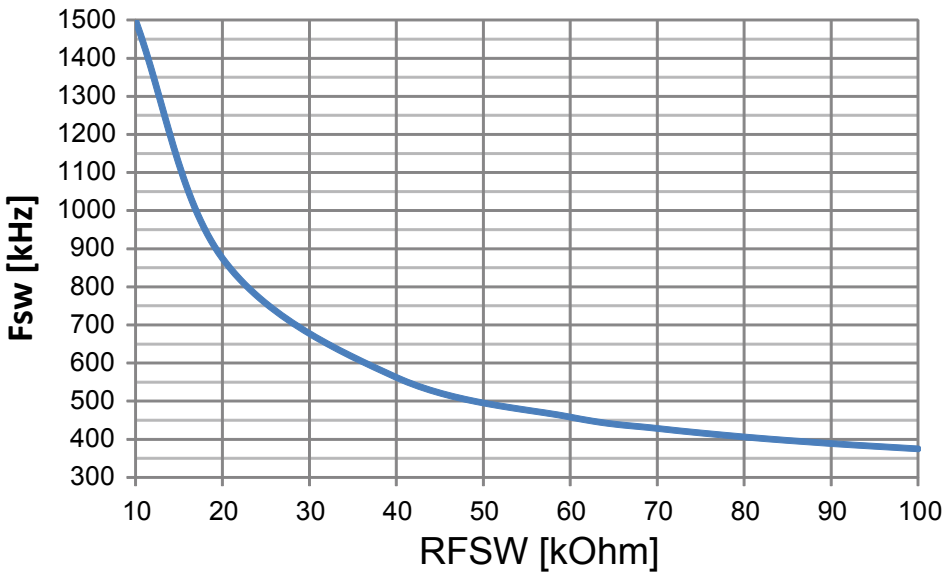
Figure 4. Oscillator and synchronization



If the FSW pin is left floating, the programmed frequency is 250 kHz (typ.); if FSW pin is connected to an external resistor the programmed switching frequency can be increased up to 1.5 MHz, as shown in Figure 5. Switching frequency programmability. The required RFSW value (expressed in kΩ) is estimated by the following equation:

$$F_{SW} = 250kHz + \frac{12500}{R_{FSW}} \quad (1)$$

Figure 5. Switching frequency programmability



To improve the line transient performance, keeping the PWM gain constant versus the input voltage, the input voltage feed-forward is implemented by changing the slope of the sawtooth ramp, according to the input voltage change (Figure 6. Feed-forward6a).

The slope of the sawtooth also changes if the oscillator frequency is programmed by the external resistor. In this manner, a frequency feed-forward is implemented (Figure 6. Feed-forward6b) in order to keep the PWM modulator gain constant versus the switching frequency.

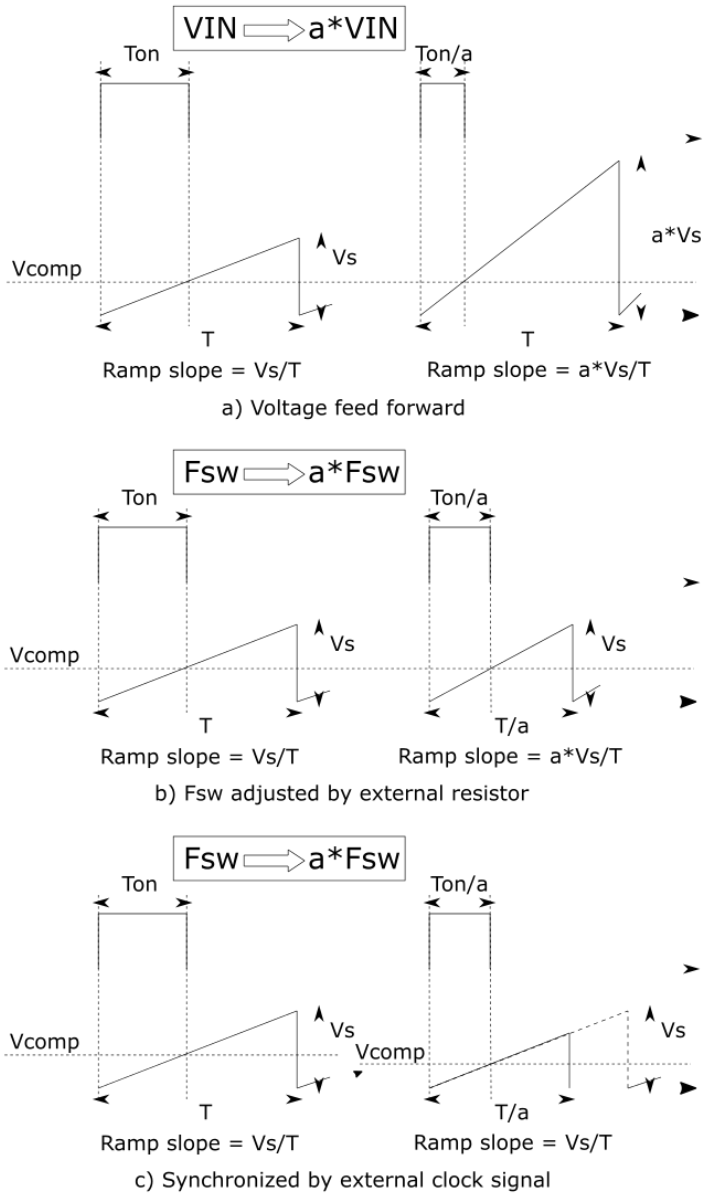
On the SYNCH pin the synchronization signal is generated. This signal has a phase shift of 180 ° with respect to the clock. This delay is useful when two devices are synchronized connecting the SYNCH pins together. When SYNCH pins are connected, the device with a higher oscillator frequency works as master, so the slave device switches at the frequency of the master but with a delay of half period. This helps reducing the RMS current flowing through the input capacitor. Up to five A7987s can be connected to the same SYNCH pin; however, the clock phase shift from master switching frequency to slaves input clock is 180 °.

The A7987 can be synchronized to work at a higher frequency, in the range 250 kHz-1500 kHz, providing the SYNCH pin with an external clock signal. The synchronization changes the sawtooth amplitude, also affecting the PWM gain (Figure 6. Feed-forward6c). This change must be taken into account when the loop stability is studied. In order to minimize the change of PWM gain, the free-running frequency should be set (with a resistor on the FSW pin) only slightly lower than the external clock frequency.

This pre-adjusting of the slave IC switching frequency keeps the truncation of the ramp sawtooth negligible.

In case two or more (up to five) A7987 SYNCH pins are tied together, the A7987 IC with higher programmed switching frequency is typically the master device; however, the SYNCH circuit is also able to synchronize with a slightly lower external frequency, so the frequency pre-adjustment with the same resistor on FSW pin, as suggested above, is required for a proper operation.

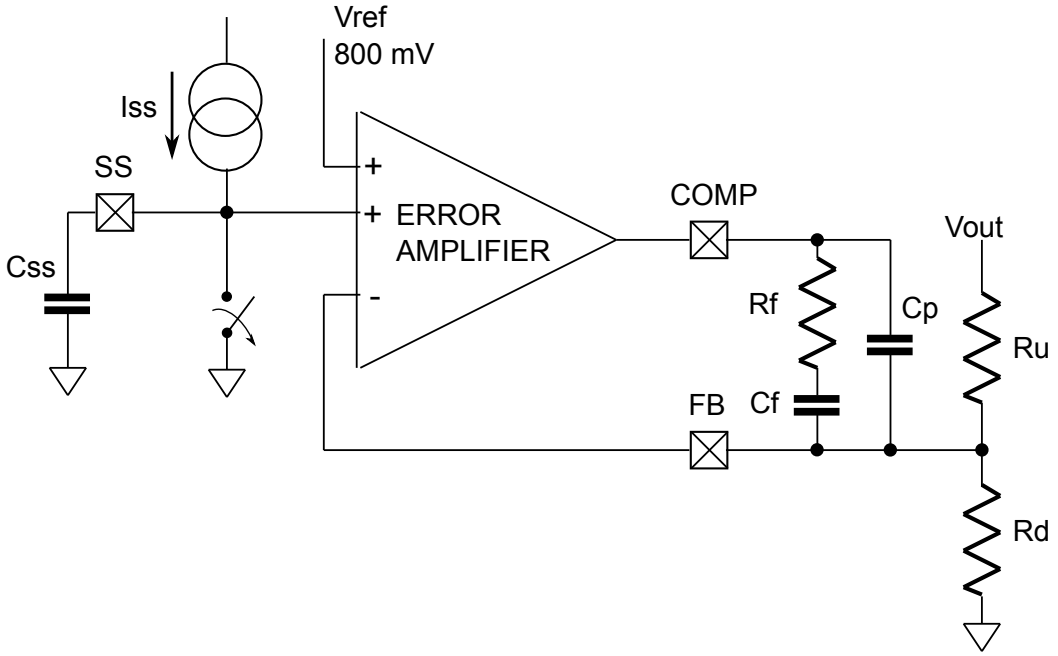
Figure 6. **Feed-forward**



5.2 Soft-start

The soft-start is essential to ensure a correct and safe start-up of the step-down converter. It avoids inrush current surge and makes the output voltage increase monotonically. The soft-start is performed by charging an external capacitor, connected between SS pin and ground, with a constant current (5 µA typ.). The SS voltage is used as reference of the switching regulator and the output voltage of the converter tracks the ramp of the SS voltage. When the SS pin voltage reaches 0.8 V level, the error amplifier switches to the internal 0.8 V ±1% reference to regulate the output voltage.

Figure 7. **Soft-start**



During the soft-start period the current limit is set to the nominal value.

The dV_{SS}/dt slope is programmed in agreement with the following equation:

$$C_{SS} = \frac{I_{SS} \cdot T_{SS}}{V_{REF}} = \frac{5_{\mu A} \cdot T_{SS}}{0.8V} \quad (2)$$

Before starting the C_{SS} capacitor charge, the soft-start circuitry turns on the discharge switch shown in Figure 7. Soft-start for $T_{SSDISCH}$ minimum time, in order to completely discharge the C_{SS} capacitor. As a consequence, the maximum value for the soft-start capacitor, which assures an almost complete discharge in case of EN signal toggle, is provided by:

$$C_{SS_MAX} \leq \frac{T_{SSDISCH}}{5 \cdot R_{SSDISCH}} \cong 270nF \quad (3)$$

given TSSDISCH = 530 µs and RSSDISCH = 380 Ω typical values. The enable feature allows the device to be in standby mode. With the EN pin lower than device OFF level, the device is disabled and the power consumption is reduced to less than 11 µA (typ.). With the EN pin higher than device ON level, the device is enabled. If the EN pin is left floating, an internal pull-down current ensures that the voltage on the pin reaches the inhibit threshold and the device is disabled. The pin is also VCC compatible.

5.3 Error amplifier and light-load management

The error amplifier (E/A) provides the error signal to be compared with the sawtooth to perform the pulse width modulation. Its non-inverting input is internally connected to a 0.8 V voltage reference and its inverting input (FB) and output (COMP) are externally available for feedback and frequency compensation. In this device the error amplifier is a voltage mode operational amplifier, therefore, with high DC gain and low output impedance. The uncompensated error amplifier characteristics are summarized in Table 6. Error amplifier characteristics:

Table 6. Error amplifier characteristics

Characteristics	Value
Low frequency gain (A0)	100 dB
GBWP	23 MHz
Output voltage swing	0 to 3.5 V
Source/sink current capability	3.1 mA / 5 mA

In continuous conduction working mode (CCM), the transfer function of the power section has two poles due to the LC filter and one zero due to the ESR of the output capacitor. Different kinds of compensation networks can be used depending on the ESR value of the output capacitor.

If the zero introduced by the output capacitor helps to compensate the double pole of the LC filter, a type II compensation network can be used. Otherwise, a type III compensation network must be used (see Section 6.4 Compensation network for details on the compensation network design).

In case of light load (i.e. if the output current is lower than the half of the inductor current ripple) the A7987 enters pulse-skipping working mode. The HS MOS is kept off if the COMP level is below 200 mV (typ.); when this bottom level is reached the integrated switch is turned on until the inductor current reaches I_{SKIP} value. So, in discontinuous conduction working mode (DCM), the HS MOS on-time is only related to the time necessary to charge the inductor up to I_{SKIP} level. Due to current sensing comparator delay, the actual inductor charge current could be slightly impacted by V_{IN} and inductance level.

In order to let the bootstrap capacitor recharge, in case of extremely light load, the A7987 is able to pull down the LX net through an integrated small LS MOS. In this way the bootstrap recharge current can flow from V_{IN} through C_{BOOT}, LX and the LS MOS.

This mechanism is activated if the HS MOS has been kept turned off for more than 3 ms (typ.).

5.4 Low VIN operation

In normal operation (i.e. VOUT programmed lower than input voltage), when the HS MOS is turned off, a minimum off-time (T_{OFFMIN}) interval is performed. In case the input voltage falls close or below the programmed output voltage (low-dropout, LDO), the A7987 control loop is able to increase the duty cycle up to 100%. However, in order to keep the boot capacitor properly recharged, a maximum HS MOS on-time is limited (T_{ONMAX}). When this limit is reached the HS MOS is turned off and a pull-down resistor between LX and GND is turned on until one of the following conditions is met:

- A negative current limit (300 mA typ.) is reached
- A time-out (1 µs typ.) is reached

So the A7987 is able to work in low-dropout operation and recover the programmed output voltage as soon as the proper input voltage level is restored.

5.5 Overcurrent protection

The A7987 implements an overcurrent protection by sensing the current flowing through the power MOSFET. Due to the noise created by the switching activity of the power MOSFET, the current sensing circuitry is disabled during the initial phase of the conduction time. This avoids an erroneous detection of a fault condition. This interval is generally known as “masking time” or “blanking time”. The masking time is 120 ns (typ.).

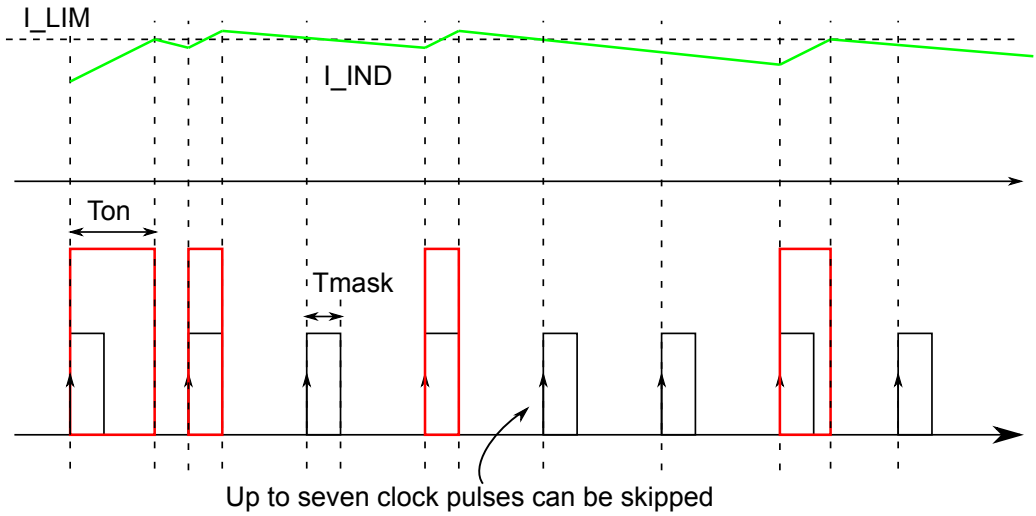
If the overcurrent limit is reached, the power MOSFET is turned off implementing pulse-by-pulse overcurrent protection. In the overcurrent condition, the device can skip turn-on pulses in order to keep the inductor current constant and equal to the current limit, assuming only a slight drift due to input and output voltage variation.

If, at the end of the “masking time”, the current is higher than the overcurrent threshold, the power MOSFET is turned off and one pulse is skipped. If, at the following switching on, when the “masking time” ends, the current is still higher than the overcurrent threshold, the device skips two pulses. This mechanism is repeated and the device can skip up to seven pulses (refer to Figure 8. OCP and frequency scaling).

If at the end of the “masking time” the current is lower than the overcurrent threshold, the number of skipped cycles is decreased by one unit.

As a consequence, the overcurrent/short-circuit protection acts by switching off the power MOSFET and reducing the switching frequency down to one-eighth of the default switching frequency, in order to keep constant the output current close to the current limit.

Figure 8. OCP and frequency scaling



If the sensed output voltage, monitored through FB pin, falls below the VFOLD threshold (400 mV typ.) the peak current limit threshold is reduced to 1/3 of the nominal value. This additional feature helps to reduce the IC stress in case of output short-circuit.

As soon as the FB pin increases above the V_{FOLD} threshold, the full peak current limit threshold is restored. This fold-back protection is disabled during the soft-start.

This kind of overcurrent protection is effective if the inductor can be completely discharged during HS MOS turn-off time, so the inductor current does not run away. In case of output short-circuit, the maximum switching frequency can be computed by the following equation:

$$F_{SW,MAX} \leq \frac{8 \cdot (V_F + R_{DCR} \cdot I_{LIM})}{V_{IN} - (R_{ON} + R_{DCR}) \cdot I_{LIM}} \cdot \frac{1}{T_{ON,MIN}} \quad (4)$$

Assuming V_F=0.6 V the free-wheeling diode direct voltage, R_{DCR}=30 mΩ the inductor parasitic resistance, I_{LIM}=I_{PK}=1.3 A the peak current limit during fold-back protection, R_{ON}=0.24 Ω the HS MOS resistance and $T_{ON,MIN}$=160 ns the minimum HS MOS on duration, the maximum F_{SW} frequency which prevents the inductor current from running away in case of output short-circuit and VIN=61 V is about 530 kHz.

If the programmed switching frequency is higher than the above computed limit, an estimation of the inductor current in case of output short-circuit fault is provided by the following equation:

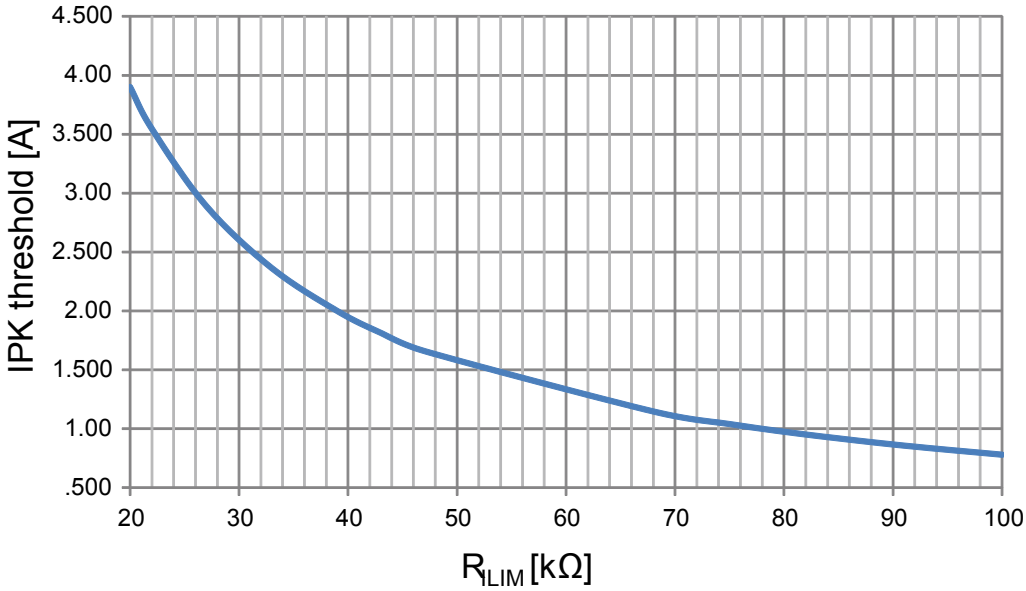
$$I_{LIM} \leq \frac{F_{SW} \cdot T_{ON} \cdot V_{IN} - 8 \cdot V_F}{8 \cdot R_{DCR} + F_{SW} \cdot T_{ON,MIN}(R_{ON} + R_{DCR})} \quad (5)$$

The peak current limit threshold (I_{LIM}) can be programmed in the range of 0.85 A-4 A by selecting the proper R_{ILIM} resistor, as suggested below:

$$R_{ILIM} = 20k\Omega \cdot \frac{I_{PK}}{I_{LIM}} \quad (6)$$

I_{PK} is the default A7987 current limit in case of R_{ILIM} is not mounted, as shown in Table 5. Electrical characteristics

Figure 9. Current limit and programming resistor



The minimum programmed current limit cannot be lower than I_{SKIP}=0.5 A (typical), also in case of fold-back detection.

5.6 Overtemperature protection

It is recommended that the device should never exceed the maximum allowable junction temperature. This temperature increase is mainly caused by the total power dissipated from the integrated power MOSFET.

To avoid any damage to the device when a high temperature is reached, the A7987 implements a thermal shutdown feature: when the junction temperature reaches 170 °C (typ.) the device turns off the power MOSFET and shuts down. When the junction temperature drops to 155 °C (typ.), the device restarts with a new soft-start sequence.

6 Application information

6.1 Input capacitor selection

The input capacitor must be rated for the maximum input operating voltage and the maximum RMS input current.

Since the step-down converter input current is a sequence of pulses from 0 A to I_{OUT}, the input capacitor must absorb the equivalent RMS current, which can be up to the load current divided by two (worst case, with duty cycle of 50%). For this reason, the quality of these capacitors must be very high to minimize the power dissipation generated by the internal ESR, thereby improving system reliability and efficiency.

The RMS input current (flowing through the input capacitor) is roughly estimated by:

$$I_{CIN,RMS} \cong I_{OUT} \cdot \sqrt{D \cdot (1 - D)} \quad (7)$$

Actual DC/DC conversion duty cycle, $D=V_{OUT}/V_{IN}$, is influenced by a few parameters:

$$D_{MAX} = \frac{V_{OUT} + V_F}{V_{IN,MIN} - V_{SW,MAX}}$$
$$D_{MIN} = \frac{V_{OUT} + V_F}{V_{IN,MAX} - V_{SW,MIN}} \quad (8)$$

where V_F is the freewheeling diode forward voltage and V_{SW} the voltage drop across the internal high-side MOSFET. Considering the range D_{MIN} to D_{MAX} it is possible to determine the maximum $I_{CIN,RMS}$ flowing through the input capacitor.

The input capacitor value must be dimensioned to safely handle the input RMS current and to limit the VIN and VCC ramp-up slew-rate to 0.5 V/µs maximum, in order to avoid the device active ESD protection turn-on.

The amount of the input voltage ripple can be roughly overestimated by:

$$V_{IN,PP} = \frac{D \cdot (1 - D) \cdot I_{OUT}}{C_{IN} \cdot F_{SW}} + R_{ES,IN} \cdot I_{OUT} \quad (9)$$

In case of MLCC ceramic input capacitors, the equivalent series resistance ($R_{ES,IN}$) is negligible.

In addition to the input RMS current handling consideration, a ceramic capacitor with appropriate voltage rating and with a value of 1 µF or higher should always be placed between VIN and ground and between VCC and the IC GND pin.

This solution is necessary for noise filtering purposes.

6.2 Output capacitor selection

The output capacitor is very important in order to satisfy the output voltage ripple requirements. Using a small inductor value is useful to reduce the size of the choke but increases the current ripple. So, to reduce the output voltage ripple, a low ESR capacitor is required. Nevertheless, the ESR of the output capacitor introduces a zero in the open loop gain, which helps to increase the phase margin of the system. If the zero goes to very high frequency, a typical drawback in case of ceramic output capacitor application, a type III compensation network must be designed.

The current, in the output capacitor, has a triangular waveform which generates a voltage ripple across it. This ripple is due to the capacitive component (charge and discharge of the output capacitor) and the resistive component (due to the voltage drop across its ESR). So the output capacitor must be selected in order to have a voltage ripple compliant with the application requirements.

The amount of the voltage ripple can be estimated starting from the current ripple obtained by the inductor selection. Assuming ΔI_L the inductor current ripple, the output voltage ripple is roughly overestimated by the equation below:

$$\Delta V_{OUT,PP} \cong \Delta I_L \cdot R_{ES,OUT} + \frac{\Delta I_L}{8 \cdot F_{SW} \cdot C_{OUT}} \quad (10)$$

Usually the resistive component of the ripple is much higher than the capacitive one, if the output capacitor adopted is not a multi-layer ceramic capacitor (MLCC) with a very low ESR value. The output capacitor is also important for loop stability: it fixes the double LC filter pole and the zero due to its ESR.

The output capacitor is the key component that provides the current to the load during a load transient which exceeds the system bandwidth. So, if the high slew rate load transient is required by the application, the output capacitor must be designed in order to sustain the load transient or absorbs the energy stored in the inductor until the converter reacts. In fact, even if the controller detects immediately the load variation and sets the duty cycle at 100% or 0%, the output current slope is limited by the inductor value, the input and output voltage. The output voltage has a drop or overshoot that depends on the ESR and capacitive charge/discharge, as roughly estimated in Eq. (11)

$$\Delta V_{OUT_LT} \cong \Delta I_{OUT} \cdot R_{ES,OUT} + \Delta I_{OUT} \cdot \frac{L \cdot \Delta I_{OUT}}{2 \cdot C_{OUT} \cdot \Delta V_L} \tag{11}$$

where ΔV_L is the voltage applied to the inductor during the load appliance or load release.

$$\Delta V_L = \begin{Bmatrix} (V_{IN} - V_{OUT}) \\ V_{OUT} \end{Bmatrix} \tag{12}$$

MLCC capacitors have a typically low ESR to minimize the ripple but also have a low capacitance that does not minimize the voltage deviation during dynamic load variations.

Electrolytic capacitors, on the other hand, have a large capacitance which minimizes voltage deviation during load transients whereas they do not show the same ESR values as the MLCCs, resulting then in higher ripple voltages.

A mix between an electrolytic and MLCC capacitor can be used to minimize ripple as well as reducing voltage deviation in dynamic mode.

The high bandwidth error amplifier of the A7987 and the external compensation feature let design a wide range of output filter configurations (including all MLCC solutions) and perform a fast transient response.

6.3 Inductor selection

The inductance value fixes the current ripple flowing through the output capacitor. So the minimum inductance value, in order to have the expected current ripple, must be selected.

The rule to fix the current ripple value is to have a ripple at 20%-40% of the output current.

In the continuous conduction mode (CCM), the required inductance value can be calculated by the following equation:

$$L = \frac{V_{OUT} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}{\Delta I_L \cdot F_{SW}} \tag{13}$$

In order to guarantee a maximum current ripple in every condition, Eq. (13) must be evaluated in case of maximum input voltage, assuming V_{OUT} fixed.

Increasing the value of the inductance helps reduce the current ripple but, at the same time, strongly impacts the converter response time to a dynamic load change. The response time is the time required by the inductor to change its current from the initial to the final value. Until the inductor has finished its charging (or discharging) time, the output current is supplied (or recovered) by the output capacitors.

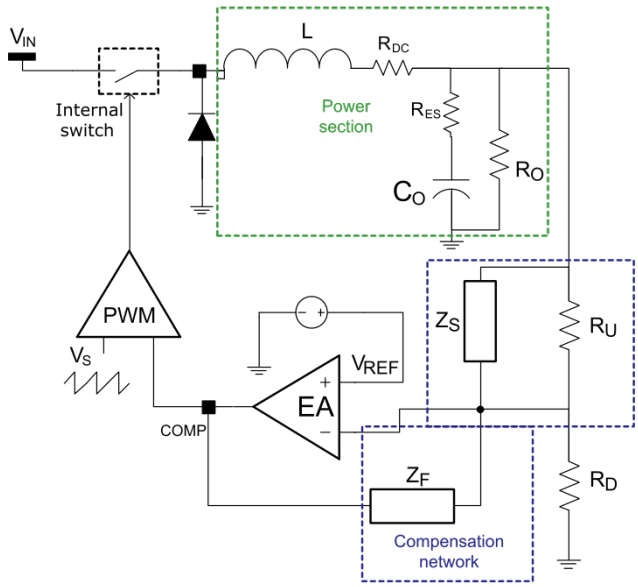
Further, if the compensation network is properly designed, during a load variation the device is able to properly change the duty cycle so improving the control loop transient response. When this condition is reached the response time is only limited by the time required to change the inductor current, basically by V_{IN}, V_{OUT} and L.

Minimizing the response time, at the end, can help to decrease the output filter total cost and to reduce the application area.

6.4 Compensation network

The compensation network must assure stability and good dynamic performance. The loop of the A7987 is based on the voltage mode control. The error amplifier is an operational amplifier with a high bandwidth. So, by selecting the compensation network the E/A is considered as ideal, that is, its bandwidth is much larger than the system one.

Figure 10. Switching regulator control loop simplified model



The transfer function of the PWM modulator, from the error amplifier output (COMP pin) to the LX pin results in an almost constant gain, due to the voltage feed-forward which generates a sawtooth with amplitude V_S directly proportional to the input voltage.

$$G_{PWO} = \frac{V_{IN}}{V_S} = \frac{1}{k_{FF}} = 30 \tag{14}$$

The synchronization of the device with an external clock provided through the SYNCH pin can modify the PWM modulator gain (see Section 5.1 Oscillator and synchronization to understand how this gain changes and how to keep it constant in spite of the external synchronization).

The transfer function of the power section (i.e. the L-C filters and the output load) is:

$$G_{LC}(s) = \frac{R_0//\left(R_{ES} + \frac{1}{sC_0}\right)}{R_0//\left(R_{ES} + \frac{1}{sC_0}\right) + sL + R_{DC}} \tag{15}$$

$$= \frac{R_0 \cdot (1 + sC_0R_{ES})}{s^2LC_0 \cdot (R_0 + R_{ES}) + s(L + C_0R_0R_{DC} + C_0R_{ES}R_{DC} + C_0R_{ES}R_0) + R_{DC} + R_0}$$

given L, R_{DC}, C_0, R_{ES} and R_0

the parameters shown in Figure 10. Switching regulator control loop simplified model. The power section transfer function can be rewritten as follows:

$$G_{LC}(s) = G_{LC0} \cdot \frac{1 + \frac{s}{2\pi \cdot f_{zESR}}}{1 + \frac{s}{2\pi \cdot Q \cdot f_{LC}} + \left(\frac{s}{2\pi \cdot f_{LC}}\right)^2}; G_{LC0} = \frac{R_0}{R_0 + R_{DC}} \cong 1 \tag{16}$$

$$f_{zESR} = \frac{1}{2\pi \cdot C_0R_{ES}}; f_{LC} = \frac{1}{2\pi\sqrt{LC_0}\sqrt{\frac{R_0 + R_{ES}}{R_0 + R_{DC}}}} \cong \frac{1}{2\pi\sqrt{LC_0}\sqrt{\frac{R_0 + R_{ES}}{R_0}}} \tag{17}$$

$$Q = \frac{\sqrt{LC_0} \cdot \sqrt{R_0 + R_{DC}} \cdot \sqrt{R_0 + R_{ES}}}{L + C_0 \cdot (R_0R_{DC} + R_0R_{ES} + R_{ES}R_{DC})} \cong \frac{\sqrt{LC_0} \cdot \sqrt{R_0 \cdot (R_0 + R_{ES})}}{L + C_0R_0R_{ES}} \tag{18}$$

with the assumption that the inductor parasitic resistance, R_{DC}, is negligible compared to R_O. The closed loop gain is then given by:

$$G_{LOOP}(s) = G_{LC}(s) \cdot G_{PWO}(s) \cdot G_{COMP}(s) \tag{19}$$

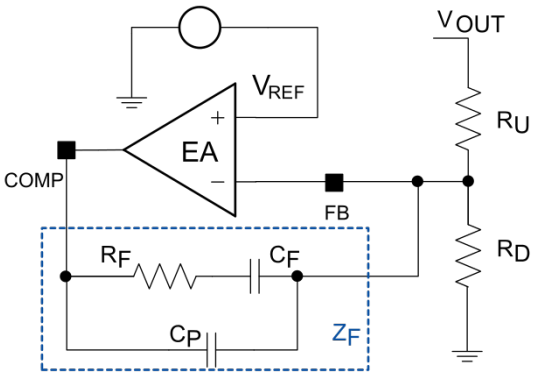
As noted in Section 6.2 Output capacitor selection, two different kinds of network can compensate the loop, depending on the value of f_{zESR}, lower or higher than the regulator required bandwidth.

In the following two paragraphs the guidelines to select the type II and type III compensation network are illustrated.

6.4.1 Type II compensation network

If the equivalent series resistance (R_{ES}) of the output capacitor introduces a zero with a frequency lower than the desired bandwidth (that is: $2\pi * R_{ES} * C_O > 1/BW$), this zero helps stabilize the loop. Electrolytic capacitors show non-negligible ESR (>30 mΩ typically), so with this kind of output capacitor the type II network combined with the zero of the ESR allows the loop to be stabilized.

Figure 11. Type II compensation network



The type II compensation network transfer function, from VOUT to COMP, is computed in the equation below:

$$G_{COMPII}(s) = -\frac{Z_F(s)}{R_U} = -\frac{1}{R_U} \cdot \frac{1 + sC_F R_F}{s \cdot (C_F + C_P) \cdot (1 + sC_F // C_P R_F}$$ (20)

$$= -1 \cdot \frac{1 + \frac{s}{2\pi \cdot f_{Z1}}}{\frac{s}{2\pi \cdot f_{P0}} \cdot \left(1 + \frac{s}{2\pi \cdot f_{P1}}\right)}$$

$$f_{Z1} = \frac{1}{2\pi \cdot C_F R_F}; f_{P0} = \frac{1}{2\pi \cdot (C_F + C_P) \cdot R_U}; f_{P1} = \frac{1}{2\pi \cdot C_F // C_P R_F}$$ (21)

The following suggestions can be followed for a quite common compensation strategy, assuming that $C_P << C_F$.

- Starting from Eq. (19) in case of a type II compensation network and electrolytic output capacitors, the control loop gain module at $s=2\pi * F_{BW}$ allows R_F/R_U ratio to be fixed:

$$\left|G_{LOOP,II}(s = 2\pi \cdot f_{BW})\right| \cong \frac{1}{k_{FF}} \cdot \frac{{f_{LC}}^2}{f_{zESR}} \cdot \frac{R_F}{R_U} \cdot \frac{1}{f_{BW}} = 1$$ (22)

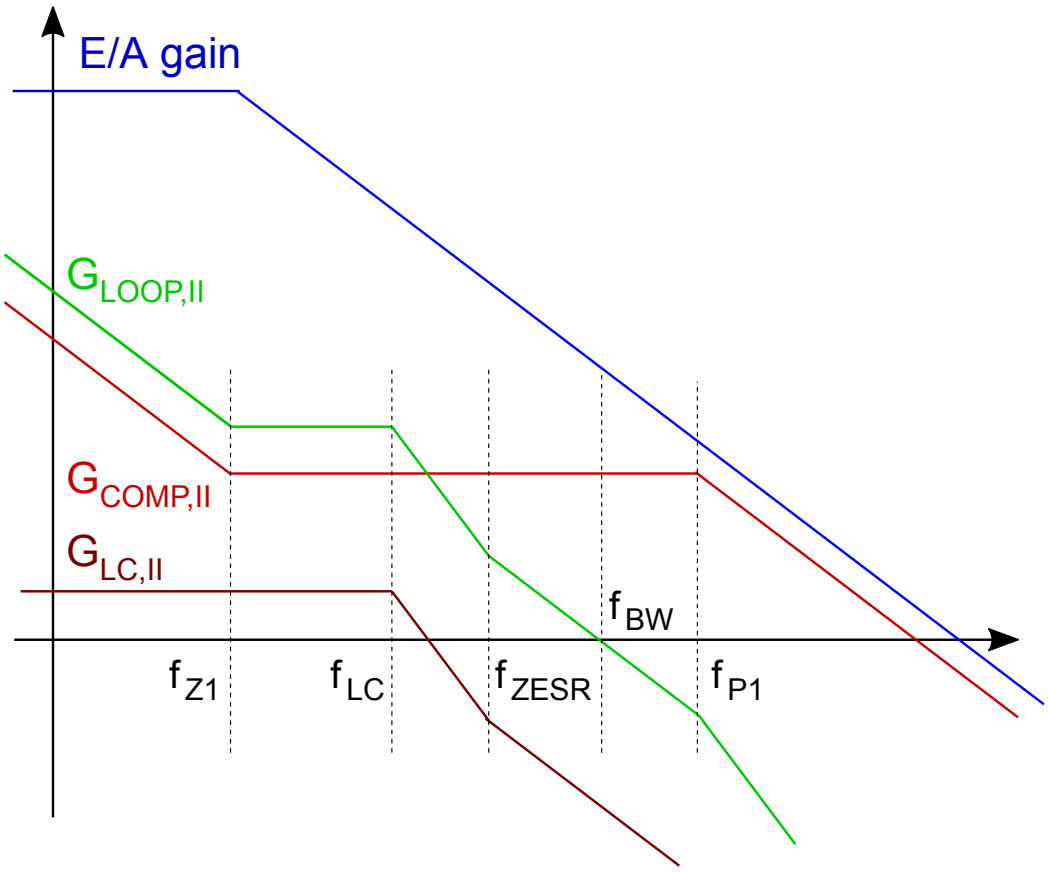
After choosing the regulator bandwidth (typically $F_{BW} < 0.2 * F_{SW}$) and a value for R_U, usually between 1 kΩ and 50 kΩ, in order to achieve C_F and C_P not comparable with a parasitic capacitance of the board, the R_F required value is computed by Eq. (22).

- Select C_F in order to place F_{Z1} below F_{LC} (typically $0.1 * F_{LC}$)
- Select C_P in order to place F_{P1} at $0.5 * F_{SW}$

$$C_F = \frac{1}{2\pi \cdot R_F \cdot 0.1 \cdot f_{LC}}; C_P = \frac{1}{2\pi \cdot R_F \cdot 0.5 \cdot f_{SW}}$$ (23)

The resultant control loop and other transfer functions gain are shown in Figure 12. Type II compensation - Bode plot

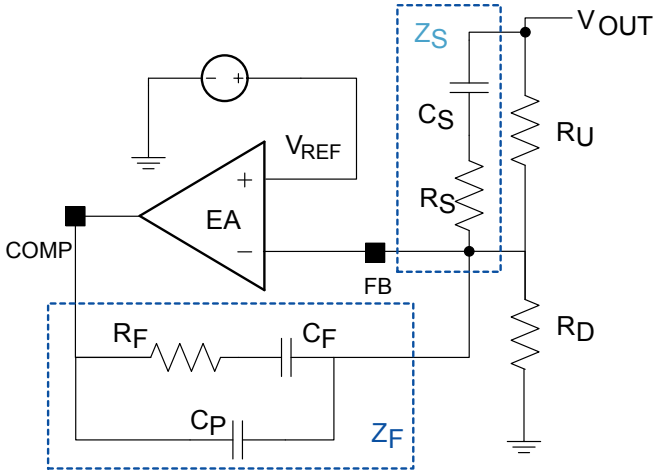
Figure 12. Type II compensation - Bode plot



6.4.2 Type III compensation network

If F_{zESR} is higher than the target loop bandwidth, as usually happens if the output filter is based on MLCC ceramic capacitors, a type III compensation network must be designed.

Figure 13. Type III compensation network



The type III compensation network transfer function, from VOUT to COMP, is computed in the equation below:

$$G_{COMPIII}(s) = -\frac{Z_F(s)}{R_U//Z_S(s)} = -1 \cdot \frac{\left(1+\frac{s}{2\pi \cdot f_{Z1}}\right)\cdot\left(1+\frac{s}{2\pi \cdot f_{Z2}}\right)}{\frac{s}{2\pi \cdot f_{P0}}\cdot\left(1+\frac{s}{2\pi \cdot f_{P1}}\right)\cdot\left(1+\frac{s}{2\pi \cdot f_{P2}}\right)} \quad (24)$$

In addition to what shown in Eq. (21), two more singularities are proper of this compensation network:

$$f_{Z2} = \frac{1}{2\pi \cdot C_S(R_U + R_S)}; f_{P2} = \frac{1}{2\pi \cdot C_S R_S} \quad (25)$$

The following suggestions can be followed for a quite common compensation strategy, assuming that C_P<<C_F and R_S<<R_U

- Starting from Eq. (19), in case of type III compensation network and MLCC ceramic output capacitors, the control loop gain module at s=2π*F_{BW} allows the R_F/R_U ratio to be fixed:

$$\left|G_{LOOP,III}(s = 2\pi \cdot f_{BW})\right| \cong \frac{1}{k_{FF}} \cdot \frac{f_{LC}}{f_{BW}} \cdot \frac{R_F}{R_U} = 1 \quad (26)$$

After choosing the regulator bandwidth (typically F_{BW}<0.2*F_{SW}) and a value for R_U, usually between 1 kΩ and 50 kΩ, in order to achieve C_F and C_P not comparable with a parasitic capacitance of the board, the R_F required value is computed by Eq. (26).

- Select C_F in order to place F_{Z1} below F_{LC} (typically 0.1*F_{LC})
- Select C_P in order to place F_{P1} at 0.5*F_{SW}

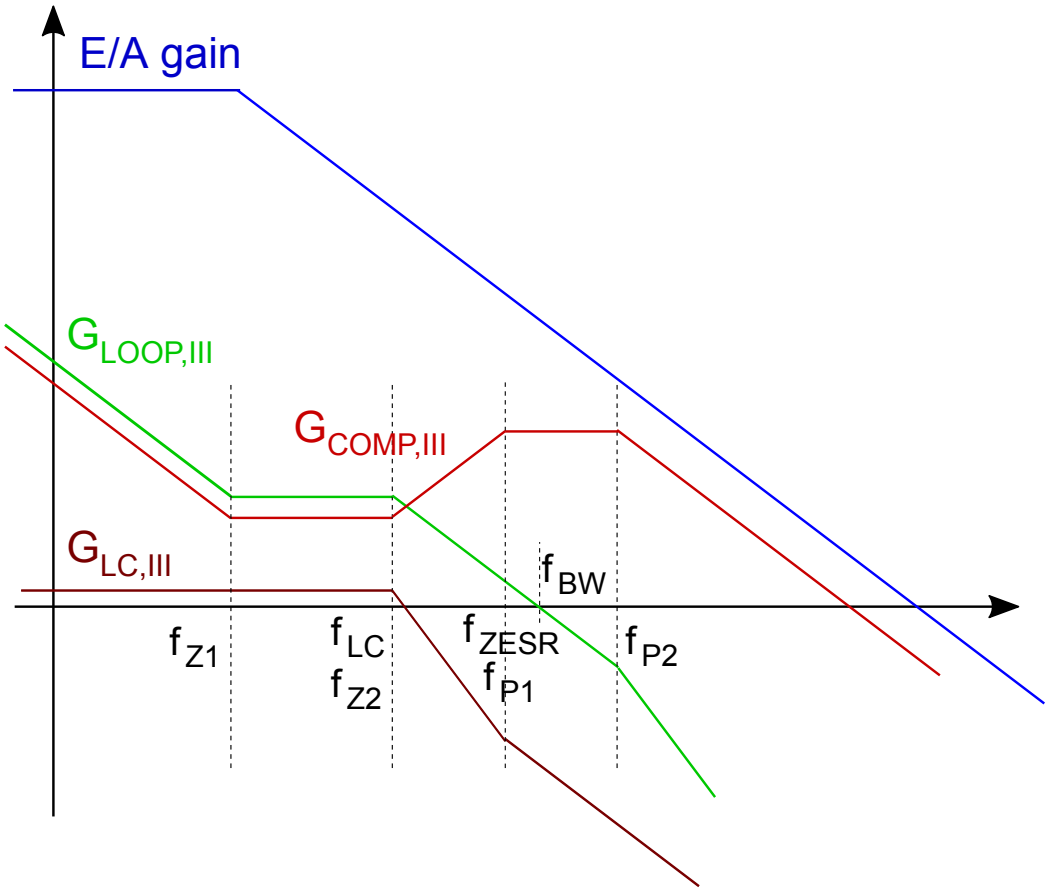
$$C_F = \frac{1}{2\pi \cdot R_F \cdot 0.1 \cdot f_{LC}}; C_P = \frac{1}{2\pi \cdot R_F \cdot 0.5 \cdot f_{SW}} \quad (27)$$

- Select C_S in order to place F_{Z2} at F_{LC}
- Select R_S in order to place F_{P2} at 0.5*F_{SW}

$$C_S = \frac{1}{2\pi \cdot R_U \cdot f_{LC}}; R_S = \frac{1}{2\pi \cdot C_S \cdot 0.5 \cdot f_{SW}} \quad (28)$$

The resultant control loop and other transfer functions gain are shown in Figure 14. Type III compensation - Bode plot

Figure 14. Type III compensation - Bode plot



6.5 Thermal considerations

The thermal design prevents the thermal shutdown of the device if junction temperature goes above 170 °C (typ.). The three different sources of losses within the device are:

- conduction losses due to the non-negligible $R_{DS(on)}$ of the power switch; these are equal to

$$P_{HS,ON} = R_{HS,ON} \cdot D \cdot (I_{OUT})^2 \quad (29)$$

where D is the duty cycle of the application and $R_{HS,ON}$ is the maximum resistance overtemperature of the power switch. Note that the duty cycle is theoretically given by the ratio between VOUT and VIN, but actually it is quite higher in order to compensate the losses of the regulator. So the conduction losses increase compared with the ideal case;

- switching losses due to power MOSFET turn-ON and OFF; these can be calculated as:

$$P_{HS,SW} = V_{IN} \cdot I_{OUT} \cdot \frac{(T_{RISE} + T_{FALL})}{2} \cdot f_{SW} \cong V_{IN} \cdot I_{OUT} \cdot T_{TR} \cdot f_{SW} \quad (30)$$

where T_{RISE} and T_{FALL} are the overlap times of the voltage across the power switch (V_{DS}) and the current flowing into it during turn-ON and turn-OFF phases. T_{TR} is the equivalent switching time. For this device the typical value for the equivalent switching time is 40 ns.

- Quiescent current losses, calculated as follows:

$$P_Q = V_{IN} \cdot I_{QOPVIN} + V_{BIAS} \cdot I_{QOPVBIAS} \quad (31)$$

where I_{QOPVIN} and $I_{QOPVBIAS}$ are the A7987 quiescent current in case of separate bias supply. If the switch-over feature is not used, the IC quiescent current is the only one from VIN, I_{QUIESC}, as summarized in Table 5. Electrical characteristics. The junction temperature T_J can be calculated as the equation below:

$$T_J = T_A + R_{th,JA} \cdot P_{TOT} \quad (32)$$

where T_A is the ambient temperature and P_{TOT} is the sum of the power losses just seen. R_{thJA} is the equivalent thermal resistance junction-to-ambient of the device.

It can be calculated as the parallel of many paths of heat conduction from the junction to the ambient. For this device the path through the exposed pad is the one conducting the largest amount of heat. The R_{thJA}, measured on the demonstration board described in the following paragraph, is about 40 °C/W for the HTTSOP16 package.

6.6 Layout considerations

The PCB layout of the switching DC/DC regulators minimizes the noise injected in high impedance nodes and interference generated by the high switching current loops.

In a step-down converter, the input loop (including the input capacitor, the power MOSFET and the freewheeling diode) is the most critical one. This is due to the fact that high value pulsed currents are flowing through it. In order to minimize the EMI, this loop must be as short as possible.

The feedback pin (FB) connection to the external resistor divider is a high impedance node, so the interference can be minimized by placing the routing of the feedback node as far as possible from the high current paths. To reduce the pick-up noise, the resistor divider must be placed very close to the device.

To filter the high frequency noise, a small bypass capacitor (1 µF or higher) must be added as close as possible to the input voltage pin of the device.

Thanks to the exposed pad of the device, the ground plane helps to reduce the junction to ambient thermal resistance; so a wide ground plane enhances the thermal performance of the converter, allowing the high power conversion.

7 Demonstration board

In this section the A7987 demonstration board is described.
The default settings are:

- Programmed V_{OUT} = 3.3V
- Max. I_{OUT} = 3 A
- F_{SW} = 500 kHz
- Soft-start 3.5 ms
- V_{BIAS} = V_{OUT}

Figure 15. A7987 demonstration board schematic

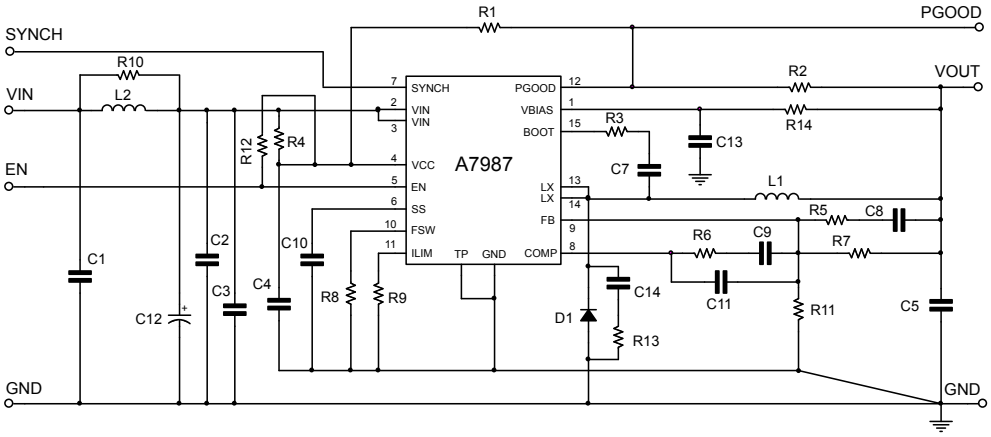


Table 7. A7987 demonstration board component list

Reference	Part	Package	Note	Manufacturer P/N
C1	N.M.			
C2	4.7 uF	1210	X7S/100 V/20%	MURATA GCM32DC72A475M Alt: GRM31CC72A475M
C3, C4	1 uF	0805	X7S/100 V/10%	MURATA GCM21BC72A105K Alt. GRM21BC72A105K
C5	47 uF	1210	X7R/6.3 V/10%	MURATA GCM32ER70J476K Alt. GRM32ER7A476K
C7, C13	100 nF	0603	10 V	
C8	4.7 nF	0603	X7R/16 V/10%	
C9	47 nF	0603	X7R/16 V/10%	
C10	22 nF	0603	X7R/16 V/10%	
C11	680 pF	0603	NPO/50 V/5%	
C12	33 uF	8mm, radial	63 V/Elect./1.7 Arms	PANASONIC EEHZA1J330P
C6, C14	N.M.			
R2, R12	100 k	0603	1% tolerance	
R3,R4, R14	0	0603		
R5	120	0603	1% tolerance	

Reference	Part	Package	Note	Manufacturer P/N
R6	1 k	0603	1% tolerance	
R7	7.5 k	0603	1% tolerance	
R8	47 k	0603	1% tolerance	
R10	0	0805		
R11	2.4 k	0603	1% tolerance	
R1, R9, R13	N.M.			
L1	10 uH	5x5 mm	4.9 A sat/ 41 mΩ	COILCRAFT XAL5050-103
L2	N.M.			
D1	STPS3L60	SMB	60 V-3 A Schottky rectifier	ST STPS3L60U-Y
U1	A7987	HTSSOP16		ST A7987

Figure 16. Demonstration board layout (top)

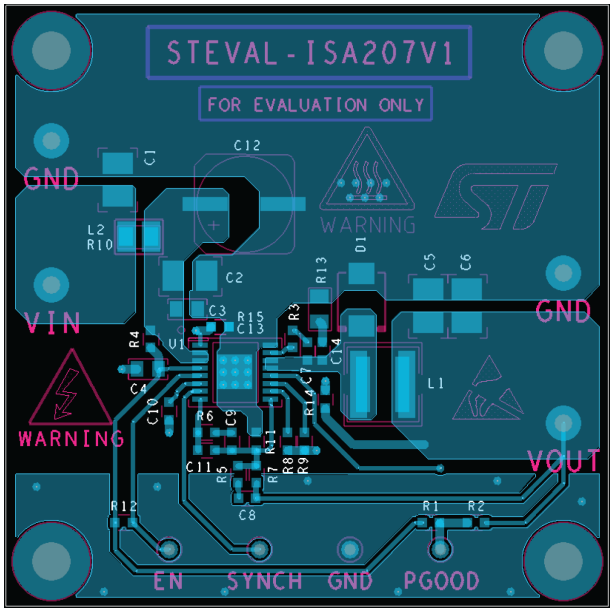


Figure 17. Demonstration board layout (bottom)

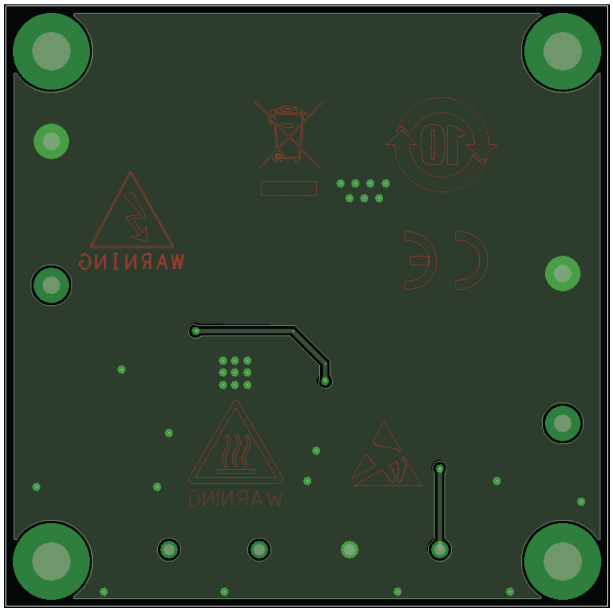


Figure 18. Efficiency vs output current V_{OUT} = 3.3 V, F_{SW} = 500 kHz

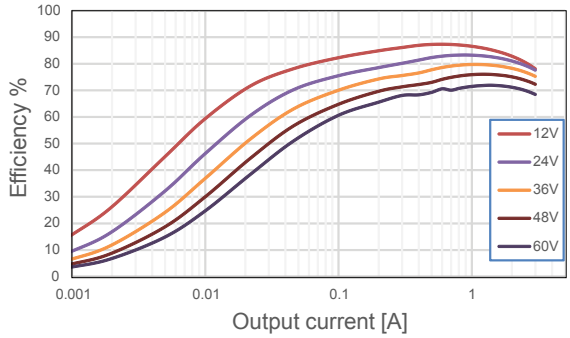


Figure 19. Junction temperature increase vs output current T_{AMB} = 25 °C

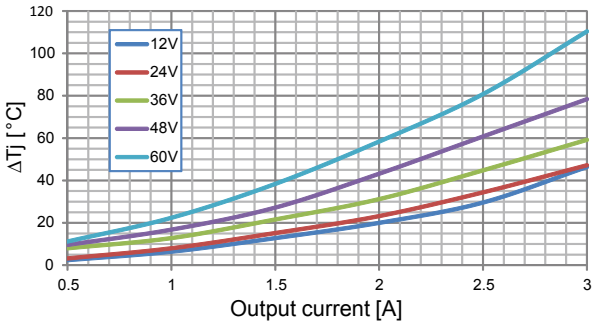


Figure 20. Input quiescent current vs input voltage. No load

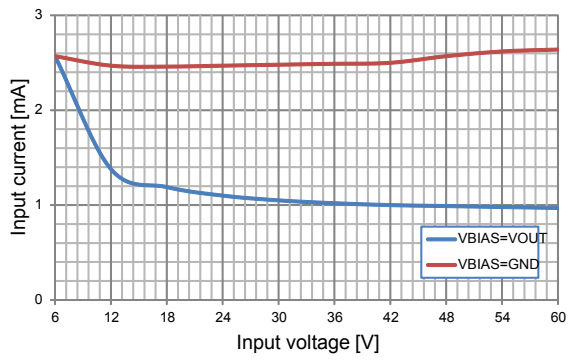


Figure 21. Input shutdown current vs input voltage

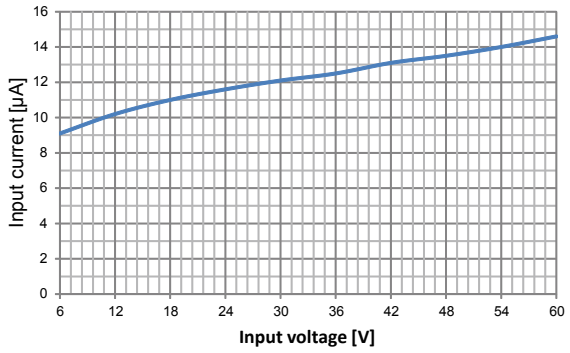


Figure 22. Load regulation. V_{OUT} = 3.3 V, F_{SW}=500 kHz

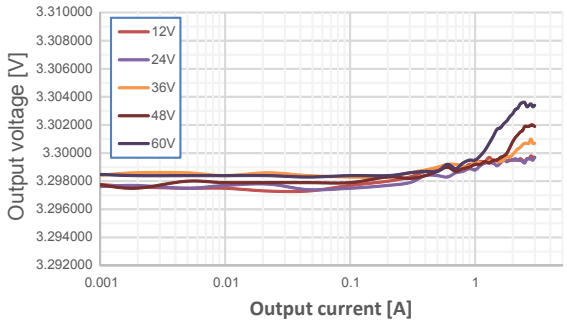
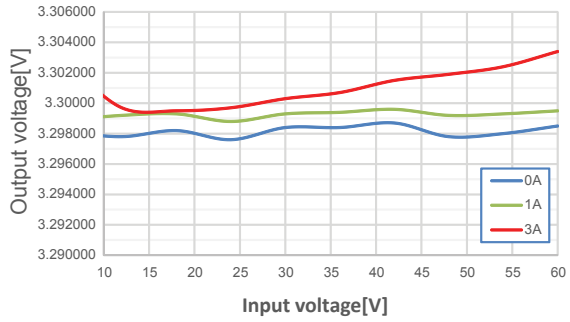


Figure 23. Line regulation. V_{OUT} = 3.3 V, F_{SW} = 500 kHz



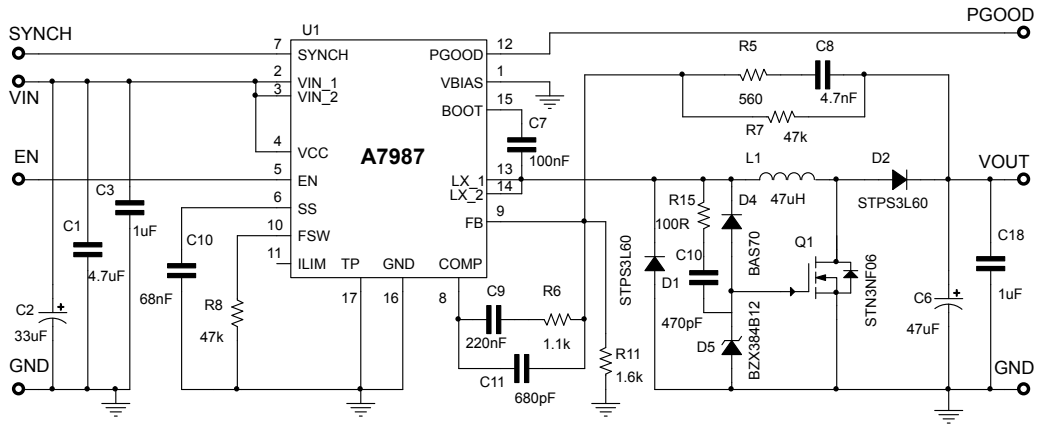
8 Application ideas

8.1 Positive buck-boost

The A7987 device can implement the step-up/down conversion with a positive output voltage.

The figure below shows the complete schematic: one power MOSFET and one Schottky diode are added to the standard buck topology to provide 24 V output voltage, with an input voltage from 18 V to 60 V. In this design example, the programmed switching frequency is 510 kHz and the maximum expected load is 0.8 A.

Figure 24. Positive buck-boost schematic example



In this topology the relationship between input and output voltage is:

$$V_{OUT} = V_{IN} \cdot \frac{D}{1-D} \tag{33}$$

so the duty cycle is given by:

$$D = \frac{V_{OUT}}{V_{OUT} + V_{IN}} \tag{34}$$

The output voltage is not limited by the maximum operating voltage of the device, because the output voltage is sensed only through the resistor divider. The external power MOSFET maximum drain to source voltage must be higher than the output voltage and also the additional diode, D2, must be rated for the same maximum voltage.

In Figure 24. Positive buck-boost schematic example a clamping network has been added to limit Q1 gate to source voltage (C10, R15 and D5) and to speed up Q1 turn-off time (D4).

The current flowing through the internal power MOSFET is transferred to the load only during the OFF-time, so according to the maximum allowed A7987 DC switch current (3.0 A), the maximum output current for the buck-boost topology can be calculated by the equation below.

$$I_{SW} = \frac{I_{OUT}}{1-D} < 3A \tag{35}$$

where I_{SW} is the average current in the embedded power MOSFET during the ON-time.

In addition to these constraints, the thermal considerations summarized in Section 6.5 Thermal considerations must also be evaluated.

Figure 25. Buck-boost PCB layout (top)

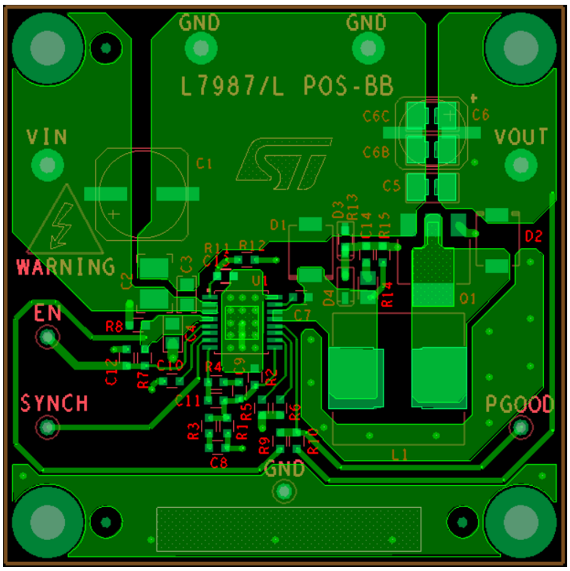
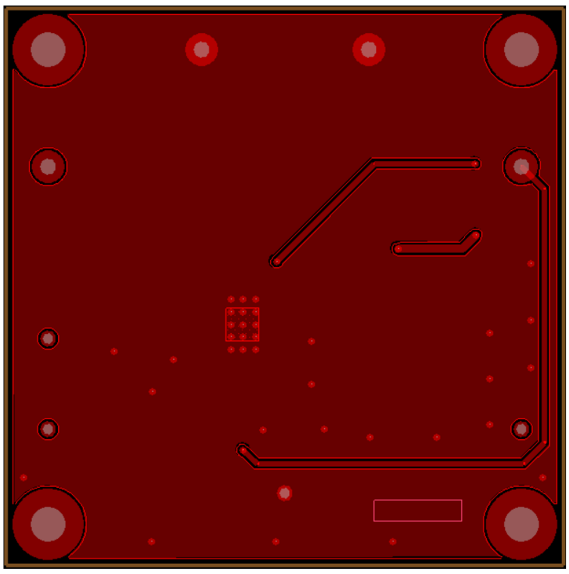


Figure 26. Buck-boost PCB layout (bottom)



The transfer function of the power section for buck-boost topology is summarized below:

$$G_{LC}(s) = G_0 \cdot \frac{\left(1 + \frac{S}{\omega_Z}\right) \cdot \left(1 - \frac{S}{\omega_{RHPZ}}\right)}{1 + \frac{S}{\omega_{LC} \cdot Q} + \frac{S^2}{\omega_{LC}{}^2}} \tag{36}$$

with below singularities and parameters:

$$\omega_Z = \frac{1}{C_0 \cdot R_{ES}}; \omega_{RHPZ} = \frac{R_0 \cdot (1-D)^2}{D \cdot L}; \omega_{LC} = \frac{1-D}{\sqrt{L \cdot C_0}} \tag{37}$$

$$D = \frac{V_0}{V_0 + V_{IN}}; Q = (1-D) \cdot R_0 \cdot \sqrt{\frac{C_0}{L}}; G_0 = \frac{V_0}{D \cdot (1-D)} \tag{38}$$

The singularity $\omega_{RHPZ} = 2\pi * f_{RHPZ}$, computed at the maximum load and minimum input voltage, is the limitation in the loop bandwidth design. Typically the maximum bandwidth, f_{BW}, is designed to be lower than one fourth of the above described singularity, in order to achieve a good phase margin.

In case ω_Z and ω_{LC} are lower than the target bandwidth, a type II compensation network is enough for loop stabilization, following the compensation strategy described in Section 6.4.1 Type II compensation network . In case ceramic or very low ESR electrolytic output capacitors are used, ω_Z is typically higher than the target f_{BW} so a type III compensation network is necessary, as described in Section 6.4.2 Type III compensation network.

8.2 Negative buck-boost

The A7987 device can implement the step-up/down conversion with a negative output voltage.

Figure 27. Negative buck-boost schematic example shows the schematic to regulate -24 V and about 0.6 A maximum load, assuming VIN falling in the range from 18 V to 36 V. No further external components are added to the standard buck topology.

Figure 27. Negative buck-boost schematic example

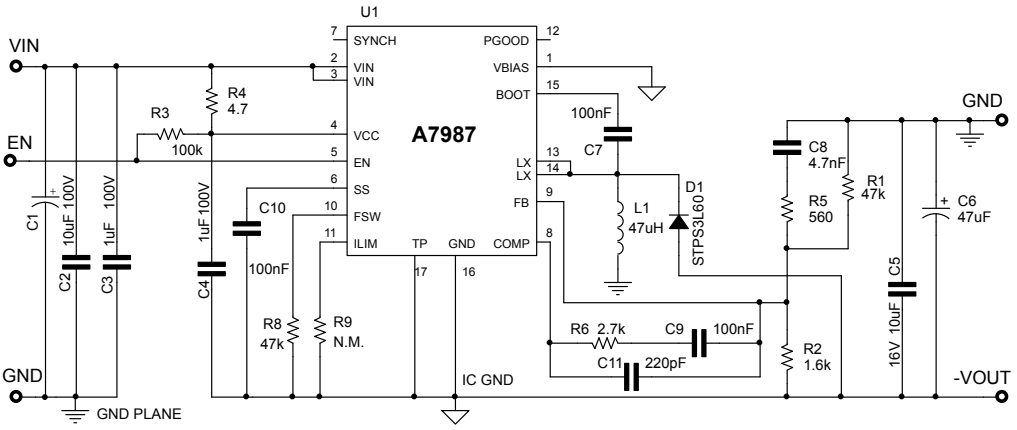


Figure 28. Negative buck-boost PCB layout (top)

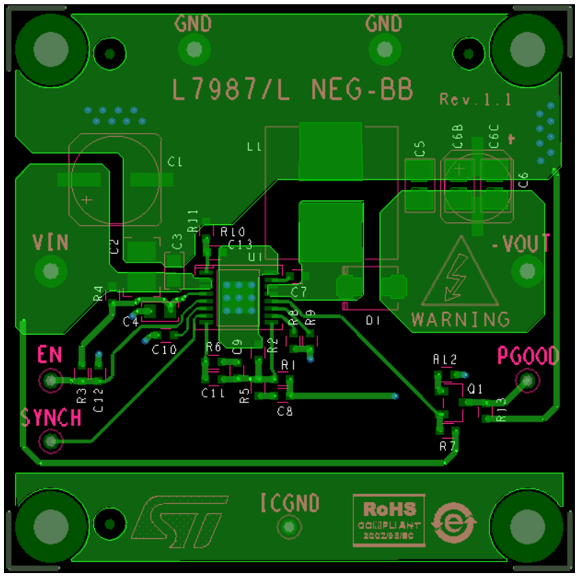
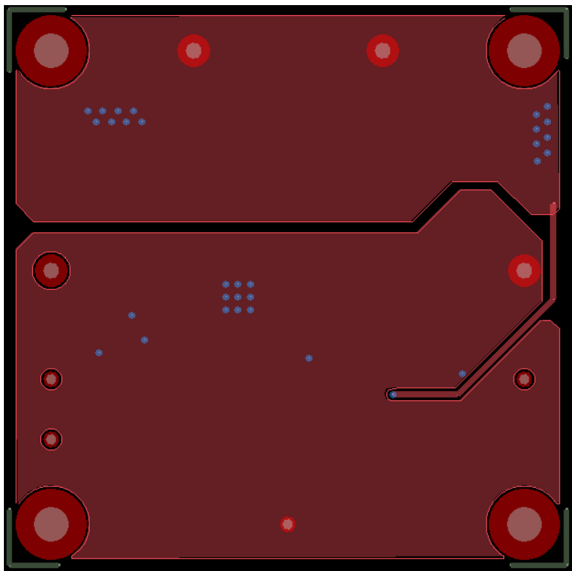


Figure 29. Negative buck-boost PCB layout (bottom)



Eq. (33) and Eq. (34) for positive buck-boost can be used to program the output voltage and estimate the working duty cycle, assuming for VOUT a positive voltage. The other considerations summarized in the previous section are also applied to the inverting buck-boost.

In this topology the device GND is shorted to VOUT, so the resulting voltage stress on the integrated power MOS is the sum of VIN and VOUT. Consequently, the maximum input voltage must be lower than:

$$V_{IN} \leq V_{IN,MAX} - |V_{OUT}| \quad (39)$$

$V_{IN,MAX}$ = 61 V is the maximum operating input voltage for the A7987, as shown in Table 5. Electrical characteristics.

Therefore, if the output voltage is -24 V, the maximum operating input voltage is close to 36 V, if also the freewheeling diode has the same reverse voltage ratings.

For control loop stability analysis and compensation, the transfer function model and considerations summarized in the previous section are also applied to this topology.

9 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

9.1 HTSSOP16 package information

Figure 30. HTSSOP16 package outline

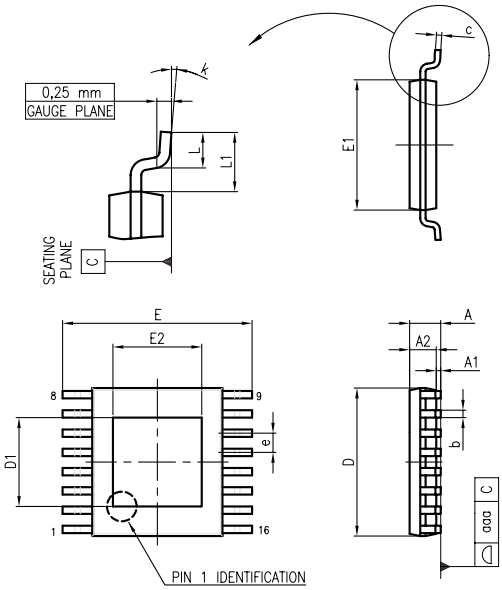


Table 8. HTSSOP16 mechanical data

Symbol	Milimeters		
	Min.	Typ.	Max.
A			1.20
A1			0.15
A2	0.80	1.00	1.05
b	0.19		0.30
c	0.09		0.20
D	4.90	5.00	5.10
D1	2.80	3.00	3.20
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
E2	2.80	3.00	3.20
e		0.65	
L	0.45	0.60	0.75
L1		1.00	
k	0.00		8.00
aaa			0.10

10 Ordering information

Table 9. Ordering information

Order code	Package	Packing
A7987	HTSSOP16	Tube
A7987TR		Tape and reel

Revision history

Table 10. Document revision history

Date	Version	Changes
19-Mar-2019	1	Initial release.
16-Jul-2019	2	Updated the title. Minor text changes throughout the document.

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