APPLICATION NOTE 5587

Selecting External Components and Compensation for Automotive Step-Up DC-DC Regulator with Preboost Reference Design

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Abstract: In this application note, the parameters and calculations needed in the selection of external components for optimal performance of the MAX16990/MAX16992 in boost configurations are reviewed. Next, the selection of compensation components is discussed and a general method that can be extrapolated to compensate any boost regulator is offered. A calculator is provided to help the user in the selection of external components, compensation design, and the evaluation of power-supply performance. A reference design, showing how the devices can be used in an automotive preboost application, is discussed as is the optimal layout for this boost regulator.

Introduction

A high-voltage boost controller, such as the MAX16990 or the MAX16992, the latter of which has 2.2MHz switching frequency capabilities, has many applications in the automotive field. Two uses are as a preboost regulator to sustain system voltage during cold-/warm-crank or as a power supply for high-brightness LEDs.

In this application note, we begin by examining how to realize an automotive high-voltage step-up DC-DC power supply with the MAX16990/MAX16992 and how to select the external components to achieve best system performance. Afterwards, we present a reference design for its preboost application.

Selection of External Components

Parameters for Choosing External Components

There are four principal design input parameters for choosing external components for optimal performance of the MAX16990 and the MAX16992.

1. Switching frequency (f_{SW})
2. Output voltage (V_{OUT})
3. Output current range (I_{OUTMIN} and I_{OUTMAX})
4. Input voltage range (V_{INMIN} and V_{INMAX})

The MAX16990 and the MAX16992 operate in different switching frequency ranges, 100kHz to 1MHz for the

former and 1MHz to 2.5MHz for the latter. Choose the version for the switching frequency you need.

Everything about the output stage (i.e., voltage and current range) is known. However, we only know the voltage range on the input stage. It would be useful to estimate the average input current range. We can do this with the following two equations:

$$I_{IN(AVG,MIN)} = \frac{V_{OUT} \times I_{OUTMIN}}{V_{INMAX} \times Eff} \qquad \text{(Eq. 1)}$$

$$I_{IN(AVG,MAX)} = \frac{V_{OUT} \times I_{OUTMAX}}{V_{INMAX} \times Eff} \qquad \text{(Eq. 2)}$$

Where the parameter Eff is the estimated efficiency of the boost regulator. We can extrapolate an initial estimation for Eff from the Typical Operating Characteristics in the MAX16990/MAX16992 data sheet and refine the estimation with the calculator after dimensioning all the external power components (nMOS, inductor, sense resistor, and rectifier diode).

Next, we need to evaluate the duty cycle range (D_{MIN} and D_{MAX}) where the regulator operates. This can be determined with the following two equations:

$$D_{MIN} = \frac{V_{OUT} + V_D - V_{INMAX}}{V_{OUT} + V_D - [(R_{DS(ON)} + R_{SENSE}) \times I_{IN(AVG,MIN)}]} \qquad \text{(Eq. 3)}$$

$$D_{MAX} = \frac{V_{OUT} + V_D - V_{INMIN}}{V_{OUT} + V_D - [(R_{DS(ON)} + R_{SENSE}) \times I_{IN(AVG,MAX)}]} \qquad \text{(Eq. 4)}$$

Where V_D is the forward voltage of the rectifier diode, $R_{DS(ON)}$ the drain-source resistance of the nMOS when turned on, and R_{SENSE} the sense resistor. Because we have not chosen R_{SENSE} yet, ignore this term in the equations for now. We will make a more accurate estimate of the duty cycle range later.

Ensure that the estimated duty cycle range is within the specification of the selected device: 4% to 93% for the MAX16990 and 24% to 85% for the MAX16992.

Inductor

To guarantee continuous-conduction mode (CCM) operation throughout the application, choose an inductor (L) higher than the critical inductance (L_C) as calculated with Equation 5:

$$L \geq L_C = \frac{0.5 \times Eff \times (V_{OUT} + V_D) \times D \times (1 - D)^2}{f_{SW} \times I_{OUT}} \qquad \text{(Eq. 5)}$$

L_C assumes its maximum value for D = 33% if it is in the calculated duty cycle range; otherwise choose the maximum value for L_C between the ones calculated at the maximum and minimum duty cycles.

The other aspect to keep in mind when choosing the proper inductor is the LIR factor. This parameter is defined as the ratio of the peak-to-peak inductor current and the average input current:

$$LIR = \frac{IL_{P-P}}{I_{IN(AVG)}} \qquad \text{(Eq. 6)}$$

The relationship between the inductor (L) and the LIR factor is shown in Equation 7:

$$LIR = \frac{(V_{OUT} + V_D - V_{IN}) \times (1 - D)}{f_{SW} \times L \times I_{IN(AVG)}}$$ (Eq. 7)

To reduce losses, choose an inductor that guarantees an LIR factor between 0.3 and 0.5. With L equal to L_C, the LIR factor is 2. Further increasing L reduces the LIR factor. The selected inductor has to have a saturation current higher than its peak current, which is:

$$IL_{PEAK} = I_{IN(AVG)} \left(1 + \frac{LIR}{2}\right)$$ (Eq. 8)

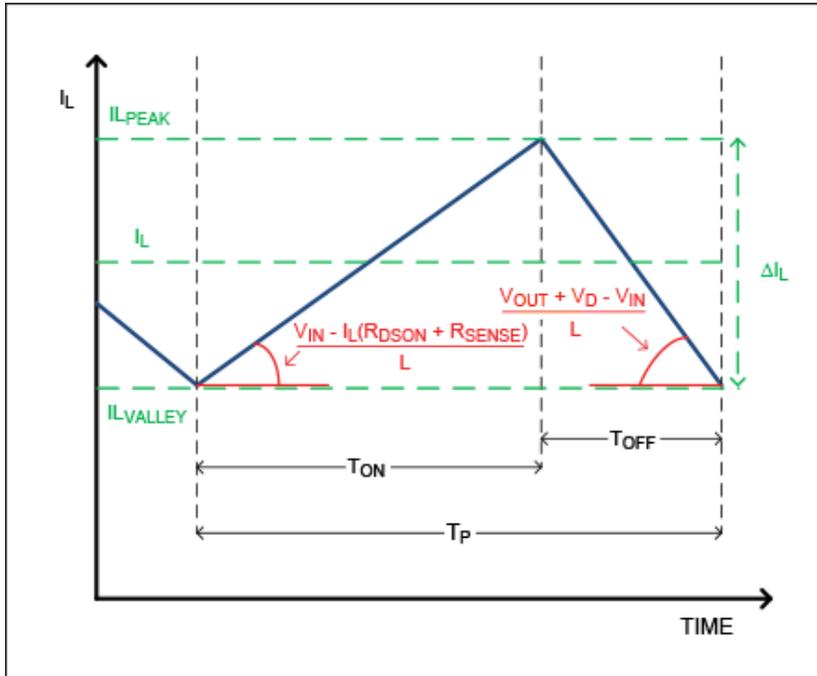**Figure 1** illustrates the inductor current shape during the switching period.

Figure 1. Inductor current of the boost regulator.

The peak inductor current coincides with the peak nMOS current and rectifier diode current. Considering this, choose the current rating of the two power components accordingly. Additionally, the maximum nMOS drain-source voltage is equal to the output voltage (V_{OUT}) plus the drop on the rectifier diode (V_D), and the maximum reverse voltage across the rectifier diode is equal to the output voltage (V_{OUT}).

Sense Resistor

Now that the peak inductor current has been calculated, it is possible to select the sense resistor (R_{SENSE}). The device triggers the current limit when the voltage on the ISNS pin reaches 212mV (min). A portion of this voltage is due to the drop on the sense resistor and another portion to the drop on the slope resistor (R_{SLOPE}), which is used for slope compensation. To leave 100mV of room for slope compensation, it is initially recommended for R_{SENSE} to generate a voltage drop of 112mV at the current limit threshold. In Equation 9, R_{SENSE} is calculated with a current limit threshold 20% higher than the peak inductor current.

$$R_{SENSE} = \frac{0.112}{1.2 \times IL_{PEAK}}$$ (Eq. 9)

Output Capacitor

Selecting the correct output capacitor (C_{OUT}) and its related ESR is very important to minimize output voltage ripple.

Assume that the output voltage ripple (V_{OUT_RIPPLE}) is equally distributed between the voltage drop, which is due to the capacitor discharging during off-time, and the ESR voltage drop.

$$C_{OUT} > \frac{I_{OUTMAX} \times D_{MAX}}{0.5 \times V_{OUT\_RIPPLE} \times f_{SW}}$$ (Eq. 10)

$$ESR < \frac{0.5 \times V_{OUT\_RIPPLE}}{I_{OUTMAX}}$$ (Eq. 11)

Compensation

After looking at these external components (the inductor, sense resistor, and output capacitor), we need to consider the external compensation components necessary for the preboost regulator. See **Figure 2** for an overview of the boost regulation loop, which is composed of the power stage (A(f)) and the feedback stage (B(f)).
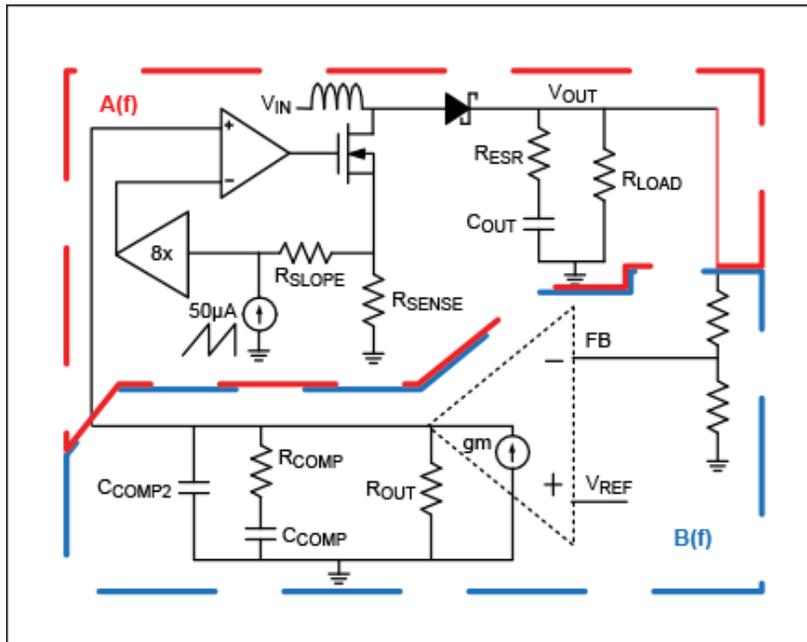

Figure 2. Boost regulator small-signal model.

In order to select the appropriate external compensation components (R_{COMP}, C_{COMP}, C_{COMP2}, and R_{SLOPE}), it is necessary to describe the loop response in the frequency domain and evaluate its stability. The regulation loop can be divided into two stages.

The first stage, A(f), is the power stage, which is composed of the current-sense circuitry, the PWM comparator, the external nMOS, the inductor (L), the output capacitor (C_{OUT}), and the load resistor (R_{LOAD}). The frequency response of this stage is described by Equation 12:

$$A(f) = ACM \times \frac{\left(1 + j\frac{f}{f_{Z,ESR}}\right) \times \left(1 - j\frac{f}{f_{Z,RHP}}\right)}{\left(1 + j\frac{f}{f_{P,LOAD}}\right) \times \left(1 + \frac{f}{\pi \times Q \times f_{SW}} + \frac{f^2}{\pi^2 \times f_{SW}^2}\right)}$$ (Eq. 12)

The DC gain ACM is:

$$ACM = \frac{(1 - D) \times R_{LOAD}}{2 \times R_{SENSE} \times CS_{GAIN}}$$ (Eq. 13)

The numerator in Equation 12 is composed of the zero introduced by the output capacitor ESR:

$$f_{Z,ESR} = \frac{1}{2\pi \times C_{OUT} \times R_{ESR}}$$ (Eq. 14)

And the right-half plane zero of the current-mode boost regulator:

$$f_{Z,RHP} = \frac{R_{LOAD} \times \left(\frac{V_{IN}}{V_{OUT}}\right)^2}{2\pi \times L}$$ (Eq. 15)

It is useful to remember that this zero acts as a normal zero from the module side but as a pole from the phase side, thereby decreasing the phase of the closed-loop frequency response.

The A(f) denominator in Equation 12 is composed of the output pole:

$$f_{P,LOAD} = \frac{1}{\pi \times C_{OUT} \times R_{LOAD}}$$ (Eq. 16)

And the double pole at half of the switching frequency, which has to be damped with slope compensation.

The second stage that characterizes the closed-loop response, B(f), is calculated with the feedback network (AFB) and the error amplifier (AEA):

$$B(f) = AFB \times AEA \times \frac{\left(1 + j\frac{f}{f_{Z,EA}}\right)}{\left(1 + j\frac{f}{f_{P,EA}}\right) \times \left(1 + j\frac{f}{f_{P2,EA}}\right)}$$ (Eq. 17)

The DC gain is calculated from the AFB and AEA gains:

$$AFB = V_{REF}/V_{OUT}$$ (Eq. 18)
$$AEA = gm \times R_{OUT}$$ (Eq. 19)

Where gm is the voltage-to-current gain of the transconductance error amplifier and R_{OUT} its output.

The error amplifier zero and main pole are determined by the external compensation components C_{COMP} and R_{COMP}:

$$f_{Z,EA} = \frac{1}{2\pi \times C_{COMP} \times R_{COMP}}$$ (Eq. 20)

$$f_{P,EA} = \frac{1}{2\pi \times C_{COMP} \times (R_{OUT} + R_{COMP})}$$

(Eq. 21)

A second error amplifier pole can be added, if needed, with a capacitor between the COMP pin and GND (C_{COMP2}):

$$f_{P2,EA} = \frac{1}{2\pi \times C_{COMP2} \times (R_{COMP}//R_{OUT})}$$

(Eq. 22)

The closed-loop response of the regulator is achieved by tying together A(f) and B(f):

$$\text{Loop}(f) = A(f) \times B(f)$$

(Eq. 23)

Once we become familiar with the loop frequency response, the first step to ensure stability is to select the proper slope compensation in order to avoid oscillation at half of the switching frequency. To do that, the Q factor, shown in Equation 24, has to be between zero and one:

$$Q = \frac{1}{\pi \times \left((1-D) \times \frac{S_e}{S_n} + \frac{1}{2} - D\right)}$$

(Eq. 24)

Where S_n is the positive inductor current ramp during on-time multiplied by the sense resistor (voltage ramp on R_{SENSE}):

$$S_n = \frac{V_{IN}}{L} \times R_{SENSE}$$

(Eq. 25)

And S_e is the slope compensation ramp multiplied by R_{SENSE} plus R_{SLOPE}:

$$S_e = I_{COMP} \times f_{SW} \times (R_{SLOPE} + R_{SENSE}), \quad I_{COMP} = 50\mu A$$

(Eq. 26)

R_{SLOPE} must have a Q factor between zero and one in all operating conditions.

The worst-case scenario for slope compensation is when the input voltage is at its minimum and the output current at its maximum.

Choosing a R_{SLOPE} higher than the value shown in Equation 27 ensures a Q factor between 0 and 1 in all operating conditions:

$$R_{SLOPE} = \frac{\left(\frac{1}{\pi} + D_{MAX} - 0.5\right) \times V_{INMIN} \times R_{SENSE}}{(1 - D_{MAX}) \times I_{COMP(MIN)} \times f_{SW} \times L} - R_{SENSE}$$

(Eq. 27)

Once R_{SLOPE} has been selected, it is possible to calculate the value of the real minimum current limit using Equation 28:

$$CL_{MIN} = \frac{0.212 - 60\mu A \times D_{MAX} \times R_{SLOPE}}{R_{SENSE}}$$

(Eq. 28)

If the current limit is too high, increase R_{SENSE} and R_{SLOPE} accordingly until the desired value is reached.

Ensure that the minimum current limit is higher than the peak inductor current.

Once the double pole at half of the switching frequency is dumped, it is necessary to choose the error amplifier compensation components to ensure good phase margin at the crossover frequency.

The first step is to choose the desired crossover frequency ($f_{C,TARGET}$), which has to be lower than $f_{SW}/10$ and $f_{Z,RHP}/10$. Initially, we assume that the zero due to the output capacitor ESR ($f_{Z,ESR}$) is ten times higher than $f_{C,TARGET}$. Under this assumption, the closed-loop frequency response can be approximated as a simple two poles and one zero system frequency response.

$$\text{Loop}'(f) = DC_{GAIN} \times \frac{\left(1 + j\frac{f}{f_{Z,EA}}\right)}{\left(1 + j\frac{f}{f_{P,EA}}\right) \times \left(1 + j\frac{f}{f_{P,LOAD}}\right)} \qquad \text{(Eq. 29)}$$

$$DC_{GAIN} = ACM \times AFB \times AEA \qquad \text{(Eq. 30)}$$

Based on the target crossover frequency and the obtained DC_{GAIN}, two cases can be considered.

The first one is when:

$$f_{P,LOAD} < \frac{f_{C,TARGET}}{10^{\frac{DC_{GAIN}}{40}}} \qquad \text{(Eq. 31)}$$

In this case (see **Figure 3**), place the error amplifier pole after the load pole :

$$C_{COMP} = \frac{10^{\frac{DC_{GAIN}}{40}}}{2\pi \times f_{C,TARGET} \times R_{OUT}} \qquad \text{(Eq. 32)}$$

And the error amplifier zero exactly on the target crossover frequency:

$$R_{COMP} = \frac{1}{2\pi \times f_{C,TARGET} \times C_{COMP}} \qquad \text{(Eq. 33)}$$

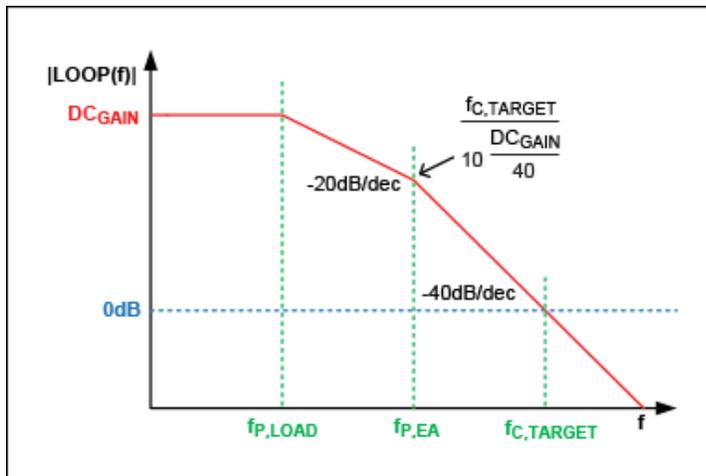This ensures a 45° positive lag on the phase margin.

Figure 3. Bode diagram of the amplitude of the closed-loop response, case 1.

The second one is when:

$$f_{P,LOAD} > \frac{f_{C,TARGET}}{10^{\frac{DC_{GAIN}}{40}}}$$

(Eq. 34)

In this case (see **Figure 4**), place the error amplifier pole before the load pole:

$$C_{COMP} = \frac{10^{\frac{DC_{GAIN} + 3 - 40 \times LOG\left(\frac{f_{C,TARGET}}{f_{P,LOAD}}\right)}{20}}}{2\pi \times f_{C,TARGET} \times R_{OUT}}$$

(Eq. 35)

And the error amplifier zero exactly on the target crossover frequency:

$$R_{COMP} = \frac{1}{2\pi \times f_{C,TARGET} \times C_{COMP}}$$

(Eq. 36)
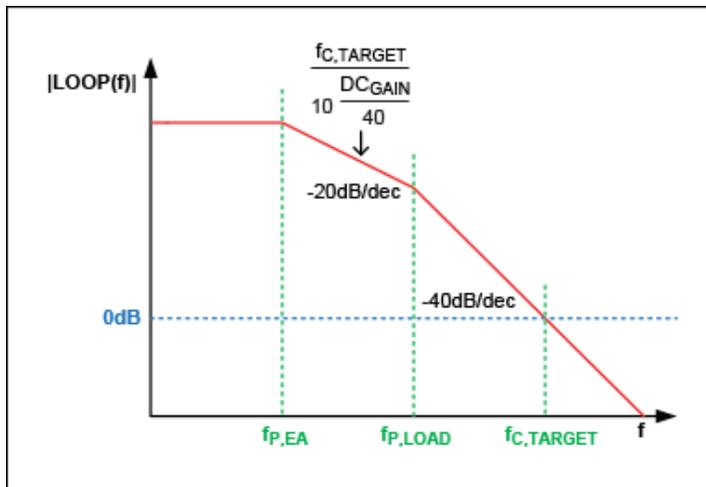
This ensures a 45° positive lag on the phase margin.

Figure 4. Bode diagram of the amplitude of the closed-loop response, case 2.

Use the calculator to estimate the obtained crossover frequency and phase margin. If they are not satisfactory, increase R_{COMP} to increase the crossover frequency and the phase margin.

If the zero from the output capacitor ESR is not negligible and affects the phase margin and crossover frequency, add a second error amplifier pole (C_{COMP2}) corresponding to the ESR zero:

$$C_{COMP2} = \frac{1}{2\pi \times f_{Z,ESR} \times (R_{COMP}//R_{OUT})}$$

(Eq. 37)

Reference Design

After discussing the external and compensation components required, we consider a reference design for an automotive preboost application.

The usual requirements for an automotive preboost application are:

f_{SW}	2.2MHz
V_{IN}	3.5V to 6V
V_{OUT}	8V
I_{OUT}	1A to 2A
V_{OUT_RIPPLE}	50mV

Estimating an efficiency (Eff) of 90%, the input current range should be:

$$I_{IN(AVG,MIN)} = \frac{V_{OUT} \times I_{OUTMIN}}{V_{INMAX} \times Eff} = \frac{8 \times 1}{6 \times 0.9} = 1.48A \qquad \text{(Eq. 38)}$$

$$I_{IN(AVG,MAX)} = \frac{V_{OUT} \times I_{OUTMAX}}{V_{INMIN} \times Eff} = \frac{8 \times 2}{3.5 \times 0.9} = 5.08A \qquad \text{(Eq. 39)}$$

The second step is to calculate the duty cycle range. To do that, it is useful to choose the nMOS resistor. In order to determine the nMOS ratings requirement, it is necessary to calculate the peak transistor current (corresponding to the peak inductor current).

Assume a maximum LIR of 0.5 when the input current is at its maximum:

$$IL_{PEAK(MAX,ESTIMATED)} = I_{IN(AVG,MAX)} \left(1 + \frac{LIR}{2}\right) = 6.35A \qquad \text{(Eq. 40)}$$

Based on this information, Fairchild's FDS5670 nMOS, which is rated for a drain current of 10A, was chosen. The typical $R_{DS(ON)}$ of this transistor is 15mΩ with a V_{GS} = 5V (the gate-source voltage of the MAX16992).

Once we have this information, we can calculate the duty cycle range ignoring R_{SENSE} for now:

$$D_{MIN} = \frac{V_{OUT} + V_D - V_{INMAX}}{V_{OUT} + V_D - [(R_{DS(ON)} + R_{SENSE}) \times I_{IN(AVG,MIN)}]} = 0.294 \qquad \text{(Eq. 41)}$$

$$D_{MAX} = \frac{V_{OUT} + V_D - V_{INMIN}}{V_{OUT} + V_D - [(R_{DS(ON)} + R_{SENSE}) \times I_{IN(AVG,MAX)}]} = 0.599 \qquad \text{(Eq. 42)}$$

Assume that the forward voltage of the rectifier diode (Diodes Incorporated's B3x0-13-F) is equal to 0.5V. The duty cycle range is compatible with the MAX16992. To guarantee continuous-conduction mode:

$$L \geq L_C = \frac{0.5 \times Eff \times (V_{OUT} + V_D) \times D \times (1 - D)^2}{f_{SW} \times I_{OUT}} = 0.26\mu H \qquad \text{(Eq. 43)}$$

In the worst-case scenario, D = 0.33% and I_{OUT} = 1A.

Based on this information, Würth Elektronik's 0.47µH inductor 744314047 was selected (I_R = 18A, I_{SAT} = 20A). With this inductor, when the input voltage is at its minimum (and the input current at its maximum):

$$LIR = \frac{(V_{OUT} + V_D - V_{INMIN}) \times (1 - D_{MAX})}{f_{SW} \times L \times I_{IN(AVG,MAX)}} = 0.38 \qquad \text{(Eq. 44)}$$

Resulting in an inductor (and nMOS) peak current of:

$$IL_{PEAK(MAX)} = I_{IN(AVG,MAX)}\left(1 + \frac{LIR}{2}\right) = 6.05A \qquad \text{(Eq. 45)}$$

This value is in accordance with the nMOS drain current rating.

Now it is possible to calculate the sense resistor:

$$R_{SENSE} = \frac{0.112}{1.2 \times IL_{PEAK(MAX)}} = 15.38m\Omega \qquad \text{(Eq. 46)}$$

A 15mΩ resistor was chosen for R_{SENSE}.

In accordance with the design specification on the output voltage ripple, the constraints on C_{OUT} are:

$$C_{OUT} > \frac{I_{OUTMAX} \times D_{MAX}}{0.5 \times V_{OUT\_RIPPLE} \times f} = 21.6\mu F \qquad \text{(Eq. 47)}$$

$$ESR < \frac{0.5 \times V_{OUT\_RIPPLE}}{I_{OUTMAX}} = 12.5m\Omega \qquad \text{(Eq. 48)}$$

Murata's 47µF GRM32ER61C476K capacitor with an ESR of 3mΩ at the switching frequency 2.2MHz was chosen.

The first parameter to select for compensation is R_{SLOPE}:

$$R_{SLOPE} = \frac{\left(\frac{1}{\pi} + D_{MAX} - 0.5\right) \times V_{INMIN} \times R_{SENSE}}{(1 - D_{MAX}) \times I_{COMP(MIN)} \times f \times L} - R_{SENSE} = 1321\Omega \qquad \text{(Eq. 49)}$$

A standard 1.3kΩ resistor was chosen. The minimum current limit threshold became:

$$CL_{MIN} = \frac{0.212 - 60\mu A \times D_{MAX} \times R_{SLOPE}}{R_{SENSE}} = 11.02A \qquad \text{(Eq. 50)}$$

The DC_{GAIN}, load pole frequency, and the right-half plane zero frequency are:

$$DC_{GAIN} = ACM \times AFB \times AEA = 91.6dB \qquad \text{(Eq. 51)}$$

$$f_{P,LOAD} = \frac{1}{\pi \times C_{OUT} \times R_{LOAD}} = 1693Hz \qquad \text{(Eq. 52)}$$

$$f_{Z,RHP} = \frac{R_{LOAD} \times \left(\frac{V_{IN}}{V_{OUT}}\right)^2}{2\pi \times L} = 259kHz \qquad \text{(Eq. 53)}$$

Which are calculated for the worst-case scenario with the input voltage at its minimum and the load current at its maximum.

Murata's 47µF capacitor has an ESR lower than 20mΩ for a frequency above 2kHz.

Thus, the ESR zero, in the worst case, is:

$$f_{Z,ESR} = \frac{1}{2\pi \times C_{OUT} \times R_{ESR}} = 169kHz \qquad \text{(Eq. 54)}$$

In this case, the maximum crossover frequency has to be lower than $f_{Z,RHP}/10 = 25.9kHz$.

Choosing a target crossover frequency of 25kHz, we must follow:

$$f_{P,LOAD} = 1693Hz > \frac{f_{C,TARGET}}{10^{\frac{DC_{GAIN}}{40}}} = 128Hz \qquad \text{(Eq. 55)}$$

In this case, the C_{COMP} target becomes:

$$C_{COMP} = \frac{10^{\frac{DC_{GAIN} + 3 - 40 \times LOG\left(\frac{f_{C,TARGET}}{f_{P,LOAD}}\right)}{20}}}{2\pi \times f_{C,TARGET} \times R_{OUT}} = 464pF \qquad \text{(Eq. 56)}$$

A standard 470pF capacitor was chosen and consequently the estimated R_{COMP} target is:

$$R_{COMP} = \frac{1}{2\pi \times f_{C,TARGET} \times C_{COMP}} = 13545\Omega \qquad \text{(Eq. 57)}$$

A standard 15kΩ resistor was chosen.

The last component remaining is C_{COMP2}:

$$C_{COMP2} = \frac{1}{2\pi \times f_{Z,ESR} \times (R_{COMP}//R_{OUT})} = 63pF \qquad \text{(Eq. 58)}$$

A standard 68pF capacitor was chosen.

With the chosen external compensation components, the error amplifier zero and pole frequencies are:

$$f_{Z,EA} = \frac{1}{2\pi \times C_{COMP} \times R_{COMP}} = 22.6kHz \qquad \text{(Eq. 59)}$$

$$f_{P,EA} = \frac{1}{2\pi \times C_{COMP} \times (R_{OUT} + R_{COMP})} = 6.8Hz \qquad \text{(Eq. 60)}$$

$$f_{P2,EA} = \frac{1}{2\pi \times C_{COMP2} \times (R_{COMP}//R_{OUT})} = 156kHz \qquad \text{(Eq. 61)}$$

Use the calculator to determine the obtained crossover frequency (f_{CROSS}) and phase margin (PM).

In this case, these two parameters are:

f_{CROSS} = 26.3kHz   (Eq. 62)

PM = 45°   (Eq. 63)

The final Bode diagrams of the closed loop regulator are illustrated in **Figure 5** and **Figure 6**.

Figure 5. Loop gain.
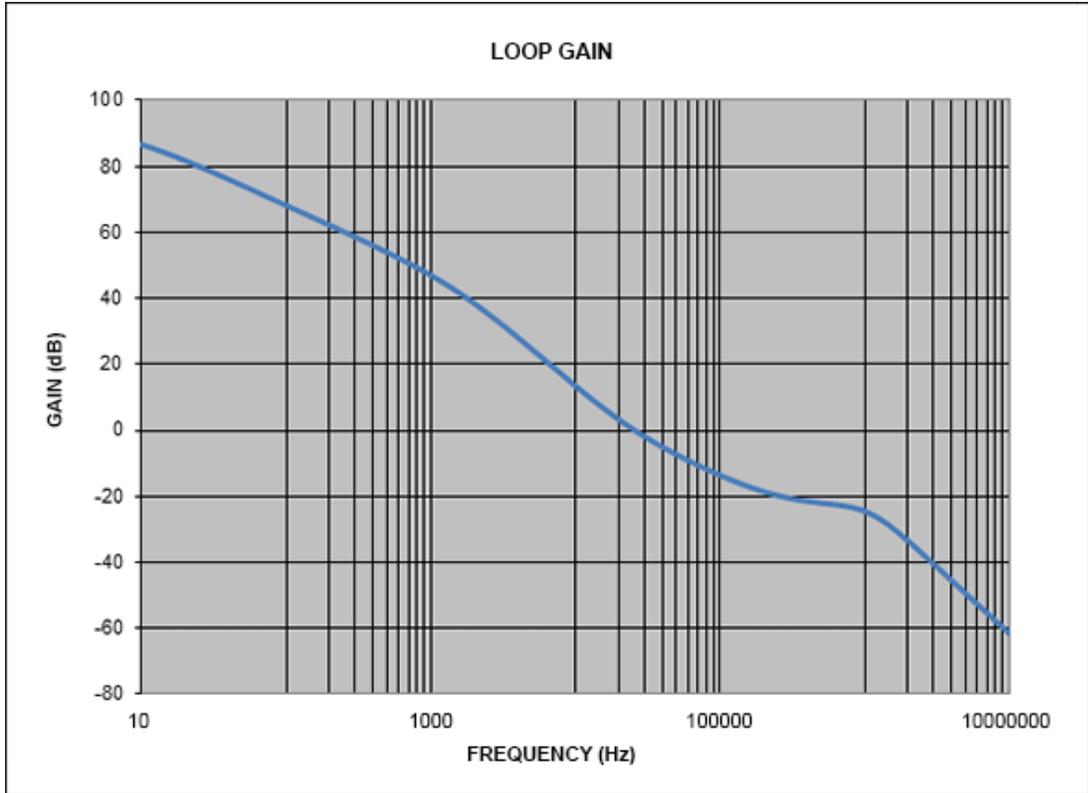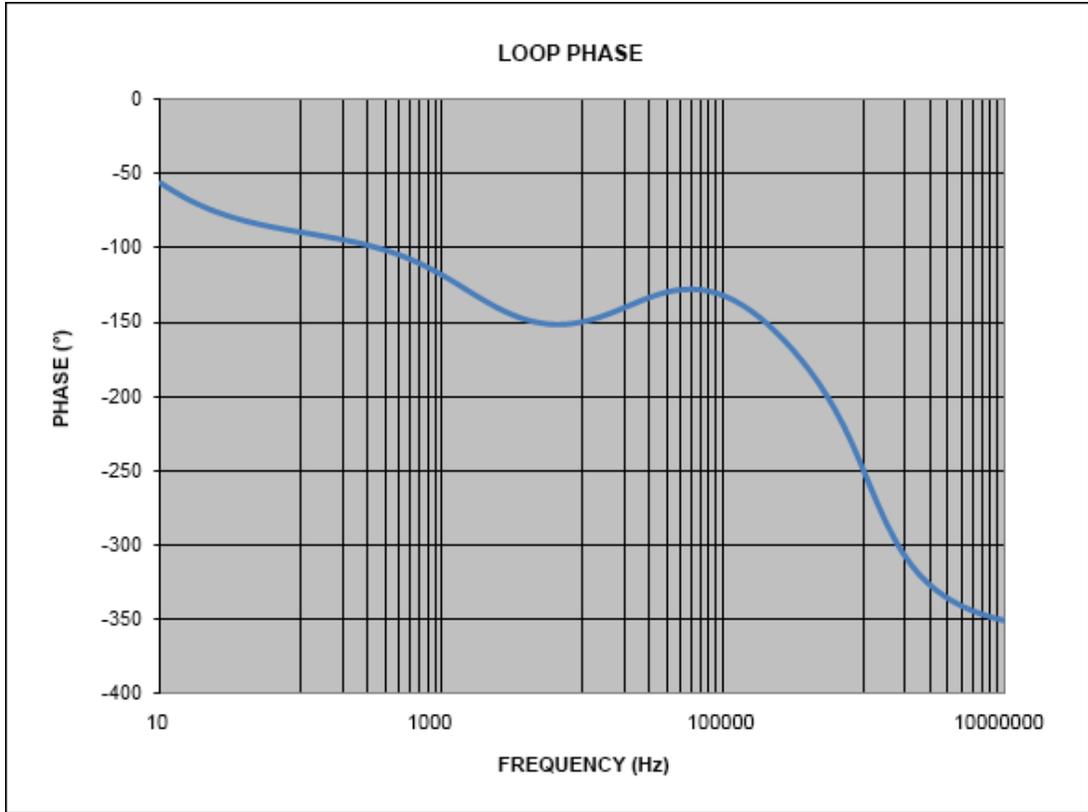
LOOP PHASE

Figure 6. Loop phase.

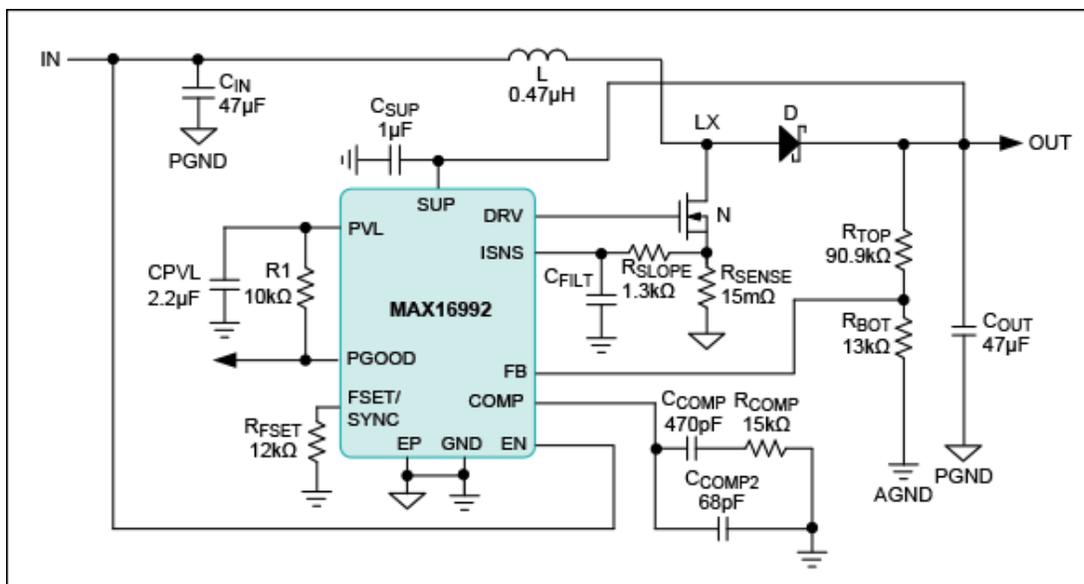| Designation	Description
N	Fairchild FDS5670 nMOS
D	Diodes Inc. B3x0-13-F
L	Würth Elektronik 744314047
C_{OUT}	Murata GRM32ER61C476K

Figure 7. Schematic of reference design.

Layout Recommendation

A good layout is very important to maximize EMI and jitter-free performance of the boost regulator. To achieve that, follow these general recommendations:

1. Place all power components on the same side of the board.

2. Keep the AC paths as short as possible. During on-time, the AC path is composed of C_{IN}, an inductor, nMOS, R_{SENSE}, and GND. During off-time, the AC path is composed of C_{IN}, an inductor, a diode, C_{OUT}, and GND.

3. Keep the switching node (LX) as compact as possible.

4. Do not route the path between the DRV pin and the gate of the nMOS with the minimum width. This net commutes at the switching frequency and has to carry the current necessary to drive the nMOS. If vias are necessary, route the net to an internal layer.

5. Connect the C_{SUP} and C_{PVL} capacitors directly to the IC, as close as possible without using vias.

6. Use a Kelvin connection between R_{SENSE} and R_{SLOPE}, and between R_{SLOPE} and the ISNS pin.

7. Use a Kelvin connection between OUT and RTOP. Keep the FB node as close as possible to the FB pin of the IC.

8. Use two separate GNDs as indicated on the schematic: PGND for power components and AGND for the signal circuitry and the EP of the MAX16992. Use a single-point connection between PGND and AGND, as close as possible to the EP.

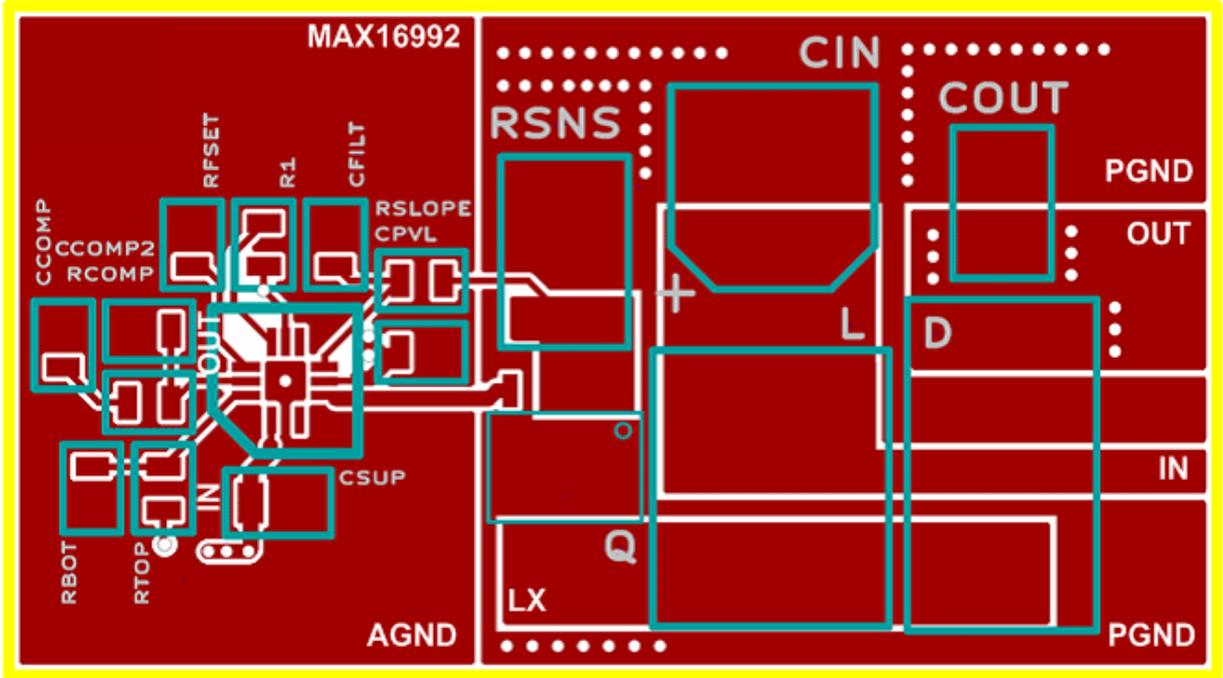A reference layout is shown in **Figure 8** through **Figure 12**.
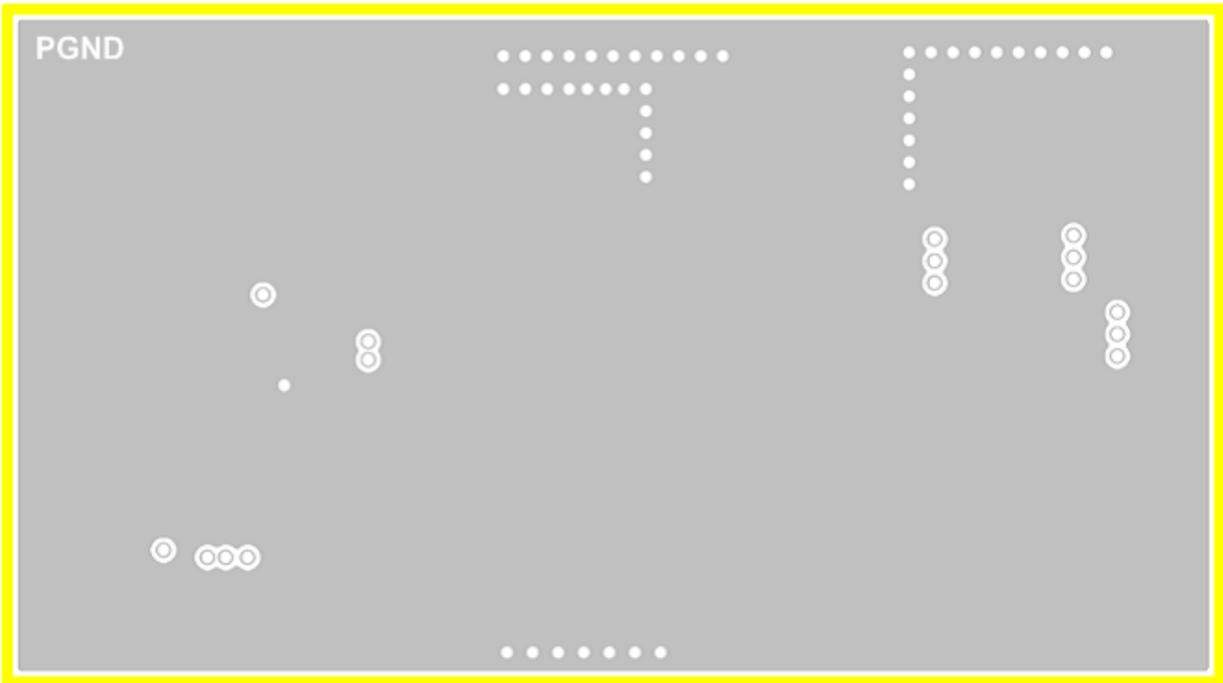
Figure 8. Reference design layout, top layer.

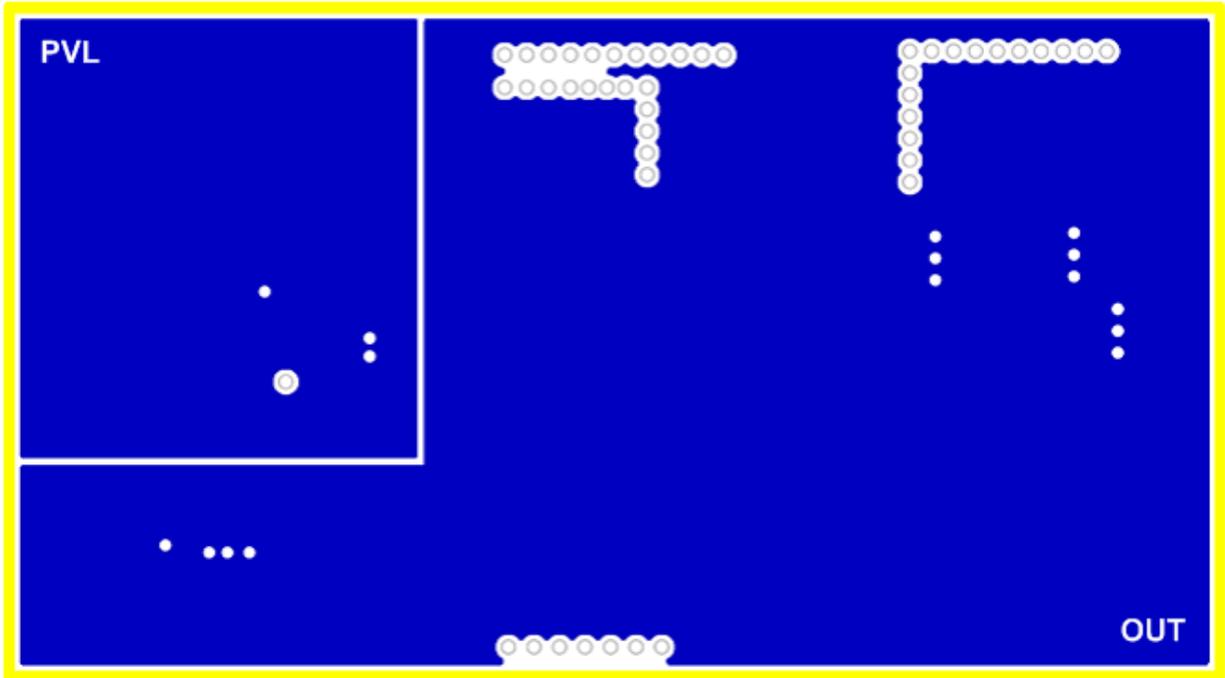*Figure 9. Reference design layout, inner layer 1.*

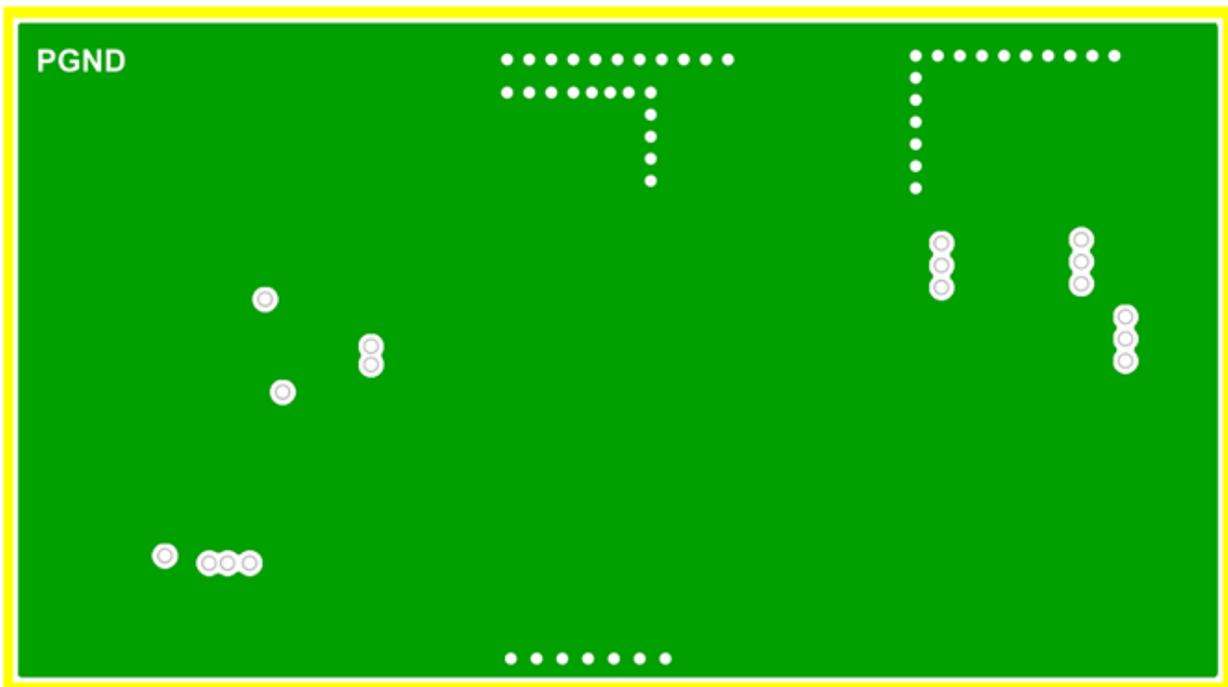*Figure 10. Reference design layout, inner layer 2.*
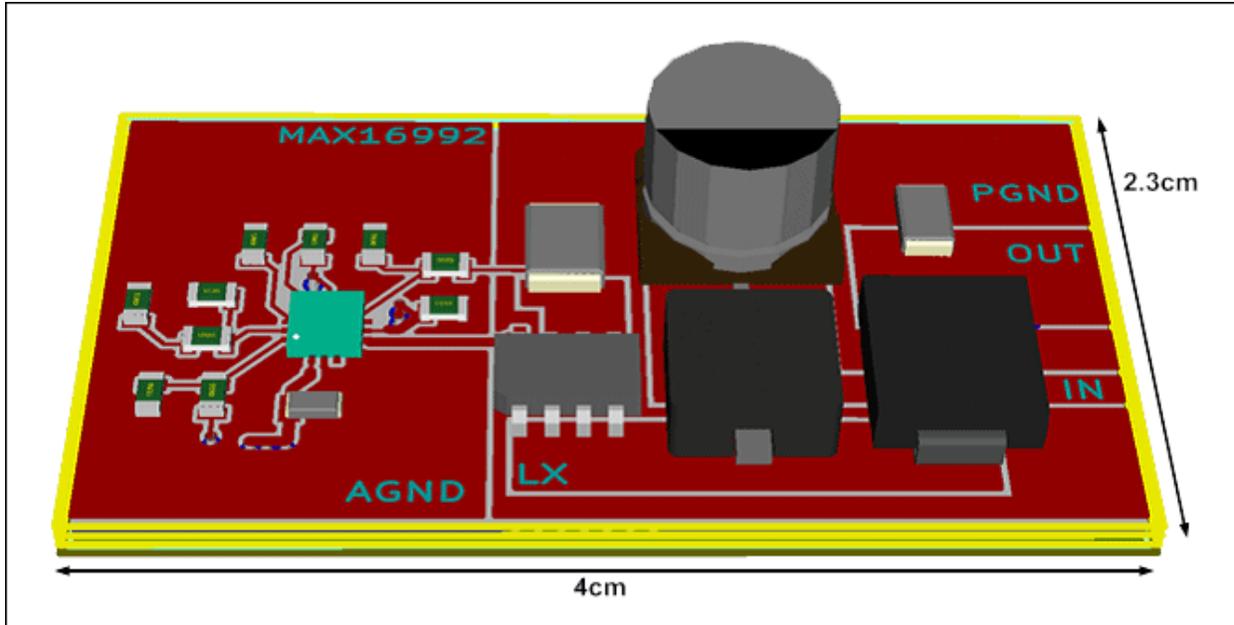

Figure 11. Reference design layout, back layer.

Figure 12. Reference design, 3D view.

Conclusion

In this application note, we learned how best to select external components and compensation for optimal performance of the MAX16990/MAX16922. We then saw how these devices can be used in automotive applications as preboost regulators and discovered the best layout to maximize EMI and minimize jitter.

Related Parts		
MAX16990	36V, 2.5MHz Automotive Boost/SEPIC Controllers	Free Samples
MAX16992	36V, 2.5MHz Automotive Boost/SEPIC Controllers	Free Samples

More Information
For Technical Support: http://www.maximintegrated.com/support
For Samples: http://www.maximintegrated.com/samples
Other Questions and Comments: http://www.maximintegrated.com/contact

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