VSC8484 Datasheet
Quad Channel WAN/LAN/Backplane XAUI to SFP+/KR Transceiver



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Contents

1 Revision History . . . 1
1.1 Revision 4.4 . . . 1
1.2 Revision 4.3 . . . 1
1.3 Revision 4.2 . . . 1
1.4 Revision 4.1 . . . 1
1.5 Revision 4.0 . . . 1
1.6 Revision 2.0 . . . 2
2 Product Overview . . . 3
2.1 Major Applications . . . 4
2.2 Features and Benefits . . . 5
3 Functional Descriptions . . . 6
3.1 Transmit Operation for XAUI to SFI Mode . . . 7
3.2 Receive Operation for SFI to XAUI Mode . . . 8
3.3 PMA . . . 8
3.3.1 Supported Data Rates and Standards . . . 9
3.3.2 Rate Auto-Negotiation . . . 9
3.3.3 Receiver (Rx) Subsection . . . 9
3.3.4 Variable Gain Amplifier Input Receiver . . . 9
3.3.5 Rx Equalizer . . . 10
3.3.6 Rx Clock and Data Recovery . . . 10
3.3.7 Rx Data Rate Selection . . . 12
3.3.8 Rx Data Path Control . . . 13
3.3.9 External Capacitors . . . 13
3.3.10 VScope Input Signal Monitoring Integrated Circuit . . . 13
3.3.11 Unity Gain Amplifier . . . 13
3.3.12 Link Monitor . . . 13
3.3.13 Transmitter (Tx) Subsection . . . 13
3.3.14 Tx Data Rate Selection . . . 14
3.3.15 Tx Data Path Control . . . 15
3.3.16 10BASE-KR Output Driver . . . 15
3.3.17 PMA Loopback . . . 17
3.3.18 PMA Linetime . . . 17
3.3.19 External Capacitors . . . 18
3.3.20 Reference Clock . . . 18
3.3.21 Reference Clock Inputs . . . 20
3.3.22 Clock Output . . . 20
3.3.23 Synchronous Ethernet Support . . . 20
3.3.24 1.25 Gbps Mode . . . 21
3.3.25 Power Down Mode . . . 22
3.3.26 Clock Distribution . . . 22
3.3.27 Operation Modes . . . 23
3.4 WAN Interface Sublayer (WIS) . . . 25
3.4.1 Operation . . . 25
3.4.2 Section Overhead . . . 28
3.4.3 A1, A2 (Frame Alignment) . . . 29
3.4.4 Loss of Signal (LOS) . . . 31
3.4.5 Loss of Optical Carrier (LOPC) . . . 31
3.4.6 Severely Errored Frame (SEF) . . . 32
3.4.7 Loss of Frame (LOF) . . . 32

3.4.8 J0 (Section Trace) . . . 32
3.4.9 Z0 (Reserved for Section Growth) . . . 33
3.4.10 Scrambling/Descrambling . . . 33
3.4.11 B1 (Section Error Monitoring) . . . 33
3.4.12 E1 (Section Orderwire) . . . 33
3.4.13 F1 (Section User Channel) . . . 33
3.4.14 DCC-S (Section Data Communication Channel) . . . 33
3.4.15 Reserved, National, and Unused Octets . . . 33
3.4.16 Line Overhead . . . 34
3.4.17 B2 (Line Error Monitoring) . . . 35
3.4.18 K1, K2 (APS Channel and Line Remote Defect Identifier) . . . 35
3.4.19 D4 to D12 (Line Data Communications Channel) . . . 37
3.4.20 M0 and M1 (STS-1/N Line Remote Error Indication) . . . 37
3.4.21 S1 (Synchronization Messaging) . . . 37
3.4.22 Z1 and Z2 (Reserved for Line Growth) . . . 37
3.4.23 E2 (Orderwire) . . . 37
3.4.24 SPE Pointer . . . 37
3.4.25 Bit Designations within Payload Pointer . . . 38
3.4.26 Pointer Types . . . 39
3.4.27 Pointer Adjustment Rule . . . 39
3.4.28 Pointer Increment/Decrement Majority Rules . . . 39
3.4.29 Pointer Interpretation States . . . 40
3.4.30 Valid Pointer Definition for Interpreter State Diagram Transitions . . . 40
3.4.31 Path Overhead . . . 41
3.4.32 J1 (Overhead Octet) . . . 42
3.4.33 B3 (STS Path Error Monitoring) . . . 42
3.4.34 C2 (STS Path Signal Label and Path Label Mismatch) . . . 43
3.4.35 G1 (Remote Path Error Indication) . . . 43
3.4.36 G1 (Path Status) . . . 43
3.4.37 F2 (Path User Channel) . . . 45
3.4.38 H4 (Multiframe Indicator) . . . 45
3.4.39 Z3-Z4 (Reserved for Path Growth) . . . 45
3.4.40 N1 (Tandem Connection Maintenance/Path Data Channel) . . . 45
3.4.41 Loss of Code Group Delineation . . . 45
3.4.42 Reading Statistical Counters . . . 45
3.4.43 Defects and Anomalies . . . 47
3.4.44 Interrupt Pins and Interrupt Masking . . . 48
3.4.45 Overhead Serial Interfaces . . . 49
3.4.46 Transmit Overhead Serial Interface (TOSI) . . . 49
3.4.47 Receive Overhead Serial Interface (ROSI) . . . 52
3.4.48 Pattern Generator and Checker . . . 52
3.5 Physical Coding Sublayer (64B/66B PCS) . . . 53
3.5.1 Control Codes . . . 54
3.5.2 Transmit Path . . . 54
3.5.3 Receive Path . . . 55
3.5.4 PCS Standard Test Modes . . . 56
3.5.5 PCS XGMII BIST . . . 56
3.6 Client/Host Interface (XAUI) . . . 58
3.6.1 XGMII Extender Sublayer (PHY XS) . . . 58
3.6.2 XAUI Receiver . . . 58
3.6.3 XAUI Receiver Equalization . . . 59
3.6.4 XAUI Clock and Data Recovery . . . 59
3.6.5 XAUI Code Group Synchronization . . . 59
3.6.6 XAUI Lane Deskew . . . 60
3.6.7 10B/8B Decoder . . . 61
3.6.8 8b/10b Encoder and Serializer . . . 61
3.6.9 XAUI Transmitter . . . 61
3.6.10 XAUI Transmitter Pre-Emphasis . . . 61

3.6.11 XAUI Power Down Mode . . . 62
3.6.12 XAUI Failover . . . 62
3.7 10GBASE-KR . . . 62
3.7.1 Auto-negotiation . . . 62
3.7.2 Technology Ability Field . . . 65
3.7.3 Transmitted Nonce . . . 66
3.7.4 Role of Firmware during Auto-negotiation . . . 66
3.7.5 Timers . . . 67
3.7.6 Advertised Ability Registers . . . 67
3.7.7 Link Control . . . 68
3.7.8 Next Pages . . . 68
3.7.9 Training . . . 68
3.7.10 Coefficient Update Field . . . 69
3.7.11 Status Report Field . . . 70
3.7.12 Training Pattern . . . 71
3.7.13 Role of Hardware and Firmware during Training . . . 71
3.7.14 Training Status . . . 73
3.7.15 Coefficient Update and Status Report . . . 74
3.7.16 BER Calculation . . . 75
3.7.17 Forward Error Correction (FEC) . . . 75
3.8 Loopback and Bypass . . . 76
3.8.1 Loopback Modes . . . 76
3.8.2 Loopback A . . . 76
3.8.3 Loopback B . . . 76
3.8.4 Loopback F . . . 76
3.8.5 Loopback G . . . 77
3.8.6 Loopback J . . . 77
3.8.7 Loopback K . . . 77
3.9 Low-Speed Serial Interfaces . . . 78
3.9.1 MDIO Interface . . . 79
3.9.2 Two-Wire Serial (Master) for Loading Firmware . . . 81
3.9.3 Two-Wire Serial Slave Interface . . . 82
3.9.4 UART . . . 83
3.9.5 JTAG . . . 83
3.10 Operating Modes . . . 84
3.10.1 Firmware Load Mode, EEPROM Address Format . . . 84
3.10.2 Default Operation . . . 85
3.11 Loading Firmware . . . 85
3.11.1 EEPROM . . . 85
3.11.2 MDIO and Two-Wire Serial Slave Interfaces . . . 86
3.12 Microcontroller Activity Monitoring . . . 87
3.13 Interrupt Pending Registers . . . 87
3.14 Multipurpose GPIO Pins . . . 88
3.15 PCS Activity Monitor LEDs . . . 91
3.16 Temperature Monitor . . . 92
4 Registers . . . 94
4.1 Global Registers . . . 94
4.1.1 GPIO Pins . . . 97
4.2 Channel Registers . . . 172
4.3 EDC Registers . . . 286
4.3.1 Hardware DC Offset Correction Logic . . . 293
5 Electrical Specifications . . . 303
5.1 DC Characteristics . . . 303
5.1.1 Low-Speed Inputs and Outputs . . . 303

5.1.2 Reference Clock . . . 304
5.1.3 MDIO Interface . . . 304
5.2 AC Characteristics . . . 304
5.2.1 Receiver Specifications . . . 304
5.2.2 Transmitter Specifications . . . 308
5.2.3 Timing and Reference Clock . . . 314
5.2.4 Two-Wire Serial (Slave) Interface . . . 314
5.2.5 MDIO Interface . . . 315
5.3 Operating Conditions . . . 316
5.4 Stress Ratings . . . 318
6 Pin Descriptions . . . 320
6.1 Pin Diagram . . . 320
6.2 Pins by Function . . . 320
6.2.1 General Purpose Inputs and Outputs . . . 321
6.2.2 JTAG Interface . . . 321
6.2.3 Management Interface . . . 322
6.2.4 Ground . . . 323
6.2.5 Power Supply . . . 323
6.2.6 Receive Path . . . 324
6.2.7 Reference Clock . . . 324
6.2.8 Clock Outputs . . . 325
6.2.9 Test and Mode Control . . . 325
6.2.10 Transmit Path . . . 326
6.2.11 XAUI Channel . . . 326
6.2.12 Reserved . . . 329
7 Package Information . . . 330
7.1 Package Drawing . . . 330
7.2 Thermal Specifications . . . 331
7.3 Moisture Sensitivity . . . 332
8 Design Guidelines . . . 333
8.1 Sync-E in LAN Mode . . . 333
8.2 Sync-E in WAN Mode . . . 334
9 Ordering Information . . . 335

Figures

Figure 1 VSC8484 Block Diagram . . . 4
Figure 2 Backplane Equalization Application Diagram . . . 4
Figure 3 KR Backplane to SFP+ Application Diagram . . . 5
Figure 4 VSC8484 Channel Datapath Block Diagram . . . 7
Figure 5 Rx Input Receiver . . . 10
Figure 6 EDC Block Diagram . . . 11
Figure 7 10BASE-KR Output Driver . . . 15
Figure 8 KR Test Pattern . . . 16
Figure 9 Reference Clock Input Receiver . . . 20
Figure 10 1G Mode . . . 22
Figure 11 REFCLK Distribution . . . 23
Figure 12 WIS Transmit and Receive Functions . . . 26
Figure 13 WIS Frame Structure . . . 27
Figure 14 STS-192c/STM-64 Section and Line Overhead Structure . . . 27
Figure 15 Path Overhead Octets . . . 28
Figure 16 Primary Synchronization State Diagram . . . 29
Figure 17 Secondary Synchronization State Diagram . . . 30
Figure 18 16-bit Designations within Payload Pointer . . . 38
Figure 19 Pointer Interpreter State Diagram . . . 40
Figure 20 Path Status (G1) Byte for ERDI_RDIN = 0 . . . 44
Figure 21 Path Status (G1) Byte for ERDI_RDIN = 1 . . . 44
Figure 22 TOSI Timing Diagram . . . 50
Figure 23 ROSI Timing Diagram . . . 52
Figure 24 PCS Block Diagram . . . 53
Figure 25 64B/66B Block Formats . . . 55
Figure 26 Simplified XAUI Inputs . . . 59
Figure 27 Loss of Synchronization State Diagram . . . 60
Figure 28 LOA State Diagram . . . 61
Figure 29 Auto-negotiation Arbitration State Diagram . . . 64
Figure 30 Rate Detection . . . 66
Figure 31 PRBS Pattern Generator . . . 71
Figure 32 Training State Diagram . . . 73
Figure 33 Coefficient Update State Diagram . . . 74
Figure 34 VSC8484 Channel Clock Block Diagram . . . 78
Figure 35 MDIO Frame Format . . . 80
Figure 36 Two-Wire Serial (slave) Register Addressing Format . . . 82
Figure 37 Write Instruction . . . 82
Figure 38 Sequential Write Instruction . . . 83
Figure 39 Read Instruction . . . 83
Figure 40 Sequential Read Instruction . . . 83
Figure 41 Receive Path Input Compliance Mask . . . 307
Figure 42 10-Gigabit Data Input Compliance Mask (SFP+) . . . 308
Figure 43 SFI Datacom Sinusoidal Jitter Tolerance . . . 308
Figure 44 SFI Transmit Differential Output Compliance Mask . . . 310
Figure 45 XAUI Receiver Input Sinusoidal Jitter Tolerance . . . 312
Figure 46 XAUI Output Compliance Mask . . . 313
Figure 47 Two-Wire Serial Interface Timing . . . 315
Figure 48 Timing with MDIO Sourced by STA . . . 316
Figure 49 Timing with MDIO Sourced by MMD . . . 316
Figure 50 Power Supply Operating Range . . . 318
Figure 51 Pin Diagram . . . 320
Figure 52 Package Drawing . . . 331
Figure 53 Sync-E LAN Mode with Free-Running Clock . . . 333
Figure 54 Sync-E LAN Mode with Hitless Clock . . . 334

Figure 55 Sync-E WAN Mode 334

Tables

Table 1 Supported Data Rates and Standards . . . 9
Table 2 Rx CDR Lock to Reference Settings . . . 11
Table 3 Rx Loss of Lock Detection Settings . . . 11
Table 4 Rx CDR Reference Clock Source Selection . . . 12
Table 5 Rx CDR Divide Ratio and Rate Selection . . . 12
Table 6 Rx Data Bus Control . . . 13
Table 7 Tx Loss of Lock Detection Settings . . . 14
Table 8 Tx CMU Reference Clock Source Selection . . . 14
Table 9 Tx CMU Divide Ratio Selection . . . 14
Table 10 Tx Transmit Data Bus Control . . . 15
Table 11 Tx Transmit Output Waveform Changes by Coefficient Update . . . 16
Table 12 Tx Output Slew Rate Control Setting . . . 16
Table 13 Tx Output Driver Rise/Fall Time Control . . . 16
Table 14 Tx Transmit Data Bus Control . . . 17
Table 15 PMA Loopback . . . 17
Table 16 PMA LINETIME . . . 17
Table 17 CRU0 and CRU1 Paths Source Selection . . . 18
Table 18 CMU0 Path Source Selection . . . 18
Table 19 CMU1 Path Source Selection . . . 19
Table 20 PMA Reference Clock Rates and Modes . . . 19
Table 21 PMA Clock Output Setting . . . 20
Table 22 PMA Rx Data Rate Mode . . . 21
Table 23 Recommended Clock Operation Modes . . . 24
Table 24 WAN Mode Enable Logic . . . 25
Table 25 Section Overhead . . . 28
Table 26 Framing Parameter Description and Values . . . 30
Table 27 Line Overhead Octets . . . 34
Table 28 K2 Encodings . . . 36
Table 29 SONET/SDH Pointer Mode Differences . . . 38
Table 30 H1/H2 Pointer Types . . . 39
Table 31 Concatenation Indication Types . . . 39
Table 32 Pointer Interpreter State Diagram Transitions . . . 40
Table 33 STS Path Overhead Octets . . . 41
Table 34 RDI-P and ERDI-P Bit Settings and Interpretation . . . 44
Table 35 PMTICK Counters . . . 46
Table 36 Defects and Anomalies . . . 47
Table 37 TOSI/ROSI Addresses . . . 50
Table 38 Control Codes . . . 54
Table 39 Checker Status Bits . . . 57
Table 40 Status Register States . . . 57
Table 41 Failover Modes . . . 62
Table 42 Technology Ability Field . . . 65
Table 43 Auto-negotiation Timers . . . 67
Table 44 Advertised Ability Fields . . . 67
Table 45 Training Frame Lengths . . . 69
Table 46 Local Transmitter Equalization Registers and Bits . . . 69
Table 47 Coefficient Update Field . . . 69
Table 48 Increment/Decrement Register States . . . 70
Table 49 Status Report Field . . . 71
Table 50 Register Settings for Training . . . 72
Table 51 1x8097 (Shadowed to 1x0097) . . . 73
Table 52 Tx Output Waveform Requirements by Coefficient Update . . . 74
Table 53 Tx Output Waveform Requirements by Coefficient Status . . . 75
Table 54 System Loopback Summary . . . 76

Table 55 Network Loopback Summary . . . 76
Table 56 MDIO Port Addresses Per Channel . . . 79
Table 57 Management Frame Format for Indirect Register Access . . . 79
Table 58 MDIO Register Address to RAM Address Mapping . . . 81
Table 59 JTAG Instruction Codes . . . 84
Table 60 Operating Modes for Pin Control . . . 85
Table 61 GPIO Functions . . . 88
Table 62 Rx PCS Activity Monitor States . . . 91
Table 63 Tx PCS Activity Monitor States . . . 92
Table 64 Temperature Monitor . . . 92
Table 65 Digital Temperature Monitor Control Register . . . 93
Table 66 Temperature Alarm Threshold Register . . . 93
Table 67 Temperature Alarm Register . . . 93
Table 68 Device ID (1Ex0000) . . . 94
Table 69 Device Revision (1Ex0001) . . . 94
Table 70 Block Level Software Reset (1Ex0002) . . . 94
Table 71 Failover Crosspoint Control (1Ex0003) . . . 96
Table 72 Timer Control (1Ex0004) . . . 96
Table 73 GPIO 0 Config/ Status (1Ex0100) . . . 97
Table 74 GPIO 0 Config2 (1Ex0101) . . . 98
Table 75 GPIO 1 Config/ Status (1Ex0102) . . . 100
Table 76 GPIO 1 Config2 (1Ex0103) . . . 101
Table 77 GPIO 2 Config/ Status (1Ex0104) . . . 103
Table 78 GPIO 2 Config2 (1Ex0105) . . . 104
Table 79 GPIO 3 Config/ Status (1Ex0106) . . . 106
Table 80 GPIO 3 Config2 (1Ex0107) . . . 107
Table 81 GPIO 4 Config/ Status (1Ex0108) . . . 109
Table 82 GPIO 4 Config2 (1Ex0109) . . . 110
Table 83 GPIO 5 Config/ Status (1Ex010A) . . . 112
Table 84 GPIO 5 Config2 (1Ex010B) . . . 113
Table 85 GPIO 6 Config/ Status (1Ex010C) . . . 115
Table 86 GPIO 6 Config2 (1Ex010D) . . . 116
Table 87 GPIO 7 Config/ Status (1Ex010E) . . . 118
Table 88 GPIO 7 Config2 (1Ex010F) . . . 119
Table 89 GPIO 8 Config/ Status (1Ex0110) . . . 121
Table 90 GPIO 8 Config2 (1Ex0111) . . . 122
Table 91 GPIO 9 Config/ Status (1Ex0112) . . . 124
Table 92 GPIO 9 Config2 (1Ex0113) . . . 125
Table 93 GPIO 10 Config/ Status (1Ex0114) . . . 127
Table 94 GPIO 10 Config2 (1Ex0115) . . . 128
Table 95 GPIO 11 Config/ Status (1Ex0116) . . . 130
Table 96 GPIO 11 Config2 (1Ex0117) . . . 131
Table 97 GPIO 12 Config/ Status (1Ex0118) . . . 133
Table 98 GPIO 12 Config2 (1Ex0119) . . . 134
Table 99 GPIO 13 Config/ Status (1Ex011A) . . . 136
Table 100 GPIO 13 Config2 (1Ex011B) . . . 137
Table 101 GPIO 14 Config/ Status (1Ex011C) . . . 139
Table 102 GPIO 14 Config2 (1Ex011D) . . . 140
Table 103 GPIO 15 Config/ Status (1Ex011E) . . . 142
Table 104 GPIO 15 Config2 (1Ex011F) . . . 143
Table 105 GPIO 16 Config/ Status (1Ex0120) . . . 145
Table 106 GPIO 16 Config2 (1Ex0121) . . . 146
Table 107 GPIO 17 Config/ Status (1Ex0122) . . . 148
Table 108 GPIO 17 Config2 (1Ex0123) . . . 149
Table 109 GPIO 18 Config/ Status (1Ex0124) . . . 151
Table 110 GPIO 18 Config2 (1Ex0125) . . . 152
Table 111 GPIO 19 Config/ Status (1Ex0126) . . . 153
Table 112 GPIO 19 Config2 (1Ex0127) . . . 155
Table 113 GPIO 20 Config/ Status (1Ex0128) . . . 157

Table 114 GPIO 20 Config2 (1Ex0129) . . . 158
Table 115 GPIO 21 Config/ Status (1Ex012A) . . . 160
Table 116 GPIO 21 Config2 (1Ex012B) . . . 161
Table 117 GPIO 22 Config/ Status (1Ex012C) . . . 163
Table 118 GPIO 22 Config2 (1Ex012D) . . . 164
Table 119 GPIO 23 Config/ Status (1Ex012E) . . . 166
Table 120 GPIO 23 Config2 (1Ex012F) . . . 167
Table 121 PMA Global Spare Control 0 (1Ex7F00) . . . 168
Table 122 PMA Global Spare Control 1 (1Ex7F01) . . . 169
Table 123 PMA Global Spare Status 0 (1Ex7F02) . . . 169
Table 124 PMA Global Refclk Select (1Ex7F10) . . . 169
Table 125 PMA Global Refclk CMU Control (1Ex7F11) . . . 170
Table 126 Factory Test Register (1Ex7FD4) . . . 170
Table 127 Temperature Monitor Threshold Settings (1Ex7FD5) . . . 170
Table 128 Temperature Monitor Regs (1Ex7FD6) . . . 171
Table 129 Factory Test Only (1Ex7FD7) . . . 171
Table 130 Checksum Control (1Ex7FE0) . . . 171
Table 131 Watchdog Counter (1Ex7FE1) . . . 172
Table 132 PMA_CTRL1: PMA Control 1 (1x0000) . . . 172
Table 133 PMA_STAT1: PMA Status 1 (1x0001) . . . 173
Table 134 PMA Device Identifier 1 (1x0002) . . . 173
Table 135 PMA Device Identifier 2 (1x0003) . . . 174
Table 136 PMA/PMD Speed Ability (1x0004) . . . 174
Table 137 PMA/PMD Devices in Package (1x0005) . . . 174
Table 138 PMA/PMD Devices in Package (1x0006) . . . 174
Table 139 PMA/PMD Control 2 (1x0007) . . . 175
Table 140 PMA/PMD Status 2 (1x0008) . . . 175
Table 141 PMD Transmit Disable (1x0009) . . . 176
Table 142 PMD Receive Signal Detect (1x000A) . . . 177
Table 143 PMA/PMD Package Identifier (1x000E) . . . 177
Table 144 PMA/PMD Package Identifier (1x000F) . . . 177
Table 145 KR Training Control (1x0096) . . . 177
Table 146 KR Training Status (1x0097) . . . 177
Table 147 KR Training LP Coeff Update (1x0098) . . . 178
Table 148 KR Training LP Status Report (1x0099) . . . 178
Table 149 KR Training LD Coeff Update (1x009A) . . . 178
Table 150 KR Training LD Status Report (1x009B) . . . 179
Table 151 KR Training Status (from Firmware) (1x8097) . . . 179
Table 152 KR Training LD Coeff Update (from Firmware) (1x809A) . . . 179
Table 153 KR Training Control 2 (1x8201) . . . 180
Table 154 KR Training Status 2 (1x8208) . . . 180
Table 155 KR Training Pattern Error Count (1x8209) . . . 180
Table 156 KR Training Frames Counted (1x820A) . . . 181
Table 157 KR Training Frames to Count (1x820B) . . . 181
Table 158 KR Training wait_timer Setting (1x820C) . . . 181
Table 159 KR Training max_wait_timer Setting 1 (1x820D) . . . 181
Table 160 KR Training max_wait_timer Setting 2 (1x820E) . . . 181
Table 161 KR FEC Ability (1x00AA) . . . 181
Table 162 KR FEC Control 1 (1x00AB) . . . 181
Table 163 KR FEC Corrected Lower (1x00AC) . . . 182
Table 164 KR FEC Corrected Upper (1x00AD) . . . 182
Table 165 KR FEC Uncorrected Lower (1x00AE) . . . 182
Table 166 KR FEC Uncorrected Upper (1x00AF) . . . 182
Table 167 KR FEC Control 2 (1x8300) . . . 182
Table 168 PMA_reset_LH (1x8000) . . . 183
Table 169 PMA_TXSTAT: PMA Tx Status (1x8001) . . . 183
Table 170 PMA_RXSTAT: PMA Rx Status (1x8002) . . . 183
Table 171 PMA_RXEDCCTRL: PMA Rx EDC Control (1x8003) . . . 183
Table 172 PMA_RXDATACTRL: PMA Rx Data Control (1x8004) . . . 184

Table 173 PMA_FIFOCTRL: PMA FIFO Control (1x8011) . . . 184
Table 174 PMA_TXDATACTRL: PMA Tx Data Control (1x8012) . . . 184
Table 175 PMA_TXOUTCTRL1: PMA Tx Output Driver Control 1 (1x8013) . . . 185
Table 176 PMA_TXOUTCTRL2: PMA Tx Output Driver Control 2 (1x8014) . . . 185
Table 177 PMA_TXRATECTRL: PMA Tx Rate Control (1x8015) . . . 185
Table 178 PMA_TXRATECTRL: PMA Tx Rate Control (1x8017) . . . 185
Table 179 PMA_TXRATECTRL: PMA Tx Rate Control (1x8018) . . . 186
Table 180 PMA_RXRATECTRL: PMA Rx Rate Control (1x8019) . . . 186
Table 181 Factory Test Register (1x8030) . . . 186
Table 182 Factory Test Register (1x8031) . . . 187
Table 183 Factory Test Register (1x8034) . . . 187
Table 184 Factory Test Register (1x8035) . . . 187
Table 185 Factory Test Register (1x8036) . . . 187
Table 186 Factory Test Register (1x8037) . . . 187
Table 187 Factory Test Register (1x8038) . . . 187
Table 188 Factory Test Register (1x8039) . . . 187
Table 189 Factory Test Register (1x803A) . . . 188
Table 190 Factory Test Register (1x803B) . . . 188
Table 191 LOS Status (1x8141) . . . 188
Table 192 LOS_Detection_Source (1x8142) . . . 188
Table 193 Factory Test Register (1x8151) . . . 188
Table 194 Driver Coeff PRESET Settings for CM1 (1x8210) . . . 189
Table 195 Driver Coeff PRESET Settings for C0 and CP1 (1x8211) . . . 189
Table 196 Driver Coeff INITIALIZE Settings for CM1 (1x8212) . . . 189
Table 197 Driver Coeff INITIALIZE Settings for C0 and CP1 (1x8213) . . . 189
Table 198 Driver Coeff Step Size (1x8214) . . . 189
Table 199 RX_ALARM Control Register (1x9000) . . . 190
Table 200 TX_ALARM Control Register (1x9001) . . . 190
Table 201 RX_ALARM Status Register (1x9003) . . . 190
Table 202 TX_ALARM Status Register (1x9004) . . . 191
Table 203 Rx Clock Output Control (1xA008) . . . 191
Table 204 Tx Clock Output Control (1xA009) . . . 192
Table 205 Vendor Specific PMA Control 2 (1xA100) . . . 192
Table 206 Vendor Specific PMA Status 2 (1xA101) . . . 193
Table 207 Vendor Specific LOPC Status (1xA200) . . . 193
Table 208 Vendor Specific LOPC Control (1xA201) . . . 194
Table 209 Reset (1xAE00) . . . 194
Table 210 WIS_CTRL1: WIS Control 1 (2x0000) . . . 195
Table 211 WIS_STAT1: WIS Status 1 (2x0001) . . . 196
Table 212 WIS_DEVID1: WIS Device Identifier 1 (2x0002) . . . 196
Table 213 WIS_DEVID2: WIS Device Identifier 2 (2x0003) . . . 196
Table 214 WIS_SPEED: WIS Speed Capability (2x0004) . . . 196
Table 215 WIS_DEVPKG1: WIS Devices in Package 1 (2x0005) . . . 197
Table 216 WIS_DEVPKG2: WIS Devices in Package 2 (2x0006) . . . 197
Table 217 WIS_CTRL2: WIS Control 2 (2x0007) . . . 197
Table 218 WIS_STAT2: WIS Status 2 (2x0008) . . . 198
Table 219 WIS_TSTPAT_CNT: WIS Test Pattern Error Counter (2x0009) . . . 199
Table 220 WIS_PKGID1: WIS Package Identifier 1 (2x000E) . . . 199
Table 221 WIS_PKGID2: WIS Package Identifier 2 (2x000F) . . . 199
Table 222 WIS_STAT3: WIS Status 3 (2x0021) . . . 199
Table 223 WIS_REI_CNT: WIS Far-End Path Block Error Count (2x0025) . . . 200
Table 224 WIS_TXJ1: WIS Tx J1s (Octets 13-0) (2x0027-002D) . . . 200
Table 225 WIS_TXJ1B: WIS Tx J1s (Octets 15-14) (2x002E) . . . 201
Table 226 WIS_RXJ1: WIS Rx J1s (Octets 15-0) (2x002F-0036) . . . 201
Table 227 WIS_REIL_CNT1: WIS Far-End Line BIP Errors 1 (2x0037) . . . 202
Table 228 WIS_REIL_CNT0: WIS Far-End Line BIP Errors 0 (2x0038) . . . 202
Table 229 WIS_B2_CNT1: WIS L-BIP Error Count 1 (2x0039) . . . 203
Table 230 WIS_B2_CNT0: WIS L-BIP Error Count 0 (2x003A) . . . 203
Table 231 WIS_B3_CNT: WIS P-BIP Block Error Count (2x003B) . . . 203

Table 232 WIS_B1_CNT: WIS S-BIP Error Count (2x003C) . . . 203
Table 233 WIS_TXJ0: WIS Tx J0s (Octets 13-0) (2x0040-0046) . . . 204
Table 234 WIS_TXJ0B: WIS Tx J0s (Octets 15-14) (2x0047) . . . 204
Table 235 WIS_RXJ0: WIS Rx J0s (2x0048-004F) . . . 205
Table 236 EWIS_TXCTRL1: WIS Vendor Specific Tx Control 1 (2xE5FF) . . . 205
Table 237 EWIS_TXCTRL2: WIS Vendor Specific Tx Control 2 (2xE600) . . . 205
Table 238 Factory Test Register (2xE601) . . . 206
Table 239 Factory Test Register (2xE602) . . . 206
Table 240 Factory Test Register (2xE603) . . . 207
Table 241 Factory Test Register (2xE604) . . . 207
Table 242 Factory Test Register (2xE605) . . . 207
Table 243 Factory Test Register (2xE606) . . . 207
Table 244 EWIS_TX_A1_A2: E-WIS Tx A1/A2 Octets (2xE611) . . . 207
Table 245 EWIS_TX_Z0_E1: E-WIS Tx Z0/E1 Octets (2xE612) . . . 207
Table 246 EWIS_TX_F1_D1: E-WIS Tx F1/D1 Octets (2xE613) . . . 208
Table 247 EWIS_TX_D2_D3: E-WIS Tx D2/D3 Octets (2xE614) . . . 208
Table 248 EWIS_TX_C2_H1: E-WIS Tx C2/H1 Octets (2xE615) . . . 208
Table 249 EWIS_TX_H2_H3: E-WIS Tx H2/H3 Octets (2xE616) . . . 208
Table 250 EWIS_TX_G1_K1: E-WIS Tx G1/K1 Octets (2xE617) . . . 208
Table 251 EWIS_TX_K2_F2: E-WIS Tx K2/F2 Octets (2xE618) . . . 209
Table 252 EWIS_TX_D4_D5: E-WIS Tx D4/D5 Octets (2xE619) . . . 209
Table 253 EWIS_TX_D6_H4: E-WIS Tx D6/H4 Octets (2xE61A) . . . 209
Table 254 EWIS_TX_D7_D8: E-WIS Tx D7/D8 Octets (2xE61B) . . . 209
Table 255 EWIS_TX_D9_Z3: E-WIS Tx D9/Z3 Octets (2xE61C) . . . 209
Table 256 EWIS_TX_D10_D11: E-WIS Tx D10/D11 Octets (2xE61D) . . . 210
Table 257 EWIS_TX_D12_Z4: E-WIS Tx D12/Z4 Octets (2xE61E) . . . 210
Table 258 EWIS_TX_S1_Z1: E-WIS Tx S1/Z1 Octets (2xE61F) . . . 210
Table 259 EWIS_TX_Z2_E2: E-WIS Tx Z2/E2 Octets (2xE620) . . . 210
Table 260 EWIS_TX_N1: E-WIS Tx N1 Octet (2xE621) . . . 210
Table 261 Reserved (2xE622) . . . 211
Table 262 EWIS_TX_MSGLEN: E-WIS Tx Trace Message Length Control (2xE700) . . . 211
Table 263 EWIS_TXJ0: E-WIS Tx J0s 16-63 (2xE800-E817) . . . 211
Table 264 EWIS_RXJ0: E-WIS Rx J0s 16-63 (2xE900-E917) . . . 212
Table 265 EWIS_TXJ1: E-WIS Tx WIS J1s 16-63 (2xEA00-EA17) . . . 212
Table 266 EWIS_RXJ1: E-WIS Rx J1s 16-63 (2xEB00-EB17) . . . 212
Table 267 EWIS_RX_FRM_CTRL1: E-WIS Rx Framer Control 1 (2xEC00) . . . 213
Table 268 EWIS_RX_FRM_CTRL2: E-WIS Rx Framer Control 2 (2xEC01) . . . 213
Table 269 EWIS_LOF_CTRL1: E-WIS Loss of Frame Control 1 (2xEC02) . . . 214
Table 270 EWIS_LOF_CTRL2: E-WIS Loss of Frame Control 2 (2xEC03) . . . 214
Table 271 EWIS_RX_CTRL1: E-WIS Rx Control 1 (2xEC10) . . . 215
Table 272 EWIS_RX_MSGLEN: E-WIS Rx Trace Message Length Control (2xEC20) . . . 215
Table 273 EWIS_RX_ERR_FRC1: E-WIS Rx Error Force Control 1 (2xEC30) . . . 216
Table 274 EWIS_RX_ERR_FRC2: E-WIS Rx Error Force Control 2 (2xEC31) . . . 217
Table 275 EWIS_MODE_CTRL: E-WIS Mode Control (2xEC40) . . . 218
Table 276 Factory Test Register (2xEC41) . . . 219
Table 277 EWIS_PRBS31_ANA_CTRL: E-WIS PRBS31 Analyzer Control (2xEC50) . . . 219
Table 278 EWIS_PRBS31_ANA_STAT: E-WIS PRBS31 Analyzer Status (2xEC51) . . . 219
Table 279 EWIS_PMTICK_CTRL: E-WIS Performance Monitor Control (2xEC60) . . . 220
Table 280 EWIS_CNT_CFG: E-WIS Counter Configuration (2xEC61) . . . 221
Table 281 EWIS_CNT_STAT: E-WIS Counter Status (2xEC62) . . . 221
Table 282 EWIS_REIP_CNT1: E-WIS P-REI Counter 1 (MSW) (2xEC80) . . . 222
Table 283 EWIS_REIP_CNT0: E-WIS P-REI Counter 0 (LSW) (2xEC81) . . . 222
Table 284 EWIS_REIL_CNT1: E-WIS L-REI Counter 1 (MSW) (2xEC90) . . . 222
Table 285 EWIS_REIL_CNT0: E-WIS L-REI Counter 0 (LSW) (2xEC91) . . . 222
Table 286 B2 Rx debug (2xECA0) . . . 222
Table 287 EWIS_B1_ERR_CNT1: E-WIS S-BIP Error Counter 1 (MSW) (2xECB0) . . . 223
Table 288 EWIS_B1_ERR_CNT0: E-WIS S-BIP Error Counter 0 (LSW) (2xECB1) . . . 223
Table 289 EWIS_B2_ERR_CNT1: E-WIS L-BIP Error Counter 1 (MSW) (2xECB2) . . . 223
Table 290 EWIS_B2_ERR_CNT0: E-WIS L-BIP Error Counter 0 (LSW) (2xECB3) . . . 223

Table 291 EWIS_B3_ERR_CNT1: E-WIS P-BIP Error Counter 1 (MSW) (2xECB4) . . . 223
Table 292 EWIS_B3_ERR_CNT0: E-WIS P-BIP Error Counter 0 (LSW) (2xECB5) . . . 224
Table 293 Framer Debug 1 (2xED00) . . . 224
Table 294 Framer Debug 2 (2xED01) . . . 224
Table 295 Framer Debug 3 (2xED02) . . . 224
Table 296 Framer Debug 4 (2xED03) . . . 224
Table 297 Framer Debug 5 (2xED04) . . . 224
Table 298 Rx SPE Debug Bus 1 (2xED05) . . . 224
Table 299 Rx SPE Debug Bus 1 (2xED06) . . . 225
Table 300 Rx SPE Debug Bus 2 (2xED07) . . . 225
Table 301 Rx SPE Debug Bus 2 (2xED08) . . . 225
Table 302 EWIS_RXTX_CTRL: E-WIS Rx to Tx Control (2xEDFF) . . . 225
Table 303 EWIS_INTR_PEND1: E-WIS Interrupt Pending 1 (2xEE00) . . . 226
Table 304 EWIS_INTR_MASKA_1: E-WIS Interrupt Mask A 1 (2xEE01) . . . 227
Table 305 EWIS_INTR_MASKB_1: E-WIS Interrupt Mask B 1 (2xEE02) . . . 229
Table 306 EWIS_INTR_STAT2: E-WIS Interrupt Status 2 (2xEE03) . . . 230
Table 307 EWIS_INTR_PEND2: E-WIS Interrupt Pending 2 (2xEE04) . . . 231
Table 308 EWIS_INTR_MASKA_2: E-WIS Interrupt Mask A 2 (2xEE05) . . . 233
Table 309 EWIS_INTR_MASKB_2: E-WIS Interrupt Mask B 2 (2xEE06) . . . 234
Table 310 WIS_FAULT_MASK (2xEE07) . . . 236
Table 311 EWIS_INTR_PEND2: E-WIS Interrupt Pending 3 (2xEE08) . . . 237
Table 312 EWIS_INTR_MASKA_3: E-WIS Interrupt Mask A 3 (2xEE09) . . . 237
Table 313 EWIS_INTR_MASKB_3: E-WIS Interrupt Mask B 3 (2xEE0A) . . . 238
Table 314 Threshold Error Status (2xEE0B) . . . 238
Table 315 WIS REI-P Threshold Level 1 (2xEE10) . . . 239
Table 316 WIS REI-P Threshold Level 2 (2xEE11) . . . 240
Table 317 WIS REI-L Threshold Level 1 (2xEE12) . . . 240
Table 318 WIS REI-L Threshold Level 2 (2xEE13) . . . 240
Table 319 WIS B1 Threshold Level 1 (2xEE14) . . . 240
Table 320 WIS B1 Threshold Level 2 (2xEE15) . . . 240
Table 321 WIS B2 Threshold Level 1 (2xEE16) . . . 241
Table 322 WIS B2 Threshold Level 2 (2xEE17) . . . 241
Table 323 WIS B3 Threshold Level 1 (2xEE18) . . . 241
Table 324 WIS B3 Threshold Level 2 (2xEE19) . . . 241
Table 325 Factory Test Registers (2xEF00 to 2xEF15) . . . 241
Table 326 PCS_CTRL1: PCS Control 1 (3x0000) . . . 241
Table 327 PCS Status 1 (3x0001) . . . 242
Table 328 PCS Device Identifier 1 (3x0002) . . . 243
Table 329 PCS Device Identifier 2 (3x0003) . . . 243
Table 330 PCS Speed Ability (3x0004) . . . 243
Table 331 PCS Devices in Package (3x0005) . . . 243
Table 332 PCS Devices in Package (3x0006) . . . 244
Table 333 PCS Control 2 Register (3x0007) . . . 244
Table 334 PCS Status 2 Register (3x0008) . . . 244
Table 335 PCS Package Identifier (3x000E) . . . 245
Table 336 PCS Package Identifier (3x000F) . . . 245
Table 337 10GBASE-X Status (3x0018) . . . 245
Table 338 10GBASE-X Control (3x0019) . . . 245
Table 339 10GBASE-R PCS Status 1 (3x0020) . . . 246
Table 340 10GBASE-R PCS Status 2 (3x0021) . . . 246
Table 341 10GBASE-R PCS Test Pattern Seed A 3 (3x0022) . . . 246
Table 342 10GBASE-R PCS Test Pattern Seed A 2 (3x0023) . . . 246
Table 343 10GBASE-R PCS Test Pattern Seed A 2 (3x0024) . . . 247
Table 344 10GBASE-R PCS Test Pattern Seed A 2 (3x0025) . . . 247
Table 345 10GBASE-R PCS Test Pattern Seed B 3 (3x0026) . . . 247
Table 346 10GBASE-R PCS Test Pattern Seed B 2 (3x0027) . . . 247
Table 347 10GBASE-R PCS Test Pattern Seed B 1 (3x0028) . . . 247
Table 348 10GBASE-R PCS Test Pattern Seed B 0 (3x0029) . . . 247
Table 349 10GBASE-R PCS Test Pattern Control (3x002A) . . . 248

Table 350 10GBASE-R PCS Test Pattern Counter (3x002B) . . . 248
Table 351 Vendor Specific USR Test (3x8000) . . . 248
Table 352 Vendor Specific USR Test (3x8001) . . . 249
Table 353 Vendor Specific USR Test (3x8002) . . . 249
Table 354 Vendor Specific USR Test (3x8003) . . . 249
Table 355 Square Wave Pulse Width (3x8004) . . . 249
Table 356 Vendor Specific PCS Control (3x8005) . . . 249
Table 357 Vendor Specific Test Error Counter 0 (3x8007) . . . 250
Table 358 Vendor Specific Test Error Counter 1 (3x8008) . . . 250
Table 359 Factory Test Only (3x8009) . . . 251
Table 360 Factory Test Only (3x800C) . . . 251
Table 361 Factory Test Only (3x800D) . . . 251
Table 362 Factory Test Only (3x800E) . . . 251
Table 363 Factory Test Only (3x800F) . . . 251
Table 364 Factory Test Only (3x8010) . . . 251
Table 365 Factory Test Only (3x8011) . . . 251
Table 366 Factory Test Only (3x8012) . . . 251
Table 367 Factory Test Only (3x8013) . . . 252
Table 368 Factory Test Only (3x8014) . . . 252
Table 369 Factory Test Only (3x8015) . . . 252
Table 370 Loopback FIFOs Stat/Ctrl (3x8016) . . . 252
Table 371 Vendor Specific PCS 1G BIST Control (3x8200) . . . 252
Table 372 Vendor Specific PCS 1G BIST Status (3x8201) . . . 253
Table 373 (3xE600) . . . 253
Table 374 PCS BIST Control 1 (3xE61A) . . . 254
Table 375 PCS BIST Control 2 (3xE61B) . . . 254
Table 376 PCS BIST Error Counter (3xE61C) . . . 254
Table 377 PCS BIST Status (3xE61D) . . . 254
Table 378 PCS Interrupt Pending 1 (3xEE00) . . . 255
Table 379 PCS Interrupt WIS_INT0 Mask 1 (3xEE01) . . . 256
Table 380 PCS Interrupt WIS_INT1 Mask 1 (3xEE02) . . . 257
Table 381 PCS Interrupt Error Status (3xEE03) . . . 257
Table 382 Tx Sequencing Error Count Threshold (3xEE04) . . . 258
Table 383 Rx Sequencing Error Count Threshold (3xEE05) . . . 258
Table 384 Tx Block Encode Error Count Threshold (3xEE06) . . . 258
Table 385 Rx Block Encode Error Count Threshold (3xEE07) . . . 258
Table 386 Tx Character Encode Error Count Threshold (3xEE08) . . . 258
Table 387 Rx Character Encode Error Count Threshold (3xEE09) . . . 259
Table 388 FEC Fixed Error Count Threshold (3xEE0A) . . . 259
Table 389 FEC Fixed Error Count Threshold (3xEE0B) . . . 259
Table 390 FEC Unfixable Error Count Threshold (3xEE0C) . . . 259
Table 391 FEC Unfixable Error Count Threshold (3xEE0D) . . . 259
Table 392 PCS Spare Control/Status (3xEF00 to 3xEF15) . . . 259
Table 393 PHYXS_CTRL1: PHY XS Control 1 (4x0000) . . . 259
Table 394 PHYXS_STAT1: PHY XS Status1 (4x0001) . . . 260
Table 395 PHYXS_DEVID1: PHY XS Device Identifier 1 (4x0002) . . . 261
Table 396 PHYXS_DEVID2: PHY XS Device Identifier 2 (4x0003) . . . 261
Table 397 PHYXS_SPEED: PHY XS Speed Capability (4x0004) . . . 261
Table 398 PHYXS_DEVPKG1: PHY XS Devices in Package 1 (4x0005) . . . 261
Table 399 PHYXS_DEVPKG2: PHY XS Devices in Package 2 (4x0006) . . . 262
Table 400 PHYXS_STAT2: PHY XS Status 2 (4x0008) . . . 262
Table 401 PHYXS_PKGID1: WIS Package Identifier 1 (4x000E) . . . 263
Table 402 PHYXS_PKGID2: WIS Package Identifier 2 (4x000F) . . . 263
Table 403 PHYXS_STAT3: PHY XS Status 3 (4x0018) . . . 263
Table 404 PHYXS_TSTCTRL1: PHY XGXS Test Control 1 (4x0019) . . . 264
Table 405 PHYXS_TSTCTRL2: PHY XS Test Control 2 (4x8000) . . . 264
Table 406 PHYXS_TSTSTAT: PHY XS Test Pattern Check Status (4x8001) . . . 265
Table 407 Factory Test Register (4x8002) . . . 265
Table 408 Factory Test Register (4x8003) . . . 265

Table 409 Factory Test Register (4x8004) . . . 266
Table 410 Factory Test Register (4x8005) . . . 266
Table 411 Factory Test Register (4x8006) . . . 266
Table 412 Factory Test Register (4x8007) . . . 266
Table 413 Factory Test Register (4x8008) . . . 266
Table 414 Factory Test Register (4x8009) . . . 266
Table 415 Factory Test Register (4x800A) . . . 267
Table 416 PHYXS_TPERR_CTRL: PHY XS Test Pattern Error Counter Control (4x800B) . . . 267
Table 417 PHYXS_TPERR_CNT0: PHY XS Test Pattern Error Counter 0 (LSW) (4x800C) . . . 267
Table 418 PHYXS_TPERR_CNT0: PHY XS Test Pattern Error Counter 1 (MSW) (4x800D) . . . 267
Table 419 PHYXS_XAUI_CTRL1: PHY XS XAUI Control 1 (4x800E) . . . 267
Table 420 PHYXS_XAUI_CTRL2: PHY XS XAUI Control 2 (4x800F) . . . 268
Table 421 PHYXS_RXEQ_CTRL: PHY XS XAUI Rx Equalization Control (4x8010) . . . 269
Table 422 PHYXS_TXPE_CTRL: PHY XS XAUI Tx Pre-emphasis Control (4x8011) . . . 269
Table 423 PHYXS_RXLOS_STAT: PHY XS Rx Loss of Signal Status (4x8012) . . . 270
Table 424 PHYXS_RXSD_STAT: PHY XS Rx Signal Detect Status (4xE600) . . . 271
Table 425 Factory Test Register (4xE601) . . . 272
Table 426 PHYXS_TXPD_CTRL: PHY XS XAUI Tx Power Down Control (4xE602) . . . 272
Table 427 PHYXS_RXPD_CTRL: PHY XS XAUI Rx Power Down Control (4xE603) . . . 273
Table 428 FC_CJPAT_SEL (4xE604) . . . 274
Table 429 Factory Test Registers (4xE610 to 4xEF15) . . . 274
Table 430 Auto-Negotiation Control (7x0000) . . . 274
Table 431 AN Status (7x0001) . . . 275
Table 432 AN Advertisement Register 1 (7x0010) . . . 275
Table 433 AN Advertisement Register 2 (7x0011) . . . 275
Table 434 AN Advertisement Register 3 (7x0012) . . . 276
Table 435 AN LP Base Page Ability Register 1 (7x0013) . . . 276
Table 436 AN LP Base Page Ability Register 2 (7x0014) . . . 276
Table 437 AN LP Base Page Ability Register 3 (7x0015) . . . 276
Table 438 AN XNP Transmit Register 1 (7x0016) . . . 276
Table 439 AN XNP Transmit Register 2 (7x0017) . . . 276
Table 440 AN XNP Transmit Register 3 (7x0018) . . . 276
Table 441 AN LP XNP Ability Register 1 (7x0019) . . . 277
Table 442 AN LP XNP Ability Register 2 (7x001A) . . . 277
Table 443 AN LP XNP Ability Register 3 (7x001B) . . . 277
Table 444 BPS (7x0030) . . . 277
Table 445 Factory Test Register (7x8001) . . . 278
Table 446 Factory Test Register (7x8013) . . . 278
Table 447 Factory Test Register (7x8014) . . . 278
Table 448 Factory Test Register (7x8015) . . . 278
Table 449 Factory Test Register (7x8019) . . . 278
Table 450 Factory Test Register (7x801A) . . . 278
Table 451 Factory Test Register (7x801B) . . . 279
Table 452 Factory Test Register (7x8030) . . . 279
Table 453 Factory Test Register (7x8040) . . . 279
Table 454 Factory Test Register (7x8041) . . . 279
Table 455 Factory Test Register (7x8042) . . . 279
Table 456 Factory Test Register (7x8043) . . . 279
Table 457 Factory Test Register (7x8044) . . . 279
Table 458 Factory Test Register (7x8045) . . . 280
Table 459 Factory Test Register (7x8046) . . . 280
Table 460 Factory Test Register (7x8047) . . . 280
Table 461 Factory Test Register (7x8048) . . . 280
Table 462 AN Vendor Status (7x8100) . . . 280
Table 463 AN break_link_timer Setting 1 (7x810E) . . . 280
Table 464 AN break_link_timer Setting 2 (7x810F) . . . 280
Table 465 AN an_wait_timer Setting 1 (7x8110) . . . 281
Table 466 AN an_wait_timer Setting 2 (7x8111) . . . 281
Table 467 AN link_fail_inhibit_short_timer Setting 1 (7x8112) . . . 281

Table 468 AN link_fail_inhibit_short_timer Setting 2 (7x8113) . . . 281
Table 469 AN link_fail_inhibit_long_timer Setting 1 (7x8114) . . . 281
Table 470 AN link_fail_inhibit_long_timer Setting 2 (7x8115) . . . 281
Table 471 AN page_detect_timer Setting 1 (7x8116) . . . 281
Table 472 AN page_detect_timer Setting 2 (7x8117) . . . 281
Table 473 AN link_status_10G_timer Setting 1 (7x8118) . . . 282
Table 474 AN link_status_10G_timer Setting 2 (7x8119) . . . 282
Table 475 AN link_status_3G_timer Setting 1 (7x811A) . . . 282
Table 476 Reserved (7x811B) . . . 282
Table 477 Reserved (7x811C) . . . 282
Table 478 AN link_status_1G_timer Setting 2 (7x811D) . . . 282
Table 479 Factory Test Register (7x811E) . . . 282
Table 480 Factory Test Register (7x811F) . . . 283
Table 481 AN Hardware Arbitration State Machine State (7x8120) . . . 283
Table 482 Factory Test Register (7x8200) . . . 283
Table 483 Factory Test Register (7x8201) . . . 284
Table 484 Factory Test Register (7x8203) . . . 284
Table 485 Factory Test Register (7x8204) . . . 284
Table 486 Factory Test Register (7x8205) . . . 284
Table 487 Factory Test Register (7x8220) . . . 284
Table 488 Factory Test Register (7xEF00) . . . 285
Table 489 Factory Test Register (7xEF01) . . . 285
Table 490 Factory Test Register (7xEF02) . . . 285
Table 491 Factory Test Register (7xEF03) . . . 285
Table 492 Factory Test Register (7xEF10) . . . 285
Table 493 Factory Test Register (7xEF11) . . . 285
Table 494 Factory Test Register (7xEF12) . . . 285
Table 495 Factory Test Register (7xEF13) . . . 285
Table 496 DC_AGC_LOS Config1 (1xB0C0) . . . 286
Table 497 DC_OFF_Timer1 (1xB0C1) . . . 288
Table 498 DC_OFF_Timer2 (1xB0C2) . . . 289
Table 499 AGC_Config2 (1xB0C3) . . . 289
Table 500 AGC_Config3 (1xB0C4) . . . 289
Table 501 AGC_Config4 (1xB0C5) . . . 290
Table 502 LOS_Config2 (1xB0C6) . . . 290
Table 503 FFE DAC 0 Control (1xB000) . . . 290
Table 504 FFE DAC 1 Control (1xB002) . . . 290
Table 505 FFE DAC 2 Control (1xB004) . . . 291
Table 506 FFE DAC 3 Control (1xB006) . . . 291
Table 507 FFE DAC 4 Control (1xB008) . . . 291
Table 508 FFE DAC 5 Control (1xB00A) . . . 291
Table 509 FFE DAC 6 Control (1xB00C) . . . 292
Table 510 FFE DAC 7 Control (1xB00E) . . . 292
Table 511 FFE DAC 8 Control (1xB010) . . . 292
Table 512 DFE DAC 0 Control (1xB018) . . . 292
Table 513 DFE DAC 1 Control (1xB01A) . . . 293
Table 514 DFE DAC 2 Control (1xB01C) . . . 293
Table 515 DFE DAC 3 Control (1xB01E) . . . 293
Table 516 FFE 0 Offset Control (1xB020) . . . 293
Table 517 FFE 1 Offset Control (1xB022) . . . 294
Table 518 FFE 2 Offset Control (1xB024) . . . 294
Table 519 FFE 3 Offset Control (1xB026) . . . 294
Table 520 FFE 4 Offset Control (1xB028) . . . 295
Table 521 FFE 5 Offset Control (1xB02A) . . . 295
Table 522 FFE 6 Offset Control (1xB02C) . . . 295
Table 523 FFE 7 Offset Control (1xB02E) . . . 296
Table 524 FFE 8 Offset Control (1xB030) . . . 296
Table 525 DFE 0 Offset Control (1xB038) . . . 296
Table 526 DFE 1 Offset Control (1xB03A) . . . 297

Table 527 DFE 2 Offset Control (1xB03C) . . . 297
Table 528 DFE 3 Offset Control (1xB03E) . . . 297
Table 529 DC Sense Mux (1xB040) . . . 297
Table 530 Peak Detect (1xB042) . . . 298
Table 531 VGA0 Gain (1xB044) . . . 298
Table 532 VGA0 Boost (1xB046) . . . 298
Table 533 VGA1 Gain (1xB048) . . . 298
Table 534 VGA1 Boost (1xB04A) . . . 299
Table 535 VGA0 Offset (1xB04C) . . . 299
Table 536 VGA1 Offset (1xB04E) . . . 299
Table 537 Latch Offset (1xB050) . . . 299
Table 538 Evalue (1xB058) . . . 299
Table 539 Pattern (1xB05A) . . . 299
Table 540 Mask (1xB05C) . . . 300
Table 541 Count (1xB05E) . . . 300
Table 542 Error Sample Timing Fine Control (1xB060) . . . 300
Table 543 Error Sample Timing Coarse Control (1xB062) . . . 300
Table 544 Eoff (1xB064) . . . 300
Table 545 EPTR (1xB066) . . . 300
Table 546 ENTR (1xB068) . . . 300
Table 547 EDC Control Misc (1xB06A) . . . 300
Table 548 Ncounto1 (1xB070) . . . 301
Table 549 Ncounto2 (1xB072) . . . 301
Table 550 Ecounto1 (1xB074) . . . 301
Table 551 Ecounto2 (1xB076) . . . 301
Table 552 Ucounto1 (1xB078) . . . 301
Table 553 Dcounto1 (1xB07A) . . . 301
Table 554 (1Ex8000) . . . 302
Table 555 MDIO and LVTTL Inputs and Outputs . . . 303
Table 556 Reference Clock . . . 304
Table 557 MDIO Interface . . . 304
Table 558 SFI Input Receiver (SFI Point D) . . . 304
Table 559 Receive Path Input . . . 305
Table 560 1.25 Gbps SFI Input Jitter . . . 306
Table 561 10-Gigabit Serial Data Input for CRU . . . 307
Table 562 SONET 10G Input Jitter . . . 307
Table 563 SFI Output Driver (SFI Point B) . . . 308
Table 564 SFI Output Specifications for Jitter Performance (SFI Point B) . . . 309
Table 565 Transmit Path SFP+ Direct Attach Copper Output . . . 310
Table 566 Transmit Path KR Output . . . 310
Table 567 Transmit Path KR Output Jitter . . . 311
Table 568 Transmit Path SONET Output Jitter . . . 311
Table 569 XAUI Input . . . 311
Table 570 XAUI Output . . . 312
Table 571 Reset . . . 314
Table 572 Reference Clock . . . 314
Table 573 Two-Wire Serial Interface . . . 314
Table 574 MDIO Interface . . . 315
Table 575 Clock Output . . . 316
Table 576 Recommended Operating Conditions . . . 317
Table 577 Stress Ratings . . . 318
Table 578 Microcontroller Pins . . . 321
Table 579 JTAG Interface Pins . . . 321
Table 580 Management Interface Pins . . . 322
Table 581 Ground Pins . . . 323
Table 582 Power Supply Pins . . . 323
Table 583 Receive Path Pins . . . 324
Table 584 Reference Clock Pins . . . 324
Table 585 Clock Pins . . . 325

Table 586 Test and Mode Control Pins 325
Table 587 Transmit Path Pins 326
Table 588 XAUI Pins 326
Table 589 Reserved Pins 329
Table 590 Thermal Resistances 332
Table 591 Ordering Information 335

1 Revision History

This section describes the changes that were implemented in this document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 4.4

In revision 4.4 of this document, the XAUI LOS signal information was clarified. For more information, see Table 422, page 269 (bits 3:2) and Table 423, page 270 (bits 3:0).

1.2 Revision 4.3

The following is a summary of the changes in revision 4.3 of this document.

- The lead-free (Pb-free) package, VSC8484YJP, was added.
- Bit descriptions for bit 11 of the PHY XS Status 3 (4x0018) register were updated.
- Bit descriptions for bits 3:0 of the PHYXS_RXLOS_STAT: PHY XS Rx Loss of Signal Status (4x8012) were updated.

1.3 Revision 4.2

The following is a summary of the changes in revision 4.2 of this document.

- The block diagram was updated to reflect pin names accurately.
- The default value for the Device ID register was updated.
- Bit descriptions for the TX_ALARM Status register were updated.
- The description for Rx Clock Output Select in the Rx Clock Output Control register was updated.
- The description for Tx Clock Output Select in the Tx Clock Output Control register was updated.
- The description for LPBK_ABILITY in the PHYXS_STAT3 register was updated.
- Information about the 1Ex8000 register was added.
- Electrical specifications for the clock output swing are now specified for half swing mode and full swing mode.
- The tolerance for the package body size dimensions was corrected.

1.4 Revision 4.1

The following is a summary of the changes in revision 4.1 of this document.

- Two-wire serial (master) interface for communication with SFP+/XFP optics modules is no longer supported.
- Pin descriptions were updated to identify which optional pins may be left unconnected.
- Pin descriptions for VDTTLL and VDTTLU were updated to specify upper and lower power supplies.

1.5 Revision 4.0

The following is a summary of the changes in revision 4.0 of this document.

- Functional descriptions were clarified to better reflect device functionality. Major sections include: XAUI failover, rewriter, two-wire serial master for SFP/SFP+ monitoring, and two-wire serial slave interface.
- Termination details for the reference clock input receiver were added.
- When enabling WAN operating mode, register bits 1xAE00.2:1 must be written high to reset the Rx and Tx PCS blocks and enable valid WAN data to pass through.
- Bit descriptions for 10GBASE-KR, KR FEC, and auto-negotiation registers were modified.
- Byte order for the WIS and EWIS transmitted and received path trace message octets was updated.
- Electrical specifications were updated based on characterization results.
- MDIO timing specifications were updated.
- The relationship between the 1.8 V and 1.2 V power supplies was clarified.
- Several design guidelines were removed.

- The equation used to calculate junction temperature was removed. For more information about calculating junction temperature, contact your Microsemi representative.
- Rx loss of signal (LOS) alarm, PMA power down mode, firmware option for auto-negotiation, and Rx EDC decision threshold control features are not supported.
- LRM applications are not supported.
- Register settings to avoid PLL runaway problems were added.
- Firmware requirements for operation in environments with large temperature variations were clarified.
- Pin assignments were updated for the Reserved signals to reflect their actual locations. The pin assignments were documented correctly in all other instances, including the pin diagram, pins by number, and pins by name.

1.6 Revision 2.0

Revision 2.0 was the first publication of this document.

2 Product Overview

The VSC8484 device is a quad-channel WAN/LAN/BP (backplane) XAUI to SFP+/KR transceiver IEEE802.3ae and IEEE802.3ap standards.

The VSC8484 device is well suited for optical module, copper twinax cable, and backplane applications with its support for a wide variety of protocols, including 10 GbE LAN, 10 Gbps WAN, 40G/100G Ethernet, and 1G legacy Ethernet.

The VSC8484 device provides MDIO and two-wire serial interfaces for accessing registers. A two-wire serial (master) interface is available to load firmware from an EEPROM. Device management functions are controlled by a powerful on-device computational engine, which consists of a fully programmable microcontroller, 128 KB on-device RAM, and a bus interface unit (BIU) for communication between low-speed serial interfaces.

The microcontroller executes the EDC algorithm for fast adaptation to stressed signals and tracking variations in the incoming signal. Status and control bits in on-device registers provide monitors and signal integrity settings from various parts of the device.

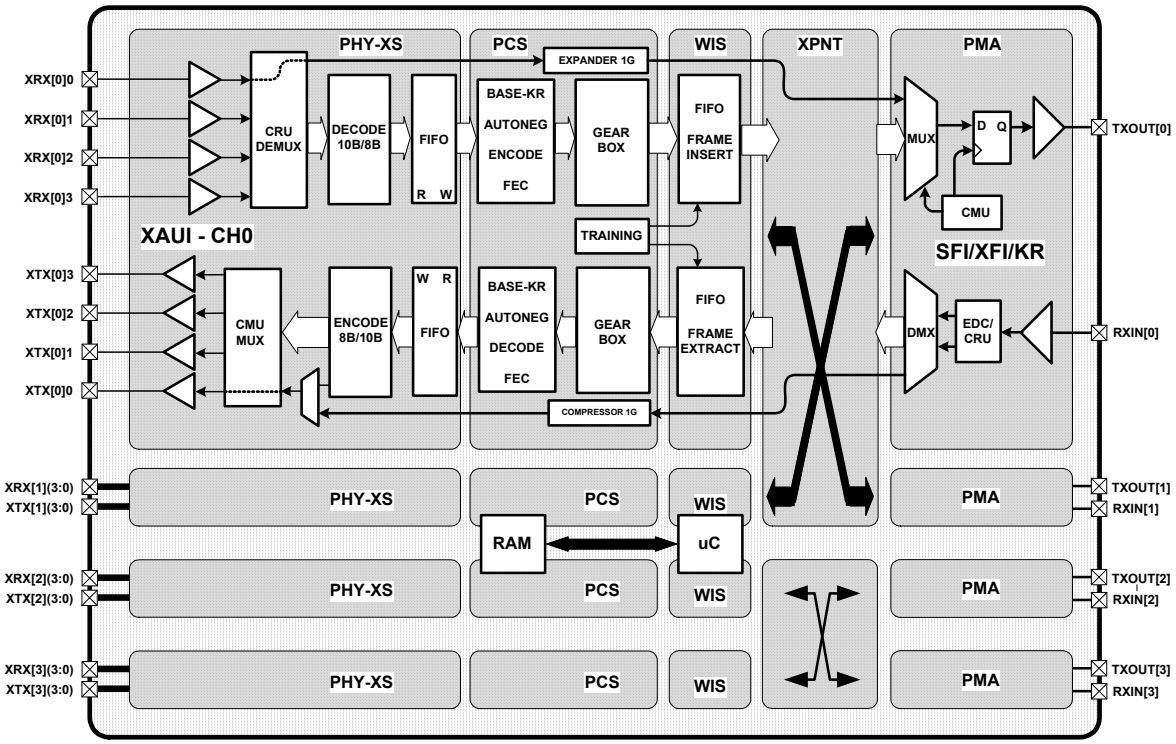
The serial side supports 1.25 Gbps and various 10 Gbps modes. Each channel consists of a receiver (Rx) and a transmitter (Tx) subsection featuring electronic dispersion compensation (EDC). Three programmable reference clock inputs (XREFCK, SREFCK, and WREFCK) support the various modes along with clock and data recovery (CDR) in the Rx and Tx subsections of all channels. Each channel of the VSC8484 device can be in a different mode within the limitations of the available reference clocks, while ensuring the Rx and Tx subsections within a channel are in the same mode.

Using a sophisticated FFE-DFE technology, the high-speed serial input receiver compensates for loss of optical and copper system performance or margin due to inter-symbol interference (ISI). The high-speed serial transmit output features a three-tap FIR filter output buffer fully compliant with the 10BASE-KR standard.

A 1.8 V and 1.2 V power supply is required for the data paths, along with an LVTTL I/O power supply selectable from 1.2 V to 3.3 V. No special power supply sequencing is required but a reset needs to be issued after stabilizing the power supplies and the device that controls the configuration pins of the VSC8484 device.

The following illustration shows a high-level block diagram for the VSC8484 device.

Figure 1 • **VSC8484 Block Diagram**



2.1 Major Applications

The VSC8484 device has the following major applications.

- 10G Ethernet line cards
- 10G backplane connections
- KR backplane to SFP+

The following illustrations show the various applications.

Figure 2 • **Backplane Equalization Application Diagram**

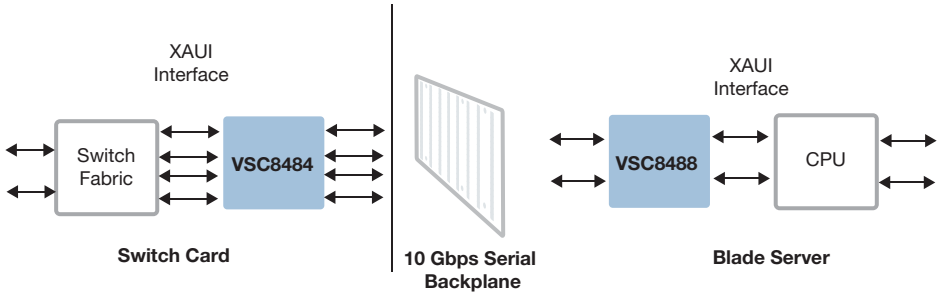
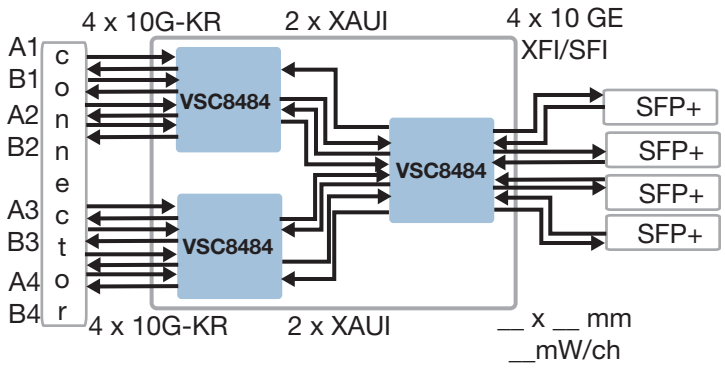


Figure 3 • **KR Backplane to SFP+ Application Diagram**



10GBASE-KR Backplane

Note: While failover with point-to-point link is supported, broadcasting mode with two copies of outputs at the same time is not supported.

2.2 Features and Benefits

The main features of the VSC8484 device are as follows:

- IEEE802.3ap, IEEE802.3ae, INF8077i, INCITS T11 10GFC, and SFF8431 electrical (SFI) specification compliant.
- 10.3125 Gbps, 9.95328 Gbps, and 1.25 Gbps pass-through.
- Supports > 220 m of FDDI grade multi-mode fiber and Cu-SFP+.
- Accessibility of the recovered clock from high-speed input and separate clock paths for CMU and CRU enable layer 1 support for synchronous Ethernet.
- Three serial interface configuration support (MDIO, two-wire serial slave, and two-wire serial master).
- Support for SR/LR/ZR and other limiting applications along with linear applications including backplanes, direct attach cable, and up to 220 m of MMF.
- XAUI failover support between channel 0 and 1 and between channel 2 and 3.
- High-speed output drivers support KR specification and SFP+ performance.
- Optional firmware to support full KR specifications including KR training.
- Embedded microcontroller with on-board RAM for flexibility and reduction in system IC count.
- VScope input signal monitoring integrated circuit for optimum eye opening and lower BER.
- Internal pattern generator and pattern checker functions, with various host-side and line-side loopbacks.
- Test clock output to a primary pin, programmable to monitor various clock domains from all channels.
- Temperature monitor with analog output readable through a primary pin, and digital output readable through registers.

3 Functional Descriptions

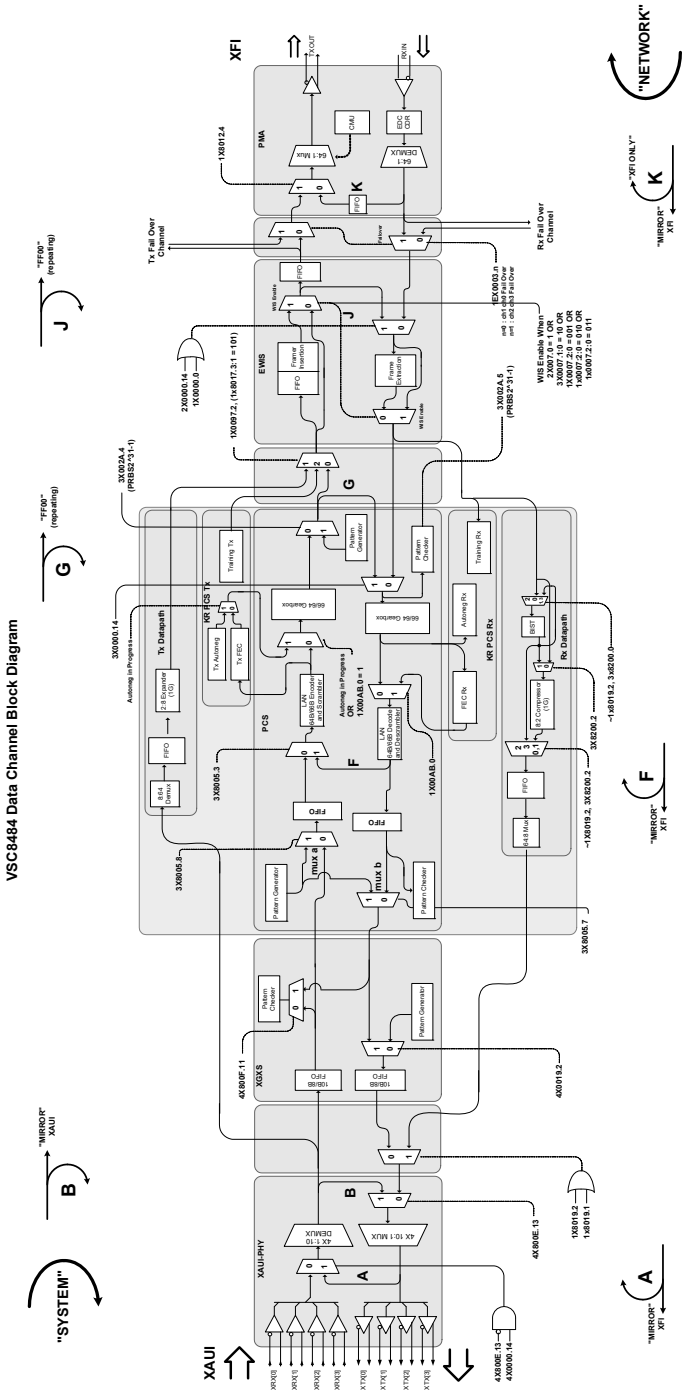
This section describes the functional aspects of the VSC8484 device, including the functional block diagram, operating modes, and major functional blocks.

The VSC8484 device has the following main sections:

- PMA
  The PMA section contains the high-speed serial I/O interfaces, an EDC circuit, a 10G CMU, and various clocking scheme circuits.
- WIS
  The WIS section contains the framing and de-framing circuits; and control and status registers to convert the data to be IEEE802.3ae WIS compliant.
- PCS
  The PCS section is composed of the PCS transmit, PCS receive, block synchronization, and BER monitor processes. The PCS functions can be further broken down into encode or decode, scramble or descramble, and gearbox functions, as well as various test and loopback modes.
- XAUI
  The XAUI section contains the 4 bit parallel XAUI I/O interface, the PHY-XS SerDes and a XAUI CMU.
- KR
  KR training and auto-negotiation support. The KR driver includes programmable equalization accomplished by a three-tap finite impulse response (FIR) structure. Three-tap delays are achieved by three flip-flops clocked by a 10 GHz clock.
- Loopback
  The loopback sections describe the different loopbacks available in the VSC8484 device, including system and network loopbacks. The various loopbacks enhance the engineering debugging and manufacturing testing capability.
- Management
  The microprocessor management section contains the core logic, the microprocessor, RAM, BIU, fail-through circuit, and the various serial management interface logic.

XAUI, PCS, WIS, and KR in each channel are identical unless otherwise specified. The following illustration shows a channel datapath block diagram of the VSC8484 device.

Figure 4 • **VSC8484 Channel Datapath Block Diagram**



3.1 Transmit Operation for XAUI to SFI Mode

The PHY XS block receives four 8B/10B encoded 3.125 Gbps (3.1875 Gbps in SAN mode) data lanes, XRX±[0:3] (XAUI interface). The clock is recovered and the data is deserialized on each of the four lanes. Synchronization is performed before the data is passed into the 10B/8B decoders. The decoded data and accompanying control bits are then presented to the FIFO. The FIFO deskews the four lanes and presents the aligned data to the PCS.

The FIFO within the PCS transfers path timing from the PHY XS recovered clock by adding or deleting idle characters during inter-packet gaps (IPG) as needed, as defined in Table 49-1 of IEEE

802.3ae-2002, to the integrated clock multiplier unit (CMU), which is driven by an external reference clock.

The eight data octets (8-bit characters) and eight control bits pass through the 64b/66b encoder, which maps XGMII data to a single 66-bit transmission block, as defined in Figure 49-7 of IEEE 802.3ae-2002.

In the PCS block, the first two bits of the 66-bit block contain the sync header, which is used to establish block boundaries for the synchronization process during the receive operation. The remaining 64 bits contain the payload. The payload passes through the scrambler, which implements the polynomial G(x) = 1 + x39 + x58. The sync header bypasses the scrambler and joins the scrambled payload at the 66:64 gearbox. The gearbox adapts between the 66-bit width of the blocks and the 64-bit width of the PMA or WIS interface.

In LAN or SAN mode (WAN_STATUS=0), the 64-bit wide data from the PCS is passed directly to the PMA. In WAN mode (WAN_STATUS=1), the 64-bit wide data is passed to the WIS. The WIS inserts the data from the PCS into SONET/SDH STS-192c frames and adds the required overhead. Within the PMA the data is serialized into the high-speed data stream (10.3125 Gbps in LAN mode, 10.51875 Gbps in SAN mode, and 9.95328 Gbps in WAN mode). The data stream and the divide by 64 clock (161.13 MHz in LAN mode, 164.35 MHz in SAN mode, and 155.52 MHz in WAN mode) are provided for line transmission on pins TXOUT± and TXCKOUT respectively.

3.2 Receive Operation for SFI to XAUI Mode

High-speed NRZ serial data is received on pins RXIN± where it can be equalized for copper trace dispersion and presented to the CRU for clock recovery.

In LAN and SAN mode, the output of the CRU is deserialized to a 64-bit bus and presented to the PCS. In WAN mode, the output of the CRU is deserialized to a 64-bit bus and presented to the WIS. The WIS extracts the data from the SONET/SDH STS-192c frames and processes the overhead. The 64-bit wide data is then presented to the PCS.

In the PCS block, the input data is presented to the 66:64 gearbox. The 66-bit block is then aligned using the embedded two-bit sync header, which generates the 64-bit payload. The payload is descrambled using the polynomial G(x) = 1 + x39 + x58. The descrambled payload and two-bit sync header pass through the 64b/66b decoder, where the block is mapped to valid XGMII data (eight octets) and control characters (eight bits).

The eight data octets and eight control bits are passed to the FIFO, where path timing is transferred from the divided (1/64) recovered clock to the divided (1/66) CMU clock. During IPG, idle characters are added or deleted as necessary to adapt between the two clock rates.

The eight data octets and eight control bits are then presented to the PHY XS block, where it is 8b/10b encoded and serialized. The serialized code words are then transmitted four at a time on the four XAUI outputs, XTX ±[0:3].

3.3 PMA

The VSC8484 PMA section consists of a receiver (Rx) and a transmitter (Tx) subsection. The receiver accepts data from the serial data input RXIN and sends the parallel data to the 64-bit parallel RXD[63:0] bit of the WIS or PCS block. A data rate clock RXCK64 (input data rate divided by 64) also accompanies the parallel data. The transmitter accepts 64-bit data from parallel TXD[63:0] bit of the WIS or PCS block and transmits at serial data output TXOUT. The transmitter subsection also provides a data rate divided by 64 clock (TXCK64).

A loopback at the 64-bit data path is also provided with a FIFO connecting the Rx and the Tx subsection. In this mode, the recovered clock from the Rx subsection is used as the reference clock for the Tx subsection forming a line timing system. The PMA also contains the Error Counter block as part of the EDC functionality.

The VSC8484 PMA also features a reference clock block that routes different reference clocks to the four-channel PMA receiver and transmitter subsection.

To support two different data rates on different channels, all three reference clock inputs, XREFCK, SREFCK, and WREFCK, are routable to all four channels of the PMA receiver subsection using two

independent paths, CRU0 and CRU1. Similarly, they are also routable to all four channels of the PMA transmitter subsection using two independent paths, CMU0 and CMU1.

Each channel's Rx and Tx then chooses the path to use as its reference clock source for Rx CRU and Tx CMU respectively. The XREFCK is always needed regardless of the device's operating mode, because it provides the clock for the internal logic including register access.

Each channel of the PMA also has two fully programmable clock outputs, TXCKOUT and RXCKOUT, that can be used to output various clock domains from the PMA.

3.3.1 Supported Data Rates and Standards

The high-speed interface is capable of operating between 9.95 Gbps and 10.52 Gbps. The following table lists the supported data rates and standards.

Table 1 • **Supported Data Rates and Standards**

Rate	Modules: XFP/SFP+	Backplane
1.25 Gbps		IEEE 802.3ap
9.95328 Gbps	IEEE 802.3ae	
10.3125 Gbps	IEEE 802.3ae IEEE 802.3aq	IEEE 803.ap
10.51875 Gbps	INCITS T11-10GFC	
4 × 10.3125 Gbps	IEEE 802.3ba	
10 × 10.3125 Gbps	IEEE 802.3ba	

3.3.2 Rate Auto-Negotiation

The VSC8484 device supports auto detection between 1.25 Gbps and 10.3125 Gbps data rates, according to the IEEE 802.3ap auto negotiation standard. The auto negotiation/auto detection feature is implemented in the firmware by polling the Rx CRU loss of lock signal and switching the CRU rate selection to different rates until the loss of lock signal indicates a lock.

Rate auto-negotiation enables devices at both ends of a link segment to advertise abilities, acknowledge receipt, and discover the common modes of operation that both devices share, and to reject the use of operational modes that are not shared by both devices. Where more than one common mode exists between the two devices, a mechanism is provided to allow the devices to resolve to a single mode of operation using a predetermined priority resolution function. The auto-negotiation function allows the devices to switch between the various operational modes in an orderly fashion, permits management to disable or enable the auto-negotiation function, and allows management to select a specific operational mode. The auto-negotiation function also provides a parallel detection function to allow backplane Ethernet devices to connect to other backplane Ethernet devices that have auto-negotiation disabled and interoperate with legacy devices that do not support clause 73 auto-negotiation.

3.3.3 Receiver (Rx) Subsection

The Rx subsection consists of a variable gain amplifier (VGA) input receiver, EDC circuitry with clock and data recovery, and a 1:64 demux. The incoming signal into the input receiver section must be SFI-compliant and conform to the specifications of SFF8431, INF8077i, or the referenced IEEE standards for 10 Gbps Ethernet applications.

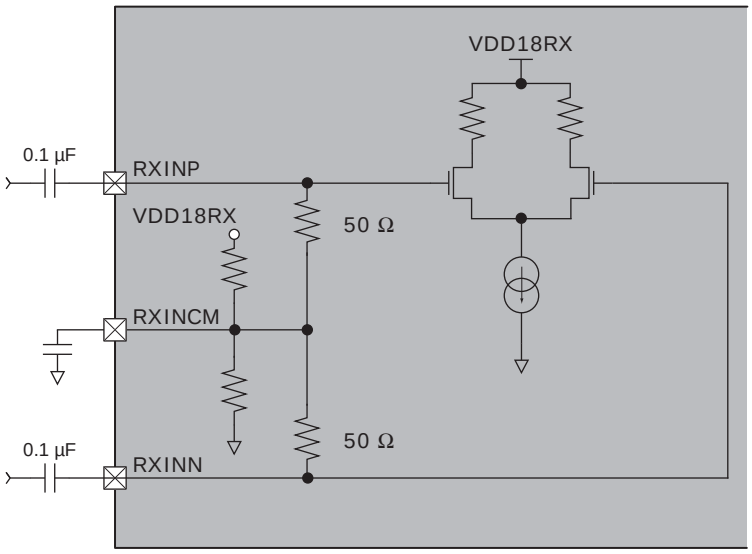
3.3.4 Variable Gain Amplifier Input Receiver

The input signal is normalized using the variable gain amplifier (VGA) and then transmitted to the equalizer core where the signal compensation occurs. The VGA provides a constant signal level to the equalizer. The optimal VGA output reference level is controlled by the firmware.

The inputs are terminated internally with 50 Ω to RXINCM. This forms a 100 Ω equivalent impedance across the differential pair to terminate the differential mode signal and a center-tapped virtual ground

brought out as the RXINCM pin to absorb common mode noise. The RXINCM pin must be AC-coupled to ground through a 0.1 µF capacitor. The following illustration shows a diagram of the Rx input receiver.

Figure 5 • **Rx Input Receiver**



3.3.5 Rx Equalizer

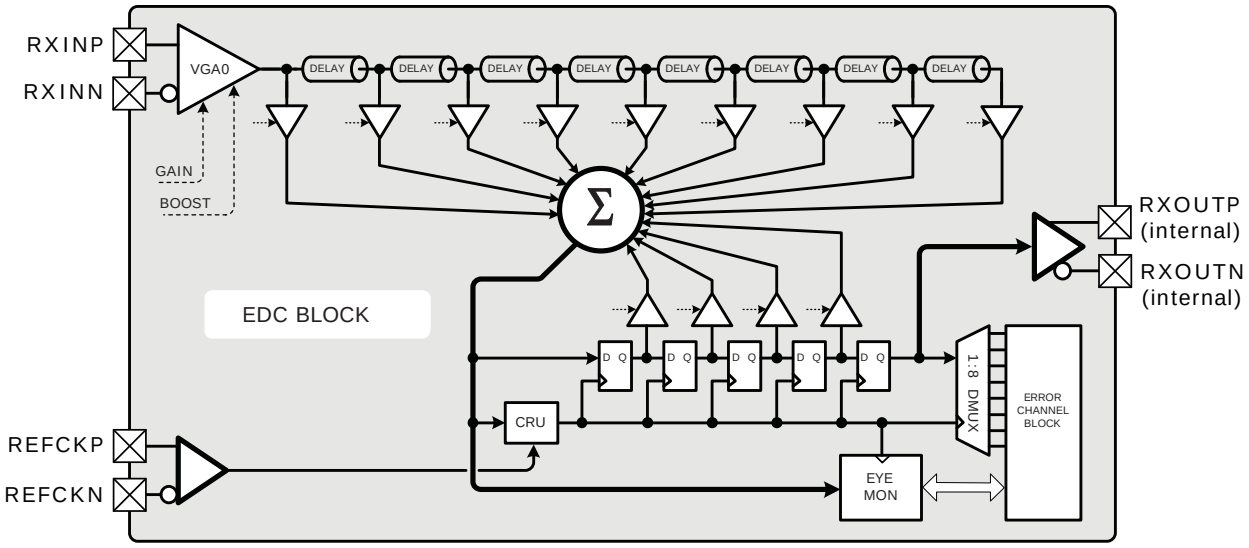
The equalizer implementation provides a high level of signal impairment compensation to ensure a robust link. In adaptive mode, the quality of the signal following the equalizer is continuously monitored, and the information is delivered to the on-device microcontroller to control the equalizer settings. The equalization algorithm optimizes FFE/DFE coefficients, AC and DC boost, and gain levels for robust performance. The algorithm is implemented by firmware. The register files provide access to various equalization settings.

The input buffer programmable equalizer can be used to compensate for the deterministic jitter. This equalization effectively reduces the ISI typically introduced by copper PCB traces. Typically for FR4 materials, low frequencies are attenuated less than high frequencies as a result of the skin effect and dielectric losses.

3.3.6 Rx Clock and Data Recovery

The Rx CDR block performs clock recovery on the incoming 10G signal from the RXIN pin. The recovered clock is used by the data recovery block to regenerate the data by sampling the output of the VGA input receiver. The data recovery section samples the waveform at the optimal phase and sets the output bit either high or low. The EDC circuit implementation automatically provides a maximally open eye at the sampling point. No manual adjustment of the sampling phase is required. The following illustration shows a diagram of the EDC block.

Figure 6 • **EDC Block Diagram**



EDC is performed in two blocks, feed forward equalization (FFE) to compensate for precursor distortion and decision feedback equalization (DFE) to compensate for post-cursor distortion. The FFE is implemented in a series of tapped delayed lines. Output of each delay line goes to a summing node. The DFE is implemented in sampling D flip-flops that sample the output of the summing node. The output of the summing node also goes to a clock recovery unit and an eye mapper/monitor block. The CRU locks the VCO frequency and phase to the incoming data. The eye mapper block changes the sampling point of the summing node output and compares it with the result of the D flip-flops sampling. Using an EDC algorithm, the eye mapper maps the incoming data eye and automatically provides the optimum FFE and DFE for maximum open eye at the sampling point. The output of the EDC blocks is data demuxed from the high-speed data input. A divided down data clock is also provided at the parallel data interface.

Under normal operating conditions, the Rx CDR is locked to the incoming high-speed data stream. The CDR can be forced to lock to the input reference clock using register PMA_RXLCK2REF. When PMA_RXLCK2REF is set high, the receiver CDR locks to the CDR reference clock. When PMA_RXLCK2REF is set low, the receiver CDR seeks to lock to the input data stream (normal operation). The following table lists the PMA_RXCLCK2REF register settings along with their results.

Table 2 • **Rx CDR Lock to Reference Settings**

PMA_RXLCK2REF Setting	Result
0 (default)	Rx CDR lock to data stream (normal operation)
1	Rx CDR lock to reference clock

The CDR provides lock-detect circuitry, which indicates whether the CDR loop has achieved proper frequency and phase lock with the incoming data. The CDR can tolerate frequency deviations between the reference clock signal and the data stream of 150 ppm. The Rx loss of lock (register PMA_RXLOL) enters an alarm state in any of the following conditions:

- No valid input signal
- Reference clock frequency and data rate differ too much
- Division ratio for the reference clock is chosen incorrectly

The following table lists the results of the Rx loss of lock detection settings.

Table 3 • **Rx Loss of Lock Detection Settings**

PMA_RXSTAT Setting	Results
0	Rx CDR Loss of Lock

Table 3 • **Rx Loss of Lock Detection Settings *(continued)***

PMA_RXSTAT Setting	Results
1 (default)	Normal operation

3.3.7 Rx Data Rate Selection

The Rx CDR supports the following data rates:

- 10.3125 Gbps LAN mode
- 9.95328 Gbps WAN mode
- 10.51875 Gbps FC mode
- 1.25 Gbps legacy gigabit Ethernet pass-through mode

Each of these modes requires a proper setting of the CDR reference clock source and the divide ratio in the CDR. The CDR reference clock is selected from two independent paths, CRU0 and CRU1, in the Reference Clock block. The CRU0 and CRU1 path can be programmed to route any one of the three reference clock inputs to the PMA. Register settings in 1Ex7F10.3:2 and 1Ex7F10.1:0 select the reference clock source for the CRU0 and CRU1 path. Register settings in 1x8019.5 then choose to either use the CRU0 or the CRU1 path as its reference clock source for each channel of the PMA Rx CDR.

The selected reference clock must have a correct clock rate according to the divide ratio setting of the CDR and the data rate setting of the CDR. Registers 1x8019.4:3 and 1x8019.2:1 determine the mode of the CDR, the data rate supported, the divide ratio, and the acceptable reference clock rate. Registers 1x8019.4:3 determine the Rx CDR divide ratio, and registers 1x8019.2:1 determine the data rate (10G or 1G).

Note: Not every combination of these registers will be valid. Be sure to exercise caution and test the settings of these two registers to ensure proper operations.

The following table summarizes the Rx CDR reference clock source selections.

Table 4 • **Rx CDR Reference Clock Source Selection**

Register	Rx CDR Reference Clock Source
0 (default)	CRU0 path
1	CRU1 path

The following table summarizes the Rx CDR divide ratio and rate selections.

Table 5 • **Rx CDR Divide Ratio and Rate Selection**

Register 1x8019.4:1	Mode	RXIN Data Rate (Gbps)	Rx CDR VCO (GHz)	Divide Ratio	Reference Clock Rate (MHz)
0100 (default)	LAN	10.3125	10.3125	66	156.25[1]
	FC	10.51875	10.51875	66	159.375
0000	LAN	10.3125	10.3125	64	161.1328125
	WAN	9.95328	9.95328	64	155.52
001x	1G	1.25	10.000	64	156.25[1]

1. The 156.25 MHz reference clock is supported in all three data rate modes, 10G and 1G. The register 1x8019.2:1 sets the Rx CDR data rate mode and must be used together with the register 1x8019.4:3 to set the Rx CDR divide ratio appropriate for the selected mode.

3.3.8 Rx Data Path Control

The RXIN data goes to a 1:64 demux, becoming a 64-bit bus. There are several settings related to the 64-bit bus from RXIN, as listed in the following table.

Table 6 • **Rx Data Bus Control**

Function	Register	Settings
Bus polarity	1x8004.2	Inverts Polarity on 64-bit bus 0: Normal (default) 1: Inverted
Data squelch	1x8004.3	Squelches 64-bit bus 0: Normal (default) 1: Squelched
MSB selection	1x8004.4	Swaps MSB of 64-bit bus 0: Disabled (MSB first). Bit 63 is MSB 1: Enabled (LSB first). Bit 0 is MSB (default)

3.3.9 External Capacitors

For loop filter control and to minimize the impact of common mode noise, especially power supply noise, the on-device CDR requires external 1.0 µF capacitors that are connected between pin RXCRUFILT and ground. These capacitors should be a multilayer ceramic dielectric with at least a 5 V working voltage rating. X7R dielectric capacitors provide better temperature stability and are recommended for this application. In addition, the RXINCM pin needs to be AC-coupled to ground using a 0.1 µF capacitor.

3.3.10 VScope Input Signal Monitoring Integrated Circuit

The VScope input signal monitoring integrated circuit displays the input signal after the input EDC chain, but before it is digitized by the CDR. There are two primary configurations, as follows:

3.3.11 Unity Gain Amplifier

The unity gain amplifier monitors the 10 Gbps input signals before signal processing and equalization.

The VScope input signal monitoring integrated circuit acts as a virtual scope to effectively observe the received data signal as presented to the EDC, before it has been processed. The autonomous adaptive filter taps must first be disabled and the front-end receiver, along with FFE tap parameters, must be set for operation as a linear, unity gain amplifier. In this mode, all DFE taps are set to zero. This mode does not require an adaptive algorithm.

3.3.12 Link Monitor

The link monitor provides the link margin after EDC signal processing.

VScope input signal monitoring integrated circuit enables design engineers and system developers to readily evaluate the effectiveness of the EDC processing capability for a given application environment. Additionally, signals can be monitored remotely without disrupting the data integrity of a live data path. By monitoring the health of a given link, optical or electrical, various types of signal degradation can be identified and corrected. This mode requires an adaptive algorithm to optimize the EDC equalizer.

3.3.13 Transmitter (Tx) Subsection

The Tx subsection consists of a 64:1 mux, a CMU, and an SFI-compliant output driver. The output buffer also supports the 10BASE-KR specifications with delay-tapped de-emphasis. The clock multiplication unit (CMU) generates the high-speed transmit clock from the various reference clock input. The on-device CMU uses a low phase noise reactance-based VCO.

The Tx CMU has a loss of lock alarm that is reported in register 1x8001.0. In the event of loss of lock the register is set to 0. The following table lists the lock status for the 1x8001.0 register settings.

Table 7 • **Tx Loss of Lock Detection Settings**

Register 1x8001.0	Tx CMU Lock Status
0	Tx CMU lock error
1 (default)	Tx CMU lock

3.3.14 Tx Data Rate Selection

An integrated clock multiplication unit generates the high-speed transmit clock from the reference clock. The CMU uses a low phase noise reactance-based VCO to ensure good jitter performance. The Tx CMU supports the following data rates:

- 10.3125 Gbps LAN mode
- 9.95328 Gbps WAN mode
- 10.51875 Gbps FC mode
- 1.25 Gbps legacy gigabit Ethernet pass-through mode

As is the case with the CDR in the Rx subsections, the proper settings on the reference clock source and the CMU divide ratio are required for proper operation. CMU0 and CMU1 are the two independent paths from the reference clock block to the Tx CMU. The Tx CMU reference clock may be on any one of the two paths (CMU0 and CMU1), the Rx CDR recovered clock, or the XAUI recovered clock. Register 1x8017.3:1 selects the source of the reference clock to the CMU. The selected reference clock must have a correct clock rate according to the divide ratio setting of the CMU (set by register 1x8017.5:4).

Note: Exercise caution when setting these two registers because not every combination of 1x8017.3:1 and 1x8017.5:4 is valid.

The following table summarizes the Tx CMU reference clock source selections.

Table 8 • **Tx CMU Reference Clock Source Selection**

Register PMA_TXREFSEL[2:0]	Tx CMU Reference Clock Source
00x	CMU0
01x (default)	CMU1
1x0	PMA Rx CDR recovered clock (divide by 64 only)
1x1	XRCVCK XAUI recovered clock (divide by 48 only)

Note: All other PMA_TXREFSEL[2:0] combinations are invalid.

The following table summarizes the Tx CMU divide ratio selections.

Table 9 • **Tx CMU Divide Ratio Selection**

Register 1x8017.5:4	Mode	TXOUT Data Rate (Gbps)	Tx CMU VCO (GHz)	Divide Ratio	Reference Clock Rate (MHz)
00 (default)	LAN	10.3125	10.3125	66	156.25
	FC	10.51875	10.51875	66	159.375
01	LAN64	10.3125	10.3125	64	161.1328125
	WAN	9.95328	9.95328	64	155.52
	1G	1.25	10	64	156.25
10	LAN16	10.3125	10.3125	16	644.53125
	WAN16	9.95328	9.95328	16	622.08

3.3.15 Tx Data Path Control

In the transmitter subsection, the 64-bit bus goes to a 64:1 mux, becoming high-speed data transmitted by the TXOUT pin. The following table summarizes the Tx transmit 64-bit bus settings.

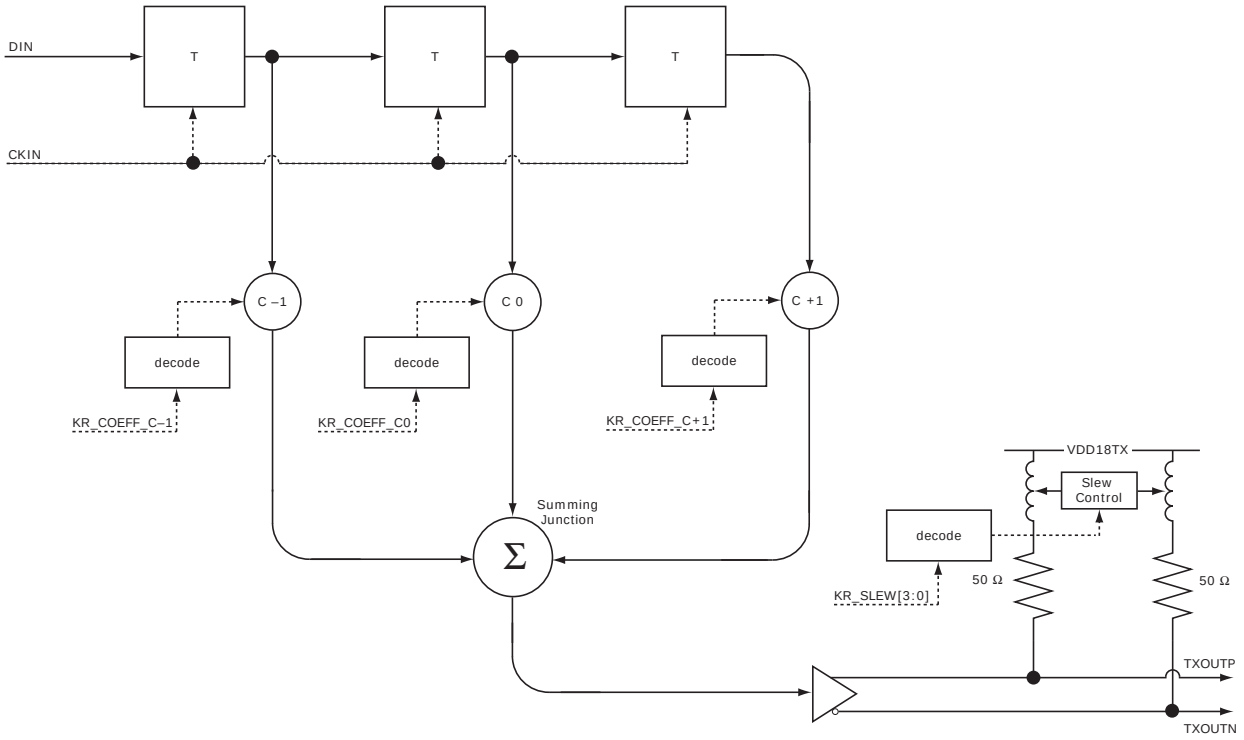
Table 10 • **Tx Transmit Data Bus Control**

Function	Register	Settings
Bus polarity	1x8012.3	Tx transmit data polarity invert 0: Normal (default) 1: Inverted
MSB selection	1x8012.2	Tx transmit data MSB select 0: No bit swapping enabled (MSB first) Bit 63 is MSB 1: Bit swapping enabled (LSB first) Bit 0 is MSB (default)
Data squelch	1x8012.1	Tx transmit manual data squelch 0: Normal 1: Squelched

3.3.16 10BASE-KR Output Driver

The high-speed output driver includes programmable equalization accomplished by a three-tap finite impulse response (FIR) structure. The three-tap delays are achieved by three flip-flops clocked by a 10 GHz clock, as shown in the following illustration. Coefficients C(–1), C(0) and C(+1) adjust the precursor, main-cursor, and post-cursor of the output waveform. The coefficients are independently adjusted by control bits 1×8013.4:0, 1×8014.12:8, and 1×8014.5:0, respectively. The bits for each coefficient are decoded in a thermometer fashion to achieve linear coefficient adjustment. The three delayed data streams, after being properly strength adjusted by their coefficients, are summed by a summing amplifier. The output driver meets the requirements defined in IEEE 802.3ap Clause 72.

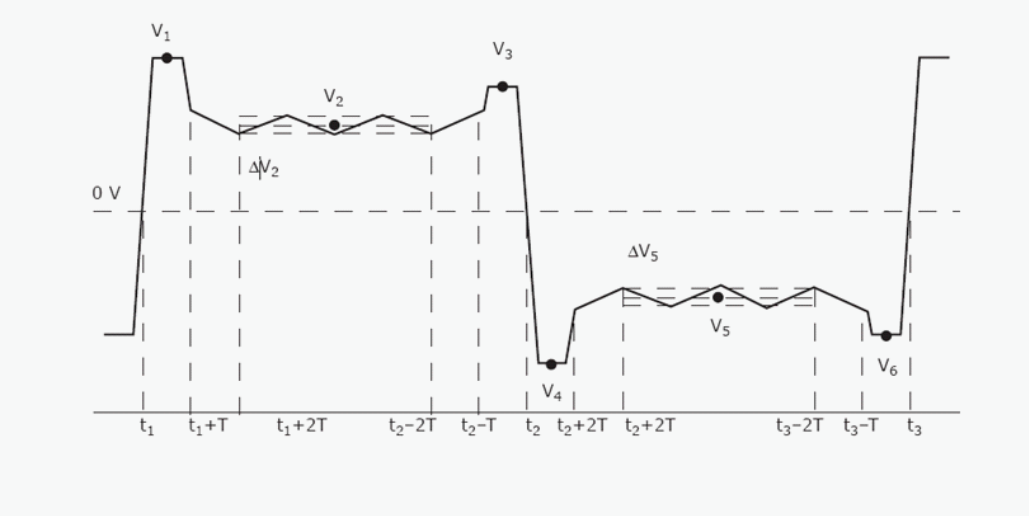
Figure 7 • **10BASE-KR Output Driver**



The final output stage has 50 Ω back-termination with inductor peaking. The output slew rate is controlled by adjusting the effectiveness of the inductors using register 1×8013.11:8.

The test pattern for the transmitter output waveform is the square wave test pattern with at least eight consecutive 1s. The following illustration shows the transmitter output waveform test, based on voltages Δ1 through Δ6, Δ2, and Δ5.

Figure 8 • **KR Test Pattern**



The output waveform is manipulated through the state of the coefficient C(-1), C(0), and C(+1). The following table lists the changes in the output waveform resulting from coefficient changes.

Table 11 • **Tx Transmit Output Waveform Changes by Coefficient Update**

Coefficient Update			**Typical Changes**		
C(+1) 63 steps 1x8014.5:0	**C(0) 31 steps 1x8014.12:8**	**C(–1) 31 steps 1x8013.4:0**	**$V_1(k) – V_1(k–1)$ mV**	**$V_2(k) – V_2(k–1)$ mV**	**$V_3(k) – V_3(k–1)$ mV**
Increment	Hold	Hold	–6.25	12.5	6.25
Decrement	Hold	Hold	6.25	–12.5	–6.25
Hold	Increment	Hold	6.25	12.5	6.25
Hold	Decrement	Hold	–6.25	–12.5	–6.25
Hold	Hold	Increment	6.25	12.5	–6.25
Hold	Hold	Decrement	–6.25	–12.5	6.25

The following table lists the adjustment ranges for the output driver slew rate control register settings.

Table 12 • **Tx Output Slew Rate Control Setting**

1x8013.11:8	**Slew Rate**
0x0	Minimum
0xF	Maximum

The rise time and fall time can be adjusted to support various data rates for Fibre Channel slew rate requirements. The following table lists the register rise time and fall time control register settings.

Table 13 • **Tx Output Driver Rise/Fall Time Control**

1x8018.7:6	**Slew Rate**
00	10G

Table 13 • **Tx Output Driver Rise/Fall Time Control**

1x8018.7:6	Slew Rate
01	Reserved
10	Reserved
11	1G

The following table lists the KR driver typical DC swing for the different combinations of tap current and slew rate settings.

Table 14 • **Tx Transmit Data Bus Control**

Slew 1x8013.11:8	C(-1) Precursor 1x8013.4:0	C(0) Main Cursor 1x8013.12:8	C(+1) Post Cursor 1x8013.5:0	Swing (mV)
0000	01111	11111	000000	400
0000	11111	11111	000000	500
0000	00000	11111	000000	300
0000	01111	11111	111111	<10

3.3.17 PMA Loopback

A loopback at 64-bit data interface from the Rx subsection to the Tx subsection is supported. This is loopback K in channel datapath block diagram. For more information, see Figure 5, page 10. To select the loopback, set register 1x8012.4 to 0. When the loopback is selected, the reference clock of the Tx CMU has to come from the recovered clock of the Rx CDR and the CMU is set in divide by 64 mode. In other words, the register 1x8017.3:1 has to be set to 1x0 and register 1x8017.5:4 has to be set to 01. The FIFO in the loopback path takes care of any phase difference between the TXD[63:0] and RXD[63:0].

Table 15 • **PMA Loopback**

Register 1x8012.4	Mode	Condition
0	Loopback Mode	1x8017.3:1 = 1x0 1x8017.5:4 = 01
1	Normal Mode	N/A

3.3.18 PMA Linetime

It is also possible to drive the PMA Tx CMU reference clock from the Rx CDR recovered clock divide by 64 without looping back the data. The Tx subsection 64-bit data is coming from TXD[63:0] from the core normally, but the Tx transmit data rate is synchronous with the Rx receive incoming data rate. This mode is known as linetime mode and is set by writing 1x0 register 1x8017.3:1 and 01 to register 1x8017.5:4 while keeping 1x8012.4 register 1.

Note: In loopback mode, the PMA has to be in linetime mode as well. However, PMA linetime mode does not necessarily means loopback mode.

Table 16 • **PMA LINETIME**

Register	Value	Mode
1x8017.3:1 1x8017.5:4 1x8012.4	1x0 01 1	Linetime mode

3.3.19 External Capacitors

For loop filter control and to minimize the impact of common mode noise, especially power supply noise, the on-device PLL require external 1.0 µF capacitors that are connected between pins CMUFILT and GND for the CMU. This capacitor should be a multilayer ceramic dielectric with at least a 5 V working voltage rating.

Note: X7R dielectric capacitors provide better temperature stability and are recommended for this application.

3.3.20 Reference Clock

There are three differential input CML level reference clocks, XREFCK, WREFCK and SREFCK. These reference clocks are managed by a reference clock block for distribution to all four channels of the Rx and Tx subsections. This block also routes the XREFCK to the core logic and to the XAUI block.

The three reference clock inputs are routable to all four channels of the PMA receiver subsections with two fully independent lines. CRU0 and CRU1. The reference clock inputs are also routable to all to all four channels of the PMA transmitter subsections with two fully independent lines, CMU0 and CMU1, as shown in the following tables.

The CRU0 and CRU1 paths can be selected to be either XREFCK, WREFCK/4, WREFCK, or SREFCK by setting registers 1Ex7F10.3:2 and 1Ex7F10.1:0. There is no SREFCK/4 choice for CRU0 and CRU1 paths. It means that the SREFCK frequency at the divide-by-16 rate is coming into the part and the Tx CMU is using the SREFCK directly and the Rx CRU cannot use the SREFCK as its reference clock source. The following table lists the register settings for the CRU0 and CRU1 paths.

Table 17 • **CRU0 and CRU1 Paths Source Selection**

Register 1Ex7F10.3:2 and 1Ex7F10.1:0	CRU0 and CRU1 Path
00 (default)	XREFCK
01	WREFCK/4
10	WREFCK
11	SREFCK

Both the CMU0 and CMU1 paths can be selected to be either XREFCK, WREFCK, or SREFCK with the optional divide by 4 for WREFCK and SREFCK. The CMU0 path is controlled by register 1Ex7F10.8:6. The CMU1 path is controlled by register 1Ex7F10.5:4. The optional divide by 4 is a circuit shared by CMU0 and CMU1. The WREFCK divide by 4 is enabled by register 1Ex7F10.10, and the SREFCK divide by 4 is enabled by register 1Ex7F10.9. The following table lists the register settings for the CMU0 path.

Table 18 • **CMU0 Path Source Selection**

Register 1Ex7F10.8:6	CMU0 Path
x0x (default)	XREFCK
x10	WREFCK
x11	SREFCK

Note: Setting 1Ex7F10.8 automatically enables the clock signal enhancer. For more information, see Figure 11, page 23. Be aware a 1.0 µF capacitor needs to be attached to the CMUFILTR pin when the clock signal enhances is enabled.

The following table lists the register settings for the CMU1 path.

Table 19 • **CMU1 Path Source Selection**

Register 1Ex7F10.5:4	CMU1 Path
0x (default)	XREFCK
10	WREFCK
11	SREFCK

For more information about the WREFCK and SREFCK divide by 4 register settings, see Table 124, page 169.

The following is the common use for each of the reference clock inputs.

- SREFCK is used in sync-E LAN and WAN modes to drive Tx CMU though CMU0 path. In this mode, this clock is externally synced to the recovered output clock from any of the channels of the same device or of other devices, and used to drive the Tx CMU directly. SREFCK is 156.25 MHz (divide by 66) in LAN mode and 155.52 MHz (divide by 64) or 622.08 MHz (divide by 16) in WAN mode.
- WREFCK is used in primarily WAN mode for both Tx CMU and Rx CRU. In WAN synch-E mode, this clock provides a WAN reference clock to the CRU only while the CMU runs off the SREFCK. WREFCK is 155.52 MHz (divide by 64) or 622.08 MHz (divide by 16).
- XREFCK is the PMA main clock during LAN single Reference Clock operation. This clock drives both Tx CMU and Rx CRU in LAN mode. In Sync-E LAN mode, this clock is used for CRU reference clock. This clock also supplies the serial interfaces/digital core and the XAUI block. This clock is 156.25 MHz and on all the time. The following table lists the PMA reference clock rates and modes.

Table 20 • **PMA Reference Clock Rates and Modes**

Mode	SREFCK (MHz)	WREFCK (MHz)	XREFCK (MHz)	Tx CMU REFCLK	Rx CDR REFCLK	Tx divide by	Rx divide by
LAN single Ref Clk			156.25	XREFCK	XREFCK	66	66
FC			159.05	XREFCK	XREFCK	66	66
WAN64		155.52	156.25	WREFCK	WREFCK	64	64
WAN16		622.08	156.25	WREFCK	WREFCK/4	16	64
Sync-E LAN66	156.25 recovered		156.25	SREFCK	XREFCK	66	66
Sync-E WAN64	155.52 recovered	155.52	156.25	SREFCK	WREFCK	64	64
Sync-E WAN16	622.08 recovered	155.52	156.25	SREFCK	WREFCK	16	64
1.25G Pass-through			156.25	XAUI Recovered 156.25 MHz	XREFCK	64	64

In addition to the preceding modes, the PMA may also support other untested and unsupported modes with custom clock configurations. Contact your local Microsemi sales representative for support using other mode settings.

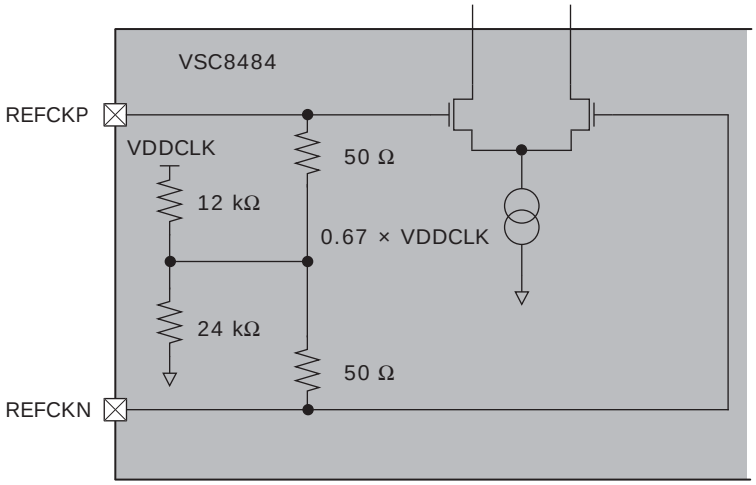
It is possible to support both 10G LAN and 10G WAN using different channels of the same device. However, if any one channel is to operate at the 10G Fibre Channel rate, then all channels in the device must operate at the 10G Fibre Channel rate. Mixing 10G Fibre Channel and LAN in the same device does not work. Mixing 10G Fibre Channel and WAN in the same device does not work either. XREFCK is the reference clock shared by all four XAUI channels. LAN/WAN data channels require the XAUI channel have a 156 MHz reference clock whereas the 10G Fibre Channel needs the XAUI channel's reference

clock to be 159 MHz. It is not possible to provide 156 MHz to one channel and 159 MHz to another channel.

3.3.21 Reference Clock Inputs

The VSC8484 device includes internal termination of 100 Ω equivalent between true and complement. An internal bias generator, nominally set at 0.67 × VDDCLK, is provided for AC-coupling. Single-ended reference clock operation is possible, and when implemented, both inputs must have equivalent termination. However, the best jitter performance is obtained using a low phase noise, differential reference clock. The following illustration shows the reference clock input receiver.

Figure 9 • **Reference Clock Input Receiver**



3.3.22 Clock Output

There are two independent and fully programmable clock outputs from the various clock sources in the PMA: RXCKOUT and TXCKOUT. RXCKOUT is primarily used in Sync-E applications and defaults to the Rx CDR recovered clock divided by 66. TXCKOUT is primarily used as a reference clock in XFP applications and defaults to Tx CMU divided by 64. The source for these two clock outputs can be changed by registers.

Table 21 • **PMA Clock Output Setting**

Register 1xA008.2:0	RXCKOUT Source	Register 1xA009.2:0	TXCKOUT Source
001	Rx CDR /64	001	Tx CMU /66
011	Tx CMU /66	011	Rx CDR /64
100	XAUI CMU VARCLK	10x	Tx CMU REFCLK copy
101	Reserved	110	Rx CDR CRU copy
110	Rx CDR /60	111	XAUI recovered clock
111	Reserved		

3.3.23 Synchronous Ethernet Support

The VSC8484 device PMA supports synchronous Ethernet applications. The RXCKOUT clock output is used for the Sync-E clock source and can be routed outside the device to the clock distributor device. The external synchronous clock is routed to the SREFCK input of the PMA. The SREFCK can either be divide by 16, 64, or 66 of the desired rate. In Sync-E LAN mode, the Rx CDR reference clock is coming from XREFCK, and Tx CMU reference clock is coming from SREFCK. In this case, XREFCK is 156.25 MHz and SREFCK is 156.25 MHz sync with the recovered clock of one channel (Sync-E master

clock). In Sync-E WAN mode, the Rx CDR reference clock is coming from WREFCK and Tx CMU reference clock is coming from SREFCK. In this case, the WREFCK is 155.52 MHz, and SREFCK can either be 155.52 MHz or 622.08 MHz sync with the recovered clock on one channel (Sync-E master clock).

In Sync-E applications, the recovered clock from clock output pin goes through an external clock distribution device.

Note: The clock output pin from the PMA can only be a divide by 66 or a divide by 64 recovered clocks.

3.3.24 1.25 Gbps Mode

In the 1.25 Gbps mode, the network side serial inputs runs in an oversampling mode at an equivalent line of 1.25 Gbps. This serial data stream is used to recover the clock. The recovered clock is used to transmit the same serial data stream (without processing) on Lane 0 or Lane 3 of the XAUI output interface. Similarly the XAUI input interface also accepts a 1.25 Gbps data stream on Lane 0 or Lane 3. This data stream is also routed to the network side serial outputs without processing. The network serial output data rate is synchronous with the incoming data rate on the XAUI input interface. The 1x8019.2:1 register sets the PMA rate mode.

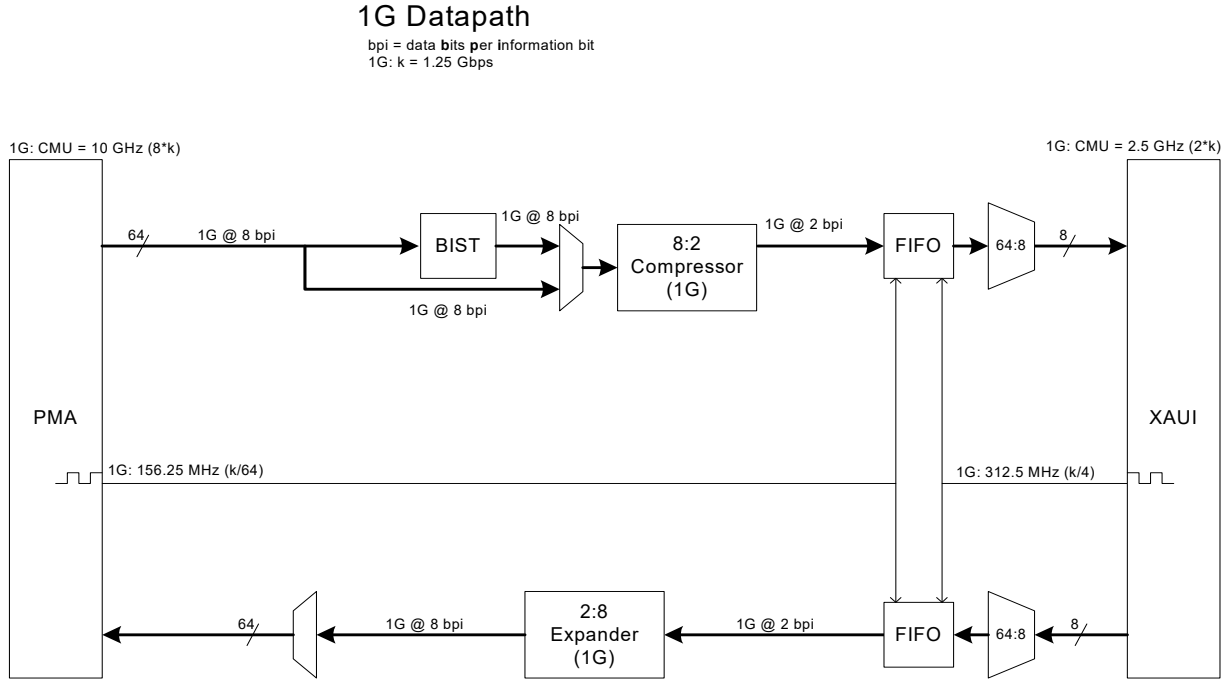
The RXIN pin accepts a 1.25 Gbps data stream and demuxes it to 64-bit at RXD[63:0]. The Rx CDR VCO runs at 10 GHz and oversamples the incoming data eight times. The Rx CDR automatically determines the correct valid data bit in the 8-bit demux output data stream and copies the valid data bit into the invalid data bits forming a valid 8-bit continuous data stream. No special processing is required at 64-bit parallel data RXD[63:0]. The incoming data from the parallel interface arrives as a 64-bit data stream at TXD[63:0]. The parallel interface (XAUI) recovered clock is routed through XRCVCK reference clock input driving the Tx CMU. In this mode, the XRCVCK is 156.25 MHz. The Tx CMU VCO runs at 10 GHz and clock each 1.25 Gbps data bit eight times. The register 1x8017.3:1 must be set to 1x1 and register 1x8017.5:4 to 01 for 1.25 Gbps mode (divide by 64). The register 1x8019.4:3 must be set to 00 and 1x8019.2:1 must be set to 10.

A single reference clock (XREFCK = 156.25 MHz) is required in the 10G and 1G Ethernet modes.

Table 22 • **PMA Rx Data Rate Mode**

Register 1x8019.2:1	Rx Data Rate (Gbps)	Mode
00 (default)	10.3125 or 9.95328	WAN, LAN, KR
1x	1.25	KX

Figure 10 • **1G Mode**



3.3.25 Power Down Mode

The PMA is powered down when any of the IEEE defined low power mode register bits are asserted (1x0000.11, 2x0000.11, 3x0000.11, and 4x0000.11). This shuts off both the receive and transmit datapaths.

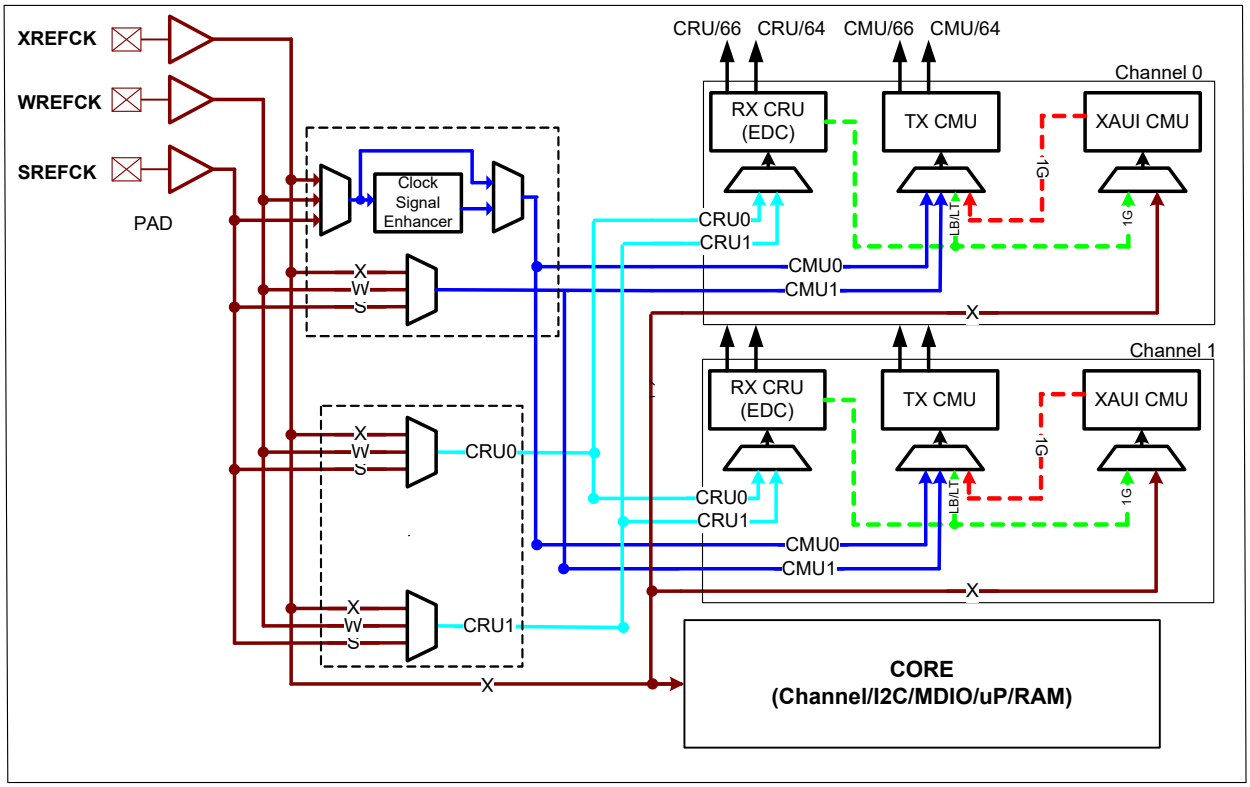
3.3.26 Clock Distribution

Three types of REFCLK inputs (XREFCK, SREFCK, and WREFCK) may be selected for the CMU and CRU. XREFCK is needed all the time for the core logic regardless of LAN, WAN, or Sync-E mode. Two CMU clock paths and two CRU clock paths may be selected to meet the specific application. In the CMU0 clock path, a clock signal enhancer circuit may be added to improve the clock quality. Usually, it is needed for clock input used with multiplier ×66 or ×64.

On the clock outputs, the RXnCKOUT or TXnCKOUT may be set to one of the following choices: CMU/64, CMU/66, CDR/64, and some test modes as indicated in the registers section. These clock outputs are provided on a per channel basis. The CMU/64 is commonly used for the reference clock of the XFP, and CDR/64 may be used as the recovered clock for Sync-E applications.

The choices for both the clock inputs and outputs are configurable through registers. The following illustration shows the reference clock distribution.

Figure 11 • **REFCLK Distribution**



3.3.27 Operation Modes

The VSC8484 device is designed to support different modes of operation for IEEE802.3ae LAN and WIS, INCITS T11-10GFC, IEEE802.3ap, and Sync-E. The following list shows the recommended modes of operations and their clocking scheme setups.

- Regular LAN applications with XREFCK = 156.25 MHz
- Regular WIS applications with XREFCK = 156.25 MHz and WREFCK = 155.52 MHz
- Regular WIS applications with XREFCK = 156.25 Mhz and WREFCK = 622.08 MHz
- Sync-E LAN applications with XREFCK = 156.25 MHz and SREFCK = 156.25 MHz
- Sync-E WAN applications with XREFCK = 156.25 MHz and WREFCK = 155.52 MHz
- One channel in LAN and one channel in WIS with XREFFCLK = 156.25 MHz and WREFCK = 622.08 MHz

XREFCK, SREFCK, and WREFCK are the three clock inputs to the VSC8484 device. The XREFCK is required in all modes of operation. It provides the clock to the core, the XAUI block, and is optionally used for the CMU and CRU blocks. In regular LAN mode, the XREFCK is used for the CMU and CRU block. In regular WIS mode, the WREFCK is used for the CMU and CRU block. In Sync-E LAN mode, the XREFCK provides the clock for the CRU, and the SREFCK is used for the CMU. In Sync-E WIS mode, the WREFCK provides the clock for the CRU, and the SREFCK is used for the CMU.

TXCLKOUTP/N and RXCLKOUTP/N are the two clock outputs per channel. Each output can be programmed to be CMU/64, CMU/66, CDR/64, and a copy of the XREFCK input. Usually, the CMU/64 is used for the clock input of the XFP module. The recovered clock CDR/64 is normally used by the system for the Sync-E clocking schemes.

Note: The XAUI output data is based on the local XREFCK and not frequency locked to the recovered clock. The clock associated with the XAUI input data is not required to be frequency locked to the local XREFCK but it should be within ±100 ppm to the XREFCK frequency.

The following table lists some recommended modes of operation with the corresponding registers setting and clock source configuration.

Table 23 • **Recommended Clock Operation Modes**

Application	Clock Configuration	Register Settings
Regular LAN application	XREFCK = 156.25 MHz	Global Register 1Ex7F10 = 0x0100 1Ex7F11 = 0x00D2 Channel Register 0 and 1 1x8017 = 0x0020
Regular WIS application with 155.52 MHz WREFCK	XREFCK = 156.25 MHz WREFCK = 155.52 MHz	Global Register 1Ex7F10 = 0x01AA Channel Register 0 and 1 1x8017 = 0x0020 1x8019 = 0x0000 2x0007 = 0x0001
Regular WIS application with 622.08 MHz WREFCK	XREFCK = 156.25 MHz WREFCK = 622.08Mz	Global Register 1Ex7F10 = 0x00A5; Channel Register 0 and 1 1x8017 = 0x0024 1x8019 = 0x0000 2x0007 = 0x0001
Sync-E LAN application	XREFCK = 156.25 MHz SREFCK = 156.25 MHz[1]	Global Register 1Ex7F10 = 0x01C0 1Ex7F11 = 0x00D2 Channel 0 as master 1x8017 = 0x0022 1xA008 = 0x0009 Channel 1 as slave 1x8017 = 0x0020
Sync-E WIS application	XREFCK = 156.25 MHz WREFCK = 155.52 MHz (default from GUI) SREFCK = 155.52 MHz[2]	Global Register 1Ex7F10 = 0x01EA Channel 0 as master 1x8017 = 0x0002 1x8019 = 0x0000 1xA008 = 0x0009 2x0007 = 0x0001 Channel 1 as slave 1x8017 = 0x0020 1x8019 = 0x0000 2x0007 = 0x0001
One channel in LAN and one channel in WIS with XREFFCLK = 156.25 MHz and WREFCK = 622.08 MHz (no Sync-E)	XREFCK = 156.25 MHz WREFCK = 622.08 MHz	Global Register 1Ex7F10 = 0x0128 1Ex7F11 = 0x00D2 Channel 0 LAN Register 1x8017 = 0x0020 Channel 1 WIS Register 1x8017 = 0x0024 1x8019 = 0x0020 2x0007 = 0x0001

1. Provided from an external clock synthesizer, which takes the recovered clock from the VSC8484 device or from other PHYs in the system, cleans up the jitter, and generates a 156.25 MHz clock that is locked to the recovered clock. RXCLKOUT0 is set to CDR/64. The recovered clock is at /64 but the SREFCK is at /66. It is the responsibility of the external clock synthesizer to do the clock rate conversion. (The SREFCK can also be set at /64 so that the external clock synthesizer needs to do the jitter clean up but not the frequency conversion.)
2. Provided from an external clock synthesizer, which takes the recovered clock from the VSC8484 device or from other PHYs in the system, cleans up the jitter, and generate a 155.52 MHz clock that is locked to the recovered clock. RXCLKOUT0 is set to CDR/64. For Sync-E WIS mode, the recovered clock is at /64 and the SREFCK is also at /64.

3.4 WAN Interface Sublayer (WIS)

The WAN interface sublayer (WIS) is defined in IEEE 802.3ae Clause 50. The VSC8484 WIS block is fully compliant with this specification. The VSC8484 device offers additional controls, ports, and registers to allow integration into a wider array of SONET/SDH equipment. Clocking requirements are a critical component for SONET/SDH equipment as discussed in earlier sections.

In addition to the SONET/SDH features addressed by WIS as defined by IEEE, most SONET/SDH framers/mappers contain additional circuitry for implementing operation, administration, maintenance and provisioning (OAM&P). These framers/mappers also support special features to enable compatibility with legacy SONET/SDH solutions. Because the VSC8484 WIS leverages Microsemi's industry-leading framer/mapper technology it contains suitable features for standard SONET/SDH equipment. This includes the transmit/receive overhead serial interfaces (TOSI/ROSI) commonly used for network customization and OAM&P, support for SONET/SDH errors not contained in the WIS standard, support for common legacy SONET/SDH implementations, and SONET/SDH jitter and timing quality.

3.4.1 Operation

WAN mode is enabled by asserting register bits. Status register bit 1xA101.3 indicates whether WAN mode is enabled. Both Rx and Tx paths have WAN mode either enabled or disabled. It is not possible to have WAN mode in the Tx path enabled while the Rx path is disabled, or vice versa. An "X" in the table represents a don't care state.

Note: After WAN mode is enabled, write both bit 2 and 1 of 1xAE00 to high to reset the Tx and Rx PCS blocks and enable valid WAN data to pass through.

Table 24 • **WAN Mode Enable Logic**

Inputs			Result
PMA_MODE (1x0007.2:0)	**PCS Type Selection (2x0007.0)**	**PCS Mode (3x0007.1:0)**	**WAN_STAT (1xA101.3**
000, 100, 101, 110, or 111	0	00	0
001, 010, or 011	X	X	
X	1	X	1
X	X	10	1

The receive portion of the WIS does the following:

- Maps data from the PCS through the WIS service interface and to the SONET/SDH synchronous payload envelope (SPE).
- Generates path, line, and section overhead octets.
- Scrambles the frame.
- Transmits the frame to the PMA service interface.

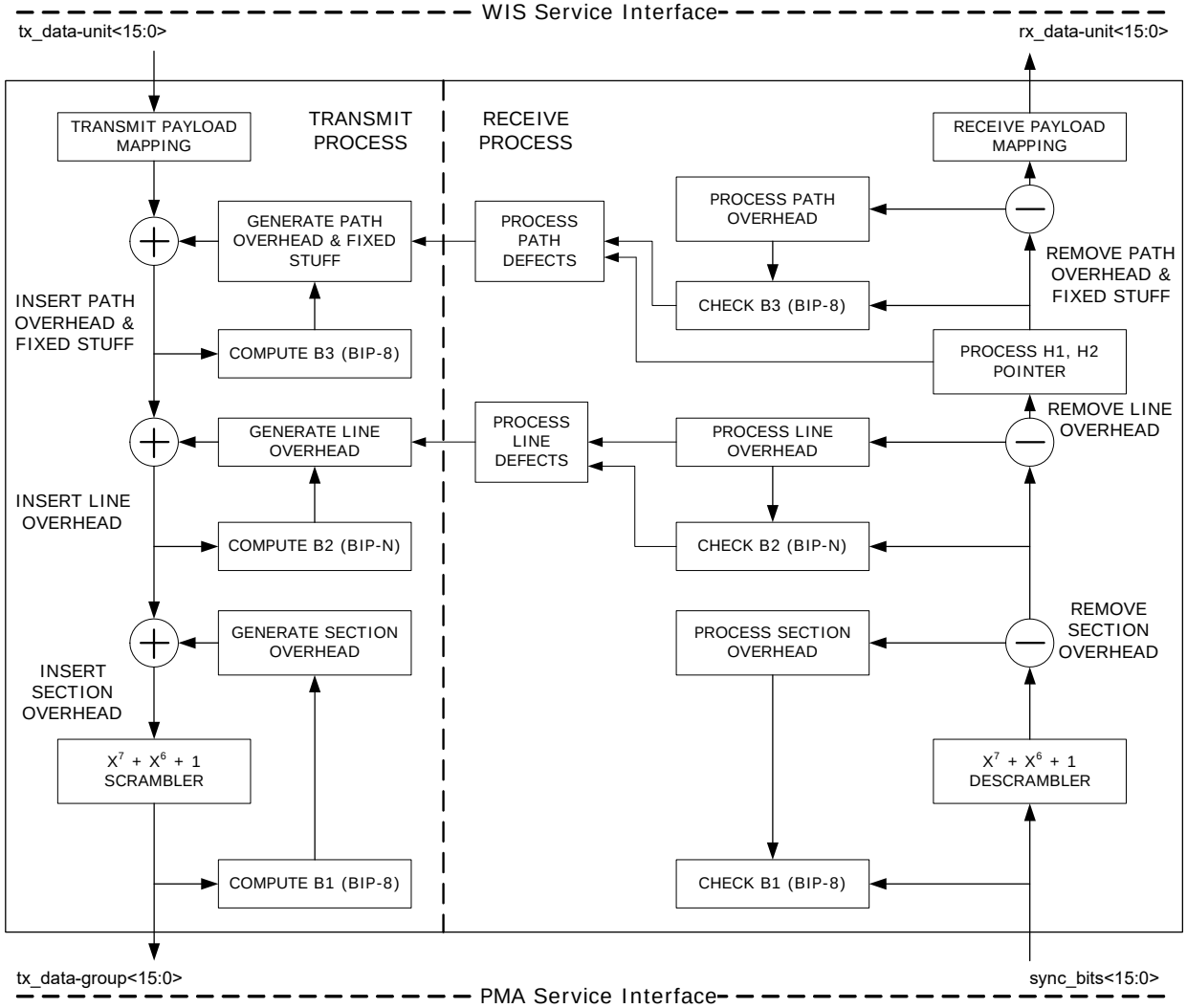
The receive portion of the WIS does the following:

- Receives data from the PMA service interface.

- Delineates octet and frame boundaries.
- Descrambles the frame.
- Processes section, line, and path overhead information that contain alarms and parity errors.
- Interprets the pointer field.
- Extracts the payload for transmittal to the PCS through the WIS service interface.

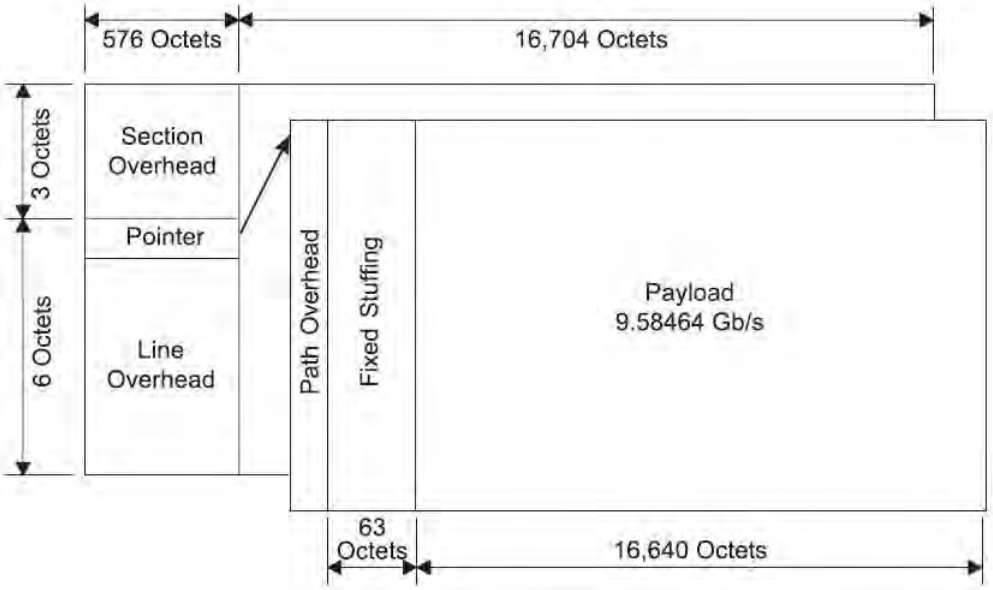
The following illustration shows the WIS block diagram.

Figure 12 • **WIS Transmit and Receive Functions**



The following illustration shows the WIS frame structure.

Figure 13 • **WIS Frame Structure**



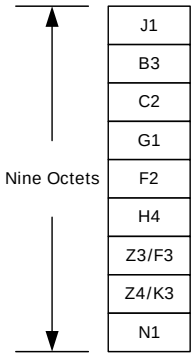
The following illustration shows the positions of the section and line overhead octets within the WIS Frame.

Figure 14 • **STS-192c/STM-64 Section and Line Overhead Structure**



The following illustration shows the path overhead octet positions.

Figure 15 • **Path Overhead Octets**



3.4.2 Section Overhead

The section overhead portion of the SONET/SDH frame supports frame synchronization, a tandem connection monitor (TCM) known as the section trace, a high-level parity check, and some OAM&P octets. The following table lists each of the octets including their function, specification, and related information.

The VSC8484 device provides a mechanism to transmit a static value as programmed by the MDIO interface. However, by definition, MDIO is not fast enough to alter the octet on a frame-by-frame basis.

Table 25 • **Section Overhead**

Overhead Octet	Function	IEEE 802.3ae WIS Usage	Recommended Value	WIS Extension
A1	Frame alignment	Supported	0×F6	Register (2xE611) TOSI and ROSI access.
A2	Frame alignment	Supported	0×28	Register (2xE611) TOSI and ROSI access.
J0	Section trace	Specified value	For more information, see J0 (Section Trace), page 32.	A 1-byte, 16-byte, or 64-byte trace message can be sent using registers 2x0040 to 2x0047, 2xE700, or 2xE800 to 2xE817 and received using registers 2x0048 to 2x004F, 2xEC20, and 2xE900 to 2xE917. TOSI and ROSI access.
Z0	Reserved for section growth	Unsupported	0×CC	Register 2xE612 TOSI and ROSI access.
B1	Section error monitoring (Section BIP-8)	Supported	Bit interleaved parity - 8 bits, as specified in T1.416	Using the TOSI, the B1 byte can be masked for test purposes. For each B1 mask bit that is cleared to 0 on the TOSI interface, the transmitted bit is left unchanged. For each B1 mask bit that is set to 1 on the TOSI interface, the transmitted bit is inverted. Using the ROSI, the B1 error locations can be extracted. Periodically latched counter (2xECB0-2xECB1) is available.
E1	Orderwire	Unsupported	0×00	Register 2xE612 TOSI and ROSI access.
F1	Section user channel	Unsupported	0×00	Register 2xE613 TOSI and ROSI access.
D1-D3	Section data communications channel (DCC)	Unsupported	0×00	Register 2xE613 to 2xE614 TOSI and ROSI access.

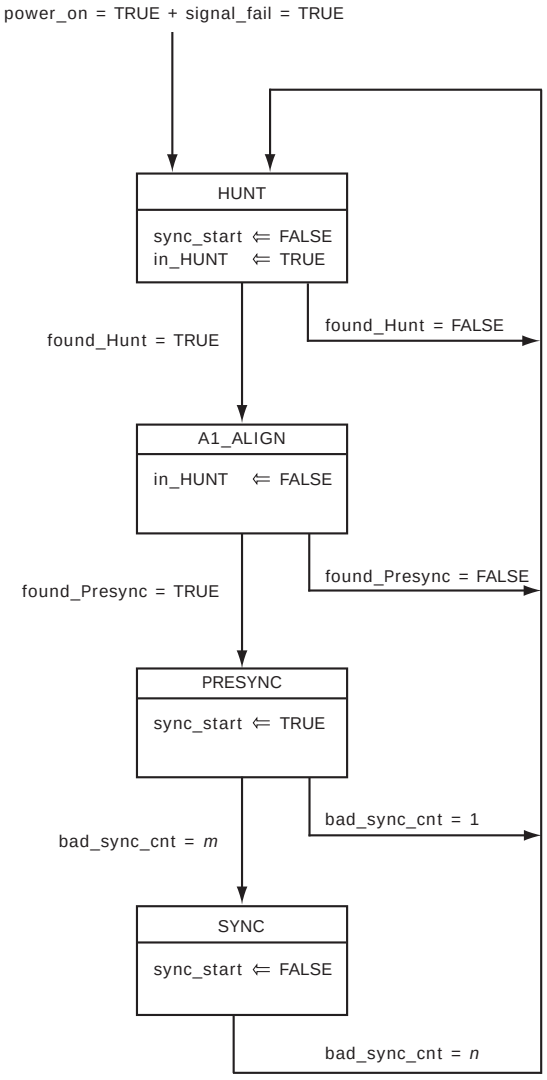
3.4.3 A1, A2 (Frame Alignment)

The SONET/SDH protocol is based on a frame structure that is delineated by the framing octets, A1 and A2. The framing octets are defined to be 0×F6 and 0×28 respectively. In the transmit direction all 192 A1 octets are sourced from the TX_A1 (2xE611.15:8) register whereas the A2 octets are sourced from the TX_A2 (2xE611.7:0) register.

In the receive direction, the frame aligner monitors the input bus from the PMA and performs word alignment. The frame alignment architecture is composed of a primary and secondary state machine. The variables are reflected in registers EWIS_RX_FRM_CTRL1 (2xEC00) and EWIS_RX_FRM_CTRL2 (2xEC01) that can be alternately reconfigured. The selected frame alignment and synchronization pattern have implications on the tolerated input BER. The higher the input BER, the less likely the frame boundary can be found. The chances of finding the frame boundary are improved by reducing the number of A1/A2 bytes required to be detected (using a smaller pattern width). According to the WIS specification, the minimum for all parameters allows a signal with an error tolerance of 10^{-12} to be framed.

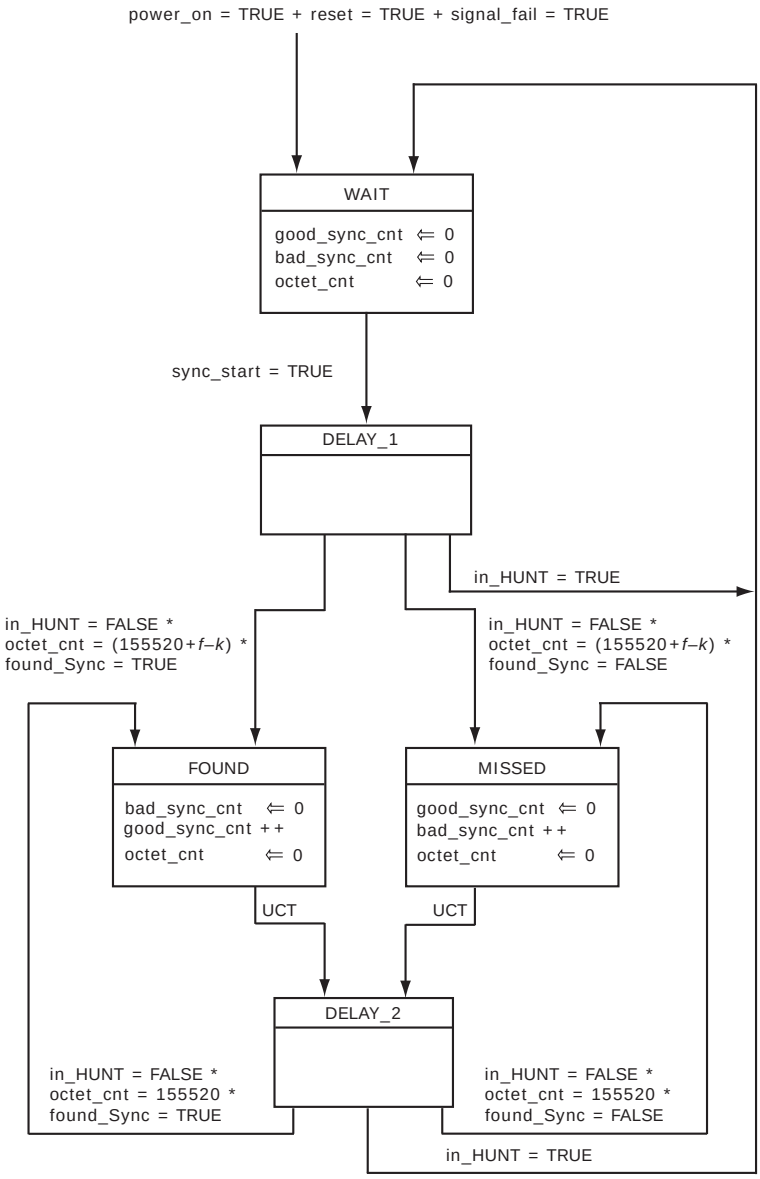
The following illustration shows the primary synchronization state diagram.

Figure 16 • **Primary Synchronization State Diagram**



The following illustration shows the secondary synchronization state diagram.

Figure 17 • **Secondary Synchronization State Diagram**



The following table lists the variables for the primary state diagram.

Table 26 • **Framing Parameter Description and Values**

Name	Description	IEEE 802.3ae Parameter	IEEE 802.3ae Range	Range	Default
Sync_Pattern width	Sequence of f consecutive A1s followed immediately by a sequence of f consecutive A2s. If f = 2, Sync_Pattern is A1A1A2A2.	f	2 to 192	0 to 16 Exceptions: If f = 0, Sync_Pattern is A1 + 4 MSBs of A2. If f = 1, Sync_Pattern is A1A1A2.	2
Hunt_Pattern width	Sequence of i consecutive A1s.	i	1 to 192	1 to 16.	4

Table 26 • **Framing Parameter Description and Values *(continued)***

Name	Description	IEEE 802.3ae Parameter	IEEE 802.3ae Range	Range	Default
Presync_Pattern A1 width	Presync_Pattern consists of a sequence of j consecutive A1s followed immediately by a sequence of k consecutive A2s.	j	16 to 190	1 to 16 If set to 0, behaves as if set to 1. If set to 17 to 31, behaves as if set to 16.	16
Presync_Pattern A2 width	Presync_Pattern consists of a sequence of j consecutive A1s followed immediately by a sequence of k consecutive A2s.	k	16 to 192	0 to 16 0 means only 4 MSB of A2 are used If set to 17 to 31, behaves as if set to 16.	16
SYNC state entry	Number of consecutive frame boundaries needed to be found after entering the PRESYNC state in order to enter the SYNC state.	m	4 to 8	1 to 15 If set to 0, behaves as if set to 1.	4
SYNC state exit	Number of consecutive frame boundary location errors detected before exiting the SYNC state.	n	1 to 8	1 to 15 If set to 0, behaves as if set to 1.	4

3.4.4 Loss of Signal (LOS)

The SONET/SDH loss of signal (LOS) alarm is tied to the PMA input receiver logic. The LOS (2x0021.6) alarm is a latch-high register; back-to-back reads provide both the event as well as status information. The LOS event also asserts the LOS_PEND (2xEE00.6) until read. This event can propagate an interrupt to either WIS_INTA or WIS_INTB based upon mask enable bits LOS_MASKA (2xEE01.6) and LOS_MASKB (2xEE02.6).

There is no hysteresis on the LOS detection. It is recommended to use system software to implement a sliding window to check on the LOS before qualifying the signal is present. Alternatively, RX_LOS can be used from the optical module (through LOPC) to qualify the input signal. In addition to analog detection, it is recommended to use digital detection such as PCS_RX_Fault to determine if the input signal is good.

When the near-end device experiences a LOS condition, it is possible to automatically transmit a remote defect indication (RDI-L) to the far end for notification purposes. The TXRDIL_ON_LOS (2xEDFF.2), if asserted, overwrites the outgoing K2 bits with the RDI-L code. In the receive path, it is possible to force a AIS-L state (alarm assertion plus forcing the payload to an all ones state) upon a detection of an LOS condition. This is accomplished by asserting RXAISL_ON_LOS (2xEDFF.5).

3.4.5 Loss of Optical Carrier (LOPC)

The input pin LOPC can be used by external optic components to directly assert the loss of optical power to the physical media device. Any change in level on the LOPC input asserts LOPC_PEND (2xEE04.11) until read. The current status of the LOPC input pin can be read using LOPC_STAT (2xEE03.11). The LOPC input can be active high or active low by setting the LOPC_POL_SEL (2xEC30.9) bit appropriately. The LOPCS_PEND bit can propagate an interrupt to either WIS_INTA or WIS_INTB based upon mask enable bits LOPC_MASKA (2xEE05.11) and LOPC_MASKB (2xEE06.11).

When the near-end device experiences an LOPC condition, it is possible to automatically transmit a remote defect indication (RDI-L) to the far end to notify it of a problem. The TXRDIL_ON_LOPC (2xEDFF.3), if asserted, overwrites the outgoing K2 bits with the RDI-L code. In the receive path, it is possible to force the receive framer into an LOF state, thereby squelching subsequent alarms and invalid

payload data processing. This is accomplished by asserting RXLOF_ON_LOPC (2xEC30.8). Similar to the LOF condition forced upon an LOPC, the RXAISL_ON_LOPC (2xEDFF.6) can force the AIS-L alarm assertion, plus force the payload to an all ones state to indicate to the PCS the lack of valid data, upon an LOPC condition.

3.4.6 Severely Errored Frame (SEF)

Upon reset, the VSC8484 device Rx WIS enters the out of frame (OOF) state with both the severely errored frame (SEF) and loss of frame (LOF) alarms active. The SEF defect is terminated when the framer enters the SYNC state. The framer enters the SYNC state after SYNC_ENTRY_CNT (2xEC01.7:4) plus 1 consecutive frame boundaries are identified. An SEF defect state is declared when the framer enters the out-of-frame (OOF) state. The frame changes from the SYNC state to the OOF state when SYNC_EXIT_CNT (2xEC01.3:0) consecutive frames with errored frame alignment words are detected. SEF is indicated by asserting SEF (2x0021.11). This register latches high providing a combination of interrupt pending and status information within consecutive reads.

An additional bi-stable interrupt pending bit SEF_PEND (2xEE00.11) is provided to propagate an interrupt to either WIS_INTA or WIS_INTB based upon mask enable bits SEF_MASKA (2xEE01.11) and SEF_MASKB (2xEE02.11).

3.4.7 Loss of Frame (LOF)

An LOF occurs when an out-of-frame state persists for an integrating period of LOF_T1 (2xEC02.11:6) frames. To provide for the case of intermittent OOFs, when not in the LOF state, the integrating timer is not reset to zero until an in-frame condition persists continuously for LOF_T2 (2xEC02.5:0) frames. Once in the LOF state, this state is left when the in-frame state persists continuously for LOF_T3 (2xEC03.6:1) frames. The LOF state is indicated by LOF (2x0021.7) being asserted. This register latches high, providing a combination of pending and status information over consecutive reads.

An additional bi-stable interrupt pending bit LOF_PEND (2xEE00.7) is provided which can propagate an interrupt to either WIS_INTA or WIS_INTB based upon mask enable bits LOF_MASKA (2xEE01.7) and LOF_MASKB (2xEE02.7).

When the near end device experiences an LOF condition, it might be required that the far end device be notified of the catastrophic condition. Transmitting an alarm indication signal (AIS-L) can accomplish this. If RXAISL_ON_LOF (2xEDFF.4) is asserted, the transmit path is preempted by the AIS-L pattern whenever an LOF alarm condition is asserted.

When the near end device experiences an LOF condition, it is possible to automatically transmit a remote defect indication (RDI-L) to the far end to notify it of a problem. The TXRDIL_ON_LOF (2xEDFF.1), if asserted, overwrites the outgoing K2 bits with the RDI-L code. In the receive path, it is possible to force a AIS-L state (alarm assertion plus forcing the payload to an all ones state) upon a detection of an LOF condition. This is accomplished by asserting RXAISL_ON_LOF (2xEDFF.4).

3.4.8 J0 (Section Trace)

The J0 octet often carries a repeating message called the section trace message. The default transmitted message length is 16-octets whose contents are defined in J0_TXMSG (2x0040-2x0047). If no active message is being broadcast, a default section trace message consisting of 15 octets of zeros and a header octet formatted according to Section 5 of ANSI T1.269-2000 is transmitted. The header octet for the 15-octets of zero would be 0×89. The default values of J0_TXMSG (2x0040-2x0047) do not contain the 0×89 value of the header octet, so software must write this value.

The J0 octet in the receive direction by default is assumed to be carrying a 16-octet continuously repeating section trace message. The message is extracted from the incoming WIS frames and stored in J0_RXMSG (2x0048-2x004F). The WIS receive process does not delineate the message boundaries, thus the message might appear rotated between new frame alignment events.

The VSC8484 device supports two alternate message types, a single repeating octet and a 64-octet message. The message type can be independently selected for the transmit and receive direction. The transmit direction is configured using J0_TXLEN (2xE700.3:2) and the J0_RXLEN (2xEC20.3:2) configures the receive path.

When the transmit direction is configured for a 64-octet message, the first 16 octets are programmed in J0_TXMSG (2x0040-2x0047) whereas the 48 remaining octets are programmed in J0_TXMSG64 (2xE800-2xE817). Likewise, the first 16 octets of the receive message are stored in J0_RXMSG (2x0048-2x004F) whereas the other 48 octets are stored in J0_RXMSG64 (2xE900-2xE917). The receive message is updated every 125 µs with the recently received octet. Any persistency or message matching is expected to take place within the station manager.

3.4.9 Z0 (Reserved for Section Growth)

The WIS standard does not support the Z0 octet and requires transmission of 0×CC in the octet locations. A different Z0 value can be transmitted by configuring TX_Z0 (2xE612.15:8). The TX_Z0 default is 0×CC.

3.4.10 Scrambling/Descrambling

The transmit signal (except for row 1 of the section overhead) is scrambled according to the standards when SCR_EN (2xE600.12) is asserted, which is the default state. When deasserted, the scrambler is disabled.

The receive signal descrambler DESCR_EN (2xEC10.1) is enabled by default; however, by deasserting this bit the descrambler can be bypassed.

3.4.11 B1 (Section Error Monitoring)

The B1 octet is a bit interleaved parity-8 (BIP-8) code using even parity calculated over the previous STS-192c frame, post scrambling. The computed BIP-8 is placed in the following outgoing SONET frame before scrambling.

In the receive direction, the incoming frame is processed and a BIP-8 is calculated. The calculated value is then compared with the B1 value received in the following frame. The difference between the calculated and received octets are accumulated into B1_CNT (2x003C). This counter rolls over after the maximum count. This counter is cleared upon device reset.

The B1_ERR_CNT[1:0] (2xECB0 to 2xECB1) registers provide a count of the number of received B1 parity errors. This register is updated with the internal count value upon a PMTICK condition, after which the internal counter is reset to zero. When the counter is nonzero, the B1_NZ_PEND (2xEE04.7) event is asserted until read. A non-latch high version of this event, B1_NZ_STAT (2xEE03.7) is also available. This event can propagate an interrupt to either WIS_INTA or WIS_INTB based upon mask enable bits B1_ERR_MASKA (2xEE05.7) and B1_ERR_MASKB (2xEE06.7).

The B1_ERR_CNT can optionally be configured to increment on a block count basis, a maximum increment of one per errored frame regardless of the number of errors received. This mode is enabled by asserting B1_BLK (2xEC61.11)

3.4.12 E1 (Section Orderwire)

The WIS standard does not support the E1 octet and requires transmission of 0×00 in the octet location. A different E1 value can be transmitted by configuring TX_E1 (2xE612.7:0), whose default is 0×00.

3.4.13 F1 (Section User Channel)

The WIS standard does not support the F1 octet and requires transmission of 0×00 in the octet location. A different F1 value can be transmitted by configuring TX_F1 (2xE613.15:8), whose default is 0×00.

3.4.14 DCC-S (Section Data Communication Channel)

The WIS standard does not support the DCC-S octets and requires transmission of 0×00 in the octet locations. Different DCC-S values can be transmitted by configuring TX_D1 (2xE613.7:0), TX_D2 (2xE614.15:8), and TX_D3 (2xE614.7:0), all of which default to 0×00.

3.4.15 Reserved, National, and Unused Octets

The VSC8484 device transmits 0×00 for all reserved, national, and unused overhead octets.

3.4.16 Line Overhead

The line overhead portion of the SONET/SDH frame supports pointer interpretation, a per channel parity check, protection switching information, synchronization status messaging, far end error reporting, and some OAM&P octets.

The VSC8484 device provides a mechanism to transmit a static value as programmed by the MDIO interface. However, by definition, MDIO is not fast enough to alter the octet on a frame-by-frame basis. The following table lists each of the octets including their function, specification, and related information.

Table 27 • **Line Overhead Octets**

Overhead Octet	Function	IEEE 802.3ae WIS Usage	Recommended Value	WIS Extension
H1-H2	Pointer	Specified value	SONET mode: STS-1: 0×62, 0×0A STS-n: 0×93, 0×FF SDH mode: STS-1: 0×6A, 0×0A STS-n: 0×9B, 0×FF	Register 2xE615 to 2xE616 TOSI and ROSI access.
H3	Pointer action	Specified value	0×00	Register 2xE616 TOSI and ROSI access.
B2	Line error monitoring (line BIP-1536)	Supported	Bit interleave parity-8, as specified in T1.416	Using the TOSI, the B2 bytes can be masked for test purposes. For each B2 mask bit that is cleared to 0 on the TOSI interface, the transmitted bit is left unchanged. For each B2 mask bit that is set to 1 on the TOSI interface, the transmitted bit is inverted. Using the ROSI, the B2 error locations can be extracted. Periodically latched counter (2xECB0-2xECB1) is available.
K1, K2	Automatic protection switch (APS) channel and line remote defect identifier (RDI-L)	Specified value	For information about K2 coding, see Table 28, page 36	Register 2xE617 to 2xE618 TOSI and ROSI access.
D4-D12	Line data communications channel (DCC)	Unsupported	0×00	Register 2xE619 to 2xE61E TOSI and ROSI access.
S1	Synchronization messaging	Unsupported	0×0F	Register 2xE61F TOSI and ROSI access.
Z1	Reserved for Line growth	Unsupported	0×00	Register 2xE61F TOSI and ROSI access.
M0/M1	STS-1/N line remote error indication (REI)	M0 unsupported, M1 supported	0×00/number of detected B2 errors in the receive path, as specified in T1.416	TOSI and ROSI access. The VSC8484 device supports a mode that uses only M1 to back report REI-L (REI_MODE = 0) and another mode which uses both M0 and M1 to back report REI-L (REI_MODE = 1). For more information, see B2 (Line Error Monitoring), page 35.
E2	Orderwire	Unsupported	0×00	Register 2xE620 TOSI and ROSI access.

Table 27 • **Line Overhead Octets *(continued)***

Z2	Reserved for Line growth	Unsupported	0×00	Register 2xE620 TOSI and ROSI access.

3.4.17 B2 (Line Error Monitoring)

The B2 octet is a BIP-8 value calculated over each of the previous STS-1 channels excluding the section overhead and pre-scrambling. As the B2 octet is calculated on an STS-1 basis, there are 192 B2 octets within an STS-192/STM-64 frame. Each of the 192 calculated BIP-8 octets are then placed in the outgoing SONET/SDH frame.

Note: For SONET mode, when the number of errors detected in the B2 octet of a receive frame is greater than 255, the total count of detected errors is transmitted in more than one frame. Even when no B2 errors are detected in subsequent frames, the number of detected B2 errors going into an accumulator are limited to 255 if more than 255 errors are detected in a frame. The Tx framer pulls the REI-L count out of the accumulator when REI-L is transmitted to be compliant with T1-105.

In the receive direction, the incoming frame is processed, and a per STS-1 BIP-8 is calculated (excluding section overhead and after descrambling) and then compared to the B2 value in the following frame. Errors are accumulated into a 32-bit counter B2_CNT (2x0039-2x003A). This counter is non-saturating and so rolls over after its maximum count. The counter is cleared only on device reset.

An additional 32-bit B2 error counter is provided at B2_ERR_CNT (2xECB2-2xECB3), which is a saturating counter and is latched and cleared based upon a PMTICK event. Errors are accumulated since the previous PMTICK event. When the counter is nonzero, the B2_NZ_PEND (2xEE04.6) event is asserted until read. A non-latch high version of this event B2_NZ_STAT (2xEE03.6) is also available. This event can propagate an interrupt to either WIS_INTA or WIS_INTB, based on mask enable bits B2_ERR_MASKA (2xEE05.6) and B2_ERR_MASKB (2xEE06.6).

The B2_ERR_CNT can optionally be configured to increment on a block count basis, a maximum increment of one per errored frame regardless of the number of errors received. This mode is enabled by asserting B2_BLK (2xEC61.10).

It is possible that two sets of B2 bytes (from two SONET/SDH frames) are received by the Rx WIS logic in a period of time when only one M0/M1 octet is transmitted. In this situation, one of the two B2 error counts delivered to the Tx WIS logic is discarded. This situation occurs when the receive data rate is faster than the transmit data rate. Similarly, when the transmit data rate is faster than the receive data rate, a B2 error count is not available for REI-L insertion into the M0/M1 octets of the transmitted SONET/SDH frame. A value of zero is transmitted in this case. This behavior is achieved by using a FIFO to transfer the detected B2 error count from the receive to transmit domains.

A FIFO overflow or underflow condition is not considered an error. Instead it is recovered from gracefully as previously described. A FIFO overflow or underflow eventually occurs unless the transmit and receive interfaces are running at the same average data rate. Because the received and transmitted frames can differ by, at most, 40 ppm (±20 ppm) and still meet the industry standards, this “slip” can happen no more often than once every 3.1 seconds.

3.4.18 K1, K2 (APS Channel and Line Remote Defect Identifier)

The K1 and K2 octets carry information regarding Automatic Protection Switching (APS) and Line Remote Defect Identifier (RDI-L). The K1 octet and the most significant five bits of the K2 octet contain the APS channel information. The transmitted values can be configured at TX_K1 (2xE617.7:0) and TX_K2 (2xE618.15:8). The default values of all zeros are compliant with the WIS standard.

The three least significant bits within the K2 octet carry the RDI-L encoding, as defined by section 7.4.1 of ANSI T1.416-1999 and as shown in the following table.

Table 28 • **K2 Encodings**

Indicator	K2 Value for Bits 6, 7, 8	Interpretation
RDI-L	110	Remote error indication. For the receive process, an RDI-L defect occurs after a programmable number of RDI-L signals are received in contiguous frames and is terminated when no RDI-L is received for the same number of contiguous frames. An RDI-L can be forced by asserting FRC_RX_RDIL (2x2xEC30.2). For the transmit process, the WIS standard does not indicate when or how to transmit RDI-L. The VSC8484 device provides the option of transmitting K2 by programming it through the TOSI, by programming it using the K2_TX MDIO register, or by programming it based on the contents of the K2_TX register with bits 6, 7, and 8 modified depending on the status of the following: LOPC, LOS, LOF, AIS-L and their associated transmit enable bits TXRDIL_ON_LOPC (2xEDFF.3), TXRDIL_ON_LOS (2xEDFF.2), TXRDIL_ON_LOF (2xEDFF.1), and TXRDIL_ON_AISL (2xEDFF.0).
AIS-L	111	Alarm indication signal (line) For the receive process, this is detected based on the settings of the K2 byte. When AIS-L is detected, the WIS link status is down and MDIO register 2x0021.4 is set high. This also contributes to errored second (ES) and severally errored second (SES) reports. For standard WIS operation, this is never transmitted.
Idle (normal)	000	Unless RDI-L exists, the standard WIS transmits idle.

Although the transmission of RDI-L is not explicitly defined within the WIS standard, the VSC8484 device allows the automatic transmission of RDI-L upon the detection of LOPC, LOS, LOF, or AIS-L conditions. These features are enabled by asserting RDIL_ON_LOPC (2xEE00.3), RDIL_ON_LOS (2xEE00.2), RDIL_ON_LOF (2xEE00.1), and RDIL_ON_AISL (2xEE00.0).

Note: The RDI-L code of 110 is transmitted by the DUT only when Rx AIS-L is asserted. For example, if AIS-L is detected by the DUT for five continuous frames in the Rx direction, then the RDI-L code is transmitted for five frames in the Tx direction, not 20 frames as stated in the ANSI T1.105 specification.

The VSC8484 device can force an RDI-L condition independent of the K2 transmit value by asserting FRC_RDIL (2xE600.2). Likewise, an AIS-L condition can be forced by asserting FRC_AISL (2xE600.1). If both conditions are forced, the AIS-L value is transmitted.

In the receive direction, the RDI-L alarm (K2[6:8] = 110, using SONET nomenclature) and the AIS-L alarm (K2[6:8] = 111, using SONET nomenclature) are not asserted until the condition persists for a programmable number of contiguous frames. This value is programmable at APS_THRES (2xEC30.7:4) and is typically set to values of 5 or 10. The AIS-L is detected by the receiver after the programmable number of frames is received, and results in the reporting of AIS-P.

The WIS standard defines RDIL (2x0021.5) and AISL (2x0021.4) as a read only latch-high register, so a read of a one in this register indicates that an error condition occurred since the last read. A second read of the register provides the current status of the event as to whether the alarm is currently asserted. RDIL_PEND (2xEE00.5) and AISL_PEND (2xEE00.4) assert whenever the RDI-L or AIS-L state changes (assert or deassert). These interrupts have associated mask enable bits, RDIL_MASK/AISL_MASK (2xEE01.5:4/2xEE02.5:4), which, if enabled, propagate an interrupt to the WIS_INTA/B pins.

For test purposes, the VSC8484 device can induce an RDI-L condition in the receive direction independent of the received K2 value by asserting FRC_RX_RDIL (2xEC30.2). Likewise, an AIS-L condition can be forced in the receive direction by asserting FRC_RX_AISL (2xEC30.3).

3.4.19 D4 to D12 (Line Data Communications Channel)

The WIS standard does not support Line Data Communications Channel (L-DCC) octets (D4-D12) and recommends transmitting 0x00 within these octets. The D4-D12 transmitted values can be programmed at (2xE619–2xE61E). The register defaults are all 0×00. The receive L-DCC octets are only accessible through the ROSI port.

3.4.20 M0 and M1 (STS-1/N Line Remote Error Indication)

The M0 and M1 octets are used for back reporting the number of B2 errors received, known as remote error indication (REI-L). The value in this octet comes from the B2 error FIFO, as discussed with the B2 octet. The WIS standard does not support the M0 octet and recommends transmitting 0x00 in place of the M0 octet. However, the WIS standard supports the M1 octet in accordance with T1.416.

Two methods for backreporting exist and are controlled by G707_2000_REIL (2×EC40.12). Because a single frame can contain up to 1536 B2 errors, whereas the M1 byte alone can only back report a maximum of 255 errors, a discrepancy exists. When G707_2000_REIL is deasserted, only the M1 byte is used and a maximum of 255 errors are backreported. When G707_2000_REIL is asserted, two octets per frame are used for back reporting, the M1 octet and the M0 octet (not the first STS-1 octet, but the second STS-1 octet). In this mode, a total of 1536 errors can be backreported per frame.

In the receive direction, the VSC8484 device detects and accumulate errors according to the G707_2000_REIL setting. The VSC8484 device deviates from the G.707 standard by not interpreting REI-L values greater than 1536 as zero. The WIS standard defines a 32-bit REI-L counter REIL_CNT (2x0037-2x0038). This counter is non-saturating and so rolls over after its maximum count. The counter is cleared only on device reset.

An additional 32-bit REI-L counter is provided at REIL_ERR_CNT (2xEC90-2xEC91), which is a saturating counter and is latched and cleared based upon a PMTICK event. Errors are accumulated since the previous PMTICK event. When the counter is nonzero, the REIL_NZ_PEND (2xEE04.2) event is asserted until read. A non-latch high version of this event REIL_NZ_STAT (2xEE03.2) is also available. This event can propagate an interrupt to either WIS_INTA or WIS_INTB based upon mask enable bits REIL_NZ_MASKA (2xEE05.2) and REIL_NZ_MASKB (2xEE06.2).

The REIL_ERR_CNT can optionally be configured to increment on a block count basis, a maximum increment of one per errored frame regardless of the number of errors received. This mode is enabled by asserting REIL_BLK (2×EC61.4).

3.4.21 S1 (Synchronization Messaging)

The S1 octet carries the synchronization status message and provides synchronization quality measures of the transmission link in the least significant 4 bits. The WIS standard does not support the S1 octet and requires the transmission of a 0×0F within the S1 octet. A value other than 0×0F can be programmed in TX_S1 (2×E61F).

3.4.22 Z1 and Z2 (Reserved for Line Growth)

The WIS standard does not support the Z1 or Z2 octets and requires the transmission of 0×00 in their locations. Different Z1 and Z2 values can be transmitted by programming the values at TX_Z1 (2×E61F) and TX_Z2 (2×E620) respectively.

3.4.23 E2 (Orderwire)

The WIS standard does not support the E2 octet and recommends transmitting 0×00 in place of the E2 octet. A value other than 0×00 can be transmitted by programming the intended value at TX_E1 (2×E620).

3.4.24 SPE Pointer

The H1 and H2 octets are used as a pointer within the SONET/SDH frame to locate the beginning of the path overhead and the beginning of the synchronous payload envelope (SPE). Within SONET/SDH, the SPE can begin anywhere within the payload area; however, IEEE Standard 802.3ae specifies that a transmitted SPE must always be positioned solely within a single SONET/SDH frame. The constant pointer value of 522 decimal (0x20A) must be contained in the first channel's H1 and H2 octets. Together

these conditions result in the H1 and H2 octets being 0×62 and 0×0A, respectively. These are the default values of TX_H1 (2xE615.7:0) and TX_H2 (2xE616.15:8). Programming these registers with alternate values does not alter the positioning of the SPE, but it might induce a loss of pointer (LOP-P) at the far end, or at least prevent the far end from extracting the proper payload. Furthermore, the WIS standard specifies the frame structure be a concatenated payload. For this reason, the H1 and H2 octets in channels 2 through 192 contain the concatenation indicator.

The VSC8484 device supports forcing the loss of pointer (LOP-P) and path alarm indication signal (AIS-P) state.

The WIS standard specifies that a 0x00 be transmitted in the H3 octet. An alternate value can be transmitted by programming TX_H3 (2xE616.7:0).

The WIS specification does not limit the pointer position within the receive SONET/SDH frame to allow interoperability to other SONET/SDH equipment. In addition to supporting the required SONET pointer rules, the VSC8484 device pointer interpreter optionally supports SDH pointers. This is selectable using the SDH_RX_MODE (2×EC40.11) bit. The following table lists the differences between SONET and SDH modes.

Table 29 • **SONET/SDH Pointer Mode Differences**

SONET	SDH
SS bits are ignored by the device pointer interpreter and not used	SS bits are set to 10 and are checked by the device pointer interpreter to determine the pointer type
All 192 bytes of H1 and H2 are checked by the pointer interpreter to determine the pointer type	The first 64 bytes are checked by the pointer interpreter to determine the pointer type (first Au-4 of an AU-4-64c)
Uses ‘8 out of 10’ GR-253-core objective increment/decrement rule	Uses majority detect increment/decrement rule

The H1 and H2 octets combine to form a word with several fields. For more information, see Figure 18, page 38.

3.4.25 Bit Designations within Payload Pointer

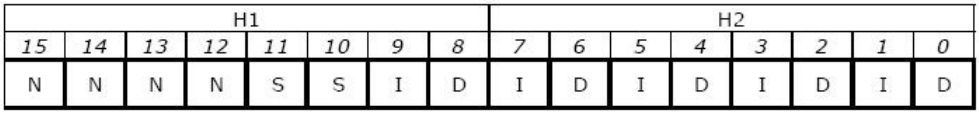
The N bits [15:12] carry a new data flag (NDF). This mechanism allows an arbitrary change in the location of the payload. NDF is indicated by at least three out of the four N bits matching the code 1001 (NDF enabled). Normal operation is indicated by three out of the four N bits matching the code 0110 (normal NDF).

The last ten bits of the pointer word (D bits and I bits) carry the pointer value. The pointer value has a range from 0 to 782 that indicates the offset between the first byte after the H3 byte and the first byte of the SPE.

The SS bits are located in bits 11 and 10 and are unused in SONET mode. In SDH mode, these bits are compared with pattern 10, and the pointer is considered invalid if it does not match.

Because the VSC8484 device only supports concatenated frames, only the first pair of bytes (H1, H2) are called the primary pointer and have a normal format. The rest of the H1/H2 bytes contain the concatenation indication (CI). The format for the CI is NDF enabled with a pointer value of all ones.

Figure 18 • **16-bit Designations within Payload Pointer**



3.4.26 Pointer Types

The VSC8484 device supports five different pointer types as described in the following table. A normal pointer indicates the current pointer, a new data flag indicates a new pointer location, and an AIS pointer indicates AIS. The pointer increment and pointer decrement mechanism adjusts the frequency offset between the frame overhead and SPE. A pointer increment is indicated by a normal NDF that has the currently accepted pointer with the I bits inverted. A pointer decrement is indicated by a normal NDF that has the currently accepted pointer with D bits inverted.

Table 30 • **H1/H2 Pointer Types**

Pointer Type	nnnn Value	Pointer Value	SS bits
Normal	Three out of the four bits matching 0110	0 to 782	Matching in SDH mode, ignored in SONET mode
New Data Flag (NDF)	Three out of the four bits matching 1001	0 to 782	Matching in SDH mode, ignored in SONET mode
AIS Pointer	1111	1111 1111 11	11
Pointer Increment	Three out of the four bits matching 0110	Current pointer with 'I' bits inverted.	Matching in SDH mode, ignored in SONET mode
Pointer Decrement	Three out of the four bits matching 0110	Current pointer with 'D' bits inverted.	Matching in SDH mode, ignored in SONET mode

Table 31 • **Concatenation Indication Types**

Pointer Type	*nnnn* Value	Pointer Value	SS bits
Normal concatenation indication	Three out of the four bits matching 1001	1111 1111 11	Matching in SDH mode, ignored in SONET mode
AIS concatenation indication	Pointer value, *nnnn* value, and SS bits are the same as the AIS pointer		
Invalid concatenation indication	Any other concatenation indication other than Normal CI or AIS CI		

3.4.27 Pointer Adjustment Rule

The VSC8484 device pointer interpreter adjusts the current pointer value according to rules listed in Section 9.1.6 of ANSI T1.105-1995. In addition, the following rule is observed: no increment/decrement is accepted for at least three frames following an increment/decrement or NDF operation.

3.4.28 Pointer Increment/Decrement Majority Rules

In SONET mode, the pointer interpreter uses more restrictive GR-253-CORE objective rules, as follows:

- An increment is indicated by eight or more bits matching non-inverted D bits and inverted I bits.
- A decrement is indicated by eight or more bits matching non-inverted I bits and inverted D bits.

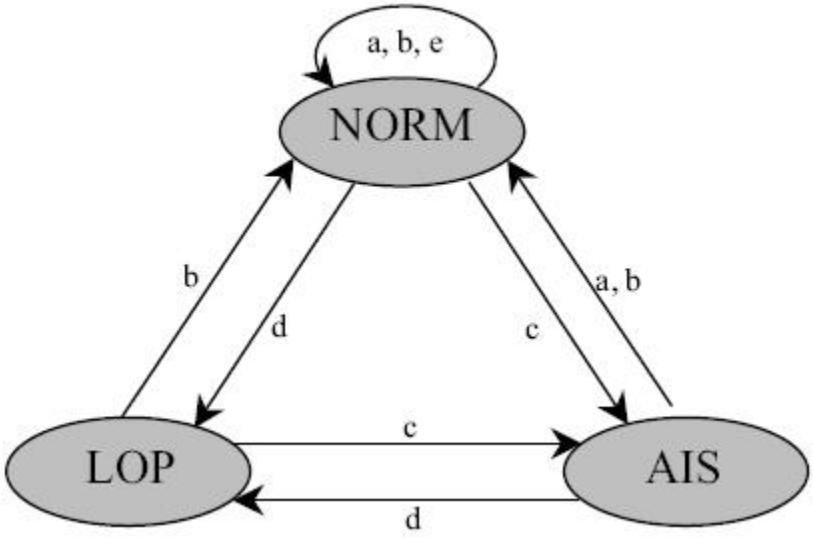
In SDH mode, the majority rules are:

- An increment is indicated by three or more inverted I bits and two or fewer inverted D bits.
- A decrement is indicated by three or more inverted D bits and two or fewer inverted I bits.
- If three or more D bits are inverted and three or more I bits are inverted, no action is taken.

3.4.29 Pointer Interpretation States

The pointer interpreter algorithm for state transitions can be modeled as a finite state machine with three states, as shown in the following illustration. The three states are normal (NORM), loss of pointer (LOP), and alarm indication state (AIS).

Figure 19 • **Pointer Interpreter State Diagram**



The conditions for transitions between these states are summarized in the following table.

Table 32 • **Pointer Interpreter State Diagram Transitions**

Transitions	States	Description	Required Persistency
a	NORM → NORM AIS → NORM	<H1><H2>=<EEEESSPP><PPPPPPPP>. NDF enabled with pointer in range (0 to 782). SS bit match (if enabled).	1 frame
b	NORM → NORM LOP → NORM AIS → NORM	<H1><H2>=<DDDDSSPP><PPPPPPPP>. NDF disabled (NORM pointer) with the same pointer value in range (0 to 782). SS bit match (if enabled).	3 frames
c	NORM → AIS LOP → AIS	<H1><H2>=<11111111><11111111>. AIS pointer (0×FFFF).	3 frames
d	NORM → LOP AIS → LOP	Anything other than transitions b and c or NDF enabled (transition a) or AIS pointer when not in AIS state or NORM pointer when not in NORM state or NORM pointer with pointer value not equal to current or increment/decrement or CONC pointer or SS bit mismatch (if comparison is enabled).	8 frames
e	Justification	Valid increment or decrement indication.	1 frame

3.4.30 Valid Pointer Definition for Interpreter State Diagram Transitions

During an AIS state, only an AIS pointer is a valid pointer. In NORM state, several definitions of “valid pointer” for the purpose of LOP detection are possible according to GR-253-CORE. The VSC8484 device follows the GR-253-CORE intended definition, but adds a single normal pointer that exactly matches the current valid pointer value.

Any change in the AIS state is reflected in the alarm bit AISP (2x0021.1). This latch-high register reports both the event and status information in consecutive reads. The AISP_PEND (2xEE00.1) bit remains asserted until read. This event can propagate an interrupt to either WIS_INTA or WIS_INTB, based on mask enable bits AISP_MASKA (2xEE01.1) and AISP_MASKB (2×EF02.1).

Similarly, any change in the LOP state is reflected in the alarm bit LOPP (2x0021.0). This latch-high register reports both the event and status information in consecutive reads. The LOPP_PEND (2xEE00.0) bit remains asserted until read. This event can propagate an interrupt to either WIS_INTA or WIS_INTB, based upon the mask enable bits LOPP_MASKA (2xEE01.1) and LOPP_MASKB (2xEE02.1).

3.4.31 Path Overhead

The path overhead portion of the SONET/SDH frame supports an end-to-end trace identifier, a payload parity check, a payload type indicator, a status indicator, and a user channel. The following table lists each of the octets, including their function.

Note: The VSC8484 device provides a mechanism to transmit a static value as programmed by the MDIO interface. However, by definition, MDIO is not fast enough to alter the octet on a frame-by-frame basis.Extended WIS TOSI and ROSI do not support path overhead.

Table 33 • **STS Path Overhead Octets**

Overhead Octet	Function	IEEE 802.3ae WIS Usage	Recommended Value	WIS Extension
J1	Path trace message	Specified value	For more information, see J1 (Overhead Octet), page 42	A 1-, 16-, or 64-byte trace message can be sent using registers (2x0027-2x002E, 2xE700, 2xEA00-2xEA17) and received using registers (2x002F-2x0036, 2xEC20, 2xEB00-2xEB17).TOSI and ROSI access.
B3	Path error monitoring (path BIP-8)	Supported	Bit interleaved parity - 8 bits, as specified in T1.416	Both SONET and SDH mode B3 calculation is supported
C2	Path signal label	Specified value	0x1A	Register (2xE615). Supports persistency and mismatch detection (2xEC40)
G1	Path status	Supported	As specified in T1.416	Ability to select between RDI-P and ERDI-P formats
F2	Path user channel	Unsupported	0x00	Register (2xE618)
H4	Multiframe indicator	Unsupported	0x00	Register (2xE61A)
Z3-Z4	Reserved for path growth	Unsupported	0x00	Register (2xE61C, 2xE61E)
N1	Tandem connection maintenance and path data channel	Unsupported	0x00	Register (2xE621). TOSI and ROSI access.

3.4.32 J1 (Overhead Octet)

By default, the J1 transmitted octet contains a 16-octet repeating path trace message whose contents are defined in J1_TXMSG (2x0027-2x002E). If no active message is being broadcast, a default path trace message is transmitted, consisting of 15 octets of zeros and a header octet formatted according to Section 5 of ANSI T1.269-2000. The header octet for the 15-octets of zero would be 0x89. The default values of J1_TXMSG (2x0027-2x002E) do not contain the 0x89 value of the header octet, thus software must write this value.

The J1 octet in the receive direction by default is assumed to be carrying a 16-octet continuously repeating path trace message. The message is extracted from the incoming WIS frames and presented in J1_RXMSG (2x002F-2x0036). The WIS receive process does not delineate the message boundaries, thus the message might appear rotated between new frame alignment events.

The VSC8484 device supports two alternate message types, a single repeating octet and a 64-octet message. The message type can be independently selected for the transmit and receive direction. The transmit direction is configured using J1_TXLEN (2xE700.1:0) whereas J1_RXLEN (2×EC20.1:0) configures the receive path.

When the transmit direction is configured for a 64-octet message, the first 16 octets are programmed in J1_TXMSG (2x0027-2x002E) whereas the 48 remaining octets are programmed in J1_TXMSG64 (2xEA00-2xEA17). Likewise, the first 16-octets of the receive message are stored in J1_RXMSG (2x002F-2x0036), whereas the other 48 octets are stored in J1_RXMSG64 (2xEB00-2xEB17). The receive message is updated every 125 µs with the recently received octet. Any persistence or message matching is expected to take place within the station manager.

3.4.33 B3 (STS Path Error Monitoring)

The B3 octet is a bit interleaved parity-8 (BIP-8) code, using even parity, calculated over the previous STS-192c SPE before scrambling. The computed BIP-8 is placed in the B3 byte of the following frame before scrambling.

In the receive direction, the incoming frame is processed and a B3 octet is calculated over the received frame. The calculated value is then compared with the B3 value received in the following frame. The difference between the calculated and received octets are accumulated in block (maximum increment of 1 per errored frame) fashion into a B3 error register, B3_CNT (2x003B). This counter is non-saturating and so rolls over. The counter is cleared upon a device reset.

An additional 32-bit B3 error counter is provided at B3_ERR_CNT (2xECB4-2xECB5), which is a saturating counter and is latched and cleared based upon a PMTICK event. Errors are accumulated starting from the previous PMTICK event. When the counter is nonzero, the B3_NZ_PEND (2xEE04.5) event is asserted until read. A non-latch high version of this event B3_NZ_STAT (2xEE03.5) is also available. This event can propagate an interrupt to either WIS_INTA or WIS_INTB, based on the mask enable bits B3_ERR_MASKA (2xEE05.5) and B3_ERR_MASKB (2xEE06.5).

The B3_ERR_CNT can optionally be configured to increment on a block count basis, a maximum increment of 1 per errored frame regardless of the number of errors received. The B3_BLK (2xEC61.9) control bit, if asserted, places the B3_ERR_CNT counter in block increment mode.

It is possible that two sets of B3 bytes (from two SONET/SDH frames) are received by the Rx WIS logic in a period of time when only one G1 octet is transmitted. In this situation, one of the two B3 error counts delivered to the Tx WIS logic is discarded. This situation occurs when the receive data rate is faster than the transmit data rate. Similarly, when the transmit data rate is faster than the receive data rate, a B3 error count is not available for REI-P insertion into the G1 octets of the transmitted SONET/SDH frame. A value of zero is transmitted in this case. This behavior is achieved by using a FIFO to transfer the detected B3 error count from the receive to transmit domains.

A FIFO overflow or underflow condition is not considered an error. Instead it is recovered from gracefully as described previously. A FIFO overflow or underflow eventually occurs, unless the transmit and receive interfaces are running at the same average data rate. Because the received and transmitted frames can differ by, at most, 40 ppm (±20 ppm) and still meet the industry standards, this “slip” can happen no more often than once every 3.1 seconds.

3.4.34 C2 (STS Path Signal Label and Path Label Mismatch)

The C2 octet contains a value intended to describe the type of payload carried within the SONET/SDH frame. The WIS standard calls for a 0×1A to be transmitted. This is the default value of TX_C2 (2xEC15).

As specified in T1.416, a path label mismatch (PLM-P) (2x0021.2) event occurs when the C2 octet in five consecutive frames contain a value other than the expected one. The expected value is set in C2_EXP (2xEC40.7:0), whose default value 0×1A is compliant with the WIS standard.

Whenever a value of 0×00 is accepted (received for five or more consecutive frames) the unequipped path pending, UNEQ_PEND (2xEE04.10), event is asserted until read. A non-latch high version of this event UNEQ_STAT (2xEE03.10) is also available. This event can propagate an interrupt to either WIS_INTA or WIS_INTB, based on the mask enable bits UNEQ_MASKA (2xEE05.10) and UNEQ_MASKB (2xEE06.10).

If the accepted value is not an unequipped label (0×00) and it differs from the programmed expected value, C2_EXP, then a path label mismatch, PLMP (2x0021.2), is asserted. Similarly the PLM_PEND (2xEE00.2) event is asserted until read. This event can propagate an interrupt to either WIS_INTA or WIS_INTB, based on the mask enable bits PLM_MASKA (2xEE01.2) and PLM_MASKB (2xEE02.2).

Although PLM-P is not a path level defect, it does cause a change in the setting of one of the ERDI-P codes. For more information, see Table 34, page 44.

3.4.35 G1 (Remote Path Error Indication)

The most significant four bits of the G1 octet is used for backreporting the number of B3 block errors received at the near end. This is typically known as path remote error indication (REI-P). The value in this octet comes from the B3 error FIFO, as discussed with the B3 octet. The WIS standard defines a 16-bit REI-P counter REIP_CNT (2x0025). The WIS standard defines this counter to operate as a block counter as opposed to an individual errored bit counter. This counter is non-saturating and so rolls over after its maximum count. The counter does not clear upon a read, but instead only upon reset as defined in the WIS specification. When the counter is nonzero, the REIP_WISNZ_PEND (2xEE04.3) event is asserted until read. A non-latch high version of this event REIP_WISNZ_STAT (2xEE03.3) is also available. This event can propagate an interrupt to either WIS_INTA or WIS_INTB, based on the mask enable bits REIP_WISNZ_MASKA (2xEE05.3) and REIP_WISNZ_MASKB (2xEE06.3), respectively.

An additional 32-bit REI-P counter is provided at REIP_ERR_CNT (2xEC80-2xEC81) which is a saturating counter and is latched and cleared based upon a PMTICK event. Errors are accumulated since the previous PMTICK event. When the counter is nonzero, the REIP_EWISNZ_PEND (2xEE04.1) event is asserted until read. A non-latch high version of this event REIP_EWISNZ_STAT (2xEE03.1) is also available. This event can propagate an interrupt to either WIS_INTA or WIS_INTB, based on the mask enable bits REIP_EWISNZ_MASKA (2xEE05.1) and REIP_EWISNZ_MASKB (2xEE06.1), respectively.

The REIP_ERR_CNT can optionally be configured to increment on a block count basis, a maximum increment of 1 per errored frame regardless of the number of errors received. This mode is enabled by asserting REIP_BLK (2xEC61.5).

3.4.36 G1 (Path Status)

In addition to backreporting the far end B3 BIP-8 error count, the G1 octet carries status information from the far end device known as path remote defect indicator (RDI-P). T1.416 allows either support of 1-bit RDI-P or 3-bit ERDI-P, but indicates ERDI-P is preferred. The VSC8484 device supports both modes and can be independently configured for the Rx and Tx directions by configuring RX_G1_MODE (2xEC40.8) and TX_G1_MODE (2xE600.10). ERDI-P is the default for both directions.

The following illustrations show the different structures for this octet.

Figure 20 • **Path Status (G1) Byte for ERDI_RDIN = 0**

G1 REI (B3)				RDI-P	Reserved		Spare
1	2	3	4	5	6	7	8
Remote Error Indicator count from B3 (0-8 value)				Remote Defect Indicator	Set to 00 by transmitter		Ignored by receiver

Figure 21 • **Path Status (G1) Byte for ERDI_RDIN = 1**

G1 REI (B3)				ERDI-P			Spare
1	2	3	4	5	6	7	8
Remote Error Indicator count from B3 (0-8 value)				Enhanced Remote Defect Indicator (see following table)			Ignored by receiver

Enhanced RDI is defined for SONET-based systems as listed in GR-253-CORE (Issue 3), reproduced here in the following table, and as a possible enhancement of SDH-based systems (G.707/Y.1322 (10/2000) Appendix VII (not an integral part of that recommendation)).

Table 34 • **RDI-P and ERDI-P Bit Settings and Interpretation**

G1 Bits 5, 6, and 7	Priority of ERDI-P Codes	Trigger	Interpretation
000/011	Not applicable	No defects.	No RDI-P defect
100/111	Not applicable	Path alarm indication signal (AIS-P). The remote device sends all ones for H1, H2, H3, and the entire STS SPE. Path loss of pointer (LOP-P).	One-bit RDI-P defect
001	4	No defects.	No ERDI-P defect
010	3	Path label mismatch (PLM-P). Path loss of code group delineation (LCD-P).	ERDI-P payload defect
101	1	Path alarm indication signal (AIS-P). The remote device sends all ones for H1, H2, H3 and entire STS SPE. Path loss of pointer (LOP-P).	ERDI-P server defect
110	2	Path unequipped (UNEQ-P). The received C2 byte is 0x00. Path trace identifier mismatch (TIM-P). This error is not automatically generated, but can be forced using MDIO.	ERDI-P connectivity defect

In the receive direction, with RX_G1_MODE (2xEC40.8) = 0, an RDI-P defect is the occurrence of the RDI-P signal in ten contiguous frames. An RDI-P defect terminates when no RDI-P signal is detected in ten contiguous frames. An RDI-P event asserts FERDIP_PEND (2xEE04.8) until read. A non-latch high version of the far-end RDI-P status can be found in FERDIP_STAT (2xEE03.8). This event can propagate an interrupt to either WIS_INTA or WIS_INTB, based on the mask enable bits FERDIP_MASKA (2xEE05.8) and FERDIP_MASKB (2xEE06.8).

When RX_G1_MODE (2xEC40.8) = 1, an ERDI-P defect is the occurrence of any one of three ERDI-P signals in 10 contiguous frames. An ERDI-P defect terminates when no ERDI-P signal is detected in 10 contiguous frames.

The 010 code triggers the latch high register bit FE_PLM-P_LCD-P (2x0021.10). It also asserts FE_PLM-P_LCD-P_PEND (2xEE00.10) until read. This event can propagate an interrupt to either

WIS_INTA or WIS_INTB, based on the mask enable bits FE_PLM-P_LCD-P_MASKA (2xEE01.10) and FE_PLM-P_LCD-P_MASKB (2xEE02.10), respectively.

The 101 code triggers the latch high register bit FE_AIS-P_LOP-P (2x0021.9). It also asserts FE_AIS-P_LOP-P_PEND (2xEE00.9) until read. This event can propagate an interrupt to either WIS_INTA or WIS_INTB, based on the mask enable bits FE_AIS-P_LOP-P_MASKA (2xEE01.9) and FE_AIS-P_LOP-P_MASKB (2xEE02.9), respectively.

The 110 code asserts the FE_UNEQ-P_PEND (2xEE04.9) until read. A non-latch-high version of this register FE_UNEQ_STAT (2xEE03.9) is also available. This event can propagate an interrupt to either WIS_INTA or WIS_INTB, based on the mask enable bits FE_UNEQ-P_MASKA (2xEE05.9) and FE_UNEQ-P_MASKB (2xEE06.9), respectively.

3.4.37 F2 (Path User Channel)

The WIS standard does not support the F2 octet and recommends transmitting 0×00 in place of the F2 octet. A value other than 0×00 can be transmitted by programming the intended value at TX_F2 (2xE618).

3.4.38 H4 (Multiframe Indicator)

The WIS standard does not support the H4 multiframe octet and recommends transmitting 0×00 in place of the H4 octet. A value other than 0×00 can be transmitted by programming the intended value at TX_H4 (2xE61A).

3.4.39 Z3-Z4 (Reserved for Path Growth)

The WIS standard does not support the Z3-Z4 octets and recommends transmitting 0×00 in their place. A value other than 0×00 can be transmitted by programming the intended value at TX_Z3 (2xE61C) and TX_Z4 (2xE61E) respectively.

3.4.40 N1 (Tandem Connection Maintenance/Path Data Channel)

The WIS standard does not support the N1 octet and recommends transmitting 0×00 in place of the N1 octet. A value other than 0×00 can be transmitted by programming the intended value at TX_N1 (2xE621).

3.4.41 Loss of Code Group Delineation

After the overhead is stripped, the payload is passed to the PCS. If the PCS block losses synchronization and cannot delineate valid code groups, the PCS passes a loss of code group delineation (LCD-P) alarm to the WIS. This alarm triggers the latch high register bit LCD-P (2x0021.3). It also asserts LCD-P_PEND (2xEE00.3) until read. This event can propagate an interrupt to either WIS_INTA or WIS_INTB, based on the mask enable bits LCD-P_MASKA (2xEE01.3) and LCD-P_MASKB (2xEE02.3), respectively.

The WIS specification calls for a LCD-P defect persisting continuously for more than 3 ms to be back reported to the far end. Upon device reset, a LCD-P is back reported until the PCS signals that valid code groups are being delineated. The LCD-P defect deasserts (and is not backreported) after the condition is absent continuously for at least 1 ms.

3.4.42 Reading Statistical Counters

The VSC8484 device contains several counters that can be read using the MDIO interface. For each error count, there are two sets of counters. The first set is the standard WIS counter implemented according to IEEE Standard 802.3ae, and the second set is for statistical counts using PMTICK.

To read the IEEE Standard 802.3ae counters, the station manager must read the most significant register of the 32-bit counter first. This read action latches the internal error counter value into the MDIO readable registers. A subsequent read of the least significant register does not latch new values, but returns the value latched at the time of the most significant register read.

Because the IEEE Standard 802.3ae counters are independently latched, it can be difficult to get a clear picture of the timeframes in which errors were received. The PMTICK counters are all latched together, thereby providing a complete snapshot in time. When PMTICK is asserted the internal error counter values are copied into their associated registers and the internal counters are reset.

There are three methods of asserting PMTICK.

- The station manager can asynchronously assert PMTICK_FRC (2xEC60.0) to latch the values at a given time, regardless of the PMTICK_ENA (2xEC60.2) setting.
- The VSC8484 device can be configured to latch and clear the statistical counters at a periodic interval as determined by the timer (count) value in PMTICK_DUR (2xEC60.15:3). In this mode the PMTICK_SRC (2xEC60.1) must be configured for internal mode and the PMTICK_ENA (2xEC60.2) bit must be asserted. The receive path clock is used to drive the PMTICK counter, thus the periodicity of the timer can vary during times of loss of lock and loss of frame.
- The VSC8484 device can be configured to latch and clear the statistical counters at the occurrence of a rising edge detected at a GPIO pin configured as a PMTICK input pin. In this mode the PMTICK_SOURCE (2xEC60.1) bit must be deasserted, and the PMTICK_ENA (2xEC60.2) must be asserted. Corresponding GPIO must be configured as the PMTICK input pin.

Regardless of PMTICK_SRC (2xEC60.1), when the PMTICK event occurs the PMTICK_PEND (2xEE04.14) is asserted until read. This event can propagate an interrupt to either WIS_INTA or WIS_INTB, based on the mask enable bits PMTICK_MASKA (2xEE05.14) and PMTICK_MASKB (2xEE06.14), respectively.

Given the size of the error counters and the maximum allowable error counts per frame, care must be taken in the frequency of polling the registers to ensure accurate values. All PMTICK counters saturate at their maximum values.

Table 35 • **PMTICK Counters**

Counter Name	Description	Registers	Maximum Increase Count Per Frame	Maximum Increase Count Per Second	Time Until Overflow
B1_ERROR_CNT	B1 section error count	B1_ERROR_CNT1, B1_ERROR_CNT0	8	64,000	67,109
B2_ERROR_CNT	B2 line error count	B2_ERROR_CNT1, B2_ERROR_CNT0	1536	12,288,000	350
B3_ERROR_CNT	B3 path error count	B3_ERROR_CNT1, B3_ERROR_CNT0	8	64,000	67,109
FAR_B3_ERROR_CNT	Far end B3 path error count	FAR_B3_ERROR_CNT1, FAR_B3_ERROR_CNT0	8	64,000	67,109
FAR_B2_ERROR_CNT	Far end B2 line error count	FAR_B2_ERROR_CNT1, FAR_B2_ERROR_CNT0	1536	12,288,000	350

Both individual and block mode accumulation of B1, B2, and B3 error indications are supported and selectable using the control bits B1_BLK, B2_BLK, and B3_BLK. In individual accumulation mode, 0, the counter is incremented for each bit mismatch between the calculated B1, B2, and/or B3 error and the extracted B1, B2, and/or B3. In block accumulation mode, 1, the counter is incremented only once for any nonzero number of bit mismatches between the calculated B1, B2, and/or B3 and the extracted B1, B2, and/or B3 (maximum of one error per frame).

3.4.43 Defects and Anomalies

All defects and anomalies listed in the following table can be forced and masked by the user. The VSC8484 device does not automatically generate TIM-P, but does support forcing defects using MDIO.

Table 36 • **Defects and Anomalies**

Defect or Anomaly	Description	Type	Force Bit	Status Bit
Far end PLM-P or LCD-P	These two errors are indistinguishable when reported by the far end through the G1 octet (ERDI-P), because the far end reports both PLM-P and LCD-P with the same error code.	Far-end defect	2xEC31.10	2x0021.10
Far end AIS-P or LOP-P	These two errors are indistinguishable when reported by the far end through the G1 octet (ERDI-P), because the far end reports both AIS-P and LOP-P with the same error code.	Far-end defect	2xEC31.12	2x0021.9
PLM-P	Path label mismatch. The detection and reporting of the PLM-P defect follows section 7.5 of ANSI T1.416-1999.	Near-end defect; propagated to PCS	2xEC31.14	2x0021.2
AIS-L	Generated on LOPC, LOS, LOF, if enabled by RXAISL_ON_LOPC (2xEDFF.6), RXAISL_ON_LOS (2xEDFF.5), RXAISL_ON_LOF (2xEDFF.4), or when forced by user.	Near-end defect	The AIS-L defect is only processed and reported by the WIS Receive process; it is never transmitted by the WIS Transmit process according to IEEE 802.3ae.	2xEC30.3/2 x0021.4
AIS-P	Path alarm indication signal.	Near-end defect; propagated to PCS	2xEC30.1	2x0021.1
LOP-P	Path loss of pointer. Nine consecutive invalid pointers result in loss of pointer detection. See Figure 19, page 40 for the pointer interpreter state machine.	Near-end defect; propagated to PCS	2xEC30.0	2x0021.0
LCD-P	Path loss of code group delineation. See Table 34, page 44. This is also reported to the far end if it persists for at least 3 ms.	Near-end defect	2xEC31.2	2x0021.3
LOPC	Loss of optical carrier alarm. This is an input from the XFP module's loss of signal output. The polarity can be inverted for use with other module types. This defect can be used independently or in place of LOS.	Near-end defect	2xEC30.12	2xEE03.11

Table 36 • **Defects and Anomalies *(continued)***

LOS	The PMA circuitry detects a Loss Of Signal (LOS) defect if the input signal falls below the assert threshold. When a PMA LOS is declared the framer is held in reset to prevent it from looking for a frame boundary.	Near-end defect	2xEC30.11	2x0021.6
SEF	Severely errored frame. Generated when device cannot frame to A1 A2 pattern. SEF indicates synchronization process is not in the SYNC state, as defined by the state diagram of IEEE 802.3ae clause 50.4.2.	Near-end defect; propagated to PCS	2xEC31.7	2x0021.11
LOF	Generated when SEF persists for 3 ms. Terminated when no SEF occurs for 1 ms to 3 ms.	Near-end defect	2xEC31.6	2x0021.7
B1 PMTICK error count is nonzero	BIP-N(S) 32-bit near-end section BIP error counter is nonzero.	Near-end anomaly	2xEC31.5	2xEE03.7
B2 PMTICK error count is nonzero	BIP-N(L) 32-bit near-end line BIP error counter is nonzero.	Near-end anomaly	2xEC31.4	2xEE03.6
B3 PMTICK error count is nonzero	BIP-N(P) 32-bit near-end path BIP error counter is nonzero.	Near-end anomaly	2xEC31.3	2xEE03.5
REI-L	Line remote error indicator octet is nonzero. Far end BIP-N(L).	Far-end anomaly	2xEC31.8	2xEE03.4
REI-L PMTICK error count is nonzero	Line remote error indicator is nonzero. Far-end BIP-N(L).	Far-end anomaly	2xEC31.1	2xEE03.2
RDI-L	Line remote defect indicator.	Far-end defect	2xEC30.2	2x0021.5
REI-P	Path remote error indicator octet is nonzero. Far-end BIP-N(P).	Far-end anomaly	2xEC31.9	2xEE03.3
REI-P PMTICK error count is nonzero	Path remote error indicator. Far end BIP-N(P).	Far-end anomaly	2xEC31.0	2xEE03.1
UNEQ-P	Unequipped path.	Near-end defect	2xEC31.15	2xEE03.10
Far end UNEQ-P	Far-end unequipped path.	Far-end defect	2xEC31.11	2xEE03.9

3.4.44 Interrupt Pins and Interrupt Masking

The VSC8484 device generates interrupts for each defect and anomaly. The interrupts for the BIP error counts (B1, B2, and B3 counters) and the interrupts for the far end error counts (REI-L and REI-P) are generated when the PMTICK counters become nonzero. Mask enable bits propagate the interrupt

pending event to the pins WIS_INTA and WIS_INTB. Each event can be optionally masked for each WIS_INTA/B pin.

The WIS_INTA and WIS_INTB are routed off-device through GPIO pins. Many specialized functions share the GPIO pins. The WIS_INTA and WIS_INTB signals do not go to dedicated pins.

For each defect or anomaly defined in IEEE 802.3ae, the VSC8484 device supports the standard WIS register. In addition the VSC8484 device supports another set of registers in the WIS Vendor Specific area. These registers provide a STATUS bit to indicate the current real-time status of the event, a PENDING bit to indicate if the STATUS bit has changed state, and two mask enable bits for each interrupt pin (WIS_INTA and WIS_INTB). The STATUS bit is set if and only if the interrupt currently exists. This STATUS bit does not latch.

The defects and anomalies are constructed in a hierarchy such that lower order alarms are squelched when higher order events are detected. For more information about the dependencies between squelches and events, see the WIS interrupt registers.

3.4.45 Overhead Serial Interfaces

The VSC8484 device includes provisions for off-device processing of the critical SONET/SDH transport overhead 9-bit words through two independent serial interfaces. The transmit overhead serial interface (TOSI) is used to insert 9-bit words into the transmit frames, and the receive overhead serial interface (ROSI) is used to recover the 9-bit words from the received frames. The interfaces each consists of three pins: a clock output, a frame pulse output, and a data input (Tx) /output (Rx). These I/O are LVTTL compatible for easy connection to an external device such as an FPGA.

Note: Extended WIS TOSI and ROSI do not support path overhead bytes.

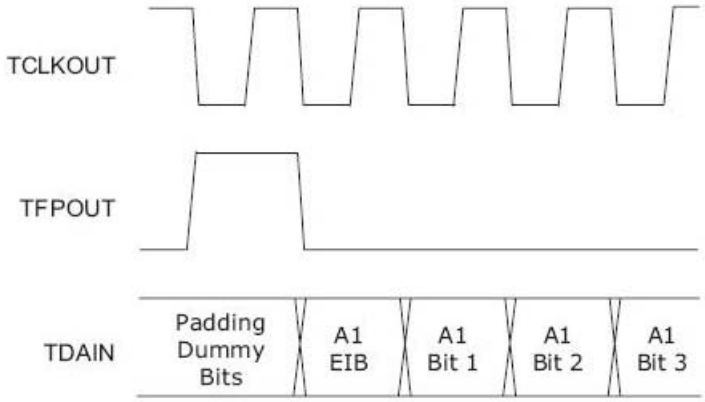
The TOSI / ROSI signals are routed off-device through GPIO pins. There is an extremely limited number of GPIO pins. IF the ROSI/TOSI interfaces are to be used, there are no GPIO pins available for any other function such as loss-of-lock for Sync-E applications, activity LED drivers, WIS_interrupts, or two-wire serial (slave) interface.

All references to TCLKOUT, TFPOUT, TDAIN, RCLKOUT, RFPOUT and RDAOUT are the TOSI/ROSI signals routed through GPIO package pins.

3.4.46 Transmit Overhead Serial Interface (TOSI)

The TOSI port enables the user to individually program 222 separate 9-bit words in the SONET/SDH overhead. The SONET/SDH frame rate is 8 kHz as signaled by the frame pulse (TFPOUT) signal. The TOSI port is clocked from a divided-down version of the WIS transmit clock made available on TCLKOUT. To provide a more standard clock rate, 9-bit dummy words are added per frame resulting in a clock running at one five-hundred-twelfth of the line rate or 19.44 MHz. For each 9-bit word, the external device indicates the desire to transmit that byte by using an enable indicator bit (EIB) that is appended to the beginning of the 9-bit word. If EIB = 0, the data on the serial interface is ignored for that overhead 9-bit word. If EIB = 1, the serial interface data takes precedence over the value generated within the VSC8484 device. The EIB is present before the 9-bit dummy words too, however its value has no effect as the 9-bit dummy words are ignored within the device. The first EIB bit should be transmitted by the external device on the first rising edge of TCLKOUT after TFPOUT, as illustrated in the following illustration. The data should be provided with the most significant bit (MSB) first. After reception of the TOSI data for a complete frame, the values are placed in the overhead for the next transmitted frame.

Figure 22 • **TOSI Timing Diagram**



Some 9-bit words are error masks, such that the transmitted 9-bit word is the XOR of the TOSI 9-bit word and the predefined value within the device if the EIB is enabled. This feature is best used for test purposes only.

The order of the 9-bit word required by the TOSI port is summarized in the following table, where the number of registers is the number of bytes on the serial interface and the number of bytes is the number of STS channels on which the byte is transmitted. For H1 and H2 pointers, bytes 2 to 192 are concatenation indication bytes consistent with STS-192c frames. There are not 192 different point locations as in STS-192 frames.

Table 37 • **TOSI/ROSI Addresses**

Byte Name	9-Bit Word	TOSI/ ROSI Byte Order	Number of Registers	Number of Bytes	Type
Frame Boundary	A1	0	1	192	Programmable byte that is identical for all locations
Frame Boundary	A2	1	1	192	Programmable byte that is identical for all locations
Section Trace	J0	2	1	1	Programmable byte
Section Growth	Z0	3	1	191	Programmable byte that is identical for all locations
Dummy Byte		4	1	1	Programmable byte
Section BIP-8	B1	5	1	1	TOSI inserts error mask; ROSI extracts XOR of B1 value and received data
Orderwire	E1	6	1	1	Programmable byte
Section User Channel	F1	7	1	1	Programmable byte
Dummy Byte		8	1	1	Programmable bytes
Section DCC 1	D1	9	1	1	Programmable byte
Section DCC 2	D2	10	1	1	Programmable byte
Section DCC 3	D3	11	1	1	Programmable byte
Dummy Byte		12	1	1	Programmable byte
Pointer 1	H1	13	1	1	Programmable byte affecting the first H1 byte

Table 37 • **TOSI/ROSI Addresses *(continued)***

Byte Name	9-Bit Word	TOSI/ ROSI Byte Order	Number of Registers	Number of Bytes	Type
Pointer 2	H2	14	1	1	Programmable byte affecting the first H2 byte
Pointer Action	H3	15	1	192	Programmable byte that is identical for all locations
Dummy Byte		16	1	1	Programmable byte
Line BIP-8	B2	17 to 208	192	192	TOSI inserts error mask for each byte; ROSI extracts XOR of B2 value and received data for each byte
Automatic Protection Switching (APS) channel and Remote Defect Indicator (RDI)	K1	209	1	1	Programmable byte
Automatic Protection Switching (APS) channel and Remote Defect Indicator (RDI)	K2	210	1	1	Programmable byte
Dummy Byte		211	1	1	Programmable byte
Line DCC 4	D4	212	1	1	Programmable byte
Line DCC 5	D5	213	1	1	Programmable byte
Line DCC 6	D6	214	1	1	Programmable byte
Dummy Byte		215	1	1	Programmable byte
Line DCC 7	D7	216	1	1	Programmable byte
Line DCC 8	D8	217	1	1	Programmable byte
Line DCC 9	D9	218	1	1	Programmable byte
Dummy Byte		219	1	1	Programmable byte
Line DCC 10	D10	220	1	1	Programmable byte
Line DCC 11	D11	221	1	1	Programmable byte
Line DCC 12	D12	222	1	1	Programmable byte
Dummy Byte		223	1	1	Programmable byte
Synchronization Message	S1	224	1	1	Programmable byte
Growth 1	Z1	225	1	191	Programmable byte that is identical for all locations
Growth 2	Z2	226	1	190/191	Programmable byte that is identical for all locations; dependent upon 2xEC40.12
STS-1 REI-L	M0	227	1	1	Programmable byte
STS-N REI-L	M1	228	1	1	Programmable byte
Orderwire 2	E2	229	1	1	Programmable byte
Dummy Byte		230	1	1	Programmable byte

Table 37 • **TOSI/ROSI Addresses *(continued)***

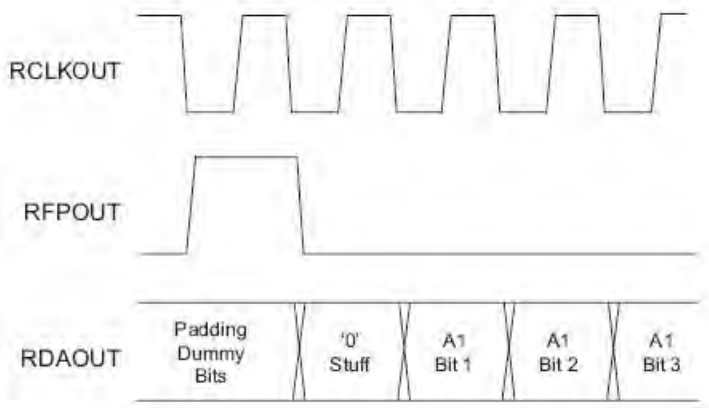
Byte Name	9-Bit Word	TOSI/ ROSI Byte Order	Number of Registers	Number of Bytes	Type
Padding Dummy Bytes		231 to 269	39		No function

3.4.47 Receive Overhead Serial Interface (ROSI)

The ROSI port extracts the same 222 overhead 9-bit words from the SONET/SDH frame, and consists of the clock output (RCLKOUT), frame pulse output (RFPOUT), and data output (RDAOUT). The ROSI port is clocked from a divided-down version of the WIS receive clock, and is valid during in-frame conditions only. As with the TOSI port, 9-bit dummy words are provided each frame period resulting in a 19.44 MHz RCLKOUT frequency. For each 9-bit word, including the 9-bit dummy words, an extra '0' bit is stuffed at the beginning of each byte so that the TOSI and ROSI clock rates are identical. The first stuff bit for each frame is transmitted by RDAOUT on the first rising edge of RCLKOUT after the frame pulse (RFPOUT), as illustrated in the following illustration.

Because the receive path overhead can be split across two frames, the VSC8484 device buffers the overhead for an additional frame time so that a complete path overhead is presented. For more information about the order for each of the 9-bit words presented on the ROSI port, see Table 37, page 50. With the exception of the M0/M1 9-bit words, the extracted 9-bit words are from the first channel position. In place of parity and error 9-bit words, the VSC8484 device outputs the result of an XOR between the calculated BIP and the received value. Therefore, a count of ones within each of the BIP 9-bit words should correspond with the internal error accumulators. The following illustration shows the functional timing for the ROSI port.

Figure 23 • **ROSI Timing Diagram**



3.4.48 Pattern Generator and Checker

The VSC8484 device implements the square wave, PRBS31, and mixed-frequency test patterns as described in section 50.3.8 of IEEE Standard 802.3ae, the test signal structure (TSS), and continuous identical digits (CID) pattern.

The square wave pattern is selected asserting WIS_TEST_PAT_SEL (2x0007.3), and the generator is enabled by asserting WIS_TEST_PAT_GEN (2x0007.1). When WIS_TEST_PAT_SEL (2x0007.3) is deasserted the mixed frequency test pattern is selected. The square wave frequency is configured according to SQ_WV_PW (2xE600.7:4). The WIS_TEST_PAT_ANA (2x0007.2) bit is used to enable the test pattern checker in the receive path. The checker does not operate on square wave receive traffic. Error counts from the mixed frequency pattern are presented in the SONET/SDH BIP-8 counters, B1_CNT (2x003C), B2_CNT (2x0039), and B3_CNT (2x003B).

The VSC8484 device supports the PRBS31 test pattern as reflected in PRBS31_SUPPORT (2x0008.1). The transmitter/generator is enabled by asserting WIS_TEST_PRBS_GEN (2x0007.4) whereas the receiver/checker is enabled by asserting WIS_TEST_PRBS_ANA (2x0007.5). As the mixed frequency/square wave test patterns have priority over the PRBS31 pattern, TEST_PAT_GEN (2x0007.1) must be disabled for the PRBS31 test pattern to be sent. Error counts from the PRBS31 checker are available in WIS_TEST_PAT_CNT (2x0009). This register does not roll over after reaching its maximum count and is cleared after every read operation. Two status bits are available from the PRBS checker. The PRBS_NZ (2xEC51.1) bit indicates whether the error counter is nonzero. The PRBS_SYNC (2xEC51.0) bit if asserted indicates that checker is synchronized and actively checking received bits. For test purposes, the PRBS generator can inject single bit errors. By asserting PRBS_INJ_ERR (2xEC50.1), a single bit error is injected, resulting in three bit errors being detected within the checker. The value of three comes from the specification, which indicates one error should be detected for each tap within the checker.

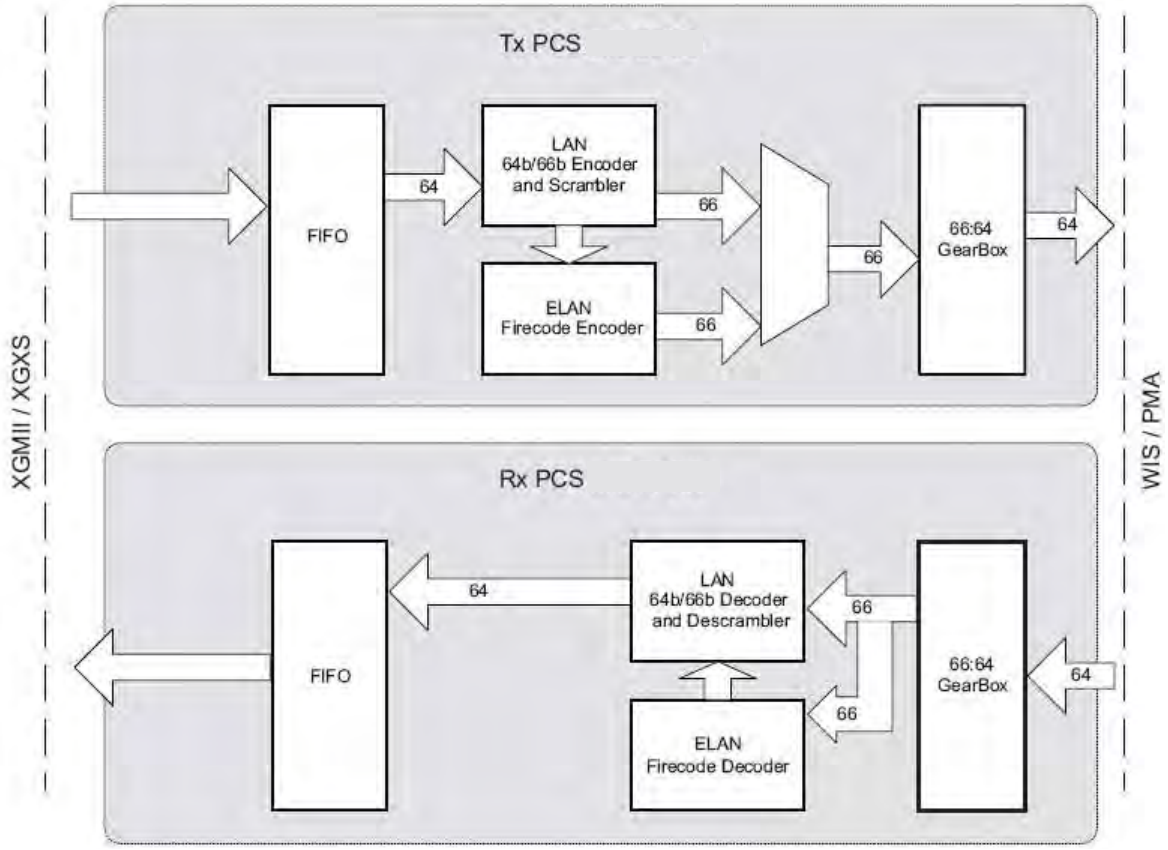
3.5 Physical Coding Sublayer (64B/66B PCS)

The physical coding sublayer (PCS) is defined in IEEE 802.3ae Clause 49. It is composed of the PCS transmit, PCS receive, block synchronization, and BER monitor processes. The PCS functions can be further broken down into encode or decode, scramble or descramble, and gearbox functions, as well as various test and loopback modes.

The PCS is responsible for transferring data between the XAUI clock domain and the WIS/PMA clock domain. In addition, the PCS encodes and scrambles the data for efficient transport across the given medium.

The following illustration shows how the PCS connects the XAUI blocks to the WIS/PMA blocks.

Figure 24 • **PCS Block Diagram**



3.5.1 Control Codes

The VSC8484 device supports the use of all control codes and ordered sets necessary for 10 GbE and 10 GFC operation. The following table lists the control characters, notation, and control codes.

Table 38 • **Control Codes**

Control Character	Notation[1]	XGMII Control Code	10-G BASE-R Control Code	10-G BASE-R O Code	8b/10b Code[2]
Idle	/I/	0×07	0×00		K28.0 or K28.3 or K28.5
Start	/S/	0×fb	Encoded by block type field		K27.7
Terminate	/T/	0×fd	Encoded by block type field		K29.7
Error	/E/	0×fe	0×1e		K30.7
Sequence ordered_set	/Q/	0×9c	Encoded by block type field plus O code	0×0	K28.4
Reserved 0	/R/	0×1c	0×2d		K28.0
Reserved 1		0×3c	0×33		K28.1
Reserved 2	/A/	0×7c	0×4b		K28.3
Reserved 3	/K/	0×bc	0×55		K28.5
Reserved 4		0×dc	0×66		K28.6
Reserved 5		0×f7	0×78		K23.7
Signal ordered_set[3]	/Fsig/	0×5c	Encoded by block type field plus O code	0×F	K28.2

1. The codes for /A/, /K/ and /R/ are used on the XAUI interface to signal idle.
2. The 8b/10b code is specified in Clause 36. Usage of the 8b/10b code for 10 Gbps operation is specified in Clause 4.
3. Reserved for INCITS T11 - 10 GFC.

3.5.2 Transmit Path

In the transmit direction, the PCS accepts data from the XGXS interface, which runs off the XAUI recovered clock and transfers the data onto the PMA transmit clock domain, through the rate-disparity compensating FIFO. Based on the FIFO's fill level, idle characters are added or removed as needed.

The deserialized XAUI input data (64-bit) is checked for validity in the PMA clock domain. Transmitted data is handled according to IEEE Standard 802.3ae Clause 49.

The characters are then processed in a two-step manner. First the 64-bits are encoded and a 2-bit header is calculated to form a single 66-bit block. The two header bits are used for block delineation and classification. The only valid header codes are 01 to indicate a payload of all data octets and 10 to indicate the presence of one or more control characters within the payload. The second step is to maintain a DC-balanced signal on the serial line, thus the 64-bit encoded payload is scrambled using a self-synchronizing scrambler that implements the polynomial $G(x) = 1 + x^{39} + x^{58}$. The header bits are not scrambled as they are already DC balanced. For debug purposes, the scrambler can be disabled by deasserting SCR_DIS (3x8005.9).

The 66-bit blocks are then passed to the PMA through a 66:64 gearbox. The gearbox merely feeds the 66-bit data into the WIS/PMA's 64-bit data path.

3.5.3 Receive Path

In the receive direction, the PCS accepts data from the WIS/PMA block and reformats it for transmission to the XGXS interface. Because of the data path width mismatches between the WIS/PMA and the PCS, a 64:66 gearbox is needed. The gearbox also performs block synchronization/alignment based upon the 2-bit synchronization header. When the receive logic receives 64 continuous valid sync headers the BLOCK_LOCK (3x0021.15) bit is asserted. This bit is a latch-low bit; therefore, a second read of the bit returns the current status. If 16 invalid block sync. headers are detected within a 125 µs period, the PCS_HIGHBER (3x0021.14) bit is asserted. This bit is a latch-high bit, and therefore a second read of the bit returns the current status.

After block synchronization is achieved, the occurrence of errored blocks are accumulated in the PCS_ERRORED_BLOCKS (3x0021.7:0) counter. An errored block is one that has one or more of the following defects:

The sync field has a value of 00 or 11.

The block type field contains a reserved value. For more information, see Table 38, page 54.

Any control character contains an incorrect value.

Any O code contains an incorrect value.

The set of eight XGMII characters does not have a corresponding block format shown in the following illustration.

Figure 25 • **64B/66B Block Formats**

Input Data	**Sync**	**Block Payload**							
Bit Position: / Data Block Format:	0 1	2							65
D0 D1 D2 D3/D4 D5 D6 D7	01	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
Control Block Formats:		**Block Type Field**							
C0 C1 C2 C3/C4 C5 C6 C7	10	0x1e	C_0	C_1	C_2	C_3	C_4	C_5	C_6	C_7
C0 C1 C2 C3/O4 D5 D6 D7	10	0x2d	C_0	C_1	C_2	C_3	O_4	D_5	D_6	D_7
C0 C1 C2 C3/S4 D5 D6 D7	10	0x33	C_0	C_1	C_2	C_3		D_5	D_6	D_7
O0 D1 D2 D3/D4 D5 D6 D7	10	0x66	D_1	D_2	D_3	O_0		D_5	D_6	D_7
O0 D1 D2 D3/O4 D5 D6 D7	10	0x55	D_1	D_2	D_3	O_0	O_4	D_5	D_6	D_7
S0 D1 D2 D3/D4 D5 D6 D7	10	0x78	D_1	D_2	D_3	D_4	D_5	D_6	D_7
O0 D1 D2 D3/C4 C5 C6 C7	10	0x4b	D_1	D_2	D_3	O_0	C_4	C_5	C_6	C_7
T0 C1 C2 C3/C4 C5 C6 C7	10	0x87		C_1	C_2	C_3	C_4	C_5	C_6	C_7
D0 T1 C2 C3/C4 C5 C6 C7	10	0x99	D_0		C_2	C_3	C_4	C_5	C_6	C_7
D0 D1 T2 C3/C4 C5 C6 C7	10	0xaa	D_0	D_1		C_3	C_4	C_5	C_6	C_7
D0 D1 D2 T3/C4 C5 C6 C7	10	0xb4	D_0	D_1	D_2		C_4	C_5	C_6	C_7
D0 D1 D2 D3/T4 C5 C6 C7	10	0xcc	D_0	D_1	D_2	D_3		C_5	C_6	C_7
D0 D1 D2 D3/D4 T5 C6 C7	10	0xd2	D_0	D_1	D_2	D_3	D_4		C_6	C_7
D0 D1 D2 D3/D4 D5 T6 C7	10	0xe1	D_0	D_1	D_2	D_3	D_4	D_5		C_7
D0 D1 D2 D3/D4 D5 D6 T7	10	0xff	D_0	D_1	D_2	D_3	D_4	D_5	D_6	

Valid blocks then recover their original payload data by being descrambled. The descrambler is the same polynomial as used by the transmitter. For test purposes, the descrambler can be disabled by asserting DSCR_DIS (3x8005.10). The data is checked for valid characters and sequencing.

The data is passed from the PMA/WIS clock domain to the XAUI clock domain through a FIFO. Based upon the FIFO's fill level, idle characters are added or removed as needed.

3.5.4 PCS Standard Test Modes

The PCS block offers all of the standard defined test pattern generators and analyzers. In addition, the VSC8484 device supports a 64-bit static user pattern and the optional PRBS31 pattern. Two error counters are available. Each are saturating counters and cleared upon a read operation. The first, PCS_ERR_CNT (3x002B), is located in the IEEE Standard area whereas the 32-bit, PCS_VSERR_CNT (3x8007-3x8008), is located in the vendor specific area.

The IEEE specification defines two test pattern modes, a square wave generator and a pseudorandom test pattern. The square wave generator is enabled by first selecting the square wave pattern by asserting PCS_TSTPAT_SEL (3x002A.1), and then enabling the test pattern generator PCS_TSTPAT_GEN (3x002A.3). The period of the square wave can be controlled in terms of bit times by writing to PCS_SQPW (3x8004) There is no associated square wave checker within the VSC8484 device. The pseudorandom test pattern is selected by deasserting PCS_TSTPAT_SEL (3x002A.1). The pseudorandom test pattern contains two data modes. When PCS_TSTDAT_SEL (3x002A.0) is deasserted, the pseudorandom pattern is a revolving series of four blocks with each block 128-bits in length. The four blocks are the resultant bit sequence produced by the PCS scrambler when preluded with the following seeds:

- PCS_SEEDA (3x0022-3x0025)
- PCS_SEEDA invert
- PCS_SEEDB (3x0026-3x0029)
- PCS_SEEDB invert

The pattern generator is enabled by asserting PCS_TSTPAT_GEN (3x002A.3), and the analyzer is enabled by asserting PCS_TSTPAT_ANA (3x002A.2). Errors are accumulated in the clear-on-read saturating counter, PCS_ERR_CNT (3x002B). In pseudorandom pattern mode, the error counter counts the number of errored blocks.

Support for the optional PRBS31 pattern is indicated by PCS_PRBS31_ABILITY (3x0020.2) whose default is high. The PRBS31 test generator is selected by asserting PCS_PRBS31_GEN (3x202A.4) whereas the checker is enabled, by asserting PCS_PRBS31_ANA (3x202A.5). IEEE standards specify that the error counter should increment for each linear feedback shift register (LFSR) tap that a bit is in error. Therefore, a single bit error increments the counter by three as there are three taps in the PRBS31 polynomial.

The user defined 64-bit static pattern can be written to PCS_USRPAT (3x8000-3x8003) and enabled by asserting PCS_USRPAT_ENA (3x8005.0) and PCS_TSTPAT_GEN (3x002A.3). Enabling the user-defined pattern enables both the generator and analyzer.

3.5.5 PCS XGMII BIST

In addition to the IEEE standard test modes, an onboard XGXS pattern generator/checker pair is located at the XGXS/PCS interface.

Depending on datapath loopback settings, the pattern can be transmitted towards the XFI or the XAUI ports, and checked from either port.

The generator sends a repeating cycle of /S/, followed by PRBS 31 payload, followed by /T/, followed by interpacket gap (IPG) consisting of series of idle /I/ bytes.

- Register 3xE61B controls the length of the IPG and the length of the payload.
- Bits 15:8 control the payload length. The length of the payload, in bytes, is equal to 64 times this value.
- Bits 7:0 control the IPG length. The length of the IPG, in bytes, is equal to 4 times this value.

The pattern checker extracts and checks the PRBS payload. /S/, /T/ and any characters in the IPG are ignored to allow for flexible IPG, which can change during rate compensation blocks in the datapath.

The 16-bit error counter at 3xE61C increments three times for every corrupted payload bit. This is a non-rollover counter.

The generator and checker are controlled by 3xE61A. The generator is started/stopped with bit 0, and the checker is started/stopped with bit 1. The error counter can be cleared with bit 2. The error counter automatically clears each time the checker is enabled (each time 3xE61A.1 transitions from 0 to 1).

The checker status bits are in 3xE61D and are defined as follows:

Table 39 • **Checker Status Bits**

Bit	Name	Description
4	Sync	Asserted when PRBS payload is error free for 128 bits after checker started
3	Fail	Asserted upon the first bit error
2	ECF	Asserted when Error Counter is Full
1	SyncErr	Asserted if checker is turned on, then off, and Sync never occurred
0	Busy	Asserted when the checker is turned on

When the checker is started, bits 4:1 are initialized to zero, and bit 0 is asserted.

During the time the checker is enabled, the status register contains a live value.

When the checker is stopped, bit 0 is deasserted, and bits 4:1 contain the status at the time the checker was stopped. Bits 4:1 will remain in that state until the checker is restarted (or a reset is issued).

The following table lists the nine possible states for the status register.

Table 40 • **Status Register States**

State	Hex Read Value	Condition
Sync = 0 Fail = 0 ECF = 0 SyncErr = 0 Busy = 0	0x0000	Checker never started.
Sync = 0 Fail = 0 ECF = 0 SyncErr = 0 Busy = 1	0x0001	Checker started but not synced to payload.
Sync = 1 Fail = 0 ECF = 0 SyncErr = 0 Busy = 1	0x0011	Checker started, synced to payload, and no bit errors encountered.
Sync = 1 Fail = 1 ECF = 0 SyncErr = 0 Busy = 1	0x0019	Checker started, synced to payload, and at least one bit error encountered.
Sync = 1 Fail = 1 ECF = 1 SyncErr = 0 Busy = 1	0x001D	Checker started, synced to payload, and enough bit errors counted to saturate the error counter.

Table 40 • **Status Register States *(continued)***

State	Hex Read Value	Condition
Sync = 1 Fail = 0 ECF = 0 SyncErr = 0 Busy = 0	0x0010	Checker disabled with no bit errors during the last test cycle.
Sync = 0 Fail = 0 ECF = 0 SyncErr = 1 Busy = 0	0x0002	Checker disabled and never synced to the payload during the last test cycle.
Sync = 1 Fail = 1 ECF = 0 SyncErr = 0 Busy = 0	0x0018	Checker disabled with at least one bit error encountered during last test cycle.
Sync = 1 Fail = 1 ECF = 1 SyncErr = 0 Busy = 0	0x001C	Checker disabled and error counter saturated during last test cycle.

3.6 Client/Host Interface (XAUI)

The client/host interface (XAUI) interface supports the following rates:

- 10 Gbe (4 × 3.125 Gbps)
- 10 GFC (4 × 3.1875 Gbps)

In bypass mode, lane 0 or lane 3 of the XAUI is capable of passing through 1.25 Gbps data or single 3.125 Gbps data to the network serial link and vice versa.

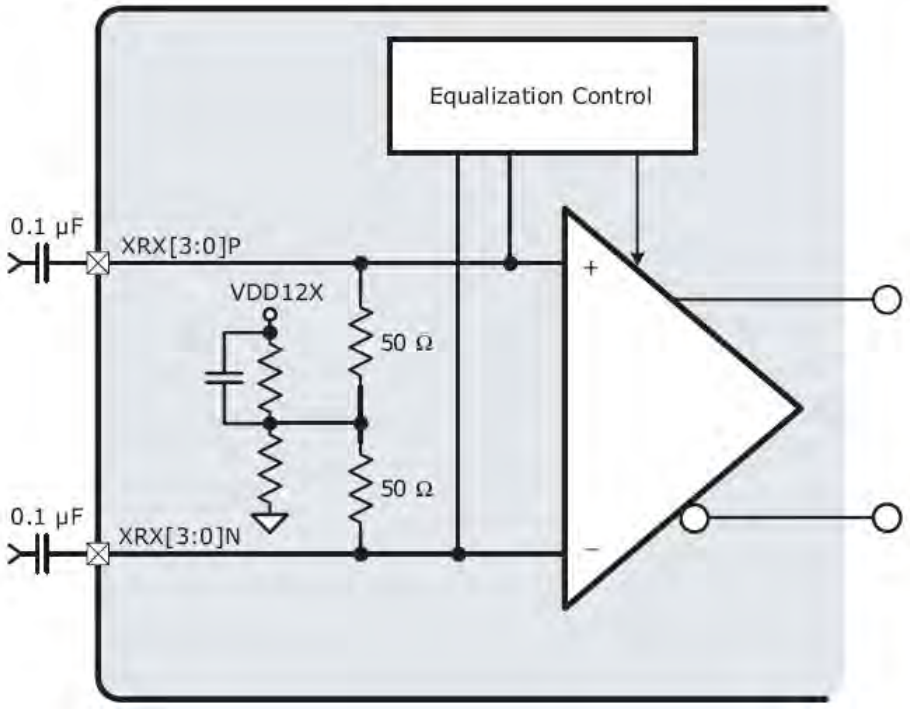
3.6.1 XGMII Extender Sublayer (PHY XS)

The PHY XS block interfaces from the four-lane 10 Gbps attachment unit interface (XAUI) to the PCS. Each AC coupled lane has 8b/10b encoded data running at 3.125 Gbps for 10 GE and 3.1875 Gbps for 10 GFC.

3.6.2 XAUI Receiver

The XAUI interface features on-device terminations of 100 Ω for all XAUI inputs, as shown in the following illustration.

Figure 26 • **Simplified XAUI Inputs**



3.6.3 XAUI Receiver Equalization

Incoming data on the XRXn inputs typically contains a substantial amount of intersymbol interference (ISI) or deterministic jitter, which reduces the ability of the receiver to recover data without errors. A programmable equalizer is included in each of the receiver's input buffers to compensate for this. This circuit is designed to effectively reduce the ISI commonly found in copper cables or backplane traces due to low frequencies being attenuated less than high frequencies as a result of the skin effect and dielectric losses. The equalizer boosts high-frequency edge response in 12 programmable levels of peaking ratio and decay time independently for each channel. The 12 programmable levels are intended to meet the equalization needs of commonly used trace lengths. Equalization level is selected or disabled on each channel independently by setting the appropriate internal register bits accessed through the MDIO management interface.

3.6.4 XAUI Clock and Data Recovery

At the XAUI receiver, each channel contains an independent clock recovery unit (CRU) that accepts the selected serial input source, extracts the high-speed clock, and retimes the data. Each CRU automatically locks on data and if the data is not present, it automatically locks to the reference clock. The clock recovery unit must perform bit synchronization, which occurs when the CRU locks onto and properly samples the incoming serial data, as described in the previous paragraph. If the CRU is not locked onto the serial data, the 10-bit data from the decoder is invalid, resulting in numerous 8b/10b decoding errors or disparity errors. It the link is disturbed (that is, the cable is disconnected or the serial data source is switched), the CRU requires 300 data edges to lock onto the data.

3.6.5 XAUI Code Group Synchronization

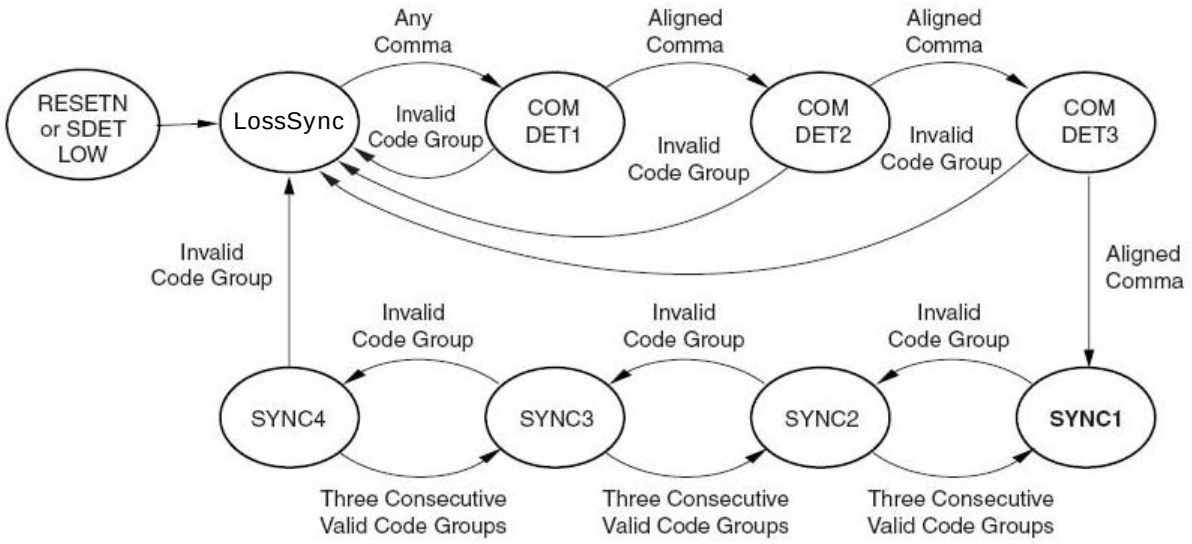
The retimed serial data stream is converted into 10-bit code groups by the deserializer. A special 7-bit comma pattern (0011111xxx or 1100000xxx where x is don't care) is recognized by the receiver and allows it to identify the 10-bit code group boundary.

Character, or code group, alignment occurs when the deserializer synchronizes the 10-bit code group boundary to a comma pattern in the incoming serial data stream. If the receiver identifies a comma pattern in the incoming data stream that is misaligned to the current framing boundary and the receiver is in LOS state, the receiver re-synchronizes the recovered data to align the data to the new comma

pattern. Re-synchronization ensures that the comma character is output on the internal 10-bit bus so that bits 0 through 9 equal 0011111xxx or 1100000xxx. If the comma pattern is aligned with the current framing boundary, then the re-synchronization does not change the current alignment.

The detection of a series of consecutive 10-bit code group violations is the mechanism by which loss of synchronization (LossSync) is declared by the XAUI receiver. The LossSync condition is cleared by the detection of a series of comma characters that are properly aligned on code group boundaries. For additional information, see IEEE 802.3ae-2002 Clause 48, Figure 48-7 and the following illustration.

Figure 27 • **Loss of Synchronization State Diagram**



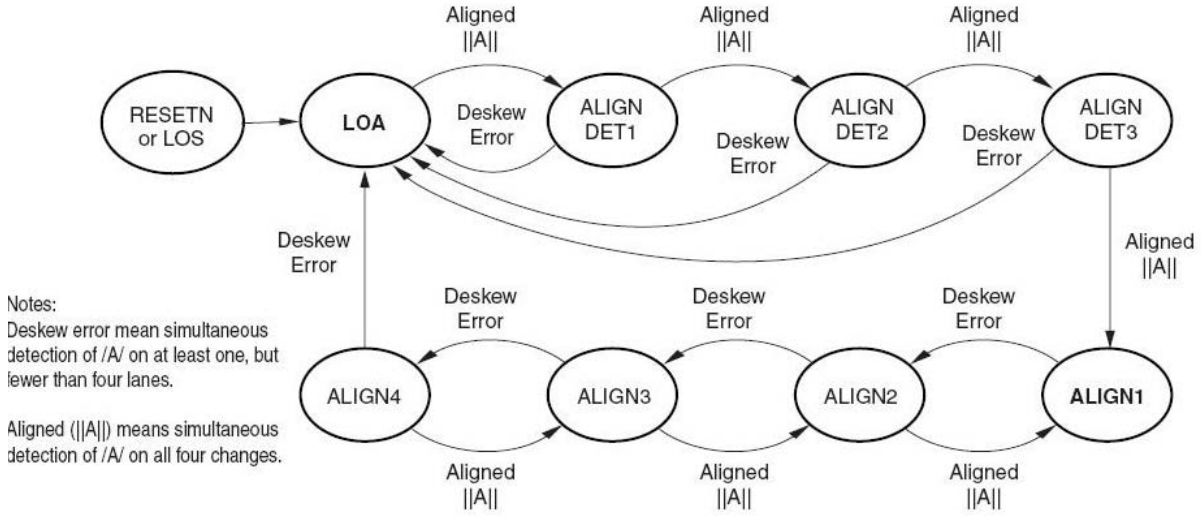
Note: Comma detection is enabled only when in the loss of synchronization (LossSync) state rather than at all times. This is desirable to prevent incorrect character realignment due to the appearance of false commas, resulting from single-bit errors.

3.6.6 XAUI Lane Deskew

XAUI bit lane skew occurs due to skew between channels of a XAUI transmitter and skew accumulated across the transmission medium. The VSC8484 device can deskew up to 63-bit periods of such interchannel skew by using elastic buffers after each of the receiver inputs. For the XAUI interface to perform deskew or channel alignment, the receiver must receive a specific code group defined in IEEE 802.3ae standard Clause 48 as the alignment code group, ||A||.

For interchannel alignment to occur, the ||A|| ordered set consisting of four ||A|| code groups must appear, one ||A|| on each of the four XAUI inputs. This provides a unique synchronization point across the four serial data streams, which are used to align the received channels. Alignment status is governed by the reception of ||A|| code groups across the inputs, as shown in the loss of alignment (LOA) state machine in the following illustration.

Figure 28 • **LOA State Diagram**



Successive synchronization points must be separated by at least 170-bit periods in order for up to 63-bit periods of interchannel skew to be corrected unambiguously. An IEEE-compliant source of XAUI data provides a minimum spacing between sync points of 17 code groups, or 170-bit periods (at least 16 other IDLE code groups must occur between consecutive occurrences of ||A||). The alignment mechanism is always enabled when code group synchronization is attained on both channels.

3.6.7 10B/8B Decoder

The 10-bit character from the deserializer is decoded in the 10B/8B decoder, which outputs the eight-bit data bytes plus control to the physical coding sublayer (PCS) section of the device.

If the 10-bit code group does not match any valid value, a code-group error is generated that increments the code-group error counter. Similarly, if the running disparity of the code group does not match the expected value, a disparity error is generated.

3.6.8 8b/10b Encoder and Serializer

Each channel contains an 8b/10b encoder that translates 8-bit input data fed internally from the PCS block into a 10-bit code word. This data is then fed into a multiplexer that serializes the parallel data, using the synthesized transmit clock. The most significant bit of the 10-bit data is transmitted first. Each channel has a serial output port, XTXn, which consists of a differential XAUI output buffer operating at 3.125 Gbps for 10 GE and 3.1875 Gbps for 10 GFC.

3.6.9 XAUI Transmitter

On the transmit side, each polarity of the CML-type output driver is back-terminated with 50 Ω resistance to the supply, providing a 100 Ω differential output impedance.

3.6.10 XAUI Transmitter Pre-Emphasis

High-speed digital waveforms are subject to skin effect phenomena, such as velocity dispersion and frequency-dependent attenuation of their Fourier components. These effects cause the signal to become increasingly distorted with increasing propagation distance along a transmission medium. The situation is exacerbated with increasing frequency. Recognizing this, the device provides the capability of signal pre-distortion, or pre-emphasis, in its transmitter section.

When used, transmit pre-emphasis causes the XAUI transmitter outputs to be distorted in a manner that is the inverse of skin effect distortion. When signal pre-emphasis is chosen, the effects of pre-distortion and skin effect distortion offset each other, and a high-quality waveform is seen at the receiving device. Several levels of signal pre-emphasis are available and are selected on an individual-channel-basis through the MDIO management interface.

Note that the settings vary with trace length and loss characteristics of the transmission material. It is recommended to experiment with these settings to obtain optimum performance.

3.6.11 XAUI Power Down Mode

The entire XAUI channel can be powered down when any of the IEEE defined low power mode register bits are asserted (1×0000.11, 2×0000.11, 3×0000.11, 4×0000.11). This shuts off both the receive and transmit datapaths.

Individual XAUI input lanes can be powered down with register bits 4×E602.14:11. Individual XAUI output lanes can be powered down with register bits 4×E603.7:4. These can be used to save power in the 1G pass-through mode.

3.6.12 XAUI Failover

XAUI interfaces in the VSC8484 device support the following failover capabilities:

- Network traffic on channel 0 is switchable to XAUI channel_1.
- Network traffic on channel 1 is switchable to XAUI channel_0.
- Network traffic on channel 2 is switchable to XAUI channel_3.
- Network traffic on channel 3 is switchable to XAUI channel_2.

The following table lists the available settings for the failover modes.

Table 41 • **Failover Modes**

Setting	Mode
1Ex0003 =0x0002	XAUI channel_2 to/from SFI channel_3 XAUI channel_3 to/from SFI channel_2
1Ex0003 =0x0001	XAUI channel_0 to/from SFI channel_1 XAUI channel_1 to/from SFI channel_0
1Ex0003 = 0x0003	XAUI channel_0 to/from SFI channel_1 XAUI channel_1 to/from SFI channel_0 XAUI channel_2 to/from SFI channel_3 XAUI channel_3 to/from SFI channel_2

3.7 10GBASE-KR

The VSC8484 device implements the 10GBASE-KR standard and includes the following:

- Training (clause 72)
- Auto-negotiation for backplane Ethernet (clause 73)
- Forward error correction (FEC) (clause 74)
- 10GBASE-KR output driver. For more information, see 10BASE-KR Output Driver, page 15.

When KR is enabled, the VSC8484 device executes. For more information, see Figure 29, page 64.

Auto-negotiation and training both require interaction with firmware running in the onboard v300 processor.

3.7.1 Auto-negotiation

The primary function of auto-negotiation (AN) is to communicate with a link partner (LP) through the exchange of differential manchester encoded (DME) frames or pages. The pages are 48 bits in length, and include a 3 bit “technology ability” field. This field is used to advertise what each device is capable of (10G_KR, 10G_KX4, 1G_KX).

A DME data cell (one bit of information) is 6.4ns for AN. For more information about DME encoding, see IEEE 802.3ap Clause 73.5.2.

Auto-negotiation is performed in hardware by the arbitration state machine (ASM).

When negotiation is complete, each device enables the mode that is the highest common denominator (HCD) of the advertised abilities. In other words, if the VSC8484 device advertises it is capable of 10G_KR, and 10GKX4, and the LP advertises 10G_KX4 and 1G_KX, the HCD ability is 10G_KX4.

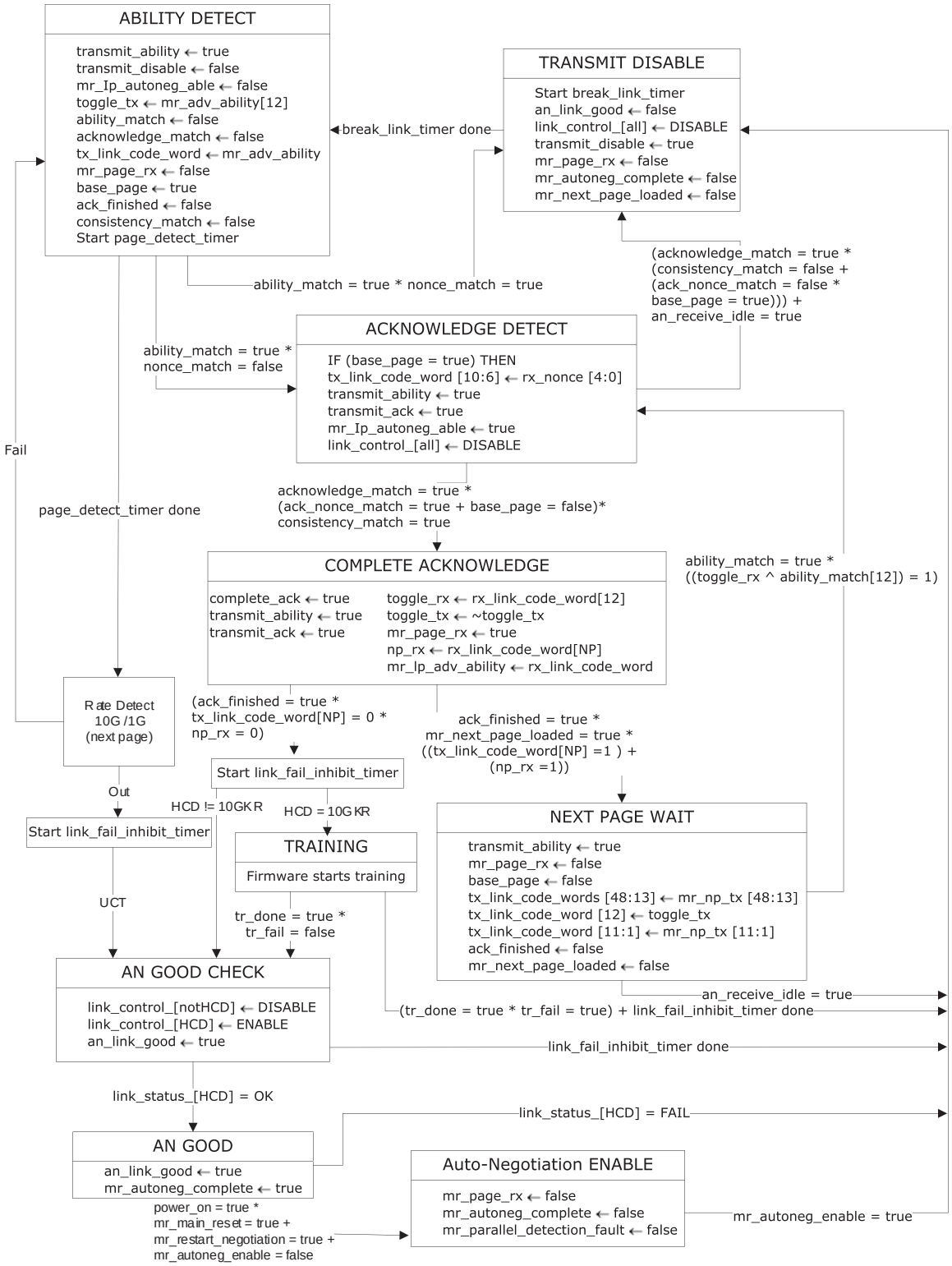
The priority order is 10G_KR, 10G_KX4, 1G_KX.

The secondary function of AN is “parallel detect” (described as rate detect here), which detects when the VSC8484 device is connected to a fixed-speed legacy device. The VSC8484 device cycles through different operating modes (10G and 1G) and determines the type of data being received. This function is performed by firmware, which then issues the link_status and rate_detect_done signals for the hardware ASM.

In the 1G mode, there is no PCS decoding of the input stream. The stream is simply recovered and passed to a XAUI lane output. Those rates can only be detected by the assertion of CDR lock. In 10G mode, the 64b/66b PCS is in the datapath, so true codeword detection is done in this case.

The following illustration shows the state diagram, which is a slightly modified version of figure 73-11 in IEEE 802.3ap.

Figure 29 • **Auto-negotiation Arbitration State Diagram**



The main differences are as follows:

- The rate detect branch executes cyclic scan of three different signaling rates
- Link training is started in AN_GOOD_CHECK state

For link_status_[*] and link_control_[*] state variables:

- 10G refers to 10 Gigabit Ethernet. Firmware monitors the PCS status register and reports link_status[10G] = OK upon block_lock.
- 1G refers to the 1.25 Gbps rate of Gigabit Ethernet.

In addition to the various timers implemented in this state machine, and documented in the standard, the following timers are used to implement the rate detection function:

- page_detect_timer: used to time out (and branch to rate-detection) while looking for DME pages.
- timer_10g: used to time out while looking for PCS block-lock.
- timer_1g: used to time out while looking for 1.25 Gbps lock at receiver.

All timers are 32-bit programmable. For more information, including a description of the rest of the state variables and timers, refer to IEEE 802.3ap Clause_73.

3.7.2 Technology Ability Field

Bits 45:21 of the base page are used to advertise supported technologies. These bits are designated A[24:0]. Only the three LSBs are used. The rest are reserved for future use.

Table 42 • **Technology Ability Field**

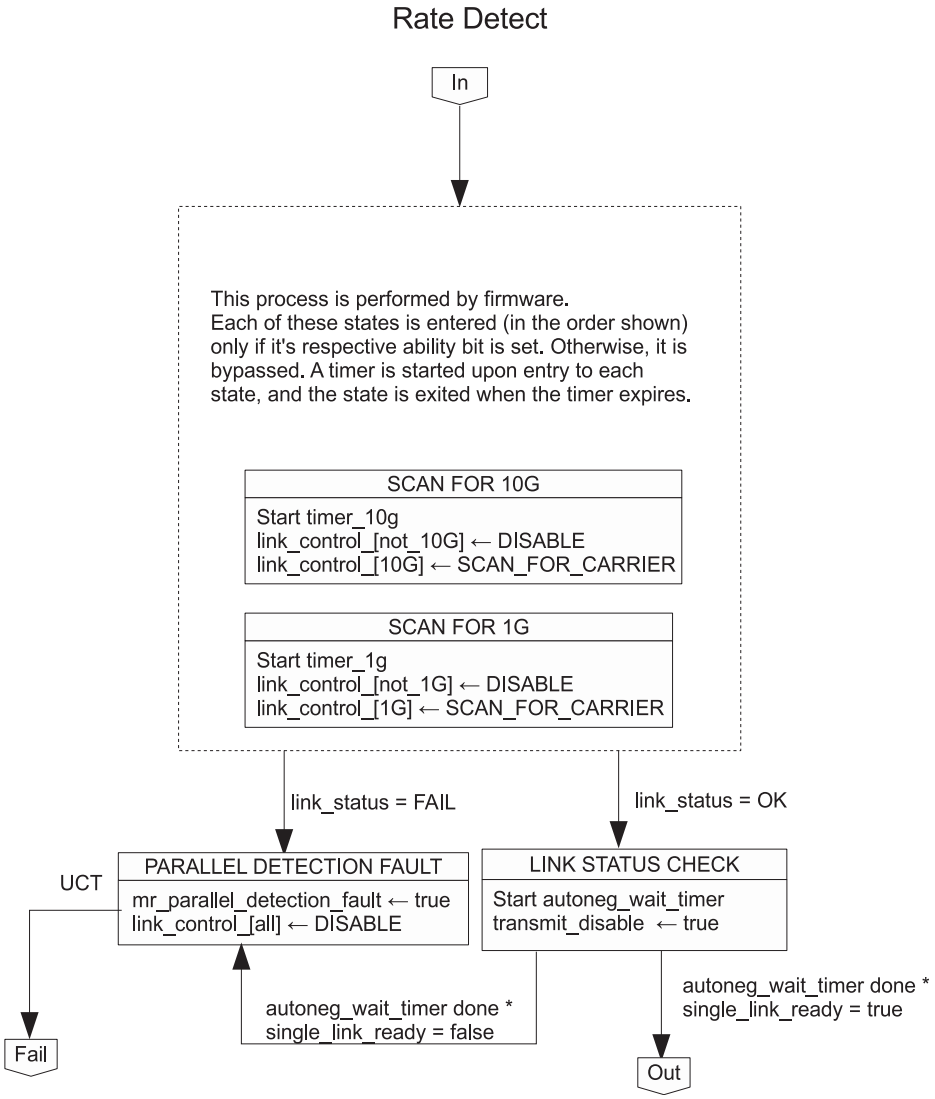
Bits	Technology
A0	1000BASE-KX
A1	10GBASE-KX4
A2	10GBASE-KR
A3 through A24	Reserved for future technology

These bits are set using MDIO according to the application for which the VSC8484 device is used. For example, if the VSC8484 device is to be used as a XAUI repeater, A1 is set.

A0 is set if the VSC8484 device is used as a Gigabit Ethernet repeater and A2 is set if the VSC8484 device is used as 10 GbE transceiver.

Rate detection is only done for those technologies advertised by the VSC8484 device.

Figure 30 • **Rate Detection**



3.7.3 Transmitted Nonce

The transmitted nonce field is generated with the polynomial $x^5 + x^2 + 1$. It is initialized to 5'b1111 and takes on a new value with each entry into the ABILITY_DETECT state.

3.7.4 Role of Firmware during Auto-negotiation

Firmware performs the following tasks:

- Set timer values, if other than default settings are desired
- Set the "advertised abilities" page using registers 7x0010 - 7x0012
- Set the "next_page" using registers 7x001–7x0018
- Handle "next_page" exchanges with link partner
- Global control of AN through register 7x0000, which contains the mr_an_enable, mr_an_reset, and mr_an_restart signals
- Configure the VSC8484 device in 10G or 1G modes, depending on the outcome of negotiation or rate detect
- Set the link status bits, 7x8200.15:13 (10G or 1G, respectively)
- Direct link training

Firmware continuously monitors the 7x8120 register:

- Bits 10:0 are a one-hot live value of the current arbitration state.
- Bit 11 is the training_required flag, which is asserted upon entry into AN_GOOD_CHECK when HCD =10G_KR.
- Bits 13:12 are reserved.
- Bit 14 is the np_rx bit, which is asserted if the link partner requests a next_page exchange.
- Bit 15 is the base_page bit, which is asserted if the received link codeword is a base_page. Otherwise, the received link codeword is a next_page.

The following states require additional activity by firmware:

- RATE_DETECT – Handle rate detect state machine and report link_status and rate_detect_done.
- COMPLETE_ACKNOWLEDGE - Determine if next_page exchanges are requested by the link partner.
- AN_GOOD_CHECK – Start training protocol if required, and when training is completed, or not required, configure the VSC8484 device for the rate given by link_HCD variable (7x8100.2:1). Report link status in 7x8200.15:13.

3.7.5 Timers

All timers run on the divided version of the 156.25 MHz reference clock. As a result, a running timer decrements every 12.8 ns.

The following table lists the timers used during auto-negotiation.

Table 43 • **Auto-negotiation Timers**

Timer	Registers	Default (hex)
break_link	7x810E, 7x810F	004D7C6D (65ms)
autoneg_wait	7x8110, 7x8111	0023C346 (30ms)
link_fail_inhibit_short	7x8112, 7x8112	0035A4E9 (45ms)
link_fail_inhibit_long	7x8114, 7x8115	025A01C5 (505ms)
page_detect	7x8116, 7x8117	0
link_status_10G	7x8118, 7x8119	0
link_status_1G	7x811C, 7x811D	0

The timer control register, 7x811E, is used to start a given timer (self-clearing bit), and hold all timers (bit 7). All timers are released to resume counting on deassertion of bit 7.

Note: These registers need to be configured for the intended application, and not left at their default values.

3.7.6 Advertised Ability Registers

The firmware will write the 48-bit link codeword base page, containing the advertised abilities, to registers 7x0010 - 7x0012. What gets written depends on the application of the VSC8484 device in the given system.

Table 44 • **Advertised Ability Fields**

Field	Codeword bits	Register bits	Default Value
FEC capability	D[47:46]	7x0012.[15:14]	2’b01
Technology ability	D[45:21]	7x0012.[13:0] 7x0011.[15:5]	25’h0000004
Transmitted nonce	D[20:16]	7x0011.[4:0]	5’b11111
NP, Ack, RF	D[15:13]	7x0010.[15:13]	3’b000
Capability bits not related to PHY	D[12:10]	7x0010.[12:10]	3’b000
Echoed nonce	D[9:5]	7x0010.[9:5]	5’b00000

Table 44 • **Advertised Ability Fields *(continued)***

Field	Codeword bits	Register bits	Default Value
Selector	D[4:0]	7x0010.[4:0]	5'b00001

The following values may change, depending upon the application.

- FEC requested - D[47]
- Technology ability - D[23:21]
- NP (Next Page bit) - D[15]

3.7.7 Link Control

The link_control_[*] variable does not exists in the ASM because the firmware has complete control of the state of the link. Firmware monitors the state of ASM and controls the behavior associated with this variable.

3.7.8 Next Pages

The firmware will control the next_page exchanges with the link partner. It does this by setting the NP bit in the transmitted codeword if there are next_pages to send, and writing to the next_page codeword registers. For more information about next_page exchanges, see section 73.7.7 of 802.3ap.

If the link partner has any next_pages to send, the NP bit of the received codeword is 1.

The ASM loads LP base_pages in the LP base_page registers {7x0015, 7x0014, 7x0013}, LP next_pages in the LP next_page registers {7x001B, 7x001A, 7x0019}.

If the link partner has next_pages to send, the ASM goes to NEXT_PAGE_WAIT state, but only after the firmware writes to the LD next_page registers {7x0018, 7x0017, 7x0016}, in that order. The mr_next_page_loaded variable is set to TRUE upon a write to 7x0016, which is a condition for transition to NEXT_PAGE_WAIT. Because of this, writing to the LD next_page registers must be done, even if there is nothing new to write. It is the only way to set the mr_next_page_loaded variable.

The firmware sets the NP bit in the base_page or next_page if the VSC8484 device has any next_pages to send.

The firmware executes the following pseudocode:

```
read 7x8120;
COMPLETE_ACKNOWLEDGE = 7x8120.5;
np_rx                = 7x8120.14;
base_page            = 7x8120.15;
np_tx = Firmware chooses to engage in next_page exchanges.
If (np_tx and base_page) then
 set 7x0010.15; // NP bit of base page
If (np_tx and not base_page) then
 set 7x0016.15; // NP bit of next page
if (COMPLETE_ACKNOWLEDGE and np_rx or np_tx) then
 if (base_page) then
    read LP base_page registers {7x0015, 7x0014, 7x0013};
 else
    read LP next_page registers {7x001B, 7x001A, 7x0019};
 write LD next_page registers {7x0018, 7x0017, 7x0016};
```

3.7.9 Training

When the state machine reaches AN_GOOD_CHECK, and the negotiated rate is 10G_KR, the training required bit (7x8120.11) is set. Firmware responds to this bit by executing as described by the training state diagram and the coefficient update state diagram. When training is complete, it sets the tr_done bit (1x8201.4).

The purpose of training is to establish the optimal settings for the VSC8484 device and the LP. For more information about the training function, see IEEE 802.3ap Clause 72.

Training takes place if the negotiated technology (HCD) is 10G_KR. It is accomplished through the use of fixed-length training frames. Each frame is 548 octets in length, and the following table lists the structure and length of the training frames.

Table 45 • **Training Frame Lengths**

Octets		
4	Frame Marker	
16	Coefficient Update	Control Channel (DME)
16	Status Report	
512	Training Pattern	

The frame marker is the 32-bit hex pattern FFFF0000.

The control channel is DME encoded. A DME data cell is 8 10G_KR UI (~776 ps). Therefore, the control channel is 256 UI. The control channel consists of the coefficient update field and status report field. Each carries 16 bits of information used for equalization of the LP's transmitter.

The following table lists the registers/bits that set the local transmitter equalization.

Table 46 • **Local Transmitter Equalization Registers and Bits**

	Registers/Bits	Default
k(–1)	1x8013.7:0	0x00
k(0)	1x8014.15:8	0x1F
K(+1)	1x8014.7:0	0x09

These registers are writeable by both firmware and hardware. Hardware updates the values based on the received coefficient update field.

3.7.10 Coefficient Update Field

The coefficient update field is used to carry transmitter correction information to the Link partners' equalizer settings.

Table 47 • **Coefficient Update Field**

Cells	Name	Description
15:14	Reserved	Transmitted as 0, ignored on reception
13	Preset	0 = Normal operation 1 = Preset coefficients
12	Initialize	0 = Normal operation 1 = Initialize coefficients
11:6	Reserved	Transmitted as 0, ignored on reception
5:4	Coefficient (+1) update	00 = Hold 01 = Increment 10 = Decrement 11 = Reserved
3:2	Coefficient (0) update	00 = Hold 01 = Increment 10 = Decrement 11 = Reserved

Table 47 • **Coefficient Update Field *(continued)***

Cells	Name	Description
1:0	Coefficient (–1) update	00 = Hold 01 = Increment 10 = Decrement 11 = Reserved

The *preset* bit is used to request the LP tap settings to:

- *k(+1)*=0
- *k(-1)*=0
- *k(0)*=max

The *initialize* bit is used to request the LP tap settings be configured such that

- R_{pre} = 1.29 ±10%
- R_{pst} = 2.57 ±10%

Each coefficient, *k*, is assigned a 2-bit field describing a requested update.

Three request encodings are defined as follows:

- Hold—the default state for a given tap is hold, which corresponds to no change in the coefficient.
- Increment/Decrement—the increment or decrement encodings are transmitted to request that the corresponding coefficient be increased or decreased. An increment or decrement request is transmitted until the update status for that tap indicates updated, maximum, or minimum. At that point, the outgoing requests for that tap are set to hold.

The coefficient update field to be transmitted is written by firmware to register 1x809A, which is shadowed directly to 1x009A (1x009A is read-only). The contents of this register are transmitted in the outgoing training frame, but only if the coeff_ready bit is asserted by firmware using 1x8201.1.

The received coefficient update field is decoded, the local tap settings adjusted accordingly, and the status report field of the outgoing training frame is assembled and transmitted. This is all handled by hardware.

The following table lists the pre-programmed registers (by firmware or default) used for preset, and initialize settings. The step size of an increment or decrement request (for each tap) is programmable.

Table 48 • **Increment/Decrement Register States**

	Register	State	Default
k(–1)	1x8210.7:0	Preset	0x0F
	1x8212.7:0	Initialize	0x0B
	1x8214.1:0	Step size	0x1
k(0)	1x8211.15:8	Preset	0x1F
	1x8213.15:8	Initialize	0x1F
	1x8214.3:2	Step size	0x1
k(1)	1x8211.7:0	Preset	0x00
	1x8213.7:0	Initialize	0x1B
	1x8214.5:1	Step size	0x1

3.7.11 Status Report Field

The transmitted status report field is used to signal state information to the LP. It is calculated and transmitted by hardware. The received status report field is decoded by hardware and placed in 1x0099. The receiver_ready bit is used to inform the LP that training is either completed, or should continue. Each

coefficient, *k,* is assigned a 2-bit field describing the status of pending updates to the coefficient. The following table lists the four status encodings: not updated, updated, maximum, and minimum.

Table 49 • **Status Report Field**

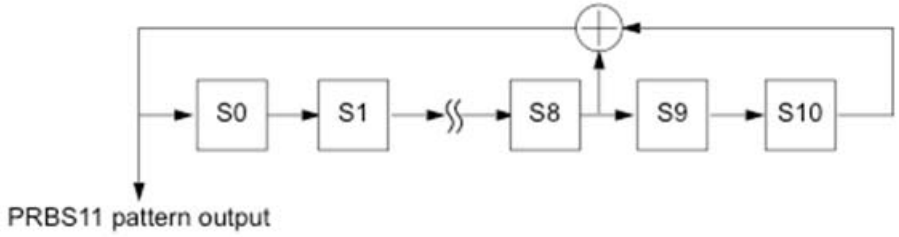
Cell	Name	Description
15	Receiver_ready	0 = Request that training continue 1 = Training complete. Ready to receive data
14:6	Reserved	Transmitted as 0, ignored on reception
5:4	coefficient (+1) status	00 = Not updated 01 = Updated 10 = Minimum 11 = Maximum
3:2	Coefficient (0) status	00 = Not updated 01 = Updated 10 = Minimum 11 = Maximum
1:0	Coefficient (–1) status	00 = Not updated 01 = Updated 10 = Minimum 11 = Maximum

3.7.12 Training Pattern

The training pattern consists of 4094 bits from the output of a PRBS11 generator, followed by two zeros, as shown in the following illustration.

Figure 31 • **PRBS Pattern Generator**

$$G(x) = 1 + x^9 + x^{11}$$



It is transmitted at 10.3125 Gbps. The PRBS11 generator is initially seeded with all ones, and then each subsequent frame is seeded with the last value of the previous frame.

The received training pattern is used to calculate BER, which is used to determine the next coefficient update values to transmit, and to adjust EDC receiver settings.

3.7.13 Role of Hardware and Firmware during Training

Training functions are handled as follows:

3.7.13.1 Hardware

- DME Frame reception, lock, and decode.
- DME Frame encoding and transmission.
- Local transmitter equalization settings based on received coefficient update field.
- Determine coefficient status bits to be transmitted in status report field.
- Training pattern: generation, reception, bit error detection/counting, and frame counting.

3.7.13.2 Firmware

- Training state machine
- Bit-error detector control
- Coefficient update field generation (based on BER)
- EDC receiver adjustments (based on BER)

To prepare for training, the firmware sets the max_wait_timer and wait_timer values, if other than default is desired. It also sets the frames_to_count register 1x820B. This determines the number of frames BER is calculated over. It can be a value from 0x0001 to 0xFFFF (decimal 32,767). The register settings can be made any time after power-up. There is no need to wait for the assertion of the training_required flag.

Table 50 • **Register Settings for Training**

Timer	Period (ms)	Register(s)	Default (hex)
wait_timer	100–300 frames (43–127 µs)	1x820C	19F1 (200 frames)
max_wait_timer	500 ms	1x820E, 1x820D	02540BE4

Firmware sets the training enable and restart bits, 1x0096.[1:0], and starts executing the training state machine.

The variable frame_lock is used by this state machine, and can be read at 1x0097.1.

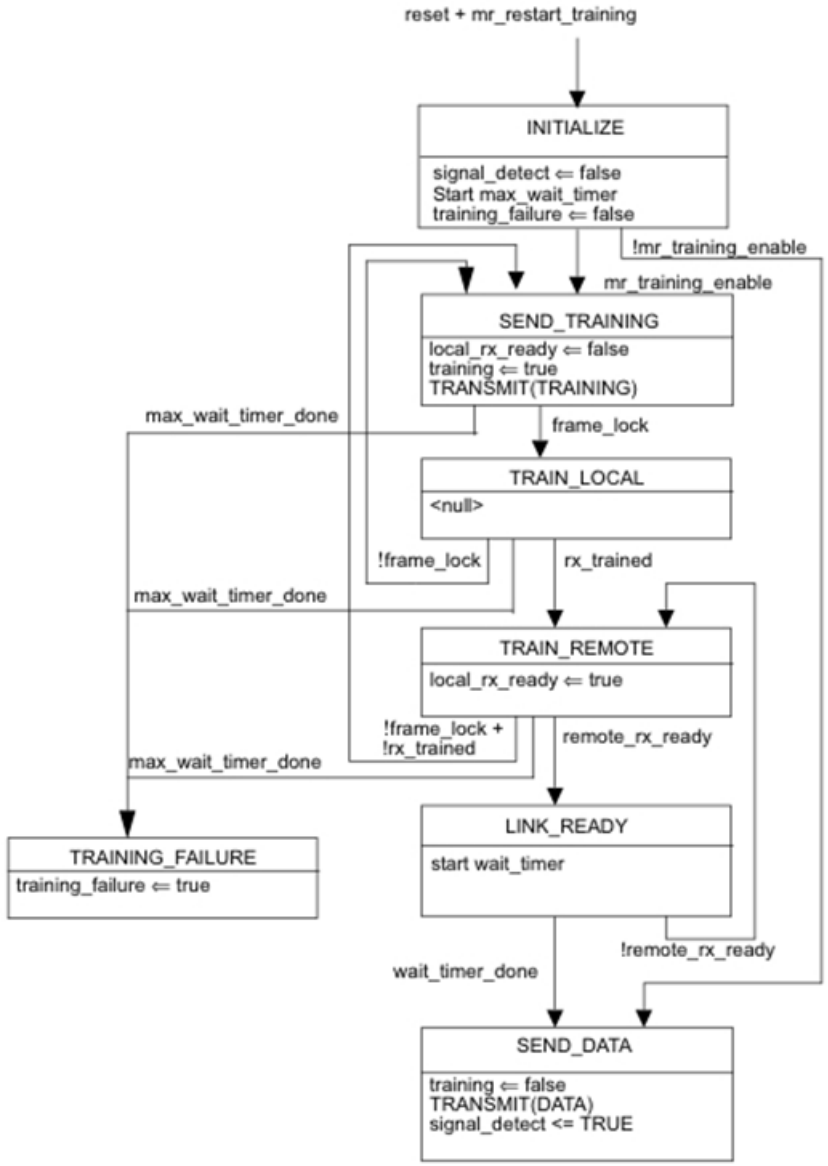
The start bit for wait_timer is 1x8201.3. The latch-high done bit can be read at 1x8208.3.

The self-clearing start bit for max_wait_timer is 1x8201.2. The latch-high done bit can be read at 1x8208.2.

After starting the timers, register 1x8208 should be monitored for timer status.

Whenever a frame is transmitted, the latch-high frame_transmit_done bit (1x8208.4) is asserted. The following illustration shows the training state diagram.

Figure 32 • **Training State Diagram**



3.7.14 Training Status

As shown in the following table, firmware will update the training status register (1x8097) as appropriate. bits 3:0 of this register are “shadowed” to the IEEE register 1x0097.

Table 51 • **1x8097 (Shadowed to 1x0097)**

15:4	RESERVED	
3	training_failure	1 = training failed 0 = no training failure
2	Training	1 = actively training 0 = not training
1	Reserved	

Table 51 • **1x8097 (Shadowed to 1x0097) *(continued)***

15:4	**RESERVED**	
0	rx_trained	1 = trained 0 = not trained

The auto-negotiation (AN) arbitration state machine (ASM) uses training_done to transition out of AN_GOOD_CHECK state if HCD=10G_KR. If the training_failure bit is set, ASM transitions to TRANSMIT_DISABLE state.

3.7.15 Coefficient Update and Status Report

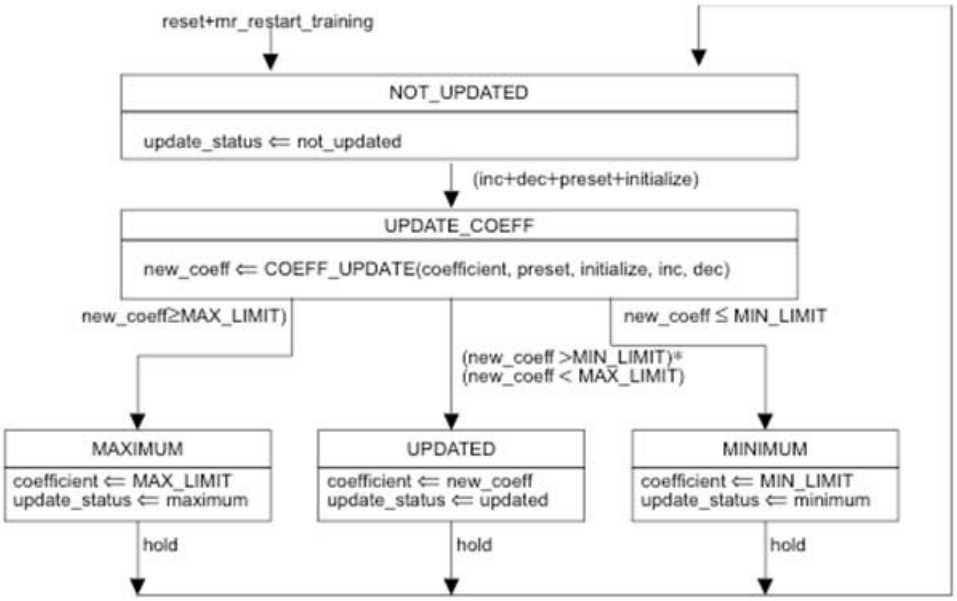
Received training frames are decoded in hardware, and the control channel fields are updated in:

- 1x0098 – Coefficient update
- 1x0099 – Status report

These registers contain the most recently decoded control channel of which no DME violations occurred.

The hardware implements the coefficient state diagram as shown in the following illustration. This diagram defines the process for updating transmit EQ coefficients in response to requests from the link partner, and also defines the coefficient update status to be reported in outgoing training frames.

Figure 33 • **Coefficient Update State Diagram**



The coefficient values, and corresponding transmitter output waveform meet the requirements listed in the following table. For more information, refer to IEEE 802.3ap Clause 72-7.

Table 52 • **Tx Output Waveform Requirements by Coefficient Update**

Coefficient Update[1]			**Requirements[2)]**		
C(1)	**C(0)**	**C(-1)**	**$v_1(k)$-$v_1(k-1)$ (mV)**	**$v_2(k)$-$v_2(k-1)$ (mV)**	**$v_3(k)$-$v_3(k-1)$ (mV)**
increment	hold	hold	–20 to -5	5 to 20	5 to 20
decrement	hold	hold	5 to 20	–20 to -5	–20 to –5
hold	increment	hold	5 to 20	5 to 20	5 to 20
hold	decrement	hold	–20 to –5	–20 to –5	–20 to –5
hold	hold	increment	5 to 20	5 to 20	–20 to –5

Table 52 • **Tx Output Waveform Requirements by Coefficient Update *(continued)***

Coefficient Update[1]			Requirements[2)]		
C(1)	C(0)	C(-1)	$v_1(k)$-$v_1(k - 1)$ (mV)	$v_2(k)$-$v_2(k - 1)$ (mV)	$v_3(k)$-$v_3(k - 1)$ (mV)
hold	hold	decrement	–20 to –5	–20 to –5	5 to 20

1. Step size requirements for the tap under test apply regardless of the current value of the other taps.
2. This difference is measured relative to the voltage prior to the assertion coefficient update *k* equal to hold.

The output waveform must meet the requirements listed in the following table for all of the limiting cases represented in the table.

Table 53 • **Tx Output Waveform Requirements by Coefficient Status**

Coefficient update			Requirements		
C(1)	C(0)	C(-1)	R_{PRE}	R_{PST}	v_2 (mV)
disabled	minimum	disabled	0.90 to 1.10	0.90 to 1.10	220 to 330
disabled	maximum	disabled	0.95 to 1.05	0.95 to 1.05	400 to 600
minimum	minimum	disabled		4.00 (min.)	
disabled	minimum	minimum	1.54 (min.)		

The coefficient update field to be transmitted is written to 1x809A. The contents of this register are “shadowed” to IEEE register 1x009A. Before updating this register, the firmware clears the tx_coeff_ready bit (1x8201.1), sets this bit to 1 upon completion of the write to 1x809A. The status report field to be transmitted is written by hardware to 1x009B.

3.7.16 BER Calculation

When the error detector bit is set (1x8201.0, self-clearing), bit errors are counted during the training pattern segment of each training frame, until the given number of frames (1x820B) has been received.

A live value of the number of frames counted is in 1x820A. A live value of the bit errors counted is in 1x8209. These are non-rollover counters.

The contents of these registers are frozen when the final frame is counted. They maintain the current counts until another start is issued at 1x8201.0 and after the start is cleared.

The received training pattern is evaluated for bit errors using the reverse of the pattern generator. For more information, see Figure 31, page 71. Invert the incoming training pattern using 1x8201.5; and the outgoing training pattern using 1x8201.6.

During the BER cycle, register 1x8208 can be monitored for a couple of things.

Bit 0 is the busy bit that is asserted during the duration of the BER cycle. Upon the completion of the last frame to be counted, this bit goes to '0'.

Bit 1 contains a latch-high flag that is set if, during frame reception, a DME violation occurs.

3.7.17 Forward Error Correction (FEC)

The KR FEC is implemented as defined in IEEE 802.3ap Clause 74.

During AN, FEC ability is advertised in bit 46 of the base page. Bit 47 is used to request FEC on the link. If both, the VSC8484 device and the LP advertises FEC ability, and either one requests FEC on the link, then FEC will be enabled.

FEC control, based on negotiated HCD, is handled by hardware. Also, FEC can be enabled independent of any other KR function. There are two vendor specific FEC bits:

- 1x8300.1 – *fec_inframe* bit, which is a latch-low bit which can be used by management to determine the lock status of the FEC receiver.
- 1x8300.0 – *fec_rstmon* bit, which is used to reset the FEC counters.

3.8 Loopback and Bypass

The VSC8484 device has two 10-gigabit data ports: XAUI and XFI. There are several options available to the user for routing traffic between the various ports. The purpose of this section is to outline the operation of several loopback modes. These modes can be extremely useful for both test and debug purposes. Data path routing and loopback controls are enabled through the MDIO interface.

3.8.1 Loopback Modes

There are two types of loopback modes: system and network. In general, system loopbacks affect XAUI traffic and network loopbacks affect SFI traffic.

The following table provides a summary of the system loopbacks.

Table 54 • **System Loopback Summary**

Loopback	Name	Loopback Enable	Retiming
B	PHY XS shallow system loopback	4×800E.13 = 1	Phase delay only, XAUI XTX[3:0] signals retimed from XAUI XRX[3:0] recovered clock
G	PCS system loopback	3x0000.14 = 1	XAUI XTX[3:0] signals retimed to XREFCKP/N
J	PMA/WIS system loopback	2x0000.14 = 1 and 1×0000.0 = 1	XAUI XTX[3:0] signals retimed to XREFCKP/N

The following table provides a summary of the network loopbacks, which primarily affect SFI traffic.

Table 55 • **Network Loopback Summary**

Loopback	Name	Loopback Enable
A	PHY XS deep network loopback	4×0000.14 = 1 and 4x800E.13 = 0
F	PCS gearbox network loopback	3x8005.3 = 1
K	PMA network loopback	1×8012.4 = 0

3.8.2 Loopback A

Loopback A is located in the XAUI PHY. It reroutes the data from the 10:1 MUX in the XAUI PHY into the 1:10 DEMUX. XFI data is retimed with PMA CRU. To enable loopback A, set both of the following: LPBK_A (4×0000.14) set to 1 and LPBK_B (4×800E.13) set to 0. The default value for bit 14 is 0 (loopback disabled). XFI ingress (RXINP/N) data is mirrored to the XAUI egress port (XTX[3:0]P/N) simultaneously without further MDIO instructions. When loopback A is enabled, the XAUI signal detect has to be disabled. To disable the XAUI signal detect, set 4xE600.1 to 1.

3.8.3 Loopback B

Loopback B routes the incoming XAUI data through the 1:10 DEMUX and then loops back before the 10b/8b decoder into the 10:1 MUX. Data is retimed by the recovered XAUI clock. No 10b/8b decoding or lane synchronization is performed. System XAUI data is also mirrored to the XFI Tx port. To enable loopback B, set the LPBK_B register (4×800E.13) to 1.

3.8.4 Loopback F

Loopback F routes the incoming XFI data after the receive PCS gearbox back into the transmit PCS gearbox. Network XFI Rx data is also mirrored to the XAUI egress port. To enable loopback F, set

LPBK_F (3x8005.3) to 1. Set the PMA CMU reference clock to the PMA Rx recovered clock (1x8017.3:1 = 1x0). Loopback F is supported in 10G mode only.

3.8.5 Loopback G

Loopback G routes the incoming XAUI data through the PCS transmit gearbox back into the PCS receive gearbox. The data transmitted to the XFI Tx port by default is a continuous stream of repeating 0×00FF words. To enable loopback G, set LPBK_G (3x0000.14) to 1. Loopback G is supported in 10G mode only.

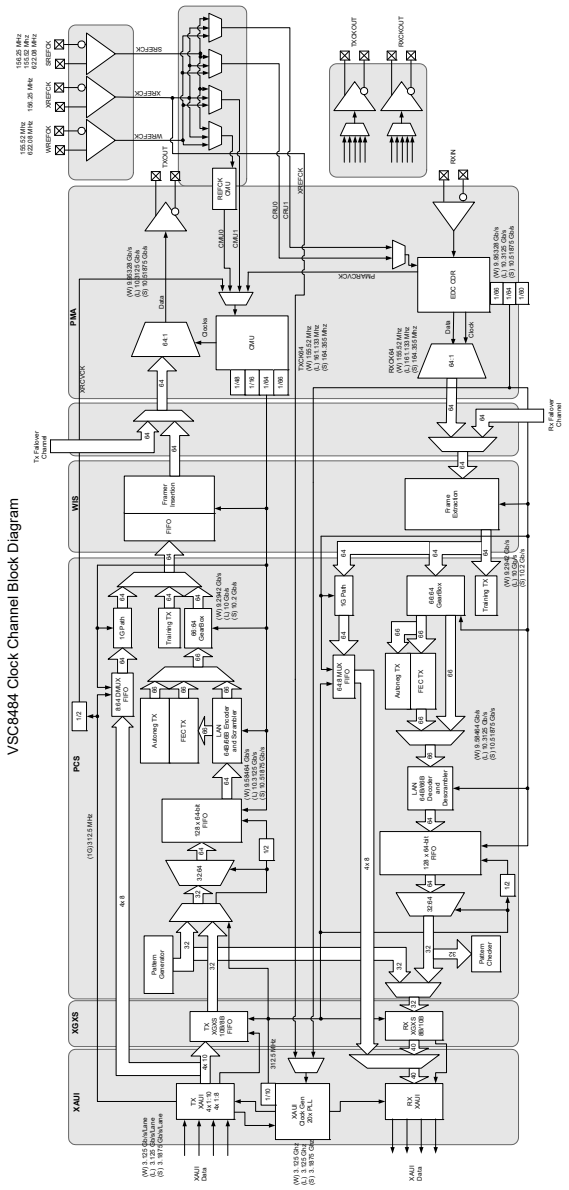
3.8.6 Loopback J

Loopback J routes the incoming XAUI data from the PCS (or WIS if enabled) back into the PCS (or WIS if enabled). This loopback is enabled for both PMA and WIS system loopbacks. The data transmitted to the XFI Tx port by default is a continuous stream of repeating 0×00FF data. To enable loopback J, set any of the following: LPBK_J_PMA (1×0000.0) set to 1 or LPBK_J_WIS (2x0000.14) set to 1. Loopback J is supported in 1G and 10G modes.

3.8.7 Loopback K

Loopback K routes the incoming 10-gigabit XFI data back to the 10-gigabit XFI output, as shown in the following illustration.

Figure 34 • **VSC8484 Channel Clock Block Diagram**



Loopback K is protocol agnostic. Data is retimed with the 10-gigabit recovered clock. Network XFI Rx data is also mirrored to the XAUI egress port. To enable loopback K, set the following: LPBKN_K (1×8012.4) set to 0 (the default is 1, disabled). Set the CMU refclk to the PMA Rx recovered clock (1x8017.3:1 = 1x0).

3.9 Low-Speed Serial Interfaces

This section contains information about the low-speed serial interfaces of the VSC8484 device. The primary control and monitor interfaces in the design are:

- MDIO
- Two-wire serial (master) used to load the firmware from an EEPROM
- Two-wire serial (slave). This interface is enabled by default after device reset. The SCL/SDA pins are brought out on GPIO pins. The two-wire serial-slave function is disabled by reconfiguring the GPIO pins to a different function.
- UART interface is enabled by default after device reset. The UART Tx/Rx pins are brought out on GPIO pins. The UART function is disabled by reconfiguring the GPIO pins to a different function.

- Miscellaneous GPIO (General Purpose Input/Outputs). GPIO pins can be used as:
  - Data/Link activity LED output driver
  - PMA loss-of-lock output for Sync-E applications
  - SFP module present input/channel
  - SFP module's TX_DISABLE output/channel
  - Two-wire serial (slave) interface for read/writing registers
  - UART interface
  - WIS ROSI/TOSI interfaces
  - WIS interrupt A/B output signals/channel
  - Output to monitor many internal nodes when debugging the part

3.9.1 MDIO Interface

This section provides an overview of the management data input/output (MDIO) serial interface. The MDIO interface contained in the VSC8484 device complies with IEEE 802.3ae Clause 45. For more information, see the IEEE standard.

MDIO instructions can be used to read registers, write registers, perform post-read-increment-address instructions, and load firmware into the internal memory.

The PADDR[4:2] pins select the MDIO port addresses to which the VSC8484 will respond. A single VSC8484 device requires the use of four MDIO port addresses, one for each channel. The port address transmitted in MDIO read/write commands to access registers in a particular VSC8484 channel is shown in the following table. The port address is a function of the PADDR pins and a pre-programmed number indicating the channel number. Up to eight VSC8484 devices can be controlled by a single MDIO host.

Table 56 • **MDIO Port Addresses Per Channel**

Channel Number	Channel's Port Address
3	{PADDR[4:2], 11}
2	{PADDR[4:2], 10}
1	{PADDR[4:2], 01}
0	{PADDR[4:2], 00}

The maximum data rate of the MDIO interface is a function of the XREFP/N frequency and the duty cycle of the MDC pin. The MDIO interface will operate at 12 Mbps when the XREFP/N frequency is greater than 144 MHz if the MDC duty cycle is 50%. The MDIO interface will operate at 12 Mbps when the XREFP/N frequency is 156.25 MHz and the MDC duty cycle is 47% to 53%. The maximum MDIO data rate is reduced to 10.6 Mbps when the XREFP/N frequency is 128 MHz with an MDC duty cycle of 50%. Contact your Microsemi sales representative to determine the maximum MDIO data rate when operating conditions are outside the noted situations.

The management frame format supports indirect addressing to provide more accessible register space within each MDIO manageable device (MMD). For more information, see Figure 35, page 80. The following table lists the management frame format.

Table 57 • **Management Frame Format for Indirect Register Access**

Frame	PRE	ST	OP	PRTAD	DEVAD	TA	Address/Data	Idle
Address	1...1	00	00	PPPPP	EEEEE	10	AAAAAAAAAAAAAAAA	Z
Write	1...1	00	01	PPPPP	EEEEE	10	DDDDDDDDDDDDDDDD	Z
Read	1...1	00	11	PPPPP	EEEEE	Z0	DDDDDDDDDDDDDDDD	Z
Read increment	1...1	00	10	PPPPP	EEEEE	Z0	DDDDDDDDDDDDDDDD	Z

A 16-bit address register stores the address of the register to be accessed by data transaction frames. The address register is overwritten by address frames. After device reset, the contents of the address register is set to 0. On power up, the contents of the address register are undefined.

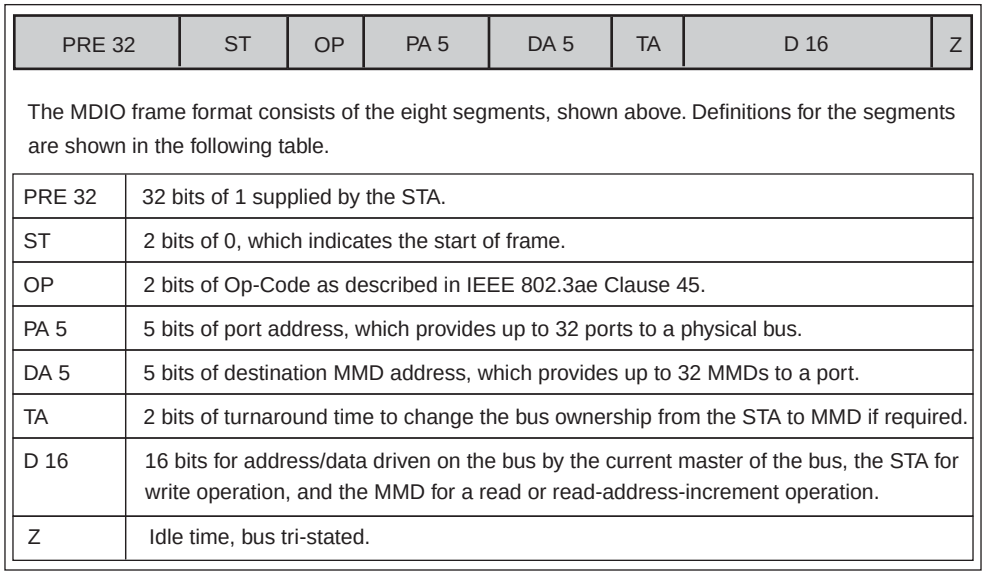
Write, read, and post-read-increment-address frames access the register address stored in the address register. Write and read frames do not modify the contents of the address register.

After receiving a post-read-increment-address frame and completing the read operation, the address register is incremented by 1. When the register contains 65,535, the address register is not incremented.

The idle condition is a high-impedance state. All tri-state drivers are disabled, and the pull-up resistor pulls the MDIO line to 1.

At the beginning of each transaction, the station management entity (STA) sends a preamble (PRE) sequence of 32 continuous 1 bits on MDIO during 32 corresponding cycles on the management data clock (MDC), providing a pattern that the MMD uses to establish synchronization. All MMDs observe the 32 continuous 1 bits before responding to any transaction.

Figure 35 • **MDIO Frame Format**



PRE 32	ST	OP	PA 5	DA 5	TA	D 16	Z

The MDIO frame format consists of the eight segments, shown above. Definitions for the segments are shown in the following table.

PRE 32	32 bits of 1 supplied by the STA.
ST	2 bits of 0, which indicates the start of frame.
OP	2 bits of Op-Code as described in IEEE 802.3ae Clause 45.
PA 5	5 bits of port address, which provides up to 32 ports to a physical bus.
DA 5	5 bits of destination MMD address, which provides up to 32 MMDs to a port.
TA	2 bits of turnaround time to change the bus ownership from the STA to MMD if required.
D 16	16 bits for address/data driven on the bus by the current master of the bus, the STA for write operation, and the MMD for a read or read-address-increment operation.
Z	Idle time, bus tri-stated.

The start of frame (ST) is indicated by the 00 pattern. Frames containing the ST = 01 pattern defined in IEEE 802.3ae Clause 22 are ignored.

The operation code (OP) indicates the type of transaction being performed by the frame:

- 00: Frame payload contains the address of the register to be accessed.
- 01: Frame payload contains data to be written to the register address supplied in the previous address frame.
- 11: Frame is a read operation.
- 10: Frame is a post-read-increment-address operation.

The port address (PRTAD) consists of 5 bits. The first bit transmitted and received is the MSB. The device address (DEVAD) also consists of 5 bits. The first bit transmitted and received is the MSB.

Turnaround (TA) is a 2-bit time spacing between the DEVAD field and the frame data field to avoid contention during a read transaction. For a read or post-read increment address transaction, the station management entity (STA) and the MDIO manageable device (MMD) remain in a high-impedance state for the first bit time of the turnaround. The MMD drives a 0 bit during the second bit time of the turnaround. For a write or address transaction, the STA drives a 1 for the first bit time of the turnaround, and a 0 for the second bit time of the turnaround.

The address or data field consists of 16 bits. For an address cycle, it contains the address of the register to be accessed on the next cycle. For read, write, and increment read cycles, the field contains the data for the register. The first bit transmitted and received is bit 15.

MDIO is a bidirectional signal that can be sourced by the station management entity (STA) or MDIO manageable device (MMD). For more information about MDIO timing specifications, see MDIO Interface, page 79.

MDIO write instructions to an invalid register address will be ignored. Read back of invalid register addresses yields 0xFFFF or 0x0000 depending on the reason the address was invalid. 0xFFFF is returned on a read of an invalid channel number which occurs when the port number in the instruction does not match pins PADDR[*]. The read data is 0xFFFF because the MDIO pin is left in high impedance state and an external pull-up brings the bus high. 0xFFFF is also returned on a read when a valid channel number is specified, but the device number is invalid. 0x0000 is returned on a read when a valid channel and device numbers are specified, but the register address does not exist in the part. Valid channel numbers are 0, 1, 2 and 3. valid device numbers are 1, 2, 3, 4, 7, 30, 31.

Firmware can be loaded into the microprocessor's RAM through the MDIO interface. Reads and writes to the RAM can be performed only when the microprocessor is held in software reset. A read of RAM address space when the µP is NOT in software reset returns all 0's since this is considered an invalid register address. Firmware is loaded into RAM through the MDIO interface by writing to device #31 in *any valid port number* (0-3). The MDIO read/write instructions operate on 16 bits of data whereas each RAM data word is 32 bits. Thus two MDIO write instructions are required to load one 32-bit word into RAM. Of the 16 register address bits in each MDIO instruction, the 15 most significant bits specify the RAM word address. The least significant register address bit indicates whether RAM data bits [31:16] or [15:0] are to be accessed. Setting the register address bit to 0 selects data bits [31:16]. Setting the register address bit to 1 selects data bits [15:0]. The following table lists the mapping of MDIO register address to RAM half data word.

Table 58 • **MDIO Register Address to RAM Address Mapping**

RAM Word Number	MS-Word	LS-Word
Word0	{15'h0000, 0}	{15'h0000, 1}
Word1	{15'h0001, 0}	{15'h0001, 1}
Word2	{15'h0002, 0}	{15'h0002, 1}
Word3	{15'h0003, 0}	{15'h0003, 1}
...	...	...
Word32,767	{15'h7FFF, 0}	{15'h7FFF, 1}

3.9.2 Two-Wire Serial (Master) for Loading Firmware

A two-wire serial master interface in the VSC8484 device is used exclusively to load firmware from an EEPROM. STWSCL and STWSDA are the two-wire serial master interface pins. The two-wire serial master interface is enabled only when firmware is to be loaded from an EEPROM. An EEPROM device is the only slave device that can be connected to the two-wire serial master interface.

The slave address sent in two-wire serial instructions from the VSC8484 to an EEPROM is a function of the STWA1 and STWA0 pins and the type of 128 kB EEPROM being addressed. The VSC8484 supports two different methods for addressing data in 128 kB EEPROMs. There is a difference in the way 64 kB pages of memory within the EEPROMs are addressed. The EEPROMs effectively make use of two slave addresses to access two 64 kB pages.

The 7-bit slave address formats transmitted by the VSC8484 consist of four fixed bits and the STWA0 and STWA1 pins as follows:

- Microchip 24xx1025: {1010, Page#, STWA1, STWA0}
- Atmel AT24C1024B: {1010, STWA1, STWA0, Page#}

Note: The two-wire serial master interface does not support multiple masters on the bus. Firmware cannot be loaded from one EEPROM into multiple VSC8484 devices. There must be one EEPROM from which firmware will be loaded for every VSC8484 device on the board.

The two-wire serial master issues a bus reset sequence before addressing the EEPROM. This reset ensures that the EEPROM is brought to an idle state, in case the firmware execution from the EEPROM

was previously interrupted and a reset was issued to the VSC8484 to restart firmware load and execution. For more information about operating modes for pin control, see Table 60, page 85.

3.9.3 Two-Wire Serial Slave Interface

The VSC8484 device supports a two-wire serial slave interface, enabling an external master device to control the VSC8484 device. The two-wire serial slave interface can read registers, write registers, and load firmware into internal memory.

The two-wire serial slave SCL and SDA pins, STWSCL_S and STWSDA_S, are multifunction general purpose I/O (GPIO) pins. The GPIO pins are configured to serve SCL and SDA functions following device reset.

A valid START condition is generated by the master device by transitioning the SDA line from high to low while the SCL line is high. Data is then transferred on the SDA line, most significant bit (MSB) first, with the SCL line clocking data. Data transitions during SCL low periods are valid (read) or latched (write) when SCL pulses high then low. Data transfers are acknowledged (ACK) by the receiving device (VSC8484) for data writes and by the master for data reads. An acknowledge is signaled by holding the SDA signal low while pulsing SCL high then low. The master terminates data transfer by generating a STOP condition by transitioning SDA low to high while SCL is high.

Note: If the external two-wire serial master device gets out of sync with the VSC8484 two-wire serial slave interface, the master device must issue a bus reset sequence, which puts the VSC8484 two-wire serial slave interface back into a state that allows it to receive future two-wire serial instructions. The external two-wire serial master device and the VSC8484 two-wire serial slave interface can become out-of-sync and freeze the bus if either is reset during an instruction.

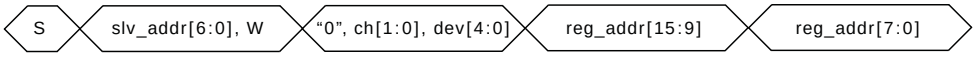
The two-wire serial slave address is a function of the MDIO port address pins PADDR[4:2] and four fixed values. The 7-bit slave address for the VSC8484 device is {1000, PADDR[4], PADDR[3], PADDR[2]}.

Note: The two-wire serial slave interface does not work with two-wire serial masters using 10-bit slave addresses.

Registers in the VSC8484 device are accessed using the 24-bit addressing scheme shown in the following illustration. The first 8 bits consist of a logic LOW, a 2-bit channel number, and the 5-bit MDIO device number of the register to be accessed. The next 16 bits consists of the actual register address. For example, the 24-bit register address for accessing register 1×8000 in channel 3 is 0×618000.

When a register is accessed, 16 bits of data are always read or written.

Figure 36 • **Two-Wire Serial (slave) Register Addressing Format**

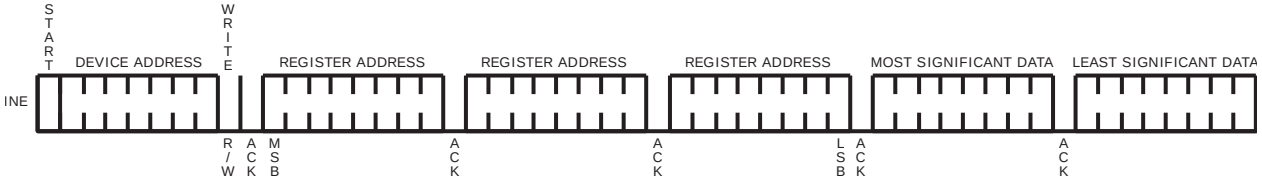


Note: An illegal two-wire serial slave read instruction to an invalid device number or register address returns a read value of 0×0000.

The two-wire serial slave interface supports auto-incrementing of register addresses to reduce the time it takes read or write sequential address registers. The auto-increment feature is useful for loading firmware into the internal memory.

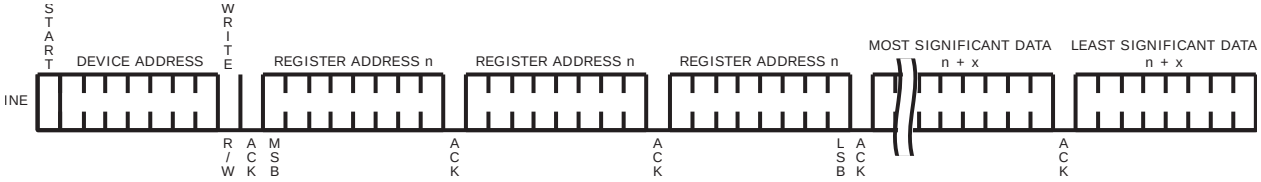
The following illustration shows the SDA pin state during support register read and write operations.

Figure 37 • **Write Instruction**



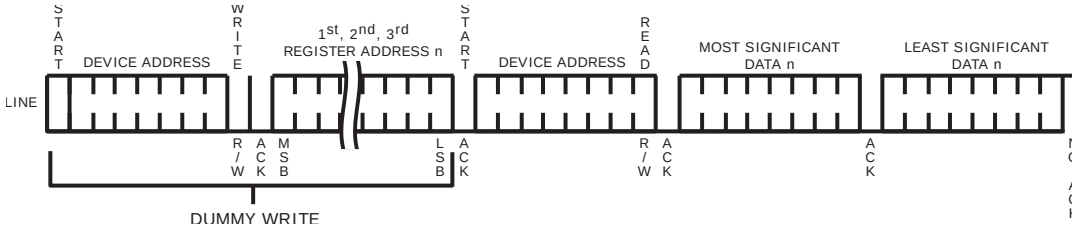
The VSC8484 device supports sequential write operations. Two bytes of data must be sent for each register address, as shown in the following illustration.

Figure 38 • **Sequential Write Instruction**



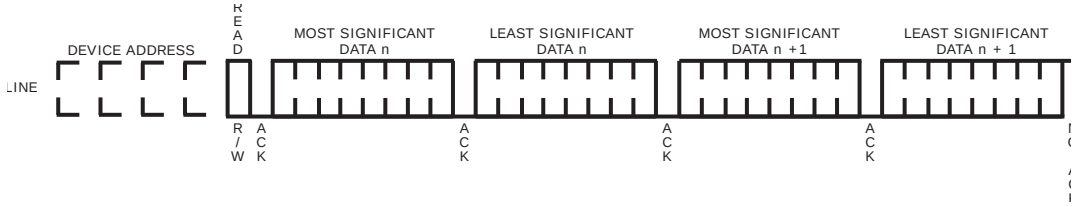
The following illustration shows a register read operation. The register to be addressed is specified by initiating a register write operation. After three register address bytes are sent to the VSC8484 device, a start condition must be sent to the VSC8484 device, followed by the device address with the read/write bit set to logic high. The two-byte register contents are then transmitted from the VSC8484 device. The two-wire serial master sends a NO ACK to the VSC8484 device after the second data byte to indicate that it is done reading data.

Figure 39 • **Read Instruction**



If an ACK is sent after the second data byte, the VSC8484 device assumes that a sequential register read is being requested and transmits the contents of the next register address. Sequential register reads continue until a NO ACK is sent. The following illustration shows a sequential read operation.

Figure 40 • **Sequential Read Instruction**



3.9.4 UART

The VSC8484 device has a UART interface for use in evaluation systems. Special firmware is required to enable the UART interface. Contact your Microsemi sales representative if you need to use this interface.

3.9.5 JTAG

The VSC8484 device has an IEEE 1149.1–2001 compliant JTAG interface. The 10 Gbps serial I/Os are not included in the JTAG boundary scan chain. Contact your Microsemi sales representative for the BSDL file containing the pin order in the boundary scan chain.

Note: For the EXTEST (0000) and CLAMP (0101) JTAG instructions, the RESETN boundary scan cell must be preloaded with a 1 before execution to prevent the JTAG TAP controller from being reset and clearing the instruction codes. To preload a 1 to the RESETN boundary scan cell, write a SAMPLE/PRELOAD instruction (0010).

After powerup, the JTAG TAP controller must be reset using the TRSTB pin in one of two ways: For designs not using JTAG features, TRSTB should be constantly driven LOW; for designs using JTAG features, TRSTB must be driven low after power is applied to the VSC8484 device to reset the JTAG TAP controller before part operation.

The following table lists the supported JTAG instruction codes. Contact your Microsemi sales representative if JTAG is used with V_{DDTTL} = 1.2 V.

Table 59 • **JTAG Instruction Codes**

Instruction	Instruction Code	Selected Data Register	Device Operating Mode	Description
EXTEST	0000	Boundary Scan	Test	JTAG instruction.
IDCODE	0001	Device ID	Normal	JTAG instruction used to read the device identification register.
SAMPLE/PRELOAD	0010	Boundary Scan	Normal	JTAG instruction.
HIGHZ	0100	Bypass	Test	JTAG instruction. Provides the ability to place all outputs in high impedance state to facilitate manufacturing test and PC board diagnostics. The XAUI serial data outputs are not put into high impedance state.
CLAMP	0101	Bypass	Test	JTAG instruction. Provides the ability to place all outputs in a predefined state while the scan process is being used for other devices on a PC board.
	0111	UDR0		
	1000	UDR1		
	1001	UDR2		
BYPASS	1111	Bypass	Normal	JTAG instruction.

3.10 Operating Modes

The VSC8484 device needs to be operated with firmware for enhanced performance, particularly in environments with large temperature variations. Use the EDC firmware for interfacing with SR/LR/ZR/ER/Cu-cable attach, and backplanes. Use the MDIO or two-wire serial (slave) interface to load the firmware from system memory. Or store the firmware in an EEPROM, and use the two-wire serial (master) interface to load the program at power-up.

Use KR auto-negotiation to set up the driver and receiver for backplane applications or use MDIO/two-wire serial programming to set up the required driver and receiver capability to compensate the fixed channel loss of the different channels over the backplane.

Two mode pins are dedicated to the different options for firmware operation.

At power up after a hardware reset, toggle the 1x80003 bit 0 from low to high and then back to low to avoid any PLL runaway. This forces the CRU to lock to reference and then to data.

After the WAN mode is enables, bit 1 and 2 of 1xAE00 need to be set high to reset the Tx and Rx PCS blocks before valid data is passed through.

3.10.1 Firmware Load Mode, EEPROM Address Format

The MODE1 and MODE0 pins are used to control the following:

Select whether firmware is loaded through the two-wire serial (master) using EEPROM or through MDIO/two-wire serial (slave). The source of the firmware needs to be known so the microprocessor's starting address of execution can be set (external EEPROM address vs. internal OCM (On Chip

Memory)) prior to deassertion of device reset. The state of the microprocessor software reset following hardware reset is also a function of the firmware load mode. The microprocessor is initially in software reset when the firmware is to be loaded through the MDIO interface. The microprocessor is not in software reset at power-up when firmware is loaded from an EEPROM. The microprocessor immediately fetches the first instruction from the EEPROM once the device's reset state has been deasserted.

128 kB EEPROMs do not have a standard protocol for accessing 64 kB memory pages because different vendors use different procedures. The address sent in the two-wire serial instruction is different. A mode pin selects the format of the address in the two-wire serial instruction to not get locked into using a specific EEPROM vendor.

Pins MODE1 and MODE0 select the modes listed in the following table:

Table 60 • **Operating Modes for Pin Control**

MODE1 Pin	MODE0 Pin	Firmware Load Method	EEPROM Slave Addressing
0	0	FW loaded through MDIO or two-wire serial (slave)	Reserved
0	1	Reserved for future use	
1	0	FW loaded from EEPROM using two-wire serial (master)	Support vendor B = Microchip 24xx1025 {4'b1010, Block, STWA[1], STWA[0]}
1	1	FW loaded from EEPROM using two-wire serial (master)	Support vendor A = Atmel AT24C1024B {4'b1010, STWA[1], STWA[0], Page}

3.10.2 Default Operation

Default operation is LAN mode for all four channels with all VCOs being driven by the XREFCK (XAUI) reference clock pin at 156.25 MHz. Register bit settings must be changed through MDIO/ P write instructions to switch to a different operating mode.

In general, for standard LAN application with SFP+ modules (SR/LR/ZR), the device is up and running after power up, without any firmware loading or register programming.

3.11 Loading Firmware

This section contains information about loading firmware to the VSC8484 device. Applications using electronic dispersion compensation (EDC) must load firmware into the VSC8484 device after powerup to enable the EDC feature. Firmware can be automatically loaded from an EEPROM connected to the VSC8484. Firmware can also be loaded through the MDIO or two-wire serial slave interfaces.

3.11.1 EEPROM

To load firmware using an EEPROM device, select the appropriate MODE pin settings. For more information about the MODE pin configuration settings, see Table 60, page 85. When enabled, firmware is automatically transferred from the EEPROM to the VSC8484 device when the hardware reset pin or microcontroller software reset is de-asserted (1Ex0002.7).

To load firmware from a single EEPROM on to multiple VSC8484 devices, program each VSC8484 device one at a time by holding the reset active for the other VSC8484 devices when it is not their turn to load firmware.

The two-wire serial (master) issues a special EEPROM RESET sequence before addressing the EEPROM. This ensures the EEPROM is bought to an idle state in the event that firmware execution from the EEPROM was previously interrupted, and a reset was issued to the VSC8484 device to restart firmware load and execution.

The EEPROM device must hold 128 kB of data. Data stored in the EEPROM is accessed through a two-wire serial interface using the STWSCL_FIRM and STWSDA_FIRM pins.

3.11.2 MDIO and Two-Wire Serial Slave Interfaces

Alternatively, firmware can be loaded to the VSC8484 memory through the MDIO or two-wire serial slave interfaces. The MODE1 pin must be driven to a logic low state for this method of loading firmware. For more information about the MODE pin configuration settings, see Table 60, page 85.

Data can be written to the VSC8484 memory only when the microcontroller is in a software reset state. To invoke a microprocessor software reset, write a logic high to register 1Ex0002.7. The microcontroller defaults to the software reset state after a hardware reset if MODE1 was driven to logic low when the hardware reset was de-asserted. Channel 0, device 31 is to be specified in the write instruction when loading the firmware into VSC8484 memory. After the firmware has been loaded into VSC8484 memory, the microcontroller software reset register 1Ex0002.7 must be cleared. Writing a logic low to the microcontroller software reset register immediately starts execution of the adaptive EDC algorithm.

To verify if the VSC8484 is ready to receive MDIO and two-wire serial instructions, read the device ID register 1Ex0000. The device is ready to receive register write instructions when the device ID is returned.

The following list contains the first few lines of a sample firmware file for illustration purposes only. The sample does not represent the actual firmware. Firmware is provided in Motorola hex format.

S00C000065646334322E7333721B

S315BFB000003C16008036D6000040966000000008213E

S315BFB000100000102100001821000020210000282177

Lines starting with S3 contain data to be loaded into the VSC8484 internal RAM. The next two digits are a hexadecimal number indicating the number of remaining bytes contained in the line. The remaining bytes in the line contain a checksum, data to be written to VSC8484 memory, and a memory address where the data is to be written. The data fields in the firmware are always 4 bytes in size to match the word size of the VSC8484 memory. The 4 bytes following the byte count is the address the microcontroller uses to access data in the VSC8484 memory. The address in this line indicates the VSC8484 memory address where the next 4 bytes of data are to be written. Subsequent 4-byte data fields are written to the next higher VSC8484 memory address. The next higher address is the current address plus four, because the microcontroller considers each byte of data one address and there are 4 bytes of data in each data word. The last byte of data in the line is the checksum value.

The following sample firmware file contains added spaces for improved readability.

S3 15 BFB00000 3C160080 36D60000 40966000 00000821 3E

S3 15 BFB00010 00001021 00001821 00002021 00002821 77

In this example, there are 21 bytes (15 hexadecimal) of data following the byte count. There are 4 bytes of address, 16 bytes of data, and 1 checksum byte. The data is mapped to the VSC8484 memory as follows:

- 3C160080 is written to microcontroller memory address BFB00000.
- 36D60000 is written to microcontroller memory address BFB00004.
- 40966000 is written to microcontroller memory address BFB00008.
- 00000821 is written to microcontroller memory address BFB0000C.
- 00001021 is written to microcontroller memory address BFB00010.

The protocol for writing data to the VSC8484 memory through MDIO and two-wire serial slave commands is the same as writing data to status or configuration registers. A 16-bit address and 16-bit data word is specified in the write instruction. For more information about using the MDIO and two-wire serial slave interfaces, see MDIO Interface, page 79 and Two-Wire Serial Slave Interface, page 82.

The 128 kB of VSC8484 internal memory is configured as 4-byte words × 32 kB addresses. To completely access the memory, 2^{15} addresses are required. The microcontroller address specified in the firmware file contains 32 bits, whereas the MDIO instruction allows only 16 address bits. The 32-bit microcontroller address must be translated to a 15-bit memory address prior to writing firmware to the VSC8484 device. Map the microcontroller address 0×BFB00000 to memory address 0×0000, 0×BFB00004 to 0×0001, 0×BFB00008 to 0×0002, and so on.

Two MDIO or two-wire serial slave write instructions must be issued to write four data bytes to each RAM address, because only two bytes of data are allowed in each instruction. One address bit in the write instruction specifies which two bytes in the VSC8484 memory are to be accessed. The two most significant RAM bytes are accessed when the byte access bit is 0. The two least significant RAM bytes are accessed when the byte access bit is 1.

The address sent in the MDIO or two-wire serial slave write instructions consists of the translated 15-bit VSC8484 memory address and the memory's byte access bit in the least significant bit position.

Based on the sample firmware, the MDIO or two-wire serial slave instructions are as follows:

- Write the data 0×3C16 to address 000000000000000_0'b, device 29, channel 0.
- Write the data 0×0080 to address 000000000000000_1'b, device 29, channel 0.
- Write the data 0×36D6 to address 000000000000001_0'b, device 29, channel 0.
- Write the data 0×0000 to address 000000000000001_1'b, device 29, channel 0.
- Write the data 0×4096 to address 000000000000010_0'b, device 29, channel 0.

After the firmware has been written to VSC8484 internal memory, write a 0 to 1Ex0002.7 in channel 0 to clear the microcontroller software reset and immediately start execution of the adaptive EDC algorithm.

A checksum of the loaded firmware is run after the microcontroller software reset is released. The VSC8484 memory is not reset at powerup by the hardware reset pin, or by any of the software reset options.

Note: Unknown initial conditions in the memory present a problem for the checksum calculation. All unused memory address space must be initialized to 0 for addresses between the microcontroller address BFB00000 to the largest address containing data, as defined in the firmware file. The checksum is calculated only over that address range. Memory addresses larger than those found in the firmware file do not need to be initialized.

The result of the checksum is reported in register 1Ex7FE0. If the checksum failed, the firmware must be reloaded.

3.12 Microcontroller Activity Monitoring

The VSC8484 automatically monitors the internal microcontroller for activity through the use of a watchdog feature (register 1Ex0004.6:4) when firmware is loaded from an EEPROM. If the watchdog logic determines that the microcontroller has stopped functioning, the firmware is automatically reloaded from the EEPROM and resumes execution.

When firmware is loaded to the VSC8484 device through the MDIO or two-wire serial slave interfaces, there is no means available to automatically reload the firmware if the microcontroller has stopped functioning. The watchdog feature must be disabled in this mode. You must determine if the microcontroller has ceased to function, and reload the firmware through the MDIO or two-wire serial slave interface.

To determine if the microcontroller is functioning normally, poll channel 0 register address 1Ex7FE1. The microcontroller increments the contents of this register by 1 every 100 ms or less. If the contents of the register stop changing, the microcontroller has malfunctioned and the VSC8484 device must be reset and firmware must be reloaded. The counter contents in register 1Ex7FE1 does not saturate at 0×FFFF. The value rolls over to 0×0000 when 0×FFFF is incremented.

The VSC8484 software is reset by writing 0×FFFF to channel 0 register address 1Ex0002. After device reset, the microcontroller goes into software reset state, allowing the firmware to be reloaded into the VSC8484.

3.13 Interrupt Pending Registers

The VSC8484 device has interrupt pending registers that may drive a hardware interrupt pin routed off the device through GPIO pins. There is a maximum of two interrupt pins per channel. The interrupt pending registers are individually masked to allow the user to select which interrupt events assert the hardware interrupt pins. The majority of the interrupt pending registers are related to WIS alarm states. For GPIO pins configured as inputs, the VSC8484 device can also assert an interrupt pending registers when incoming signals change state. The GPI interrupt pending signals do not contribute to any of the

channel specific WIS hardware interrupt pins. The GPI interrupts are intended to be polled by the firmware and let the firmware take appropriate action when the input changes state.

Interrupt pending registers are asserted when an interrupt event occurs. The interrupt pending register is cleared when the register is read. In situations when an interrupt event occurs at the same time the alarm's interrupt pending register is being cleared, the VSC8484 device first clears the interrupt pending register then reasserts the pending register. The minimum interrupt pending deassertion time is configured in register 1Ex0023. Any interrupt event that occurs within the minimum time window of the interrupt pending register being cleared will have interrupt pending reservation delayed to guarantee the minimum deassertion time. The minimum interrupt pending deassertion time can be programmed from two XREFCK clock periods to over 3 µs. The actual deassertion time is a function of XREFCK frequency as noted in the register description of 1Ex0023.

Note: The minimum deassertion time applies to each individual interrupt pending register. There is no guaranteed minimum deassertion time on the interrupt pin because multiple asynchronous interrupt events contribute to the interrupt pin logic and may occur at any time.

There is no hardware guarantee an interrupt pending register will remain asserted for any amount of time. Reading the interrupt pending register clears the register immediately, even if the register had just been asserted just one cycle sooner. This theoretically could result in a "glitch" on the interrupt pin that the host can not detect. Nor can the host figure out which interrupt caused the asserted state because the interrupt pending bit is now cleared. This situation is avoided if interrupt processing software never clears an interrupt pending register unless it had been previously set.

All interrupt pending registers share the same minimum interrupt pending register deassertion time programmed in 1Ex0023 except channel register 1xA200.0. This second LOPC interrupt pending register has a hard-coded minimum deassertion time of two XREFCK clock cycles. This LOPC interrupt pending register is available in case the firmware needs to know when the LOPC pin changes state in a more timely manner than a large value of 1Ex0023. The LOPC interrupt pending register in 1xA200.0 does not contribute to the WIS hardware interrupt pins. The LOPC interrupt pending register in 2xEE04.11 does contribute to the WIS hardware interrupt pins and does make use of the minimum interrupt pending deassertion time programmed in 1Ex0023.

3.14 Multipurpose GPIO Pins

The VSC8484 device has general purpose input/output (GPIO) pins that serve multiple functions. The GPIO pins are bidirectional I/Os, the driver portion of which is an open-drain buffer. The following table lists the functions that each pin supports and the registers used to program the pin functions. Leave GPIO pins unconnected when not used. When configured as output, they are open-drained and a pull-up is required.

Table 61 • **GPIO Functions**

Pin Name	Pin Configuration Registers	Pin Functions
GPIO_0	1Ex0100, 1Ex0101	Traditional I/O Observed internal signals MOD_ABS_Channel_0 (default) PMTICK ROSI frame pulse 0 Tx Activity LED WIS_INTB
GPIO_1	1Ex0102, 1Ex0103	Traditional I/O (default) Observed internal signals ROSI_CLK_0 Rx Activity LED WIS_INTA

Table 61 • **GPIO Functions *(continued)***

Pin Name	Pin Configuration Registers	Pin Functions
GPIO_2	1Ex0104, 1Ex0105	Traditional I/O Observed internal signals Slave two-wire serial - SDA (default) ROSI_DATA_0 Tx Activity LED WIS_INTB
GPIO_3	1Ex0106, 1Ex0107	Traditional I/O Observed internal signals Slave two-wire serial - SCL (default) TOSI_FRAME_PULSE_0 Rx Activity LED WIS_INTB
GPIO_4	1Ex0108, 1Ex0109	Traditional I/O (default) Observed internal signals TOSI_CLK_0 Tx Activity LED WIS_INTB
GPIO_5	1Ex010A, 1Ex010B	Traditional I/O Observed internal signals TOSI_INPUT_0 Rx Activity LED WIS_INTA
GPIO_6	1Ex010C, 1Ex010D	Traditional I/O (default) Observed internal signals ROSI frame pulse 1 Tx Activity LED WIS_INTB
GPIO_7	1Ex010E, 1Ex010F	Traditional I/O (default) Observed internal signals ROSI_CLK_1 Rx Activity LED WIS_INTA
GPIO_8	1Ex0110, 1Ex0111	Traditional I/O (default) Observed internal signals ROSI_DATA_1 Tx Activity LED WIS_INTB Mod_ABS channel 1
GPIO_9	1Ex0112, 1Ex0113	Traditional I/O (default) Observed internal signals TOSI_FRAME_PULSE_1 Rx Activity LED WIS_INTA
GPIO_10	1Ex0114, 1Ex0115	Traditional I/O (default) Observed internal signals TOSI_CLK_1 Tx Activity LED WIS_INTB

Table 61 • **GPIO Functions *(continued)***

Pin Name	Pin Configuration Registers	Pin Functions
GPIO_11	1Ex0116, 1Ex0117	Traditional I/O (default) Observed internal signals TOSI_INPUT_1 Rx Activity LED WIS_INTA
GPIO_12	1Ex0118, 1Ex0119	Traditional I/O (default) Observed internal signals ROSI frame pulse 2 Tx Activity LED WIS_INTB
GPIO_13	1Ex011A, 1Ex011B	Traditional I/O (default) Observed internal signals ROSI_CLK_2 Rx Activity LED WIS_INTA
GPIO_14	1Ex011C, 1Ex011D	Traditional I/O (default) Observed internal signals ROSI_DATA_2 Tx Activity LED WIS_INTB Mod_ABS channel 2
GPIO_15	1Ex011E, 1Ex011F	Traditional I/O (default) Observed internal signals TOSI_FRAME_PULSE_2 Rx Activity LED WIS_INTA
GPIO_16	1Ex0120, 1Ex0121	Traditional I/O (default) Observed internal signals TOSI_CLK_2 Tx Activity LED WIS_INTB
GPIO_17	1Ex0122, 1Ex0123	Traditional I/O (default) Observed internal signals TOSI_INPUT_2 Rx Activity LED WIS_INTA
GPIO_18	1Ex0124, 1Ex0125	Traditional I/O Observed internal signals UART-Tx (Default) ROSI_FRAME_PULSE_3 Tx Activity LED WIS_INTB
GPIO_19	1Ex0126, 1Ex0127	Traditional I/O Observed internal signals UART-Rx (Default) ROSI_CLK_3 Rx Activity LED WIS_INTA

Table 61 • **GPIO Functions *(continued)***

Pin Name	Pin Configuration Registers	Pin Functions
GPIO_20	1Ex0128, 1Ex0129	Traditional I/O (default) Observed internal signals ROSI_DATA_3 Tx Activity LED WIS_INTA
GPIO_21	1Ex012A, 1Ex012B	Traditional I/O Observed internal signals Mod_ABS channel 3 (default) PMTICK TOSI_FRAME_PULSE_3 Rx Activity LED WIS_INTA
GPIO_22	1Ex012C, 1Ex012D	Traditional I/O (default) Observed internal signals TOSI_CLK_3 Tx Activity LED WIS_INSTB
GPIO_23	1Ex012E, 1Ex012F	Traditional I/O Observed internal signals TOSI_INPUT_3 Rx Activity LED WIS_INTA

When a GPIO pin is programmed to be a traditional I/O, the pin can be driven high or low, and can serve as an input and an LED driver capable of blinking at various rates. An interrupt pending register can optionally be asserted when the pin is in input mode and the pin changes state. All of these functions can be configured using the pin configuration register settings shown in the preceding table.

The GPIO pin's output driver is automatically enabled when the pin function is set to observe internal signals. The second configuration listed for each pin selects which internal signal is transmitted from the pin. For more information about the list of signals that can be observed, see Channel Registers, page 172.

3.15 PCS Activity Monitor LEDs

The GPIO pins can be configured to output 10G PCS link and data activity status from each channel. When the GPIO pins are configured to report PCS activity status, register bits 1xA100.4:3 and 1xA100.6:5 are used to select the various Rx and Tx reporting modes. The open drain GPIO pins are expected to be connected to LEDs. The LEDs are turned on when the pin sinks current.

The following table lists the states of the Rx PCS activity monitor.

Table 62 • **Rx PCS Activity Monitor States**

Setting	Rx Activity LED Reports	Description
1xA100.4:3 = 00	Link status	The LED is ON when the Rx link is up. The Rx link is up when either the PCS is in the block lock condition and the FEC is disabled in 1x00AB.0 or the FEC has achieved lock when the FEC is enabled.
1xA100.4:3 = 01	Reserved	

Table 62 • **Rx PCS Activity Monitor States**

Setting	Rx Activity LED Reports	Description
1xA100.4:3 = 10	Link status and data activity	The LED is off when the link is down. The LED is on steady if the link is up, but no ||S|| characters are being received. The LED blinks for 0.5 seconds after a ||S|| character is received. The LED blinks continuously when ||S|| characters are received continuously. The LED is held on steady for 5 seconds after the link comes up, even if ||S|| characters are detected sooner.

The following table lists the states of the Tx PCS activity monitor.

Table 63 • **Tx PCS Activity Monitor States**

Setting	Tx Activity LED Reports	Description
1xA100.6:5 = 00	Link status	The LED is ON when the Tx link is up. The Tx link is up when the XAUI lanes are aligned (4x0018.12=1).
1xA100.6:5 = 01	Reserved	
1xA100.6:5 = 10	Link status and data activity	The LED is off when the link is down. The LED is on steady if the link is up, but no ||S|| characters are being transmitted. The LED blinks for 0.5 seconds after a ||S|| character is transmitted. The LED blinks continuously when ||S|| characters are transmitted continuously. The LED is held on steady for 5 seconds after the link comes up, even if ||S|| characters are transmitted sooner.

3.16 Temperature Monitor

The VSC8484 device features both an analog and a digital temperature monitor. The analog temperature monitor has dedicated primary output pin TMON. The analog temperature monitor is disabled by default. To enable it, write a low to register 1Ex7FD6.14. The analog temperature monitor requires a 3.3 V power supply to the pin VDDTTLL.

Table 64 • **Temperature Monitor**

Register 1Ex7FD6.14	Temperature Monitor
0	Enable
1	Disable (default)

The digital temperature monitor is also disabled by default. It can be enabled by writing high to register 1E×7FD6.12. To initiate a measurement, set register 1E×7FD6.11 to high. All other writes to this register are ignored until the measurement is done, indicated by a high in register 1E×7FD6.10. This register will be high, indicating that the measured value presented in register 1E×7FD6.7:0 was updated. The register then goes low after it is read.

There are two temperature alarm bits and an alarm threshold register. The threshold register is read/write. The upper byte of the threshold register contains the high temperature threshold value. The lower byte contains the low threshold value. By default, the high threshold is set to 0×FF, and the low threshold is set to 0×00. The alarms become valid when the TMON_DONE bit is asserted, and remains at that state until the next measurement is performed.

The following tables show the digital temperature monitor configuration registers.

Table 65 • **Digital Temperature Monitor Control Register**

Register Name	Address	Function	State
TMON_ENABLE	1E×7FD6.12	Enable	0: Disabled (default) 1: Enabled
TMON_RUN	1E×7FD6.11	Start	0: No measurement (default) 1: Start measurement
TMON_DONE	1E×7FD6.10	Complete	0: TMON_OUT contains last measured value 1: TMON_OUT updated
TMON_OUT<7:0>	1E×7FD6.7:0	Result	Always contains the last measurement

Table 66 • **Temperature Alarm Threshold Register**

Register Name	Address	Function	State
TMON_TH_HI<7:0>	1E×FECF.15:8	High temperature alarm threshold	Default = 0×FF
TMON_TH_LO<7:0>	1E×7FD5.7:0	Low temperature alarm threshold	Default = 0×00

Table 67 • **Temperature Alarm Register**

Register Name	Address	Function	State
TMON_ALARM_HI	1E×7FD6.9	Temperature exceeds high threshold setting	0: Temp ≤ high threshold 1: Temp > high threshold
TMON_ALARM_LO	1E×7FD6.8	Temperature below low threshold setting	0: Temp ≥ low threshold 1: Temp < low threshold

4 Registers

This section provides information about the register tables and descriptions for the VSC8484 device. The registers marked reserved and factory test should not be read or written to, because doing so may produce undesired effects.

The default value documented for registers is based on the value at reset; however, in some cases, that value may change immediately after reset.

The access type for each register is shown using the following abbreviations:

- RO: Read Only
- ROCR: Read Only, Clear on Read
- RO/LH: Read Only, Latch High
- RO/LL: Read Only, Latch Low
- RW: Read and Write
- RWSC: Read Write Self Clearing

Note: Use two consecutive reads to obtain the current status of latch low and latch high registers.

4.1 Global Registers

This section provides information about the Global registers. These device 1E registers are common to all four channels. These registers can be accessed using the MDIO port address for channels 0 to 3 when using the MDIO interface. Channel numbers 0 to 3 may be specified in the register address when using the two-wire serial (slave) interface.

Table 68 • **Device ID (1Ex0000)**

Bit	Name	Description	Access	Default
15:0	Device ID	Device product number	RO	0x8484

Table 69 • **Device Revision (1Ex0001)**

Bit	Name	Description	Access	Default
15:4	Reserved		RW	0
3:0	Device Revision	Device revision number	RO	0010

Table 70 • **Block Level Software Reset (1Ex0002)**

Bit	Name	Description	Access	Default
15	Software reset EDC 3	Resets register map flip-flops in EDC block. 0: Normal operation 1: Reset	RW SC	0
14	Software reset EDC 2	Resets register map flip-flops in EDC block. 0: Normal operation 1: Reset	RW SC	0

Table 70 • **Block Level Software Reset (1Ex0002)** ***(continued)***

Bit	Name	Description	Access	Default
13	Software reset EDC 1	Resets register map flip-flops in EDC 1 block. 0: Normal operation 1: Reset	RW SC	0
12	Software reset EDC 0	Resets register map flip-flops in EDC 0 block. 0: Normal operation 1: Reset	RW SC	0
11	Software reset channel 3	Resets the datapath and register map flip-flops 0: Normal operation 1: Reset	RW SC	0
10	Software reset channel 2	Resets the datapath and register map flip-flops 0: Normal operation 1: Reset	RW SC	0
9	Software reset channel 1	Resets the datapath and register map flip-flops of channel 1 0: Normal operation 1: Reset controls physical channel #3 in dual channel mode.	RW SC	0
8	Software reset channel 0	Resets the datapath and register map flip-flops of channel 0 0: Normal operation 1: Reset	RW SC	0
7	Software reset microprocessor	0: Normal operation 1: Reset **Note:** MODE1 and MODE0 pins determine the method to load firmware	RW	0 if firmware is loaded from an EEPROM 1 if firmware is loaded through the MDIO or two-wire serial (slave) interfaces
6	Software reset BIU	0: Normal operation 1: Reset	RW SC	0
5	Software reset TWS slave	0: Normal operation 1: Reset	RW SC	0
4	Software reset TWS master	0: Normal operation 1: Reset	RW SC	0
3	Software reset MDIO	0: Normal operation 1: Reset	RW SC	0
2	Software reset UART	0: Normal operation 1: Reset	RW SC	0
1	Global reg reset	0: Normal operation 1: Reset resets all global registers to default values.	RW SC	0

Table 70 • **Block Level Software Reset (1Ex0002) *(continued)***

Bit	Name	Description	Access	Default
0	Software reset chip	0: Normal operation 1: Reset resets every flip-flop in the device EXCEPT the global register block.	RW SC	0

Table 71 • **Failover Crosspoint Control (1Ex0003)**

Bit	Name	Description	Access	Default
15:2	Reserved		RW	0
1		Enables failover crosspoint between data paths 2 and 3. 0: Failover disabled. 1: Failover enabled. PMA3 is connected WIS/PCS/XAUI datapath2 and PMA2 is connected WIS/PCS/XAUI datapath3.	RW	0
0		Enables failover crosspoint between data paths 0 and 1. 0: Failover disabled. 1: Failover enabled. PMA1 is connected WIS/PCS/XAUI datapath0 and PMA0 is connected WIS/PCS/XAUI datapath1.	RW	0

Table 72 • **Timer Control (1Ex0004)**

Bit	Name	Description	Access	Default
15:7	Reserved		RW	0
6	Timer 4 watchdog reset status	Watchdog reset status 1: Reset happened 0: Reset didn't happen or was cleared	RO LH	0
5	Timer 4 watchdog enable	Timer 4 watchdog enable status 1: Enabled 0: Disabled	RW	1 if firmware is loaded from an EEPROM 0 if firmware is loaded through the MDIO or two-wire serial (slave) interfaces
4	Timer 4 enable	Timer 4 enable status 1: Enabled 0: Disabled	RW	1 if firmware is loaded from an EEPROM 0 if firmware is loaded through the MDIO or two-wire serial (slave) interfaces
3:0	Reserved		RW	0

Note: Registers 1Ex0005 through 1Ex0032 are reserved for factory testing only.

4.1.1 GPIO Pins

The following tables list the details for the GPIO pins.

Table 73 • **GPIO 0 Config/ Status (1Ex0100)**

Bit	Name	Description	Access	Default
15	Traditional GPIO 0 Output Tri-state Control	Controls whether the pin is in input or output mode. Applies only when bit 2:0=000 0: Output mode 1: Input mode	RW	1
14:13	Traditional GP0IO 0 Pin Function Selection	Applies only when bit 2:0=000 When bit 15=0 (output mode): 00: bit 12 is driven out the pin. 01: drive repeating LOW/Hi-Z pattern at 1Hz, 2Hz, and 5Hz. When=1 (input mode): 00: no interrupt is generated. 01: interrupt generated on the rising edge of pin. 10: interrupt generated on the falling edge of pin. 11: interrupt generated on the both rising and falling edge of pin.	RW	00
12	Traditional GPIO 0 Output data	Logic value transmitted from pin when pin is configured as a traditional general purpose output=000 and 0 0: Output data = 0 1: Output data = 1	RW	0
11	General Purpose Input Interrupt Pending	GPIO0 must be configured as a general purpose input and have interrupt generation enabled. 0: no interrupt event since the last time the register was read 1: an interrupt event has occurred clear on read	RO	0
10	General Purpose Input Status	Indicates the present value of the GPIO0 pin 0: Present value of GPIO0 pin is 0 1: Present value of GPIO0 pin is 1	RO	
9	PMTICK Enable 1	0: Pin is not used as a PMTICK input. 1: Enable use of this pin as a PMTICK input. Pin must be configured as a general purpose input for these bit to serve a purpose.	RW	0
8	Module Status Input Enable - channel 0	0: interrupt generation logic for channel 0's module status is disabled. 1: Enable use of this pin to drive interrupt generation logic for channel 0's module status. Pin must be configured as a general purpose input for these bit to serve a purpose.	RW	0

Table 73 • **GPIO 0 Config/ Status (1Ex0100) *(continued)***

Bit	Name	Description	Access	Default
7:5	GPIO0 WIS Interrupt Selection	Determines the WIS interrupt status transmitted from the pin when=010 000: WIS interrupt B from channel 0 001: WIS interrupt B from channel 1 010: WIS interrupt B from channel 2 011: WIS interrupt B from channel 3 100: Logical AND of WIS interrupt B from all channels 101: Logical OR of WIS interrupt B from all channels 110: Reserved 111: Reserved	RW	000
4:3	GPIO0 Link Activity Selection	Determines which channel's link activity is transmitted from the pin when=001 00: Tx link activity from channel 0 01: Tx link activity from channel 1 10: Tx link activity from channel 2 11: Tx link activity from channel 3	RW	00
2:0	GPIO0 Pin Function Selection	Selects the GPIO pin's functionality. 000: Traditional GPIO behavior 001: PCS activity LED output 010: WIS interrupt output 011: Transmit internal signals 100-111: Reserved	RW	000

Table 74 • **GPIO 0 Config2 (1Ex0101)**

Bit	Name	Description	Access	Default
15:7	Reserved		RW	0

Table 74 • **GPIO 0 Config2 (1Ex0101)** ***(continued)***

Bit	Name	Description	Access	Default
6:0	GPIO0 Internal Node Selection	Determines which channel's link activity is transmitted from the pin when=011 0x7F to 0x6C: Reserved 0x6B: ch3_sw_los 0x6A: ch3_sw_losn 0x69: ch3_hw_los 0x68: ch3_hw_losn 0x67: ch2_sw_los 0x66: ch2_sw_losn 0x65: ch2_hw_los 0x64: ch2_hw_losn 0x63: ch1_sw_los 0x62: ch1_sw_losn 0x61: ch1_hw_los 0x60: ch1_hw_losn 0x5F to 0x58: Reserved 0x57: ch0_sw_los 0x56: ch0_sw_losn 0x55: ch0_hw_los 0x54: ch0_hw_losn 0x53: ref_cmu_loln 0x52: Reserved 0x51: Reserved 0x50: ch0_rosi_frame_pulse_output 0x4F to 0x4C: Reserved 0x4B: ch1_txen_inverted 0x4A: ch1_txen 0x49: ch0_txen_inverted 0x48: ch0_txen 0x47: Reserved 0x46: Reserved 0x45: ch1_rxalarm 0x44: ch0_rxalarm 0x43: Reserved 0x42: Reserved 0x41: ch1_txalarm 0x40: ch0_txalarm 0x3F: Reserved 0x3E: Reserved 0x3D: ch1_lopc 0x3C: ch0_lopc 0x3B to 0x08: Reserved 0x07: ch1_pma_rxlol 0x06: ch1_pma_rxloln 0x05: ch0_pma_rxlol 0x04: ch0_pma_rxloln 0x03 to 0x00: Reserved	RW	0

Table 75 • **GPIO 1 Config/ Status (1Ex0102)**

Bit	Name	Description	Access	Default
15	Traditional GPIO 1 Output Tri-state Control	Controls whether the pin is in input or output mode. Applies only when bit 2:0 gpio1_pinfunc_sel=000 0: Output mode 1: Input mode	RW	1
14:13	Traditional GP0IO 1 Pin Function Selection	Applies only when bit 2:0, gpio1_pinfunc_sel=000 When bit 15, gpio1_trad_tri=0 (output mode): 00: bit 12, gpio1_trad_datareg is driven out the pin. 01: drive repeating LOW/Hi-Z pattern at 1Hz. 01: drive repeating LOW/Hi-Z pattern at 2Hz. 01: drive repeating LOW/Hi-Z pattern at 5Hz. When gpio1_trad_tri=1 (input mode): 00: no interrupt is generated. 01: interrupt generated on the rising edge of pin. 10: interrupt generated on the falling edge of pin. 11: interrupt generated on the both rising and falling edge of pin.	RW	00
12	Traditional GPIO 1 Output data	Logic value transmitted from pin when pin is configured as a traditional general purpose output (gpio1_pinfunc_sel=000 and gpio1_trad_tri=0) 0: Output data = 0 1: Output data = 1	RW	0
11	General Purpose Input Interrupt Pending	GPIO1 must be configured as a general purpose input and have interrupt generation enabled. 0: no interrupt event since the last time the register was read 1: an interrupt event has occurred clear on read	RO	0
10	General Purpose Input Status	Indicates the present value of the GPIO1 pin 0: Present value of GPIO1 pin is 0 1: Present value of GPIO1 pin is 1	RO	
9:8	Reserved		RW	0
7:5	GPIO1 WIS Interrupt Selection	Determines the WIS interrupt status transmitted from the pin when gpio1_pinfunc_sel=010 000: WIS interrupt A from channel 0 001: WIS interrupt A from channel 1 010: WIS interrupt A from channel 2 011: WIS interrupt A from channel 3 100: Logical AND of WIS interrupt A from all channels 101: Logical OR of WIS interrupt A from all channels 110-111: Reserved	RW	000

Table 75 • **GPIO 1 Config/ Status (1Ex0102) *(continued)***

Bit	Name	Description	Access	Default
4:3	GPIO1 Link Activity Selection	Determines which channel's link activity is transmitted from the pin when gpio1_pinfunc_sel=001 00: Rx link activity from channel 0 01: Rx link activity from channel 1 10: Rx link activity from channel 2 11: Rx link activity from channel 3	RW	00
2:0	GPIO1 Pin Function Selection	Selects the GPIO pin's functionality. 000: Traditional GPIO behavior 001: PCS activity LED output 010: WIS interrupt output 011: Transmit internal signals 100-111: Reserved	RW	000

Table 76 • **GPIO 1 Config2 (1Ex0103)**

Bit	Name	Description	Access	Default
15:7	Reserved		RW	0

Table 76 • **GPIO 1 Config2 (1Ex0103)** ***(continued)***

Bit	Name	Description	Access	Default
6:0	GPIO1 Internal Node Selection	Determines which channel's link activity is transmitted from the pin when gpio1_pinfunc_sel=011 0x7F to 0x6C: Reserved 0x6B: ch3_sw_los 0x6A: ch3_sw_losn 0x69: ch3_hw_los 0x68: ch3_hw_losn 0x67: ch2_sw_los 0x66: ch2_sw_losn 0x65: ch2_hw_los 0x64: ch2_hw_losn 0x63: ch1_sw_los 0x62: ch1_sw_losn 0x61: ch1_hw_los 0x60: ch1_hw_losn 0x5F to 0x58: Reserved 0x57: ch0_sw_los 0x56: ch0_sw_losn 0x55: ch0_hw_los 0x54: ch0_hw_losn 0x53: ref_cmu_loln 0x52: Reserved 0x51: Reserved 0x50: ch0_rosi_sclk 0x4F to 0x4C: Reserved 0x4B: ch1_txen_inverted 0x4A: ch1_txen 0x49: ch0_txen_inverted 0x48: ch0_txen 0x47: Reserved 0x46: Reserved 0x45: ch1_rxalarm 0x44: ch0_rxalarm 0x43: Reserved 0x42: Reserved 0x41: ch1_txalarm 0x40: ch0_txalarm 0x3F: Reserved 0x3E: Reserved 0x3D: ch1_lopc 0x3C: ch0_lopc 0x3B to 0x08: Reserved 0x07: ch1_pma_rxlol 0x06: ch1_pma_rxloln 0x05: ch0_pma_rxlol 0x04: ch0_pma_rxloln 0x03 to 0x00: Reserved	RW	0

Table 77 • **GPIO 2 Config/ Status (1Ex0104)**

Bit	Name	Description	Access	Default
15	Traditional GPIO 2 Output Tri-state Control	Controls whether the pin is in input or output mode. Applies only when bit 2:0, gpio2_pinfunc_sel=000 0: Output mode 1: Input mode	RW	1
14:13	Traditional GP0IO 2 Pin Function Selection	Applies only when bit 2:0, gpio2_pinfunc_sel=000 When bit 15, gpio2_trad_tri=0 (output mode): 00: bit 12, gpio2_trad_datareg is driven out the pin. 01: drive repeating LOW/Hi-Z pattern at 1Hz. 01: drive repeating LOW/Hi-Z pattern at 2Hz. 01: drive repeating LOW/Hi-Z pattern at 5Hz. When gpio2_trad_tri= 1 (input mode): 00: no interrupt is generated. 01: interrupt generated on the rising edge of pin. 10: interrupt generated on the falling edge of pin. 11: interrupt generated on the both rising and falling edge of pin.	RW	00
12	Traditional GPIO 2 Output data	Logic value transmitted from pin when pin is configured as a traditional general purpose output (gpio2_pinfunc_sel=000 and gpio2_trad_tri=0) 0: Output data = 0 1: Output data = 1	RW	0
11	General Purpose Input Interrupt Pending	GPIO2 must be configured as a general purpose input and have interrupt generation enabled. 0: no interrupt event since the last time the register was read 1: an interrupt event has occurred clear on read	RO	0
10	General Purpose Input Status	Indicates the present value of the GPIO2 pin 0: Present value of GPIO2 pin is 0 1: Present value of GPIO2 pin is 1	RO	
9:8	Reserved		RW	0
7:5	GPIO2 WIS Interrupt Selection	Determines the WIS interrupt status transmitted from the pin when gpio2_pinfunc_sel=010 000: WIS interrupt B from channel 0 001: WIS interrupt B from channel 1 010: WIS interrupt B from channel 2 011: WIS interrupt B from channel 3 100: Logical AND of WIS interrupt B from all channels 101: Logical OR of WIS interrupt B from all channels 110-111: Reserved	RW	000

Table 77 • **GPIO 2 Config/ Status (1Ex0104) *(continued)***

Bit	Name	Description	Access	Default
4:3	GPIO2 Link Activity Selection	Determines which channel's link activity is transmitted from the pin when gpio2_pinfunc_sel=001 00: Tx link activity from channel 0 01: Tx link activity from channel 1 10: Tx link activity from channel 2 11: Tx link activity from channel 3	RW	00
2:0	GPIO2 Pin Function Selection	Selects the GPIO pin's functionality. 000: Traditional GPIO behavior 001: PCS activity LED output 010: WIS interrupt output 011: Transmit internal signals 100: SDA for STW (slave) 101-111: Reserved	RW	100

Table 78 • **GPIO 2 Config2 (1Ex0105)**

Bit	Name	Description	Access	Default
15:7	Reserved		RW	0

Table 78 • **GPIO 2 Config2 (1Ex0105)** ***(continued)***

Bit	Name	Description	Access	Default
6:0	GPIO2 Internal Node Selection	Determines which channel's link activity is transmitted from the pin when gpio2_pinfunc_sel=011 0x7F to 0x6C: Reserved 0x6B: ch3_sw_los 0x6A: ch3_sw_losn 0x69: ch3_hw_los 0x68: ch3_hw_losn 0x67: ch2_sw_los 0x66: ch2_sw_losn 0x65: ch2_hw_los 0x64: ch2_hw_losn 0x63: ch1_sw_los 0x62: ch1_sw_losn 0x61: ch1_hw_los 0x60: ch1_hw_losn 0x5F to 0x58: Reserved 0x57: ch0_sw_los 0x56: ch0_sw_losn 0x55: ch0_hw_los 0x54: ch0_hw_losn 0x53: ref_cmu_loln 0x52: Reserved 0x51: Reserved 0x50: ch0_rosi_sclk 0x4F to 0x4C: Reserved 0x4B: ch1_txen_inverted 0x4A: ch1_txen 0x49: ch0_txen_inverted 0x48: ch0_txen 0x47: Reserved 0x46: Reserved 0x45: ch1_rxalarm 0x44: ch0_rxalarm 0x43: Reserved 0x42: Reserved 0x41: ch1_txalarm 0x40: ch0_txalarm 0x3F: Reserved 0x3E: Reserved 0x3D: ch1_lopc 0x3C: ch0_lopc 0x3B to 0x08: Reserved 0x07: ch1_pma_rxlol 0x06: ch1_pma_rxloln 0x05: ch0_pma_rxlol 0x04: ch0_pma_rxloln 0x03 to 0x00: Reserved	RW	0

Table 79 • **GPIO 3 Config/ Status (1Ex0106)**

Bit	Name	Description	Access	Default
15	Traditional GPIO 3 Output Tri-state Control	Controls whether the pin is in input or output mode. Applies only when bit 2:0. gpio3_pinfunc_sel=000 0: Output mode 1: Input mode	RW	1
14:13	Traditional GP0IO 3 Pin Function Selection	Applies only when bit 2:0, gpio3_pinfunc_sel=000 When bit 15, gpio3_trad_tri=0 (output mode): 00: bit12, gpio3_trad_datareg is driven out the pin. 01: drive repeating LOW/Hi-Z pattern at 1Hz. 01: drive repeating LOW/Hi-Z pattern at 2Hz. 01: drive repeating LOW/Hi-Z pattern at 5Hz. When gpio3_trad_tri=1 (input mode): 00: no interrupt is generated. 01: interrupt generated on the rising edge of pin. 10: interrupt generated on the falling edge of pin. 11: interrupt generated on the both rising and falling edge of pin.	RW	00
12	Traditional GPIO 3 Output data	Logic value transmitted from pin when pin is configured as a traditional general purpose output (gpio3_pinfunc_sel=000 and gpio3_trad_tri=0) 0: Output data = 0 1: Output data = 1	RW	0
11	General Purpose Input Interrupt Pending	GPIO3 must be configured as a general purpose input and have interrupt generation enabled. 0: no interrupt event since the last time the register was read 1: an interrupt event has occurred clear on read	RO	0
10	General Purpose Input Status	Indicates the present value of the GPIO3 pin 0: Present value of GPIO3 pin is 0 1: Present value of GPIO3 pin is 1	RO	
9:8	Reserved		RW	0
7:5	GPIO3 WIS Interrupt Selection	Determines the WIS interrupt status transmitted from the pin when gpio3_pinfunc_sel=010 000: WIS interrupt B from channel 0 001: WIS interrupt B from channel 1 010: WIS interrupt B from channel 2 011: WIS interrupt B from channel 3 100: Logical AND of WIS interrupt B from all channels 101: Logical OR of WIS interrupt B from all channels 110-111: Reserved	RW	000

Table 79 • **GPIO 3 Config/ Status (1Ex0106) *(continued)***

Bit	Name	Description	Access	Default
4:3	GPIO3 Link Activity Selection	Determines which channel's link activity is transmitted from the pin when gpio3_pinfunc_sel=001 00: Rx link activity from channel 0 01: Rx link activity from channel 1 10: Rx link activity from channel 2 11: Rx link activity from channel 3	RW	00
2:0	GPIO3 Pin Function Selection	Selects the GPIO pin's functionality. 000: Traditional GPIO behavior 001: PCS activity LED output 010: WIS interrupt output 011: Transmit internal signals 100: SCL for STW (slave) 101-111: Reserved	RW	100

Table 80 • **GPIO 3 Config2 (1Ex0107)**

Bit	Name	Description	Access	Default
15:7	Reserved		RW	0

Table 80 • **GPIO 3 Config2 (1Ex0107) *(continued)***

Bit	Name	Description	Access	Default
6:0	GPIO3 Internal Node Selection	Determines which channel's link activity is transmitted from the pin when gpio3_pinfunc_sel=011 0x7F to 0x6C: Reserved 0x6B: ch3_sw_los 0x6A: ch3_sw_losn 0x69: ch3_hw_los 0x68: ch3_hw_losn 0x67: ch2_sw_los 0x66: ch2_sw_losn 0x65: ch2_hw_los 0x64: ch2_hw_losn 0x63: ch1_sw_los 0x62: ch1_sw_losn 0x61: ch1_hw_los 0x60: ch1_hw_losn 0x5F to 0x58: Reserved 0x57: ch0_sw_los 0x56: ch0_sw_losn 0x55: ch0_hw_los 0x54: ch0_hw_losn 0x53: ref_cmu_loln 0x52: Reserved 0x51: Reserved 0x50: ch0_tosi_frame_pulse_output 0x4F to 0x4C: Reserved 0x4B: ch1_txen_inverted 0x4A: ch1_txen 0x49: ch0_txen_inverted 0x48: ch0_txen 0x47: Reserved 0x46: Reserved 0x45: ch1_rxalarm 0x44: ch0_rxalarm 0x43: Reserved 0x42: Reserved 0x41: ch1_txalarm 0x40: ch0_txalarm 0x3F: Reserved 0x3E: Reserved 0x3D: ch1_lopc 0x3C: ch0_lopc 0x3B to 0x08: Reserved 0x07: ch1_pma_rxlol 0x06: ch1_pma_rxloln 0x05: ch0_pma_rxlol 0x04: ch0_pma_rxloln 0x03 to 0x00: Reserved	RW	0

Table 81 • **GPIO 4 Config/ Status (1Ex0108)**

Bit	Name	Description	Access	Default
15	Traditional GPIO 4 Output Tri-state Control	Controls whether the pin is in input or output mode. Applies only when bit 2:0, gpio4_pinfunc_sel=000 0: Output mode 1: Input mode	RW	1
14:13	Traditional GP0IO 4 Pin Function Selection	Applies only when bit 2:0, gpio4_pinfunc_sel=000 When bit 15, gpio4_trad_tri=0 (output mode): 00: bit 12, gpio4_trad_datareg is driven out the pin. 01: drive repeating LOW/Hi-Z pattern at 1Hz. 01: drive repeating LOW/Hi-Z pattern at 2Hz. 01: drive repeating LOW/Hi-Z pattern at 5Hz. When gpio4_trad_tri=1 (input mode): 00: no interrupt is generated. 01: interrupt generated on the rising edge of pin. 10: interrupt generated on the falling edge of pin. 11: interrupt generated on the both rising and falling edge of pin.	RW	00
12	Traditional GPIO 4 Output data	Logic value transmitted from pin when pin is configured as a traditional general purpose output (gpio4_pinfunc_sel=000 and gpio4_trad_tri=0) 0: Output data = 0 1: Output data = 1	RW	0
11	General Purpose Input Interrupt Pending	GPIO4 must be configured as a general purpose input and have interrupt generation enabled. 0: no interrupt event since the last time the register was read 1: an interrupt event has occurred clear on read	RO	0
10	General Purpose Input Status	Indicates the present value of the GPIO4 pin 0: Present value of GPIO4 pin is 0 1: Present value of GPIO4 pin is 1	RO	
9:8	Reserved		RW	0
7:5	GPIO4 WIS Interrupt Selection	Determines the WIS interrupt status transmitted from the pin when gpio4_pinfunc_sel=010 000: WIS interrupt B from channel 0 001: WIS interrupt B from channel 1 010: WIS interrupt B from channel 2 011: WIS interrupt B from channel 3 100: Logical AND of WIS interrupt B from all channels 101: Logical OR of WIS interrupt B from all channels 110-111: Reserved	RW	000

Table 81 • **GPIO 4 Config/ Status (1Ex0108) *(continued)***

Bit	Name	Description	Access	Default
4:3	GPIO4 Link Activity Selection	Determines which channel's link activity is transmitted from the pin when gpio4_pinfunc_sel=001 00: Tx link activity from channel 0 01: Tx link activity from channel 1 10: Tx link activity from channel 2 11: Tx link activity from channel 3	RW	00
2:0	GPIO4 Pin Function Selection	Selects the GPIO pin's functionality. 000: Traditional GPIO behavior 001: PCS activity LED output 010: WIS interrupt output 011: Transmit internal signals 100-111: Reserved	RW	000

Table 82 • **GPIO 4 Config2 (1Ex0109)**

Bit	Name	Description	Access	Default
15:7	Reserved		RW	0

Table 82 • **GPIO 4 Config2 (1Ex0109)** ***(continued)***

Bit	Name	Description	Access	Default
6:0	GPIO4 Internal Node Selection	Determines which channel's link activity is transmitted from the pin when gpio4_pinfunc_sel=011 0x7F to 0x6C: Reserved 0x6B: ch3_sw_los 0x6A: ch3_sw_losn 0x69: ch3_hw_los 0x68: ch3_hw_losn 0x67: ch2_sw_los 0x66: ch2_sw_losn 0x65: ch2_hw_los 0x64: ch2_hw_losn 0x63: ch1_sw_los 0x62: ch1_sw_losn 0x61: ch1_hw_los 0x60: ch1_hw_losn 0x5F to 0x58: Reserved 0x57: ch0_sw_los 0x56: ch0_sw_losn 0x55: ch0_hw_los 0x54: ch0_hw_losn 0x53: ref_cmu_loln 0x52: Reserved 0x51: Reserved 0x50: ch0_tosi_sclk 0x4F to 0x4C: Reserved 0x4B: ch1_txen_inverted 0x4A: ch1_txen 0x49: ch0_txen_inverted 0x48: ch0_txen 0x47: Reserved 0x46: Reserved 0x45: ch1_rxalarm 0x44: ch0_rxalarm 0x43: Reserved 0x42: Reserved 0x41: ch1_txalarm 0x40: ch0_txalarm 0x3F: Reserved 0x3E: Reserved 0x3D: ch1_lopc 0x3C: ch0_lopc 0x3B to 0x08: Reserved 0x07: ch1_pma_rxlol 0x06: ch1_pma_rxloln 0x05: ch0_pma_rxlol 0x04: ch0_pma_rxloln 0x03 to 0x00: Reserved	RW	0

Table 83 • **GPIO 5 Config/ Status (1Ex010A)**

Bit	Name	Description	Access	Default
15	Traditional GPIO 5 Output Tri-state Control	Controls whether the pin is in input or output mode. Applies only when bit 2:0, gpio5_pinfunc_sel=000 0: Output mode 1: Input mode	RW	1
14:13	Traditional GP0IO 5 Pin Function Selection	Applies only when bit 2:0, gpio5_pinfunc_sel=000 When bit 15, gpio5_trad_tri=0 (output mode): 00: bit 12, gpio5_trad_datareg is driven out the pin. 01: drive repeating LOW/Hi-Z pattern at 1Hz. 01: drive repeating LOW/Hi-Z pattern at 2Hz. 01: drive repeating LOW/Hi-Z pattern at 5Hz. When gpio5_trad_tri=1 (input mode): 00: no interrupt is generated. 01: interrupt generated on the rising edge of pin. 10: interrupt generated on the falling edge of pin. 11: interrupt generated on the both rising and falling edge of pin.	RW	00
12	Traditional GPIO 5 Output data	Logic value transmitted from pin when pin is configured as a traditional general purpose output (gpio5_pinfunc_sel=000 and gpio5_trad_tri=0) 0: Output data = 0 1: Output data = 1	RW	0
11	General Purpose Input Interrupt Pending	GPIO5 must be configured as a general purpose input and have interrupt generation enabled. 0: no interrupt event since the last time the register was read 1: an interrupt event has occurred clear on read	RO	0
10	General Purpose Input Status	Indicates the present value of the GPIO5 pin 0: Present value of GPIO5 pin is 0 1: Present value of GPIO5 pin is 1	RO	
9	Reserved		RW	0
8	Channel 0 TOSI Data Input Enable	0: Channel 0's TOSI is disabled. 1: Enable use of this pin as channel 0's TOSI Data Input. Pin must be configured as a general purpose input for these bit to serve a purpose.	RW	0

Table 83 • **GPIO 5 Config/ Status (1Ex010A)** ***(continued)***

Bit	Name	Description	Access	Default
7:5	GPIO5 WIS Interrupt Selection	Determines the WIS interrupt status transmitted from the pin when gpio5_pinfunc_sel=010 000: WIS interrupt A from channel 0 001: WIS interrupt A from channel 1 010: WIS interrupt A from channel 2 011: WIS interrupt A from channel 3 100: Logical AND of WIS interrupt A from all channels 101: Logical OR of WIS interrupt A from all channels 110-111: Reserved	RW	000
4:3	GPIO5 Link Activity Selection	Determines which channel's link activity is transmitted from the pin when gpio5_pinfunc_sel=001 00: Rx link activity from channel 0 01: Rx link activity from channel 1 10: Rx link activity from channel 2 11: Rx link activity from channel 3	RW	00
2:0	GPIO5 Pin Function Selection	Selects the GPIO pin's functionality. 000: Traditional GPIO behavior 001: PCS activity LED output 010: WIS interrupt output 011: Transmit internal signals 100-111: Reserved	RW	101

Table 84 • **GPIO 5 Config2 (1Ex010B)**

Bit	Name	Description	Access	Default
15:7	Reserved		RW	0

Table 84 • **GPIO 5 Config2 (1Ex010B)** ***(continued)***

Bit	Name	Description	Access	Default
6:0	GPIO5 Internal Node Selection	Determines which channel's link activity is transmitted from the pin when gpio5_pinfunc_sel=011 0x7F to 0x6C: Reserved 0x6B: ch3_sw_los 0x6A: ch3_sw_losn 0x69: ch3_hw_los 0x68: ch3_hw_losn 0x67: ch2_sw_los 0x66: ch2_sw_losn 0x65: ch2_hw_los 0x64: ch2_hw_losn 0x63: ch1_sw_los 0x62: ch1_sw_losn 0x61: ch1_hw_los 0x60: ch1_hw_losn 0x5F to 0x58: Reserved 0x57: ch0_sw_los 0x56: ch0_sw_losn 0x55: ch0_hw_los 0x54: ch0_hw_losn 0x53: ref_cmu_loln 0x52: Reserved 0x51: Reserved 0x50: Reserved 0x4F to 0x4C: Reserved 0x4B: ch1_txen_inverted 0x4A: ch1_txen 0x49: ch0_txen_inverted 0x48: ch0_txen 0x47: Reserved 0x46: Reserved 0x45: ch1_rxalarm 0x44: ch0_rxalarm 0x43: Reserved 0x42: Reserved 0x41: ch1_txalarm 0x40: ch0_txalarm 0x3F: Reserved 0x3E: Reserved 0x3D: ch1_lopc 0x3C: ch0_lopc 0x3B to 0x08: Reserved 0x07: ch1_pma_rxlol 0x06: ch1_pma_rxloln 0x05: ch0_pma_rxlol 0x04: ch0_pma_rxloln 0x03 to 0x00: Reserved	RW	0

Table 85 • **GPIO 6 Config/ Status (1Ex010C)**

Bit	Name	Description	Access	Default
15	Traditional GPIO 6 Output Tri-state Control	Controls whether the pin is in input or output mode. Applies only when gpio6_pinfunc_sel=000 0: Output mode 1: Input mode	RW	1
14:13	Traditional GP0IO 6 Pin Function Selection	Applies only when gpio6_pinfunc_sel=000 When gpio6_trad_tri=0 (output mode): 00: gpio6_trad_datareg is driven out the pin. 01: drive repeating LOW/Hi-Z pattern at 1Hz. 01: drive repeating LOW/Hi-Z pattern at 2Hz. 01: drive repeating LOW/Hi-Z pattern at 5Hz. When gpio6_trad_tri=1 (input mode): 00: no interrupt is generated. 01: interrupt generated on the rising edge of pin. 10: interrupt generated on the falling edge of pin.,11: interrupt generated on the both rising and falling edge of pin.	RW	00
12	Traditional GPIO 6 Output data	Logic value transmitted from pin when pin is configured as a traditional general purpose output (gpio6_pinfunc_sel=000 and gpio6_trad_tri=0) 0: Output data = 0 1: Output data = 1	RW	0
11	General Purpose Input Interrupt Pending	GPIO6 must be configured as a general purpose input and have interrupt generation enabled. 0: no interrupt event since the last time the register was read 1: an interrupt event has occurred clear on read	RO	0
10	General Purpose Input Status	Indicates the present value of the GPIO6 pin 0: Present value of GPIO6 pin is 0 1: Present value of GPIO6 pin is 1	RO	
9:8	Reserved		RW	0
7:5	GPIO6 WIS Interrupt Selection	Determines the WIS interrupt status transmitted from the pin when gpio6_pinfunc_sel=010 000: WIS interrupt B from channel 0 001: WIS interrupt B from channel 1 010: WIS interrupt B from channel 2 011: WIS interrupt B from channel 3 100: Logical AND of WIS interrupt B from all/both channels 101: Logical OR of WIS interrupt B from all/both channels 110-111: Reserved	RW	000
4:3	GPIO6 Link Activity Selection	Determines which channel's link activity is transmitted from the pin when gpio6_pinfunc_sel=001 00: Tx link activity from channel 0 01: Tx link activity from channel 1 10: Tx link activity from channel 2 11: Tx link activity from channel 3	RW	00

Table 85 • **GPIO 6 Config/ Status (1Ex010C)** ***(continued)***

Bit	Name	Description	Access	Default
2:0	GPIO6 Pin Function Selection	Selects the GPIO pin's functionality. 000: Traditional GPIO behavior 001: PCS activity LED output 010: WIS interrupt output 011: Transmit internal signals 100-111: Reserved	RW	000

Table 86 • **GPIO 6 Config2 (1Ex010D)**

Bit	Name	Description	Access	Default
15:7	Reserved		RW	0

Table 86 • **GPIO 6 Config2 (1Ex010D)** ***(continued)***

Bit	Name	Description	Access	Default
6:0	GPIO6 Internal Node Selection	Determines which channel's link activity is transmitted from the pin when gpio6_pinfunc_sel=011 0x7F to 0x6C: Reserved 0x6B: ch3_sw_los 0x6A: ch3_sw_losn 0x69: ch3_hw_los 0x68: ch3_hw_losn 0x67: ch2_sw_los 0x66: ch2_sw_losn 0x65: ch2_hw_los 0x64: ch2_hw_losn 0x63: ch1_sw_los 0x62: ch1_sw_losn 0x61: ch1_hw_los 0x60: ch1_hw_losn 0x5F to 0x58: Reserved 0x57: ch0_sw_los 0x56: ch0_sw_losn 0x55: ch0_hw_los 0x54: ch0_hw_losn 0x53: ref_cmu_loln 0x52: Reserved 0x51: Reserved 0x50: ch1_rosi_frm_pulse 0x4F: ch3_txen_inverted 0x4E: ch3_txen 0x4D: ch2_txen_inverted 0x4C: ch2_txen 0x4B: ch1_txen_inverted 0x4A: ch1_txen 0x49: ch0_txen_inverted 0x48: ch0_txen 0x47: ch3_rxalarm 0x46: ch2_rxalarm 0x45: ch1_rxalarm 0x44: ch0_rxalarm 0x43: ch3_txalarm 0x42: ch2_txalarm 0x41: ch1_txalarm 0x40: ch0_txalarm 0x3F: ch3_lopc; 0x3E: ch2_lopc 0x3D: ch1_lopc 0x3C: ch0_lopc 0x0B: ch3_pma_rxlol 0x0A: ch3_pma_rxloln 0x09: ch2_pma_rxlol 0x08: ch2_pma_rxloln 0x07: ch1_pma_rxlol 0x06: ch1_pma_rxloln 0x05: ch0_pma_rxlol 0x04: ch0_pma_rxloln * All other register bits: Reserved	RW	0

Table 87 • **GPIO 7 Config/ Status (1Ex010E)**

Bit	Name	Description	Access	Default
15	Traditional GPIO 7 Output Tri-state Control	Controls whether the pin is in input or output mode. Applies only when gpio7_pinfunc_sel=000 0: Output mode 1: Input mode	RW	1
14:13	Traditional GP0IO 7 Pin Function Selection	Applies only when gpio7_pinfunc_sel=000 When gpio7_trad_tri=0 (output mode): 00: gpio7_trad_datareg is driven out the pin. 01: drive repeating LOW/Hi-Z pattern at 1Hz. 01: drive repeating LOW/Hi-Z pattern at 2Hz. 01: drive repeating LOW/Hi-Z pattern at 5Hz. When gpio7_trad_tri=1 (input mode): 00: no interrupt is generated. 01: interrupt generated on the rising edge of pin. 10: interrupt generated on the falling edge of pin. 11: interrupt generated on the both rising and falling edge of pin.	RW	00
12	Traditional GPIO 7 Output data	Logic value transmitted from pin when pin is configured as a traditional general purpose output (gpio7_pinfunc_sel=000 and gpio7_trad_tri=0) 0: Output data = 0 1: Output data = 1	RW	0
11	General Purpose Input Interrupt Pending	GPIO7 must be configured as a general purpose input and have interrupt generation enabled. 0: no interrupt event since the last time the register was read 1: an interrupt event has occurred clear on read	RO	0
10	General Purpose Input Status	Indicates the present value of the GPIO7 pin 0: Present value of GPIO7 pin is 0 1: Present value of GPIO7 pin is 1	RO	
9:8	Reserved		RW	0
7:5	GPIO7 WIS Interrupt Selection	Determines the WIS interrupt status transmitted from the pin when gpio7_pinfunc_sel=010 000: WIS interrupt A from channel 0 001: WIS interrupt A from channel 1 010: WIS interrupt A from channel 2 011: WIS interrupt A from channel 3 100: Logical AND of WIS interrupt A from all/both channels 101: Logical OR of WIS interrupt A from all/both channels 110-111: Reserved	RW	000
4:3	GPIO7 Link Activity Selection	Determines which channel's link activity is transmitted from the pin when gpio7_pinfunc_sel=001 00: Rx link activity from channel 0 01: Rx link activity from channel 1 10: Rx link activity from channel 2 11: Rx link activity from channel 3	RW	00

Table 87 • **GPIO 7 Config/ Status (1Ex010E) *(continued)***

Bit	Name	Description	Access	Default
2:0	GPIO7 Pin Function Selection	Selects the GPIO pin's functionality. 000: Traditional GPIO behavior 001: PCS activity LED output 010: WIS interrupt output 011: Transmit internal signals 100-111: Reserved	RW	000

Table 88 • **GPIO 7 Config2 (1Ex010F)**

Bit	Name	Description	Access	Default
15:7	Reserved		RW	0

Table 88 • **GPIO 7 Config2 (1Ex010F)** ***(continued)***

Bit	Name	Description	Access	Default
6:0	GPIO7 Internal Node Selection	Determines which channel's link activity is transmitted from the pin when gpio7_pinfunc_sel=011 0x7F to 0x6C: Reserved 0x6B: ch3_sw_los 0x6A: ch3_sw_losn 0x69: ch3_hw_los 0x68: ch3_hw_losn 0x67: ch2_sw_los 0x66: ch2_sw_losn 0x65: ch2_hw_los 0x64: ch2_hw_losn 0x63: ch1_sw_los 0x62: ch1_sw_losn 0x61: ch1_hw_los 0x60: ch1_hw_losn 0x5F to 0x58: Reserved 0x57: ch0_sw_los 0x56: ch0_sw_losn 0x55: ch0_hw_los 0x54: ch0_hw_losn 0x53: ref_cmu_loln 0x52: Reserved 0x51: Reserved 0x50: ch1_rosi_sclk 0x4F: ch3_txen_inverted 0x4E: ch3_txen 0x4D: ch2_txen_inverted 0x4C: ch2_txen 0x4B: ch1_txen_inverted 0x4A: ch1_txen 0x49: ch0_txen_inverted 0x48: ch0_txen 0x47: ch3_rxalarm 0x46: ch2_rxalarm 0x45: ch1_rxalarm 0x44: ch0_rxalarm 0x43: ch3_txalarm 0x42: ch2_txalarm 0x41: ch1_txalarm 0x40: ch0_txalarm 0x3F: ch3_lopc; 0x3E: ch2_lopc 0x3D: ch1_lopc 0x3C: ch0_lopc 0x0B: ch3_pma_rxlol 0x0A: ch3_pma_rxloln 0x09: ch2_pma_rxlol 0x08: ch2_pma_rxloln 0x07: ch1_pma_rxlol 0x06: ch1_pma_rxloln 0x05: ch0_pma_rxlol 0x04: ch0_pma_rxloln * All other register bits: Reserved	RW	0

Table 89 • **GPIO 8 Config/ Status (1Ex0110)**

Bit	Name	Description	Access	Default
15	Traditional GPIO 8 Output Tri-state Control	Controls whether the pin is in input or output mode. Applies only when gpio8_pinfunc_sel=000 0: Output mode 1: Input mode	RW	1
14:13	Traditional GP0IO 8 Pin Function Selection	Applies only when gpio8_pinfunc_sel=000 When gpio8_trad_tri=0 (output mode): 00: gpio8_trad_datareg is driven out the pin. 01: drive repeating LOW/Hi-Z pattern at 1Hz. 01: drive repeating LOW/Hi-Z pattern at 2Hz. 01: drive repeating LOW/Hi-Z pattern at 5Hz. When gpio8_trad_tri=1 (input mode): 00: no interrupt is generated. 01: interrupt generated on the rising edge of pin. 10: interrupt generated on the falling edge of pin. 11: interrupt generated on the both rising and falling edge of pin.	RW	00
12	Traditional GPIO 8 Output data	Logic value transmitted from pin when pin is configured as a traditional general purpose output (gpio8_pinfunc_sel=000 and gpio8_trad_tri=0) 0: Output data = 0 1: Output data = 1	RW	0
11	General Purpose Input Interrupt Pending	GPIO8 must be configured as a general purpose input and have interrupt generation enabled. 0: no interrupt event since the last time the register was read 1: an interrupt event has occurred clear on read	RO	0
10	General Purpose Input Status	Indicates the present value of the GPIO8 pin 0: Present value of GPIO8 pin is 0 1: Present value of GPIO8 pin is 1	RO	
9	Reserved		RW	0
8	Module Status Input Enable - channel 1	0: interrupt generation logic for channel 1's module status is disabled. 1: Enable use of this pin to drive interrupt generation logic for channel 1's module status. Pin must be configured as a general purpose input for these bit to serve a purpose.	RW	0
7:5	GPIO8 WIS Interrupt Selection	Determines the WIS interrupt status transmitted from the pin when gpio8_pinfunc_sel=010 000: WIS interrupt B from channel 0 001: WIS interrupt B from channel 1 010: WIS interrupt B from channel 2 011: WIS interrupt B from channel 3 100: Logical AND of WIS interrupt B from all/both channels 101: Logical OR of WIS interrupt B from all/both channels 110-111: Reserved	RW	000

Table 89 • **GPIO 8 Config/ Status (1Ex0110) *(continued)***

Bit	Name	Description	Access	Default
4:3	GPIO8 Link Activity Selection	Determines which channel's link activity is transmitted from the pin when gpio8_pinfunc_sel=001 00: Tx link activity from channel 0 01: Tx link activity from channel 1 10: Tx link activity from channel 2 11: Tx link activity from channel 3	RW	00
2:0	GPIO8 Pin Function Selection	Selects the GPIO pin's functionality. 000: Traditional GPIO behavior 001: PCS activity LED output 010: WIS interrupt output 011: Transmit internal signals 100-111: Reserved	RW	000

Table 90 • **GPIO 8 Config2 (1Ex0111)**

Bit	Name	Description	Access	Default
15:7	Reserved		RW	0

Table 90 • **GPIO 8 Config2 (1Ex0111)** ***(continued)***

Bit	Name	Description	Access	Default
6:0	GPIO8 Internal Node Selection	Determines which channel's link activity is transmitted from the pin when gpio8_pinfunc_sel=011 0x7F to 0x6C: Reserved 0x6B: ch3_sw_los 0x6A: ch3_sw_losn 0x69: ch3_hw_los 0x68: ch3_hw_losn 0x67: ch2_sw_los 0x66: ch2_sw_losn 0x65: ch2_hw_los 0x64: ch2_hw_losn 0x63: ch1_sw_los 0x62: ch1_sw_losn 0x61: ch1_hw_los 0x60: ch1_hw_losn 0x5F to 0x58: Reserved 0x57: ch0_sw_los 0x56: ch0_sw_losn 0x55: ch0_hw_los 0x54: ch0_hw_losn 0x53: ref_cmu_loln 0x52: Reserved 0x51: Reserved 0x50: ch1_rosi_sdat 0x4F: ch3_txen_inverted 0x4E: ch3_txen 0x4D: ch2_txen_inverted 0x4C: ch2_txen 0x4B: ch1_txen_inverted 0x4A: ch1_txen 0x49: ch0_txen_inverted 0x48: ch0_txen 0x47: ch3_rxalarm 0x46: ch2_rxalarm 0x45: ch1_rxalarm 0x44: ch0_rxalarm 0x43: ch3_txalarm 0x42: ch2_txalarm 0x41: ch1_txalarm 0x40: ch0_txalarm 0x3F: ch3_lopc; 0x3E: ch2_lopc 0x3D: ch1_lopc 0x3C: ch0_lopc 0x0B: ch3_pma_rxlol 0x0A: ch3_pma_rxloln 0x09: ch2_pma_rxlol 0x08: ch2_pma_rxloln 0x07: ch1_pma_rxlol 0x06: ch1_pma_rxloln 0x05: ch0_pma_rxlol 0x04: ch0_pma_rxloln * All other register bits: Reserved	RW	0

Table 91 • **GPIO 9 Config/ Status (1Ex0112)**

Bit	Name	Description	Access	Default
15	Traditional GPIO 9 Output Tri-state Control	Controls whether the pin is in input or output mode. Applies only when gpio9_pinfunc_sel=000 0: Output mode 1: Input mode	RW	1
14:13	Traditional GP0IO 9 Pin Function Selection	Applies only when gpio9_pinfunc_sel=000 When gpio9_trad_tri=0 (output mode): 00: gpio9_trad_datareg is driven out the pin. 01: drive repeating LOW/Hi-Z pattern at 1Hz. 01: drive repeating LOW/Hi-Z pattern at 2Hz. 01: drive repeating LOW/Hi-Z pattern at 5Hz. When gpio9_trad_tri=1 (input mode): 00: no interrupt is generated. 01: interrupt generated on the rising edge of pin. 10: interrupt generated on the falling edge of pin. 11: interrupt generated on the both rising and falling edge of pin.	RW	00
12	Traditional GPIO 9 Output data	Logic value transmitted from pin when pin is configured as a traditional general purpose output (gpio9_pinfunc_sel=000 and gpio9_trad_tri=0) 0: Output data = 0 1: Output data = 1	RW	0
11	General Purpose Input Interrupt Pending	GPIO9 must be configured as a general purpose input and have interrupt generation enabled. 0: no interrupt event since the last time the register was read 1: an interrupt event has occurred clear on read	RO	0
10	General Purpose Input Status	Indicates the present value of the GPIO9 pin 0: Present value of GPIO9 pin is 0 1: Present value of GPIO9 pin is 1	RO	
9:8	Reserved		RW	0
7:5	GPIO9 WIS Interrupt Selection	Determines the WIS interrupt status transmitted from the pin when gpio9_pinfunc_sel=010 000: WIS interrupt A from channel 0 001: WIS interrupt A from channel 1 010: WIS interrupt A from channel 2 011: WIS interrupt A from channel 3 100: Logical AND of WIS interrupt A from all/both channels 101: Logical OR of WIS interrupt A from all/both channels 110-111: Reserved	RW	000
4:3	GPIO9 Link Activity Selection	Determines which channel's link activity is transmitted from the pin when gpio9_pinfunc_sel=001 00: Rx link activity from channel 0 01: Rx link activity from channel 1 10: Rx link activity from channel 2 11: Rx link activity from channel 3	RW	00

Table 91 • **GPIO 9 Config/ Status (1Ex0112) *(continued)***

Bit	Name	Description	Access	Default
2:0	GPIO9 Pin Function Selection	Selects the GPIO pin's functionality. 000: Traditional GPIO behavior 001: PCS activity LED output 010: WIS interrupt output 011: Transmit internal signals 100-111: Reserved	RW	000

Table 92 • **GPIO 9 Config2 (1Ex0113)**

Bit	Name	Description	Access	Default
15:7	Reserved		RW	0

Table 92 • **GPIO 9 Config2 (1Ex0113) *(continued)***

Bit	Name	Description	Access	Default
6:0	GPIO9 Internal Node Selection	Determines which channel's link activity is transmitted from the pin when gpio9_pinfunc_sel=011 0x7F to 0x6C: Reserved 0x6B: ch3_sw_los 0x6A: ch3_sw_losn 0x69: ch3_hw_los 0x68: ch3_hw_losn 0x67: ch2_sw_los 0x66: ch2_sw_losn 0x65: ch2_hw_los 0x64: ch2_hw_losn 0x63: ch1_sw_los 0x62: ch1_sw_losn 0x61: ch1_hw_los 0x60: ch1_hw_losn 0x5F to 0x58: Reserved 0x57: ch0_sw_los 0x56: ch0_sw_losn 0x55: ch0_hw_los 0x54: ch0_hw_losn 0x53: ref_cmu_loln 0x52: Reserved 0x51: Reserved 0x50: ch1_tosi_frm_pulse 0x4F: ch3_txen_inverted 0x4E: ch3_txen 0x4D: ch2_txen_inverted 0x4C: ch2_txen 0x4B: ch1_txen_inverted 0x4A: ch1_txen 0x49: ch0_txen_inverted 0x48: ch0_txen 0x47: ch3_rxalarm 0x46: ch2_rxalarm 0x45: ch1_rxalarm 0x44: ch0_rxalarm 0x43: ch3_txalarm 0x42: ch2_txalarm 0x41: ch1_txalarm 0x40: ch0_txalarm 0x3F: ch3_lopc; 0x3E: ch2_lopc 0x3D: ch1_lopc 0x3C: ch0_lopc 0x0B: ch3_pma_rxlol 0x0A: ch3_pma_rxloln 0x09: ch2_pma_rxlol 0x08: ch2_pma_rxloln 0x07: ch1_pma_rxlol 0x06: ch1_pma_rxloln 0x05: ch0_pma_rxlol 0x04: ch0_pma_rxloln * All other register bits: Reserved	RW	0

Table 93 • **GPIO 10 Config/ Status (1Ex0114)**

Bit	Name	Description	Access	Default
15	Traditional GPIO 10 Output Tri-state Control	Controls whether the pin is in input or output mode. Applies only when gpio10_pinfunc_sel=000 0: Output mode 1: Input mode	RW	1
14:13	Traditional GP0IO 10 Pin Function Selection	Applies only when gpio10_pinfunc_sel=000 When gpio10_trad_tri=0 (output mode): 00: gpio10_trad_datareg is driven out the pin. 01: drive repeating LOW/Hi-Z pattern at 1Hz. 01: drive repeating LOW/Hi-Z pattern at 2Hz. 01: drive repeating LOW/Hi-Z pattern at 5Hz. When gpio10_trad_tri=1 (input mode): 00: no interrupt is generated. 01: interrupt generated on the rising edge of pin. 10: interrupt generated on the falling edge of pin. 11: interrupt generated on the both rising and falling edge of pin.	RW	00
12	Traditional GPIO 10 Output data	Logic value transmitted from pin when pin is configured as a traditional general purpose output (gpio10_pinfunc_sel=000 and gpio10_trad_tri=0) 0: Output data = 0 1: Output data = 1	RW	0
11	General Purpose Input Interrupt Pending	GPIO10 must be configured as a general purpose input and have interrupt generation enabled. 0: no interrupt event since the last time the register was read 1: an interrupt event has occurred clear on read	RO	0
10	General Purpose Input Status	Indicates the present value of the GPIO10 pin 0: Present value of GPIO10 pin is 0 1: Present value of GPIO10 pin is 1	RO	
9:8	Reserved		RW	0
7:5	GPIO10 WIS Interrupt Selection	Determines the WIS interrupt status transmitted from the pin when gpio10_pinfunc_sel=010 000: WIS interrupt B from channel 0 001: WIS interrupt B from channel 1 010: WIS interrupt B from channel 2 011: WIS interrupt B from channel 3 100: Logical AND of WIS interrupt B from all/both channels 101: Logical OR of WIS interrupt B from all/both channels 110-111: Reserved	RW	000

Table 93 • **GPIO 10 Config/ Status (1Ex0114) *(continued)***

Bit	Name	Description	Access	Default
4:3	GPIO10 Link Activity Selection	Determines which channel's link activity is transmitted from the pin when gpio10_pinfunc_sel=001 00: Tx link activity from channel 0 01: Tx link activity from channel 1 10: Tx link activity from channel 2 11: Tx link activity from channel 3	RW	00
2:0	GPIO10 Pin Function Selection	Selects the GPIO pin's functionality. 000: Traditional GPIO behavior 001: PCS activity LED output 010: WIS interrupt output 011: Transmit internal signals 100-111: Reserved	RW	000

Table 94 • **GPIO 10 Config2 (1Ex0115)**

Bit	Name	Description	Access	Default
15:7	Reserved		RW	0

Table 94 • **GPIO 10 Config2 (1Ex0115) *(continued)***

Bit	Name	Description	Access	Default
6:0	GPIO10 Internal Node Selection	Determines which channel's link activity is transmitted from the pin when gpio10_pinfunc_sel=011 0x7F to 0x6C: Reserved 0x6B: ch3_sw_los 0x6A: ch3_sw_losn 0x69: ch3_hw_los 0x68: ch3_hw_losn 0x67: ch2_sw_los 0x66: ch2_sw_losn 0x65: ch2_hw_los 0x64: ch2_hw_losn 0x63: ch1_sw_los 0x62: ch1_sw_losn 0x61: ch1_hw_los 0x60: ch1_hw_losn 0x5F to 0x58: Reserved 0x57: ch0_sw_los 0x56: ch0_sw_losn 0x55: ch0_hw_los 0x54: ch0_hw_losn 0x53: ref_cmu_loln 0x52: Reserved 0x51: Reserved 0x50: ch1_tosi_sclk 0x4F: ch3_txen_inverted 0x4E: ch3_txen 0x4D: ch2_txen_inverted 0x4C: ch2_txen 0x4B: ch1_txen_inverted 0x4A: ch1_txen 0x49: ch0_txen_inverted 0x48: ch0_txen 0x47: ch3_rxalarm 0x46: ch2_rxalarm 0x45: ch1_rxalarm 0x44: ch0_rxalarm 0x43: ch3_txalarm 0x42: ch2_txalarm 0x41: ch1_txalarm 0x40: ch0_txalarm 0x3F: ch3_lopc; 0x3E: ch2_lopc 0x3D: ch1_lopc 0x3C: ch0_lopc 0x0B: ch3_pma_rxlol 0x0A: ch3_pma_rxloln 0x09: ch2_pma_rxlol 0x08: ch2_pma_rxloln 0x07: ch1_pma_rxlol 0x06: ch1_pma_rxloln 0x05: ch0_pma_rxlol 0x04: ch0_pma_rxloln * All other register bits: Reserved	RW	0

Table 95 • **GPIO 11 Config/ Status (1Ex0116)**

Bit	Name	Description	Access	Default
15	Traditional GPIO 11 Output Tri-state Control	Controls whether the pin is in input or output mode. Applies only when gpio11_pinfunc_sel=000 0: Output mode 1: Input mode	RW	1
14:13	Traditional GP0IO 11 Pin Function Selection	Applies only when gpio11_pinfunc_sel=000 When gpio11_trad_tri=0 (output mode): 00: gpio11_trad_datareg is driven out the pin. 01: drive repeating LOW/Hi-Z pattern at 1Hz. 01: drive repeating LOW/Hi-Z pattern at 2Hz. 01: drive repeating LOW/Hi-Z pattern at 5Hz. When gpio11_trad_tri=1 (input mode): 00: no interrupt is generated. 01: interrupt generated on the rising edge of pin. 10: interrupt generated on the falling edge of pin. 11: interrupt generated on the both rising and falling edge of pin.	RW	00
12	Traditional GPIO 11 Output data	Logic value transmitted from pin when pin is configured as a traditional general purpose output (gpio11_pinfunc_sel=000 and gpio11_trad_tri=0) 0: Output data = 0 1: Output data = 1	RW	0
11	General Purpose Input Interrupt Pending	GPIO11 must be configured as a general purpose input and have interrupt generation enabled. 0: no interrupt event since the last time the register was read 1: an interrupt event has occurred clear on read	RO	0
10	General Purpose Input Status	Indicates the present value of the GPIO11 pin 0: Present value of GPIO11 pin is 0 1: Present value of GPIO11 pin is 1	RO	
9	Reserved		RW	0
8	Channel 1 TOSI Data Input Enable	0: Channel 1's TOSI is disabled. 1: Enable use of this pin as channel 1's TOSI Data Input. Pin must be configured as a general purpose input for these bit to serve a purpose.	RW	0
7:5	GPIO11 WIS Interrupt Selection	Determines the WIS interrupt status transmitted from the pin when gpio11_pinfunc_sel=010 000: WIS interrupt A from channel 0 001: WIS interrupt A from channel 1 010: WIS interrupt A from channel 2 011: WIS interrupt A from channel 3 100: Logical AND of WIS interrupt A from all/both channels 101: Logical OR of WIS interrupt A from all/both channels 110-111: Reserved	RW	000

Table 95 • **GPIO 11 Config/ Status (1Ex0116) *(continued)***

Bit	Name	Description	Access	Default
4:3	GPIO11 Link Activity Selection	Determines which channel's link activity is transmitted from the pin when gpio11_pinfunc_sel=001 00: Rx link activity from channel 0 01: Rx link activity from channel 1 10: Rx link activity from channel 2 11: Rx link activity from channel 3	RW	00
2:0	GPIO11 Pin Function Selection	Selects the GPIO pin's functionality. 000: Traditional GPIO behavior 001: PCS activity LED output 010: WIS interrupt output 011: Transmit internal signals 100-111: Reserved	RW	000

Table 96 • **GPIO 11 Config2 (1Ex0117)**

Bit	Name	Description	Access	Default
15:7	Reserved		RW	0

Table 96 • **GPIO 11 Config2 (1Ex0117) *(continued)***

Bit	Name	Description	Access	Default
6:0	GPIO11 Internal Node Selection	Determines which channel's link activity is transmitted from the pin when gpio11_pinfunc_sel=011 0x7F to 0x6C: Reserved 0x6B: ch3_sw_los 0x6A: ch3_sw_losn 0x69: ch3_hw_los 0x68: ch3_hw_losn 0x67: ch2_sw_los 0x66: ch2_sw_losn 0x65: ch2_hw_los 0x64: ch2_hw_losn 0x63: ch1_sw_los 0x62: ch1_sw_losn 0x61: ch1_hw_los 0x60: ch1_hw_losn 0x5F to 0x58: Reserved 0x57: ch0_sw_los 0x56: ch0_sw_losn 0x55: ch0_hw_los 0x54: ch0_hw_losn 0x53: ref_cmu_loln 0x52: Reserved 0x51: Reserved 0x50: Reserved 0x4F: ch3_txen_inverted 0x4E: ch3_txen 0x4D: ch2_txen_inverted 0x4C: ch2_txen 0x4B: ch1_txen_inverted 0x4A: ch1_txen 0x49: ch0_txen_inverted 0x48: ch0_txen 0x47: ch3_rxalarm 0x46: ch2_rxalarm 0x45: ch1_rxalarm 0x44: ch0_rxalarm 0x43: ch3_txalarm 0x42: ch2_txalarm 0x41: ch1_txalarm 0x40: ch0_txalarm 0x3F: ch3_lopc; 0x3E: ch2_lopc 0x3D: ch1_lopc 0x3C: ch0_lopc 0x0B: ch3_pma_rxlol 0x0A: ch3_pma_rxloln 0x09: ch2_pma_rxlol 0x08: ch2_pma_rxloln 0x07: ch1_pma_rxlol 0x06: ch1_pma_rxloln 0x05: ch0_pma_rxlol 0x04: ch0_pma_rxloln * All other register bits: Reserved	RW	0

Table 97 • **GPIO 12 Config/ Status (1Ex0118)**

Bit	Name	Description	Access	Default
15	Traditional GPIO 12 Output Tri-state Control	Controls whether the pin is in input or output mode. Applies only when gpio12_pinfunc_sel=000 0: Output mode 1: Input mode	RW	1
14:13	Traditional GP0IO 12 Pin Function Selection	Applies only when gpio12_pinfunc_sel=000 When gpio12_trad_tri=0 (output mode): 00: gpio12_trad_datareg is driven out the pin. 01: drive repeating LOW/Hi-Z pattern at 1Hz. 01: drive repeating LOW/Hi-Z pattern at 2Hz. 01: drive repeating LOW/Hi-Z pattern at 5Hz. When gpio12_trad_tri=1 (input mode): 00: no interrupt is generated. 01: interrupt generated on the rising edge of pin. 10: interrupt generated on the falling edge of pin. 11: interrupt generated on the both rising and falling edge of pin.	RW	00
12	Traditional GPIO 12 Output data	Logic value transmitted from pin when pin is configured as a traditional general purpose output (gpio12_pinfunc_sel=000 and gpio12_trad_tri=0) 0: Output data = 0 1: Output data = 1	RW	0
11	General Purpose Input Interrupt Pending	GPIO12 must be configured as a general purpose input and have interrupt generation enabled. 0: no interrupt event since the last time the register was read 1: an interrupt event has occurred clear on read	RO	0
10	General Purpose Input Status	Indicates the present value of the GPIO12 pin 0: Present value of GPIO12 pin is 0 1: Present value of GPIO12 pin is 1	RO	
9:8	Reserved		RW	0
7:5	GPIO12 WIS Interrupt Selection	Determines the WIS interrupt status transmitted from the pin when gpio12_pinfunc_sel=010 000: WIS interrupt B from channel 0 001: WIS interrupt B from channel 1 010: WIS interrupt B from channel 2 011: WIS interrupt B from channel 3 100: Logical AND of WIS interrupt B from all/both channels 101: Logical OR of WIS interrupt B from all/both channels 110-111: Reserved	RW	000

Table 97 • **GPIO 12 Config/ Status (1Ex0118) *(continued)***

Bit	Name	Description	Access	Default
4:3	GPIO12 Link Activity Selection	Determines which channel's link activity is transmitted from the pin when gpio12_pinfunc_sel=001 00: Tx link activity from channel 0 01: Tx link activity from channel 1 10: Tx link activity from channel 2 11: Tx link activity from channel 3	RW	00
2:0	GPIO12 Pin Function Selection	Selects the GPIO pin's functionality. 000: Traditional GPIO behavior 001: PCS activity LED output 010: WIS interrupt output 011: Transmit internal signals 100-111: Reserved	RW	000

Table 98 • **GPIO 12 Config2 (1Ex0119)**

Bit	Name	Description	Access	Default
15:7	Reserved		RW	0

Table 98 • **GPIO 12 Config2 (1Ex0119) *(continued)***

Bit	Name	Description	Access	Default
6:0	GPIO12 Internal Node Selection	Determines which channel's link activity is transmitted from the pin when gpio12_pinfunc_sel=011 0x7F to 0x6C: Reserved 0x6B: ch3_sw_los 0x6A: ch3_sw_losn 0x69: ch3_hw_los 0x68: ch3_hw_losn 0x67: ch2_sw_los 0x66: ch2_sw_losn 0x65: ch2_hw_los 0x64: ch2_hw_losn 0x63: ch1_sw_los 0x62: ch1_sw_losn 0x61: ch1_hw_los 0x60: ch1_hw_losn 0x5F to 0x58: Reserved 0x57: ch0_sw_los 0x56: ch0_sw_losn 0x55: ch0_hw_los 0x54: ch0_hw_losn 0x53: ref_cmu_loln 0x52: Reserved 0x51: Reserved 0x50: ch2_rosi_frm_pulse 0x4F: ch3_txen_inverted 0x4E: ch3_txen 0x4D: ch2_txen_inverted 0x4C: ch2_txen 0x4B: ch1_txen_inverted 0x4A: ch1_txen 0x49: ch0_txen_inverted 0x48: ch0_txen 0x47: ch3_rxalarm 0x46: ch2_rxalarm 0x45: ch1_rxalarm 0x44: ch0_rxalarm 0x43: ch3_txalarm 0x42: ch2_txalarm 0x41: ch1_txalarm 0x40: ch0_txalarm 0x3F: ch3_lopc; 0x3E: ch2_lopc 0x3D: ch1_lopc 0x3C: ch0_lopc 0x0B: ch3_pma_rxlol 0x0A: ch3_pma_rxloln 0x09: ch2_pma_rxlol 0x08: ch2_pma_rxloln 0x07: ch1_pma_rxlol 0x06: ch1_pma_rxloln 0x05: ch0_pma_rxlol 0x04: ch0_pma_rxloln * All other register bits: Reserved	RW	0

Table 99 • **GPIO 13 Config/ Status (1Ex011A)**

Bit	Name	Description	Access	Default
15	Traditional GPIO 13 Output Tri-state Control	Controls whether the pin is in input or output mode. Applies only when gpio13_pinfunc_sel=000 0: Output mode 1: Input mode	RW	1
14:13	Traditional GP0IO 13 Pin Function Selection	Applies only when gpio13_pinfunc_sel=000 When gpio13_trad_tri=0 (output mode): 00: gpio13_trad_datareg is driven out the pin. 01: drive repeating LOW/Hi-Z pattern at 1Hz. 01: drive repeating LOW/Hi-Z pattern at 2Hz. 01: drive repeating LOW/Hi-Z pattern at 5Hz. When gpio13_trad_tri=1 (input mode): 00: no interrupt is generated. 01: interrupt generated on the rising edge of pin. 10: interrupt generated on the falling edge of pin. 11: interrupt generated on the both rising and falling edge of pin.	RW	00
12	Traditional GPIO 13 Output data	Logic value transmitted from pin when pin is configured as a traditional general purpose output (gpio13_pinfunc_sel=000 and gpio13_trad_tri=0) 0: Output data = 0 1: Output data = 1	RW	0
11	General Purpose Input Interrupt Pending	GPIO13 must be configured as a general purpose input and have interrupt generation enabled. 0: no interrupt event since the last time the register was read 1: an interrupt event has occurred clear on read	RO	0
10	General Purpose Input Status	Indicates the present value of the GPIO13 pin 0: Present value of GPIO13 pin is 0 1: Present value of GPIO13 pin is 1	RO	
9:8	Reserved		RW	0
7:5	GPIO13 WIS Interrupt Selection	Determines the WIS interrupt status transmitted from the pin when gpio13_pinfunc_sel=010 000: WIS interrupt A from channel 0 001: WIS interrupt A from channel 1 010: WIS interrupt A from channel 2 011: WIS interrupt A from channel 3 100: Logical AND of WIS interrupt A from all/both channels 101: Logical OR of WIS interrupt A from all/both channels 110-111: Reserved	RW	000

Table 99 • **GPIO 13 Config/ Status (1Ex011A) *(continued)***

Bit	Name	Description	Access	Default
4:3	GPIO13 Link Activity Selection	Determines which channel's link activity is transmitted from the pin when gpio13_pinfunc_sel=001 00: Rx link activity from channel 0 01: Rx link activity from channel 1 10: Rx link activity from channel 2 11: Rx link activity from channel 3	RW	00
2:0	GPIO13 Pin Function Selection	Selects the GPIO pin's functionality. 000: Traditional GPIO behavior 001: PCS activity LED output 010: WIS interrupt output 011: Transmit internal signals 100-111: Reserved	RW	000

Table 100 • **GPIO 13 Config2 (1Ex011B)**

Bit	Name	Description	Access	Default
15:7	Reserved		RW	0

Table 100 • **GPIO 13 Config2 (1Ex011B)** ***(continued)***

Bit	Name	Description	Access	Default
6:0	GPIO13 Internal Node Selection	Determines which channel's link activity is transmitted from the pin when gpio13_pinfunc_sel=011 0x7F to 0x6C: Reserved 0x6B: ch3_sw_los 0x6A: ch3_sw_losn 0x69: ch3_hw_los 0x68: ch3_hw_losn 0x67: ch2_sw_los 0x66: ch2_sw_losn 0x65: ch2_hw_los 0x64: ch2_hw_losn 0x63: ch1_sw_los 0x62: ch1_sw_losn 0x61: ch1_hw_los 0x60: ch1_hw_losn 0x5F to 0x58: Reserved 0x57: ch0_sw_los 0x56: ch0_sw_losn 0x55: ch0_hw_los 0x54: ch0_hw_losn 0x53: ref_cmu_loln 0x52: Reserved 0x51: Reserved 0x50: ch2_rosi_sclk 0x4F: ch3_txen_inverted 0x4E: ch3_txen 0x4D: ch2_txen_inverted 0x4C: ch2_txen 0x4B: ch1_txen_inverted 0x4A: ch1_txen 0x49: ch0_txen_inverted 0x48: ch0_txen 0x47: ch3_rxalarm 0x46: ch2_rxalarm 0x45: ch1_rxalarm 0x44: ch0_rxalarm 0x43: ch3_txalarm 0x42: ch2_txalarm 0x41: ch1_txalarm 0x40: ch0_txalarm 0x3F: ch3_lopc; 0x3E: ch2_lopc 0x3D: ch1_lopc 0x3C: ch0_lopc 0x0B: ch3_pma_rxlol 0x0A: ch3_pma_rxloln 0x09: ch2_pma_rxlol 0x08: ch2_pma_rxloln 0x07: ch1_pma_rxlol 0x06: ch1_pma_rxloln 0x05: ch0_pma_rxlol 0x04: ch0_pma_rxloln * All other register bits: Reserved	RW	0

Table 101 • **GPIO 14 Config/ Status (1Ex011C)**

Bit	Name	Description	Access	Default
15	Traditional GPIO 14 Output Tri-state Control	Controls whether the pin is in input or output mode. Applies only when gpio14_pinfunc_sel=000 0: Output mode 1: Input mode	RW	1
14:13	Traditional GP0IO 14 Pin Function Selection	Applies only when gpio14_pinfunc_sel=000 When gpio14_trad_tri=0 (output mode): 00: gpio14_trad_datareg is driven out the pin. 01: drive repeating LOW/Hi-Z pattern at 1Hz. 01: drive repeating LOW/Hi-Z pattern at 2Hz. 01: drive repeating LOW/Hi-Z pattern at 5Hz. When gpio14_trad_tri=1 (input mode): 00: no interrupt is generated. 01: interrupt generated on the rising edge of pin. 10: interrupt generated on the falling edge of pin. 11: interrupt generated on the both rising and falling edge of pin.	RW	00
12	Traditional GPIO 14 Output data	Logic value transmitted from pin when pin is configured as a traditional general purpose output (gpio14_pinfunc_sel=000 and gpio14_trad_tri=0) 0: Output data = 0 1: Output data = 1	RW	0
11	General Purpose Input Interrupt Pending	GPIO14 must be configured as a general purpose input and have interrupt generation enabled. 0: no interrupt event since the last time the register was read 1: an interrupt event has occurred clear on read	RO	0
10	General Purpose Input Status	Indicates the present value of the GPIO14 pin 0: Present value of GPIO14 pin is 0 1: Present value of GPIO14 pin is 1	RO	
9	Reserved		RW	0
8	Module Status Input Enable - channel 2	0: interrupt generation logic for channel 2's module status is disabled. 1: Enable use of this pin to drive interrupt generation logic for channel 2's module status. Pin must be configured as a general purpose input for these bit to serve a purpose.	RW	0

Table 101 • **GPIO 14 Config/ Status (1Ex011C)** ***(continued)***

Bit	Name	Description	Access	Default
7:5	GPIO14 WIS Interrupt Selection	Determines the WIS interrupt status transmitted from the pin when gpio14_pinfunc_sel=010 000: WIS interrupt B from channel 0 001: WIS interrupt B from channel 1 010: WIS interrupt B from channel 2 011: WIS interrupt B from channel 3 100: Logical AND of WIS interrupt B from all/both channels 101: Logical OR of WIS interrupt B from all/both channels 110: Reserved 111: Reserved	RW	000
4:3	GPIO14 Link Activity Selection	Determines which channel's link activity is transmitted from the pin when gpio14_pinfunc_sel=001 00: Tx link activity from channel 0 01: Tx link activity from channel 1 10: Tx link activity from channel 2 11: Tx link activity from channel 3	RW	00
2:0	GPIO14 Pin Function Selection	Selects the GPIO pin's functionality. 000: Traditional GPIO behavior 001: PCS activity LED output 010: WIS interrupt output 011: Transmit internal signals 100-111: Reserved	RW	000

Table 102 • **GPIO 14 Config2 (1Ex011D)**

Bit	Name	Description	Access	Default
15:7	Reserved		RW	0

Table 102 • **GPIO 14 Config2 (1Ex011D)** ***(continued)***

Bit	Name	Description	Access	Default
6:0	GPIO14 Internal Node Selection	Determines which channel's link activity is transmitted from the pin when gpio14_pinfunc_sel=011 0x7F to 0x6C: Reserved 0x6B: ch3_sw_los 0x6A: ch3_sw_losn 0x69: ch3_hw_los 0x68: ch3_hw_losn 0x67: ch2_sw_los 0x66: ch2_sw_losn 0x65: ch2_hw_los 0x64: ch2_hw_losn 0x63: ch1_sw_los 0x62: ch1_sw_losn 0x61: ch1_hw_los 0x60: ch1_hw_losn 0x5F to 0x58: Reserved 0x57: ch0_sw_los 0x56: ch0_sw_losn 0x55: ch0_hw_los 0x54: ch0_hw_losn 0x53: ref_cmu_loln 0x52: Reserved 0x51: Reserved 0x50: ch2_rosi_sdat 0x4F: ch3_txen_inverted 0x4E: ch3_txen 0x4D: ch2_txen_inverted 0x4C: ch2_txen 0x4B: ch1_txen_inverted 0x4A: ch1_txen 0x49: ch0_txen_inverted 0x48: ch0_txen 0x47: ch3_rxalarm 0x46: ch2_rxalarm 0x45: ch1_rxalarm 0x44: ch0_rxalarm 0x43: ch3_txalarm 0x42: ch2_txalarm 0x41: ch1_txalarm 0x40: ch0_txalarm 0x3F: ch3_lopc; 0x3E: ch2_lopc 0x3D: ch1_lopc 0x3C: ch0_lopc 0x0B: ch3_pma_rxlol 0x0A: ch3_pma_rxloln 0x09: ch2_pma_rxlol 0x08: ch2_pma_rxloln 0x07: ch1_pma_rxlol 0x06: ch1_pma_rxloln 0x05: ch0_pma_rxlol 0x04: ch0_pma_rxloln * All other register bits: Reserved	RW	0

Table 103 • **GPIO 15 Config/ Status (1Ex011E)**

Bit	Name	Description	Access	Default
15	Traditional GPIO 15 Output Tri-state Control	Controls whether the pin is in input or output mode. Applies only when gpio15_pinfunc_sel=000 0: Output mode 1: Input mode	RW	1
14:13	Traditional GP0IO 15 Pin Function Selection	Applies only when gpio15_pinfunc_sel=000 When gpio15_trad_tri=0 (output mode): 00: gpio15_trad_datareg is driven out the pin. 01: drive repeating LOW/Hi-Z pattern at 1Hz. 01: drive repeating LOW/Hi-Z pattern at 2Hz. 01: drive repeating LOW/Hi-Z pattern at 5Hz. When gpio15_trad_tri=1 (input mode): 00: no interrupt is generated. 01: interrupt generated on the rising edge of pin. 10: interrupt generated on the falling edge of pin. 11: interrupt generated on the both rising and falling edge of pin.	RW	00
12	Traditional GPIO 15 Output data	Logic value transmitted from pin when pin is configured as a traditional general purpose output (gpio15_pinfunc_sel=000 and gpio15_trad_tri=0) 0: Output data = 0 1: Output data = 1	RW	0
11	General Purpose Input Interrupt Pending	GPIO15 must be configured as a general purpose input and have interrupt generation enabled. 0: no interrupt event since the last time the register was read 1: an interrupt event has occurred clear on read	RO	0
10	General Purpose Input Status	Indicates the present value of the GPIO15 pin 0: Present value of GPIO15 pin is 0 1: Present value of GPIO15 pin is 1	RO	
9:8	Reserved		RW	0
7:5	GPIO15 WIS Interrupt Selection	Determines the WIS interrupt status transmitted from the pin when gpio15_pinfunc_sel=010 000: WIS interrupt A from channel 0 001: WIS interrupt A from channel 1 010: WIS interrupt A from channel 2 011: WIS interrupt A from channel 3 100: Logical AND of WIS interrupt A from all/both channels 101: Logical OR of WIS interrupt A from all/both channels 110: Reserved 111: Reserved	RW	000

Table 103 • **GPIO 15 Config/ Status (1Ex011E)** ***(continued)***

Bit	Name	Description	Access	Default
4:3	GPIO15 Link Activity Selection	Determines which channel's link activity is transmitted from the pin when gpio15_pinfunc_sel=001 00: Rx link activity from channel 0 01: Rx link activity from channel 1 10: Rx link activity from channel 2 11: Rx link activity from channel 3	RW	00
2:0	GPIO15 Pin Function Selection	Selects the GPIO pin's functionality. 000: Traditional GPIO behavior 001: PCS activity LED output 010: WIS interrupt output 011: Transmit internal signals 100-111: Reserved	RW	000

Table 104 • **GPIO 15 Config2 (1Ex011F)**

Bit	Name	Description	Access	Default
15:7	Reserved		RW	0

Table 104 • **GPIO 15 Config2 (1Ex011F)** ***(continued)***

Bit	Name	Description	Access	Default
6:0	GPIO15 Internal Node Selection	Determines which channel's link activity is transmitted from the pin when gpio15_pinfunc_sel=011 0x7F to 0x6C: Reserved 0x6B: ch3_sw_los 0x6A: ch3_sw_losn 0x69: ch3_hw_los 0x68: ch3_hw_losn 0x67: ch2_sw_los 0x66: ch2_sw_losn 0x65: ch2_hw_los 0x64: ch2_hw_losn 0x63: ch1_sw_los 0x62: ch1_sw_losn 0x61: ch1_hw_los 0x60: ch1_hw_losn 0x5F to 0x58: Reserved 0x57: ch0_sw_los 0x56: ch0_sw_losn 0x55: ch0_hw_los 0x54: ch0_hw_losn 0x53: ref_cmu_loln 0x52: Reserved 0x51: Reserved 0x50: ch2_tosi_frm_pulse 0x4F: ch3_txen_inverted 0x4E: ch3_txen 0x4D: ch2_txen_inverted 0x4C: ch2_txen 0x4B: ch1_txen_inverted 0x4A: ch1_txen 0x49: ch0_txen_inverted 0x48: ch0_txen 0x47: ch3_rxalarm 0x46: ch2_rxalarm 0x45: ch1_rxalarm 0x44: ch0_rxalarm 0x43: ch3_txalarm 0x42: ch2_txalarm 0x41: ch1_txalarm 0x40: ch0_txalarm 0x3F: ch3_lopc; 0x3E: ch2_lopc 0x3D: ch1_lopc 0x3C: ch0_lopc 0x0B: ch3_pma_rxlol 0x0A: ch3_pma_rxloln 0x09: ch2_pma_rxlol 0x08: ch2_pma_rxloln 0x07: ch1_pma_rxlol 0x06: ch1_pma_rxloln 0x05: ch0_pma_rxlol 0x04: ch0_pma_rxloln * All other register bits: Reserved	RW	0

Table 105 • **GPIO 16 Config/ Status (1Ex0120)**

Bit	Name	Description	Access	Default
15	Traditional GPIO 16 Output Tri-state Control	Controls whether the pin is in input or output mode. Applies only when gpio16_pinfunc_sel=000 0: Output mode 1: Input mode	RW	1
14:13	Traditional GP0IO 16 Pin Function Selection	Applies only when gpio16_pinfunc_sel=000 When gpio16_trad_tri=0 (output mode): 00: gpio16_trad_datareg is driven out the pin. 01: drive repeating LOW/Hi-Z pattern at 1Hz. 01: drive repeating LOW/Hi-Z pattern at 2Hz. 01: drive repeating LOW/Hi-Z pattern at 5Hz. When gpio16_trad_tri=1 (input mode): 00: no interrupt is generated. 01: interrupt generated on the rising edge of pin. 10: interrupt generated on the falling edge of pin. 11: interrupt generated on the both rising and falling edge of pin.	RW	00
12	Traditional GPIO 16 Output data	Logic value transmitted from pin when pin is configured as a traditional general purpose output (gpio16_pinfunc_sel=000 and gpio16_trad_tri=0) 0: Output data = 0 1: Output data = 1	RW	0
11	General Purpose Input Interrupt Pending	GPIO16 must be configured as a general purpose input and have interrupt generation enabled. 0: no interrupt event since the last time the register was read 1: an interrupt event has occurred clear on read	RO	0
10	General Purpose Input Status	Indicates the present value of the GPIO16 pin 0: Present value of GPIO16 pin is 0 1: Present value of GPIO16 pin is 1	RO	
9:8	Reserved		RW	0
7:5	GPIO16 WIS Interrupt Selection	Determines the WIS interrupt status transmitted from the pin when gpio16_pinfunc_sel=010 000: WIS interrupt B from channel 0 001: WIS interrupt B from channel 1 010: WIS interrupt B from channel 2 011: WIS interrupt B from channel 3 100: Logical AND of WIS interrupt B from all/both channels 101: Logical OR of WIS interrupt B from all/both channels 110: Reserved 111: Reserved	RW	000

Table 105 • **GPIO 16 Config/ Status (1Ex0120) *(continued)***

Bit	Name	Description	Access	Default
4:3	GPIO16 Link Activity Selection	Determines which channel's link activity is transmitted from the pin when gpio16_pinfunc_sel=001 00: Tx link activity from channel 0 01: Tx link activity from channel 1 10: Tx link activity from channel 2 11: Tx link activity from channel 3	RW	00
2:0	GPIO16 Pin Function Selection	Selects the GPIO pin's functionality. 000: Traditional GPIO behavior 001: PCS activity LED output 010: WIS interrupt output 011: Transmit internal signals 100-111: Reserved	RW	000

Table 106 • **GPIO 16 Config2 (1Ex0121)**

Bit	Name	Description	Access	Default
15:7	Reserved		RW	0

Table 106 • **GPIO 16 Config2 (1Ex0121)** ***(continued)***

Bit	Name	Description	Access	Default
6:0	GPIO16 Internal Node Selection	Determines which channel's link activity is transmitted from the pin when gpio16_pinfunc_sel=011 0x7F to 0x6C: Reserved 0x6B: ch3_sw_los 0x6A: ch3_sw_losn 0x69: ch3_hw_los 0x68: ch3_hw_losn 0x67: ch2_sw_los 0x66: ch2_sw_losn 0x65: ch2_hw_los 0x64: ch2_hw_losn 0x63: ch1_sw_los 0x62: ch1_sw_losn 0x61: ch1_hw_los 0x60: ch1_hw_losn 0x5F to 0x58: Reserved 0x57: ch0_sw_los 0x56: ch0_sw_losn 0x55: ch0_hw_los 0x54: ch0_hw_losn 0x53: ref_cmu_loln 0x52: Reserved 0x51: Reserved 0x50: ch2_tosi_sclk 0x4F: ch3_txen_inverted 0x4E: ch3_txen 0x4D: ch2_txen_inverted 0x4C: ch2_txen 0x4B: ch1_txen_inverted 0x4A: ch1_txen 0x49: ch0_txen_inverted 0x48: ch0_txen 0x47: ch3_rxalarm 0x46: ch2_rxalarm 0x45: ch1_rxalarm 0x44: ch0_rxalarm 0x43: ch3_txalarm 0x42: ch2_txalarm 0x41: ch1_txalarm 0x40: ch0_txalarm 0x3F: ch3_lopc; 0x3E: ch2_lopc 0x3D: ch1_lopc 0x3C: ch0_lopc 0x0B: ch3_pma_rxlol 0x0A: ch3_pma_rxloln 0x09: ch2_pma_rxlol 0x08: ch2_pma_rxloln 0x07: ch1_pma_rxlol 0x06: ch1_pma_rxloln 0x05: ch0_pma_rxlol 0x04: ch0_pma_rxloln * All other register bits: Reserved	RW	0

Table 107 • **GPIO 17 Config/ Status (1Ex0122)**

Bit	Name	Description	Access	Default
15	Traditional GPIO 17 Output Tri-state Control	Controls whether the pin is in input or output mode. Applies only when gpio17_pinfunc_sel=000 0: Output mode 1: Input mode	RW	1
14:13	Traditional GP0IO 17 Pin Function Selection	Applies only when gpio17_pinfunc_sel=000 When gpio17_trad_tri=0 (output mode): 00: gpio17_trad_datareg is driven out the pin. 01: drive repeating LOW/Hi-Z pattern at 1Hz. 01: drive repeating LOW/Hi-Z pattern at 2Hz. 01: drive repeating LOW/Hi-Z pattern at 5Hz. When gpio17_trad_tri=1 (input mode): 00: no interrupt is generated. 01: interrupt generated on the rising edge of pin. 10: interrupt generated on the falling edge of pin. 11: interrupt generated on the both rising and falling edge of pin.	RW	00
12	Traditional GPIO 17 Output data	Logic value transmitted from pin when pin is configured as a traditional general purpose output (gpio17_pinfunc_sel=000 and gpio17_trad_tri=0) 0: Output data = 0 1: Output data = 1	RW	0
11	General Purpose Input Interrupt Pending	GPIO17 must be configured as a general purpose input and have interrupt generation enabled. 0: no interrupt event since the last time the register was read 1: an interrupt event has occurred clear on read	RO	0
10	General Purpose Input Status	Indicates the present value of the GPIO17 pin 0: Present value of GPIO17 pin is 0 1: Present value of GPIO17 pin is 1	RO	
9	Reserved		RW	0
8	Channel 2 TOSI Data Input Enable	0: Channel 2's TOSI is disabled. 1: Enable use of this pin as channel 2's TOSI Data Input. Pin must be configured as a general purpose input for these bit to serve a purpose.	RW	0
7:5	GPIO17 WIS Interrupt Selection	Determines the WIS interrupt status transmitted from the pin when gpio17_pinfunc_sel=010 000: WIS interrupt A from channel 0 001: WIS interrupt A from channel 1 010: WIS interrupt A from channel 2 011: WIS interrupt A from channel 3 100: Logical AND of WIS interrupt A from all/both channels 101: Logical OR of WIS interrupt A from all/both channels 110: Reserved 111: Reserved	RW	000

Table 107 • **GPIO 17 Config/ Status (1Ex0122) *(continued)***

Bit	Name	Description	Access	Default
4:3	GPIO17 Link Activity Selection	Determines which channel's link activity is transmitted from the pin when gpio17_pinfunc_sel=001 00: Rx link activity from channel 0 01: Rx link activity from channel 1 10: Rx link activity from channel 2 11: Rx link activity from channel 3	RW	00
2:0	GPIO17 Pin Function Selection	Selects the GPIO pin's functionality. 000: Traditional GPIO behavior 001: PCS activity LED output 010: WIS interrupt output 011: Transmit internal signals 100-111: Reserved	RW	000

Table 108 • **GPIO 17 Config2 (1Ex0123)**

Bit	Name	Description	Access	Default
15:7	Reserved		RW	0

Table 108 • **GPIO 17 Config2 (1Ex0123)** ***(continued)***

Bit	Name	Description	Access	Default
6:0	GPIO17 Internal Node Selection	Determines which channel's link activity is transmitted from the pin when gpio17_pinfunc_sel=011 0x7F to 0x6C: Reserved 0x6B: ch3_sw_los 0x6A: ch3_sw_losn 0x69: ch3_hw_los 0x68: ch3_hw_losn 0x67: ch2_sw_los 0x66: ch2_sw_losn 0x65: ch2_hw_los 0x64: ch2_hw_losn 0x63: ch1_sw_los 0x62: ch1_sw_losn 0x61: ch1_hw_los 0x60: ch1_hw_losn 0x5F to 0x58: Reserved 0x57: ch0_sw_los 0x56: ch0_sw_losn 0x55: ch0_hw_los 0x54: ch0_hw_losn 0x53: ref_cmu_loln 0x52: Reserved 0x51: Reserved 0x50: Reserved 0x4F: ch3_txen_inverted 0x4E: ch3_txen 0x4D: ch2_txen_inverted 0x4C: ch2_txen 0x4B: ch1_txen_inverted 0x4A: ch1_txen 0x49: ch0_txen_inverted 0x48: ch0_txen 0x47: ch3_rxalarm 0x46: ch2_rxalarm 0x45: ch1_rxalarm 0x44: ch0_rxalarm 0x43: ch3_txalarm 0x42: ch2_txalarm 0x41: ch1_txalarm 0x40: ch0_txalarm 0x3F: ch3_lopc; 0x3E: ch2_lopc 0x3D: ch1_lopc 0x3C: ch0_lopc 0x0B: ch3_pma_rxlol 0x0A: ch3_pma_rxloln 0x09: ch2_pma_rxlol 0x08: ch2_pma_rxloln 0x07: ch1_pma_rxlol 0x06: ch1_pma_rxloln 0x05: ch0_pma_rxlol 0x04: ch0_pma_rxloln * All other register bits: Reserved	RW	0

Table 109 • **GPIO 18 Config/ Status (1Ex0124)**

Bit	Name	Description	Access	Default
15	Traditional GPIO 18 Output Tri-state Control	Controls whether the pin is in input or output mode. Applies only when bit 2:0, gpio18_pinfunc_sel=000 0: Output mode 1: Input mode	RW	1
14:13	Traditional GPIO 18 Pin Function Selection	Applies only when bit 2:0, gpio18_pinfunc_sel=000 When bit 15, gpio18_trad_tri=0 (output mode): 00: bit 12, gpio18_trad_datareg is driven out the pin. 01: drive repeating LOW/Hi-Z pattern at 1Hz. 01: drive repeating LOW/Hi-Z pattern at 2Hz. 01: drive repeating LOW/Hi-Z pattern at 5Hz. When gpio18_trad_tri=1 (input mode): 00: no interrupt is generated. 01: interrupt generated on the rising edge of pin. 10: interrupt generated on the falling edge of pin. 11: interrupt generated on the both rising and falling edge of pin.	RW	00
12	Traditional GPIO 18 Output data	Logic value transmitted from pin when pin is configured as a traditional general purpose output (gpio18_pinfunc_sel=000 and gpio18_trad_tri=0) 0: Output data = 0 1: Output data = 1	RW	0
11	General Purpose Input Interrupt Pending	GPIO18 must be configured as a general purpose input and have interrupt generation enabled. 0: no interrupt event since the last time the register was read 1: an interrupt event has occurred clear on read	RO	0
10	General Purpose Input Status	Indicates the present value of the GPIO18 pin 0: Present value of GPIO18 pin is 0 1: Present value of GPIO18 pin is 1	RO	
9:8	Reserved		RW	0
7:5	GPIO18 WIS Interrupt Selection	Determines the WIS interrupt status transmitted from the pin when gpio18_pinfunc_sel=010 000: WIS interrupt B from channel 0 001: WIS interrupt B from channel 1 010: WIS interrupt B from channel 2 011: WIS interrupt B from channel 3 100: Logical AND of WIS interrupt B from all channels 101: Logical OR of WIS interrupt B from all channels 110: Reserved 111: Reserved	RW	000

Table 109 • **GPIO 18 Config/ Status (1Ex0124) *(continued)***

Bit	Name	Description	Access	Default
4:3	GPIO18 Link Activity Selection	Determines which channel's link activity is transmitted from the pin when gpio18_pinfunc_sel=001 00: Tx link activity from channel 0 01: Tx link activity from channel 1 10: Tx link activity from channel 2 11: Tx link activity from channel 3	RW	00
2:0	GPIO18 Pin Function Selection	Selects the GPIO pin's functionality. 000: Traditional GPIO behavior 001: PCS activity LED output 010: WIS interrupt output 011: Transmit internal signals 100: UART Tx 101-111: Reserved	RW	100

Table 110 • **GPIO 18 Config2 (1Ex0125)**

Bit	Name	Description	Access	Default
15:7	Reserved		RW	0

Table 110 • **GPIO 18 Config2 (1Ex0125) *(continued)***

Bit	Name	Description	Access	Default
6:0	GPIO18 Internal Node Selection	Determines which channel's link activity is transmitted from the pin when gpio18_pinfunc_sel=011 0x7F to 0x64: Reserved 0x63: ch1_sw_los 0x62: ch1_sw_losn 0x61: ch1_hw_los 0x60: ch1_hw_losn 0x5F to 0x58: Reserved 0x57: ch0_sw_los 0x56: ch0_sw_losn 0x55: ch0_hw_los 0x54: ch0_hw_losn 0x53: ref_cmu_loln 0x52: Reserved 0x51: Reserved 0x50: ch1_rosi_frm_pulse 0x4F: Reserved 0x4E: Reserved 0x4D: Reserved 0x4C: Reserved 0x4B: ch1_txen_inverted 0x4A: ch1_txen 0x49: ch0_txen_inverted 0x48: ch0_txen 0x47: Reserved 0x46: Reserved 0x45: ch1_rxalarm 0x44: ch0_rxalarm 0x43: Reserved 0x42: Reserved 0x41: ch1_txalarm 0x40: ch0_txalarm 0x3F: Reserved 0x3E: Reserved 0x3D: ch1_lopc 0x3C: ch0_lopc 0x3B to 0x08: Reserved 0x07: ch1_pma_rxlol 0x06: ch1_pma_rxloln 0x05: ch0_pma_rxlol 0x04: ch0_pma_rxloln 0x03 to 0x00: Reserved	RW	0

Table 111 • **GPIO 19 Config/ Status (1Ex0126)**

Bit	Name	Description	Access	Default
15	Traditional GPIO 19 Output Tri-state Control	Controls whether the pin is in input or output mode. Applies only when gpio19_pinfunc_sel=000 0: Output mode 1: Input mode	RW	1

Table 111 • **GPIO 19 Config/ Status (1Ex0126)** ***(continued)***

Bit	Name	Description	Access	Default
14:13	Traditional GPIO 19 Pin Function Selection	Applies only when bit 2:0, gpio19_pinfunc_sel=000 When bit 15, gpio19_trad_tri=0 (output mode): 00: bit 12, gpio19_trad_datareg is driven out the pin. 01: drive repeating LOW/Hi-Z pattern at 1Hz. 01: drive repeating LOW/Hi-Z pattern at 2Hz. 01: drive repeating LOW/Hi-Z pattern at 5Hz. When gpio19_trad_tri=1 (input mode): 00: no interrupt is generated. 01: interrupt generated on the rising edge of pin. 10: interrupt generated on the falling edge of pin. 11: interrupt generated on the both rising and falling edge of pin.	RW	00
12	Traditional GPIO 19 Output data	Logic value transmitted from pin when pin is configured as a traditional general purpose output (gpio19_pinfunc_sel=000 and gpio19_trad_tri=0) 0: Output data = 0 1: Output data = 1	RW	0
11	General Purpose Input Interrupt Pending	GPIO19 must be configured as a general purpose input and have interrupt generation enabled. 0: no interrupt event since the last time the register was read 1: an interrupt event has occurred clear on read	RO	0
10	General Purpose Input Status	Indicates the present value of the GPIO19 pin 0: Present value of GPIO19 pin is 0 1: Present value of GPIO19 pin is 1	RO	
9:8	Reserved		RW	0
7:5	GPIO19 WIS Interrupt Selection	Determines the WIS interrupt status transmitted from the pin when gpio19_pinfunc_sel=010 000: WIS interrupt A from channel 0 001: WIS interrupt A from channel 1 010: WIS interrupt A from channel 2 011: WIS interrupt A from channel 3 100: Logical AND of WIS interrupt A from all channels 101: Logical OR of WIS interrupt A from all channels 110: Reserved 111: Reserved	RW	000
4:3	GPIO19 Link Activity Selection	Determines which channel's link activity is transmitted from the pin when gpio19_pinfunc_sel=001 00: Rx link activity from channel 0 01: Rx link activity from channel 1 10: Rx link activity from channel 2 11: Rx link activity from channel 3	RW	00

Table 111 • **GPIO 19 Config/ Status (1Ex0126) *(continued)***

Bit	Name	Description	Access	Default
2:0	GPIO19 Pin Function Selection	Selects the GPIO pin's functionality. 000: Traditional GPIO behavior 001: PCS activity LED output 010: WIS interrupt output 011: Transmit internal signals 100: UART Rx 101-111: Reserved	RW	100

Table 112 • **GPIO 19 Config2 (1Ex0127)**

Bit	Name	Description	Access	Default
15:7	Reserved		RW	0

Table 112 • **GPIO 19 Config2 (1Ex0127)** ***(continued)***

Bit	Name	Description	Access	Default
6:0	GPIO19 Internal Node Selection	Determines which channel's link activity is transmitted from the pin when gpio19_pinfunc_sel=011 0x7F to 0x6C: Reserved 0x6B: ch3_sw_los 0x6A: ch3_sw_losn 0x69: ch3_hw_los 0x68: ch3_hw_losn 0x67: ch2_sw_los 0x66: ch2_sw_losn 0x65: ch2_hw_los 0x64: ch2_hw_losn 0x63: ch1_sw_los 0x62: ch1_sw_losn 0x61: ch1_hw_los 0x60: ch1_hw_losn 0x5F to 0x58: Reserved 0x57: ch0_sw_los 0x56: ch0_sw_losn 0x55: ch0_hw_los 0x54: ch0_hw_losn 0x53: ref_cmu_loln 0x52: Reserved 0x51: Reserved 0x50: ch1_rosi_sclk_1 0x4F: Reserved 0x4E: Reserved 0x4D: Reserved 0x4C: Reserved 0x4B: ch1_txen_inverted 0x4A: ch1_txen 0x49: ch0_txen_inverted 0x48: ch0_txen 0x47: Reserved 0x46: Reserved 0x45: ch1_rxalarm 0x44: ch0_rxalarm 0x43: Reserved 0x42: Reserved 0x41: ch1_txalarm 0x40: ch0_txalarm 0x3F: Reserved 0x3E: Reserved 0x3D: ch1_lopc 0x3C: ch0_lopc 0x3B to 0x08: Reserved 0x07: ch1_pma_rxlol 0x06: ch1_pma_rxloln 0x05: ch0_pma_rxlol 0x04: ch0_pma_rxloln 0x03 to 0x00: Reserved	RW	0

Table 113 • **GPIO 20 Config/ Status (1Ex0128)**

Bit	Name	Description	Access	Default
15	Traditional GPIO 20 Output Tri-state Control	Controls whether the pin is in input or output mode. Applies only when bit 2:0, gpio20_pinfunc_sel=000 0: Output mode 1: Input mode	RW	1
14:13	Traditional GPIO 20 Pin Function Selection	Applies only when bit 2:0, gpio20_pinfunc_sel=000 When bit 15, gpio20_trad_tri=0 (output mode): 00: bit 12, gpio20_trad_datareg is driven out the pin. 01: drive repeating LOW/Hi-Z pattern at 1Hz. 01: drive repeating LOW/Hi-Z pattern at 2Hz. 01: drive repeating LOW/Hi-Z pattern at 5Hz. When gpio20_trad_tri=1 (input mode): 00: no interrupt is generated. 01: interrupt generated on the rising edge of pin. 10: interrupt generated on the falling edge of pin. 11: interrupt generated on the both rising and falling edge of pin.	RW	00
12	Traditional GPIO 20 Output data	Logic value transmitted from pin when pin is configured as a traditional general purpose output (gpio20_pinfunc_sel=000 and gpio20_trad_tri=0) 0: Output data = 0 1: Output data = 1	RW	0
11	General Purpose Input Interrupt Pending	GPIO20 must be configured as a general purpose input and have interrupt generation enabled. 0: no interrupt event since the last time the register was read 1: an interrupt event has occurred clear on read	RO	0
10	General Purpose Input Status	Indicates the present value of the GPIO20 pin 0: Present value of GPIO20 pin is 0 1: Present value of GPIO20 pin is 1	RO	
9:8	Reserved		RW	0
7:5	GPIO20 WIS Interrupt Selection	Determines the WIS interrupt status transmitted from the pin when gpio20_pinfunc_sel=010 000: WIS interrupt A from channel 0 001: WIS interrupt A from channel 1 010: WIS interrupt A from channel 2 011: WIS interrupt A from channel 3 100: Logical AND of WIS interrupt A from all channels 101: Logical OR of WIS interrupt A from all channels 110: Reserved 111: Reserved	RW	000

Table 113 • **GPIO 20 Config/ Status (1Ex0128) *(continued)***

Bit	Name	Description	Access	Default
4:3	GPIO20 Link Activity Selection	Determines which channel's link activity is transmitted from the pin when gpio20_pinfunc_sel=001 00: Tx link activity from channel 0 01: Tx link activity from channel 1 10: Tx link activity from channel 2 11: Tx link activity from channel 3	RW	00
2:0	GPIO20 Pin Function Selection	Selects the GPIO pin's functionality. 000: Traditional GPIO behavior 001: PCS activity LED output 010: WIS interrupt output 011: Transmit internal signals 100-111: Reserved	RW	000

Table 114 • **GPIO 20 Config2 (1Ex0129)**

Bit	Name	Description	Access	Default
15:7	Reserved		RW	0

Table 114 • **GPIO 20 Config2 (1Ex0129)** ***(continued)***

Bit	Name	Description	Access	Default
6:0	GPIO20 Internal Node Selection	Determines which channel's link activity is transmitted from the pin when gpio20_pinfunc_sel=011 0x7F to 0x6C: Reserved 0x6B: ch3_sw_los 0x6A: ch3_sw_losn 0x69: ch3_hw_los 0x68: ch3_hw_losn 0x67: ch2_sw_los 0x66: ch2_sw_losn 0x65: ch2_hw_los 0x64: ch2_hw_losn 0x63: ch1_sw_los 0x62: ch1_sw_losn 0x61: ch1_hw_los 0x60: ch1_hw_losn 0x5F to 0x58: Reserved 0x57: ch0_sw_los 0x56: ch0_sw_losn 0x55: ch0_hw_los 0x54: ch0_hw_losn 0x53: ref_cmu_loln 0x52: Reserved 0x51: Reserved 0x50: ch1_rosi_sdat 0x4F: Reserved 0x4E: Reserved 0x4D: Reserved 0x4C: Reserved 0x4B: ch1_txen_inverted 0x4A: ch1_txen 0x49: ch0_txen_inverted 0x48: ch0_txen 0x47: Reserved 0x46: Reserved 0x45: ch1_rxalarm 0x44: ch0_rxalarm 0x43: Reserved 0x42: Reserved 0x41: ch1_txalarm 0x40: ch0_txalarm 0x3F: Reserved 0x3E: Reserved 0x3D: ch1_lopc 0x3C: ch0_lopc 0x3B to 0x08: Reserved 0x07: ch1_pma_rxlol 0x06: ch1_pma_rxloln 0x05: ch0_pma_rxlol 0x04: ch0_pma_rxloln 0x03 to 0x00: Reserved	RW	0

Table 115 • **GPIO 21 Config/ Status (1Ex012A)**

Bit	Name	Description	Access	Default
15	Traditional GPIO 21 Output Tri-state Control	Controls whether the pin is in input or output mode. Applies only when bit 2:0, gpio21_pinfunc_sel=000 0: Output mode 1: Input mode	RW	1
14:13	Traditional GP0IO 21 Pin Function Selection	Applies only when bit 2:0, gpio21_pinfunc_sel=000 When bit 15, gpio21_trad_tri=0 (output mode): 00: bit 12, gpio21_trad_datareg is driven out the pin. 01: drive repeating LOW/Hi-Z pattern at 1Hz. 01: drive repeating LOW/Hi-Z pattern at 2Hz. 01: drive repeating LOW/Hi-Z pattern at 5Hz. When gpio21_trad_tri=1 (input mode): 00: no interrupt is generated. 01: interrupt generated on the rising edge of pin. 10: interrupt generated on the falling edge of pin. 11: interrupt generated on the both rising and falling edge of pin.	RW	00
12	Traditional GPIO 21 Output data	Logic value transmitted from pin when pin is configured as a traditional general purpose output (gpio21_pinfunc_sel=000 and gpio21_trad_tri=0) 0: Output data = 0 1: Output data = 1	RW	0
11	General Purpose Input Interrupt Pending	GPIO21 must be configured as a general purpose input and have interrupt generation enabled. 0: no interrupt event since the last time the register was read 1: an interrupt event has occurred clear on read	RO	0
10	General Purpose Input Status	Indicates the present value of the GPIO21 pin 0: Present value of GPIO21 pin is 0 1: Present value of GPIO21 pin is 1	RO	
9	PMTICK Enable 2	0: Pin is not used as a PMTICK input. 1: Enable use of this pin as a PMTICK input. Pin must be configured as a general purpose input for these bit to serve a purpose.	RW	0
8	Module Status Input Enable - channel 1	0: interrupt generation logic for channel 1's module status is disabled. 1: Enable use of this pin to drive interrupt generation logic for channel 1's module status. Pin must be configured as a general purpose input for these bit to serve a purpose.	RW	0

Table 115 • **GPIO 21 Config/ Status (1Ex012A)** ***(continued)***

Bit	Name	Description	Access	Default
7:5	GPIO21 WIS Interrupt Selection	Determines the WIS interrupt status transmitted from the pin when gpio21_pinfunc_sel=010 000: WIS interrupt A from channel 0 001: WIS interrupt A from channel 1 010: WIS interrupt A from channel 2 011: WIS interrupt A from channel 3 100: Logical AND of WIS interrupt A from all channels 101: Logical OR of WIS interrupt A from all channels 110: Reserved 111: Reserved	RW	000
4:3	GPIO21 Link Activity Selection	Determines which channel's link activity is transmitted from the pin when gpio21_pinfunc_sel=001 00: Rx link activity from channel 0 01: Rx link activity from channel 1 10: Rx link activity from channel 2 11: Rx link activity from channel 3	RW	00
2:0	GPIO21 Pin Function Selection	Selects the GPIO pin's functionality. 000: Traditional GPIO behavior 001: PCS activity LED output 010: WIS interrupt output 011: Transmit internal signals 100-111: Reserved	RW	000

Table 116 • **GPIO 21 Config2 (1Ex012B)**

Bit	Name	Description	Access	Default
15:7	Reserved		RW	0

Table 116 • **GPIO 21 Config2 (1Ex012B)** ***(continued)***

Bit	Name	Description	Access	Default
6:0	GPIO21 Internal Node Selection	Determines which channel's link activity is transmitted from the pin when gpio21_pinfunc_sel=011 0x7F to 0x6C: Reserved 0x6B: ch3_sw_los 0x6A: ch3_sw_losn 0x69: ch3_hw_los 0x68: ch3_hw_losn 0x67: ch2_sw_los 0x66: ch2_sw_losn 0x65: ch2_hw_los 0x64: ch2_hw_losn 0x63: ch1_sw_los 0x62: ch1_sw_losn 0x61: ch1_hw_los 0x60: ch1_hw_losn 0x5F to 0x58: Reserved 0x57: ch0_sw_los 0x56: ch0_sw_losn 0x55: ch0_hw_los 0x54: ch0_hw_losn 0x53: ref_cmu_loln 0x52: Reserved 0x51: Reserved 0x50: ch1_tosi_sclk 0x4F: Reserved 0x4E: Reserved 0x4D: Reserved 0x4C: Reserved 0x4B: ch1_txen_inverted 0x4A: ch1_txen 0x49: ch0_txen_inverted 0x48: ch0_txen 0x47: Reserved 0x46: Reserved 0x45: ch1_rxalarm 0x44: ch0_rxalarm 0x43: Reserved 0x42: Reserved 0x41: ch1_txalarm 0x40: ch0_txalarm 0x3F: Reserved 0x3E: Reserved 0x3D: ch1_lopc 0x3C: ch0_lopc 0x3B to 0x08: Reserved 0x07: ch1_pma_rxlol 0x06: ch1_pma_rxloln 0x05: ch0_pma_rxlol 0x04: ch0_pma_rxloln 0x03 to 0x00: Reserved	RW	0

Table 117 • **GPIO 22 Config/ Status (1Ex012C)**

Bit	Name	Description	Access	Default
15	Traditional GPIO 22 Output Tri-state Control	Controls whether the pin is in input or output mode. Applies only when bit 2:0, gpio22_pinfunc_sel=000 0: Output mode 1: Input mode	RW	1
14:13	Traditional GP0IO 22 Pin Function Selection	Applies only when bit 2:0, gpio22_pinfunc_sel=000 When bit 15, gpio22_trad_tri=0 (output mode): 00: bit 12, gpio22_trad_datareg is driven out the pin. 01: drive repeating LOW/Hi-Z pattern at 1Hz. 01: drive repeating LOW/Hi-Z pattern at 2Hz. 01: drive repeating LOW/Hi-Z pattern at 5Hz. When gpio22_trad_tri=1 (input mode): 00: no interrupt is generated. 01: interrupt generated on the rising edge of pin. 10: interrupt generated on the falling edge of pin. 11: interrupt generated on the both rising and falling edge of pin.	RW	00
12	Traditional GPIO 22 Output data	Logic value transmitted from pin when pin is configured as a traditional general purpose output (gpio22_pinfunc_sel=000 and gpio22_trad_tri=0) 0: Output data = 0 1: Output data = 1	RW	0
11	General Purpose Input Interrupt Pending	GPIO22 must be configured as a general purpose input and have interrupt generation enabled. 0: no interrupt event since the last time the register was read 1: an interrupt event has occurred clear on read	RO	0
10	General Purpose Input Status	Indicates the present value of the GPIO22 pin 0: Present value of GPIO22 pin is 0 1: Present value of GPIO22 pin is 1	RO	
9:8	Reserved		RW	0
7:5	GPIO22 WIS Interrupt Selection	Determines the WIS interrupt status transmitted from the pin when gpio22_pinfunc_sel=010 000: WIS interrupt B from channel 0 001: WIS interrupt B from channel 1 010: WIS interrupt B from channel 2 011: WIS interrupt B from channel 3 100: Logical AND of WIS interrupt B from all channels 101: Logical OR of WIS interrupt B from all channels 110: Reserved 111: Reserved	RW	000

Table 117 • **GPIO 22 Config/ Status (1Ex012C)** ***(continued)***

Bit	Name	Description	Access	Default
4:3	GPIO22 Link Activity Selection	Determines which channel's link activity is transmitted from the pin when gpio22_pinfunc_sel=001 00: Tx link activity from channel 0 01: Tx link activity from channel 1 10: Tx link activity from channel 2 11: Tx link activity from channel 3	RW	00
2:0	GPIO22 Pin Function Selection	Selects the GPIO pin's functionality. 000: Traditional GPIO behavior 001: PCS activity LED output 010: WIS interrupt output 011: Transmit internal signals 100-111: Reserved	RW	000

Table 118 • **GPIO 22 Config2 (1Ex012D)**

Bit	Name	Description	Access	Default
15:7	Reserved		RW	0

Table 118 • **GPIO 22 Config2 (1Ex012D)** ***(continued)***

Bit	Name	Description	Access	Default
6:0	GPIO22 Internal Node Selection	Determines which channel's link activity is transmitted from the pin when gpio22_pinfunc_sel=011 0x7F to 0x6C: Reserved 0x6B: ch3_sw_los 0x6A: ch3_sw_losn 0x69: ch3_hw_los 0x68: ch3_hw_losn 0x67: ch2_sw_los 0x66: ch2_sw_losn 0x65: ch2_hw_los 0x64: ch2_hw_losn 0x63: ch1_sw_los 0x62: ch1_sw_losn 0x61: ch1_hw_los 0x60: ch1_hw_losn 0x5F to 0x58: Reserved 0x57: ch0_sw_los 0x56: ch0_sw_losn 0x55: ch0_hw_los 0x54: ch0_hw_losn 0x53: ref_cmu_loln 0x52: Reserved 0x51: Reserved 0x50: ch1_tosi_sclk 0x4F: Reserved 0x4E: Reserved 0x4D: Reserved 0x4C: Reserved 0x4B: ch1_txen_inverted 0x4A: ch1_txen 0x49: ch0_txen_inverted 0x48: ch0_txen 0x47: Reserved 0x46: Reserved 0x45: ch1_rxalarm 0x44: ch0_rxalarm 0x43: Reserved 0x42: Reserved 0x41: ch1_txalarm 0x40: ch0_txalarm 0x3F: Reserved 0x3E: Reserved 0x3D: ch1_lopc 0x3C: ch0_lopc 0x3B to 0x08: Reserved 0x07: ch1_pma_rxlol 0x06: ch1_pma_rxloln 0x05: ch0_pma_rxlol 0x04: ch0_pma_rxloln 0x03 to 0x00: Reserved	RW	0

Table 119 • **GPIO 23 Config/ Status (1Ex012E)**

Bit	Name	Description	Access	Default
15	Traditional GPIO 23 Output Tri-state Control	Controls whether the pin is in input or output mode. Applies only when bit 2:0, gpio23_pinfunc_sel=000 0: Output mode 1: Input mode	RW	1
14:13	Traditional GP0IO 23 Pin Function Selection	Applies only when bit 2:0, gpio23_pinfunc_sel=000 When bit 15, gpio23_trad_tri=0 (output mode): 00: bit 12, gpio23_trad_datareg is driven out the pin. 01: drive repeating LOW/Hi-Z pattern at 1Hz. 01: drive repeating LOW/Hi-Z pattern at 2Hz. 01: drive repeating LOW/Hi-Z pattern at 5Hz. When gpio23_trad_tri=1 (input mode): 00: no interrupt is generated. 01: interrupt generated on the rising edge of pin. 10: interrupt generated on the falling edge of pin. 11: interrupt generated on the both rising and falling edge of pin.	RW	00
12	Traditional GPIO 23 Output data	Logic value transmitted from pin when pin is configured as a traditional general purpose output (gpio23_pinfunc_sel=000 and gpio23_trad_tri=0) 0: Output data = 0 1: Output data = 1	RW	0
11	General Purpose Input Interrupt Pending	GPIO23 must be configured as a general purpose input and have interrupt generation enabled. 0: no interrupt event since the last time the register was read 1: an interrupt event has occurred clear on read	RO	0
10	General Purpose Input Status	Indicates the present value of the GPIO23 pin 0: Present value of GPIO23 pin is 0 1: Present value of GPIO23 pin is 1	RO	
9	Reserved		RW	0
8	Channel 1 TOSI Data Input Enable	0: Channel 1’s TOSI is disabled. 1: Enable use of this pin as channel 1’s TOSI Data Input. Pin must be configured as a general purpose input for these bit to serve a purpose.	RW	0

Table 119 • **GPIO 23 Config/ Status (1Ex012E)** ***(continued)***

Bit	Name	Description	Access	Default
7:5	GPIO23 WIS Interrupt Selection	Determines the WIS interrupt status transmitted from the pin when gpio23_pinfunc_sel=010 000: WIS interrupt A from channel 0 001: WIS interrupt A from channel 1 010: WIS interrupt A from channel 2 011: WIS interrupt A from channel 3 100: Logical AND of WIS interrupt A from all channels 101: Logical OR of WIS interrupt A from all channels 110: Reserved 111: Reserved	RW	000
4:3	GPIO23 Link Activity Selection	Determines which channel's link activity is transmitted from the pin when gpio23_pinfunc_sel=001 00: Rx link activity from channel 0 01: Rx link activity from channel 1 10: Rx link activity from channel 2 11: Rx link activity from channel 3	RW	00
2:0	GPIO23 Pin Function Selection	Selects the GPIO pin's functionality. 000: Traditional GPIO behavior 001: PCS activity LED output 010: WIS interrupt output 011: Transmit internal signals 100-111: Reserved	RW	101

Table 120 • **GPIO 23 Config2 (1Ex012F)**

Bit	Name	Description	Access	Default
15:7	Reserved		RW	0

Table 120 • **GPIO 23 Config2 (1Ex012F)** ***(continued)***

Bit	Name	Description	Access	Default
6:0	GPIO23 Internal Node Selection	Determines which channel's link activity is transmitted from the pin when gpio23_pinfunc_sel=011 0x7F to 0x6C: Reserved 0x6B: ch3_sw_los 0x6A: ch3_sw_losn 0x69: ch3_hw_los 0x68: ch3_hw_losn 0x67: ch2_sw_los 0x66: ch2_sw_losn 0x65: ch2_hw_los 0x64: ch2_hw_losn 0x63: ch1_sw_los 0x62: ch1_sw_losn 0x61: ch1_hw_los 0x60: ch1_hw_losn 0x5F to 0x58: Reserved 0x57: ch0_sw_los 0x56: ch0_sw_losn 0x55: ch0_hw_los 0x54: ch0_hw_losn 0x53: ref_cmu_loln 0x52 to 0x4C: Reserved 0x4B: ch1_txen_inverted 0x4A: ch1_txen 0x49: ch0_txen_inverted 0x48: ch0_txen 0x47: Reserved 0x46: Reserved 0x45: ch1_rxalarm 0x44: ch0_rxalarm 0x43: Reserved 0x42: Reserved 0x41: ch1_txalarm 0x40: ch0_txalarm 0x3F: Reserved 0x3E: Reserved 0x3D: ch1_lopc 0x3C: ch0_lopc 0x3B to 0x08: Reserved 0x07: ch1_pma_rxlol 0x06: ch1_pma_rxloln 0x05: ch0_pma_rxlol 0x04: ch0_pma_rxloln 0x03 to 0x00: Reserved	RW	0

Table 121 • **PMA Global Spare Control 0 (1Ex7F00)**

Bit	Name	Description	Access	Default
15:0	PMA Glob Spare Control0		RW	0

Table 122 • **PMA Global Spare Control 1 (1Ex7F01)**

Bit	Name	Description	Access	Default
15:0	PMA Glob Spare Control1		RW	0

Table 123 • **PMA Global Spare Status 0 (1Ex7F02)**

Bit	Name	Description	Access	Default
15:0	PMA Glob Spare Status		RO	0

Table 124 • **PMA Global Refclk Select (1Ex7F10)**

Bit	Name	Description	Access	Default
15:11	Reserved		RO	0
10	WREFCK Rate Select[1]	Selects rate of incoming WREFCK as either ~155.52 MHz (/64 rate) or ~622.08 MHz (/16 rate) 0: ~155.52 MHz (/64 rate) 1: ~622.08 MHz (/16 rate)	RW	0
9	SREFCK Rate Select[1]	Selects rate of incoming SREFCK as either ~155.52/156.25 MHz (/64 rate) or ~622.08/625 MHz (/16 rate) 0: ~155.52/156.25 MHz (/64 rate) 1: ~622.08/625MHz (/16 rate)	RW	0
8:6	Tx CMU Refclk Select 0	Selects Tx CMU reference clock source 0 (selectable by channel's device 1 address 8017 bits 3:1 = 00x) 00x: XREFCK from PAD 010: WREFCK from PAD 011: SREFCK from PAD 10x: XREFCK from CMU clkgen 110: WREFCK from CMU clkgen 111: SREFCK from CMU clkgen	RW	000
5:4	Tx CMU Refclk Select 1	Selects Tx CMU reference clock source 1 (selectable by channel's device 1 address 8017 bits 3:1 = 01x) 0x: XREFCK from PAD 10: WREFCK from PAD 11: SREFCK from PAD	RW	00
3:2	Rx Refclk Select 1	Selects Rx CRU reference clock source 1 (selectable by channel's device 1 address 8019 bit 5 = 1) 00: XREFCK from PAD 01: WREFCK/4 from PAD 10: WREFCK from PAD 11: SREFCK from PAD	RW	00

Table 124 • **PMA Global Refclk Select (1Ex7F10) *(continued)***

Bit	Name	Description	Access	Default
1:0	Rx Refclk Select 0	Selects Rx CRU reference clock source 0 (selectable by channel's device 1 address 8019 bit 5 = 0) 00: XREFCK from PAD 01: WREFCK/4 from PAD 10: WREFCK from PAD 11: SREFCK from PAD	RW	00

1. For more information about selecting the appropriate clock rate based on the recommended clock operating mode, see Table 23, page 24.

Table 125 • **PMA Global Refclk CMU Control (1Ex7F11)**

Bit	Name	Description	Access	Default
15:8	Reserved		RO	0
7	REFCLK CMU Loss of Lock Error	0: REFCLK CMU Lock Error 1: REFCLK CMU Lock	RO/LL	
6	REFCLK CMU Loss of Lock Error	0: REFCLK CMU Lock Error 1: REFCLK CMU Lock	RO	
4	Global CMU Refclk divide ratio	Selects /64 or /66 divide ratio for global CMU 0: div-by-64 1: div-by-66	RW	0
3	Global CMU Loop Bandwidth Control	0: 14 MHz 1: 7 MHz	RW	0
2:1	Global CMU Loop Bandwidth Override Control		RW	01
0	Global CMU Loop Bandwidth Override Select	0: Disable Override 1: Enable Override	RW	0

Table 126 • **Factory Test Register (1Ex7FD4)**

Bit	Name	Description	Access	Default
15:4	Reserved	Factory test only.	RO	0
3:0	Reserved	Factory test only. Do not modify this bit group.	RW	1000

Table 127 • **Temperature Monitor Threshold Settings (1Ex7FD5)**

Bit	Name	Description	Access	Default
15:8	High Temp Threshold Setting	Determines trigger for high temp alarm	RW	0xFF
7:0	Low Temp Threshold Setting	Determines trigger for low temp alarm	RW	0

Table 128 • **Temperature Monitor Regs (1Ex7FD6)**

Bit	Name	Description	Access	Default
15	Reserved	Reserved (Ignore when read)	RO	0
14	Disable Analog Temp Monitor	0: Analog Temperature Monitor Enable 1: Analog Temperature Monitor Disable	RW	1
13	Reserved	Reserved (Ignore when read)	RO	0
12	Enable Digital Temp Monitor	Enables the temperature monitor block 0: disable block 1: enable block goes to reference voltages and comparators	RW	0
11	Temp Monitor Run	0: Normal Operation 1: Initiates the temperature sampling process	RW SC	0
10	Temp Monitor Done Status	0: Temp sampling in progress. 1: Temperature Sampling Complete	RO/LH	0
9	High Temp Alarm	0: Temp is at or below high threshold setting 1: Temp is above high threshold setting	RO	
8	Low Temp Alarm	0: Temp is at or above low threshold setting 1: Temp is below low threshold setting	RO	
7:0	Temp Monitor Reading	This is the digital reading of the temperature monitor. Value is not valid unless = 'Temp Monitor Done'= status=1.	RO	

Table 129 • **Factory Test Only (1Ex7FD7)**

Bit	Name	Description	Access	Default
15:0	Reserved		RW	0

Note: Registers 1Ex7FD8 through 1Ex7FDF are reserved as "Spare Status" or for factory testing only.

Table 130 • **Checksum Control (1Ex7FE0)**

Bit	Name	Description	Access	Default
15:2	Reserved	Factory test only. Do not modify.	RW	All zeros
1	Checksum Done Status	Controlled by firmware. 0: Checksum routine is still running 1: Checksum routine is complete	RW[1]	0
0	Checksum Pass or Fail Status	Controlled by firmware. 0: Fail 1: Pass **Note:** The pass or fail status is not valid unless the checksum status in bit 1 reports 1.	RW[1]	0

1. Do not write to this bit.

Table 131 • **Watchdog Counter (1Ex7FE1)**

Bit	Name	Description	Access	Default
15:0	Watchdog Counter	Watchdog counter. Incremented by one through the firmware every 100 ms or less. Value rolls over to 0x0000 when 0xFFFF is incremented by one. **Note:** If the watchdog counter does not increment, the on-chip microprocessor is hung and needs to be reset. See Microcontroller Activity Monitoring, page 87.	RW	All zeros

Note: Registers from 1Ex7FE2 through 1Ex7FFF are reserved for factory testing only.

4.2 Channel Registers

This section provides information about the Channel registers.

Table 132 • **PMA_CTRL1: PMA Control 1 (1x0000)**

Bit	Name	Description	Access	Default
15	SOFT_RST	Reset all MMDs. 0: Normal operation. 1: Resets the entire channel.	RW SC	0
14	Reserved	Reserved (ignore when read)	RO	0
13	SPEED_SEL_A	Indicates whether the device operates at 10 Gbps and above 0: Unspecified 1: Operation at 10 Gbps and above	RO	1
12	Reserved	Reserved (ignore when read)	RO	0
11	LOW_PWR_PMA	0: Normal Operation. The internal TXEN signal will not be set to 0 due to the Low Power register bit. 1: Low Power Mode. Power dissipated in the core datapath, XAUI interface and PMA interface is reduced. The appropriate PMA connected to this channel is powered down when this bit is set. The PMA connected to this channel is a function of the datapath failover crosspoint control in global registers 1Ex0003.1 and 1Ex003.0. The internal TXEN signal will be 0. The TXEN signal can be routed out a GPIO pin to shut off the optics module's Tx driver if that is desirable. TXEN-inverted can also be transmitted from a GPIO pin.	RW	0
10:7	Reserved	Reserved (ignore when read)	RO	0
6	SPEED_SEL_B	Indicates whether the device operates at 10 Gbps and above 0: Unspecified 1: Operation at 10 Gbps and above	RO	1

Table 132 • **PMA_CTRL1: PMA Control 1 (1x0000)** ***(continued)***

Bit	Name	Description	Access	Default
5:2	SPEED_SEL_C	Speed selection 1xxx: Reserved x1xx: Reserved xx1x: Reserved 0001: Reserved 0000: 10 Gbps	RO	0
1	Reserved	Reserved (ignore when read)	RO	0
0	LPBK_J_PMA	PMA/WIS system loopback J 0: Disable 1: Enable SFI output transmits all zeros by default.	RW	0

Table 133 • **PMA_STAT1: PMA Status 1 (1x0001)**

Bit	Name	Description	Access	Default
15:8	Reserved	Reserved (ignore when read)	RO	0
7	FAULT	Indicates a fault condition on either the transmit or receive paths. 0: Fault condition not detected. (PMA receive local fault (1x0008.10) = 0) AND (PMA transmit local fault (1x0008.11) = 0) 1: Fault condition detected. (PMA receive local fault (1x0008.10) = 1) OR (PMA transmit local fault (1x0008.11) = 1)	RO	
6:3	Reserved	Reserved (ignore when read)	RO	0
2	Receive link status	0: PMA/PMD receive link down. Pma_rxloln=0 AND suppress_rxlol=0 1: PMA/PMD receive link up. Pma_loln=1 OR suppress_rxlol=1	RO/LL	
1	Low power ability	0: PMA/PMD does not support low power mode 1: PMA/PMD supports low power mode	RO	1
0	Reserved	Reserved (ignore when read)	RO	0

Table 134 • **PMA Device Identifier 1 (1x0002)**

Bit	Name	Description	Access	Default
15:0	Dev_ID_MSW	Upper 16 bits of a 32-bit unique PMA device identifier. Bits 3-18 of the device manufacturer's OUI.	RO	0x0007

Table 135 • **PMA Device Identifier 2 (1x0003)**

Bit	Name	Description	Access	Default
15:0	Dev_ID_LSW	Lower 16 bits of a 32-bit unique PMA device identifier. Bits 19-24 of the device manufacturer's OUI. Six-bit model number, and a four-bit revision number.	RO	0x0400

Table 136 • **PMA/PMD Speed Ability (1x0004)**

Bit	Name	Description	Access	Default
15:1	Reserved for future speeds	Value always 0, writes ignored.	RO	0
0	10G capable	0: PMA/PMD is not capable of operating at 10 Gbps 1: PMA/PMD is capable of operating at 10 Gbps	RO	1

Table 137 • **PMA/PMD Devices in Package (1x0005)**

Bit	Name	Description	Access	Default
15:6	Reserved	Ignore when read.	RO	0
5	DTE XS present	0: DTE XS not present in package 1: DTE XS present in package	RO	0
4	PHY XS present	0: PHY XS not present in package 1: PHY XS present in package	RO	1
3	PCS present	0: PCS not present in package 1: PCS present in package	RO	1
2	WIS present	0: WIS not present in package 1: WIS present in package	RO	1
1	PMD/PMA present	0: PMD/PMA not present in package 1: PMD/PMA present in package	RO	1
0	Clause 22 registers present	0: Clause 22 not registers present in package 1: Clause 22 registers present in package	RO	0

Table 138 • **PMA/PMD Devices in Package (1x0006)**

Bit	Name	Description	Access	Default
15	Vendor specific device 2 present	0: Vendor specific device 2 not present in package 1: Vendor specific device 2 present in package	RO	0
14	Vendor specific device 1 present	0: Vendor specific device 1 not present in package 1: Vendor specific device 1 present in package	RO	0
13:0	Reserved	Ignore when read.	RO	0

Table 139 • **PMA/PMD Control 2 (1x0007)**

Bit	Name	Description	Access	Default
15:3	Reserved		RO	
2:0	Vendor specific device 2 present	Indicates the PMA type selected 111: 10GBASE-SR 110: 10GBASE-LR 101: 10GBASE-ER 100: 10GBASE-LX-4 011: 10GBASE-SW 010: 10GBASE-LW 001: 10GBASE-EW 000 Reserved WAN mode is enabled when 10GBASE-SW, 10GBASE-LW or 10GBASE-EW is selected.	RW	111

Table 140 • **PMA/PMD Status 2 (1x0008)**

Bit	Name	Description	Access	Default
15:14	Device present	Reflects the presence of a MMD responding at this address. 00: No device responding at this address. 01: No device responding at this address. 10: Device responding at this address. 11: No device responding at this address.	RO	10
13	Transmit fault ability	0: PMA/PMD does not have the ability to detect a fault condition on the transmit path 1: PMA/PMD has the ability to detect a fault condition on the transmit path	RO	1
12	Receive fault ability	0: PMA/PMD does not have the ability to detect a fault condition on the receive path 1: PMA/PMD has the ability to detect a fault condition on the receive path	RO	1
11	Transmit fault	0: No fault condition on transmit path. 1: Fault condition on transmit path.	RO/LH	
10	Receive fault	0: No fault condition on receive path. 1: Fault condition on receive path.	RO/LH	
9	Reserved	Ignore when read.	RO	0
8	PMD transmit disable ability	0: PMD does not have the ability to disable the transmit path 1: PMD has the ability to disable the transmit path	RO	1
7	10GBASE-SR ability	0: PMA/PMD is not able to perform 10GBASE-SR 1: PMA/PMD is able to perform 10GBASE-SR	RO	1
6	10GBASE-LR ability	0: PMA/PMD is not able to perform 10GBASE-LR 1: PMA/PMD is able to perform 10GBASE-LR	RO	1

Table 140 • **PMA/PMD Status 2 (1x0008)** ***(continued)***

Bit	Name	Description	Access	Default
5	10GBASE-ER ability	0: PMA/PMD is not able to perform 10GBASE-ER 1: PMA/PMD is able to perform 10GBASE-ER	RO	1
4	10GBASE-LX4 ability	0: PMA/PMD is not able to perform 10GBASE-LX4 1: PMA/PMD is able to perform 10GBASE-LX4	RO	0
3	10GBASE-SW ability	0: PMA/PMD is not able to perform 10GBASE-SW 1: PMA/PMD is able to perform 10GBASE-SW	RO	1
2	10GBASE-LW ability	0: PMA/PMD is not able to perform 10GBASE-LW 1: PMA/PMD is able to perform 10GBASE-LW	RO	1
1	10GBASE-EW ability	0: PMA/PMD is not able to perform 10GBASE-EW 1: PMA/PMD is able to perform 10GBASE-EW	RO	1
0	PMA loopback ability	0: PMA does not have the ability to perform a loopback function 1: PMA has the ability to perform a loopback function	RO	1

Table 141 • **PMD Transmit Disable (1x0009)**

Bit	Name	Description	Access	Default
15:5	Reserved	Value always 0, writes ignored.	RO	0
4	PMD transmit disable 1	Value always 0, writes ignored.	RO	0
3	Reserved	Value always 0, writes ignored.	RO	0
2	Reserved	Value always 0, writes ignored.	RO	0
1	PMD transmit disable 0	Value always 0, writes ignored.	RO	0
0	Global PMD transmit disable	0: Transmit enabled. The internal TXEN signal will not be set to 0 due to this register bit. 1: Transmit disabled. The internal TXEN signal will be 0. The TXEN signal can be routed out a GPIO pin to shut off the optics module's Tx driver if that is desirable. TXEN-inverted can also be transmitted from a GPIO pin. The internal TXEN signal is also 0 when the channel is in low power mode. The TXEN output for this channel is a function of the datapath failover crosspoint control in global registers 1Ex0003.1 and 1Ex003.0. The optics module disabled when this bit is set is the optics module associated with this channel's datapath.	RW	0

Table 142 • **PMD Receive Signal Detect (1x000A)**

Bit	Name	Description	Access	Default
15:5	Reserved	Value always 0, writes ignored.	RO	0
4	PMD receive signal detect 3	Do not support this function, value always 0	RO	0
3	PMD receive signal detect 2	Do not support this function, value always 0	RO	0
2	PMD receive signal detect 1	Do not support this function, value always 0	RO	0
1	PMD receive signal detect 0	Do not support this function, value always 0	RO	0
0	Global PMD receive signal detect	0: Signal not detected on receive. 1: Signal detected on receive.	RO	

Table 143 • **PMA/PMD Package Identifier (1x000E)**

Bit	Name	Description	Access	Default
15:0	PKG_ID_MSW	Upper 16 bits of a 32-bit unique PMA package identifier. Bits 3-18 of the device manufacturer's OUI.	RO	0

Table 144 • **PMA/PMD Package Identifier (1x000F)**

Bit	Name	Description	Access	Default
15:0	PKG_ID_LSW	Lower 16 bits of a 32-bit unique PMA package identifier. Bits 19-24 of the device manufacturer's OUI. Six-bit model number, and a four-bit revision number.	RO	0

Table 145 • **KR Training Control (1x0096)**

Bit	Name	Description	Access	Default
15:2	Reserved		RO	0
1	KR Training Enable	0: Training disabled 1: Training enabled	RW	0
0	KR Restart Training	0: No Op 1: Restart training	RW SC	0

Table 146 • **KR Training Status (1x0097)**

Bit	Name	Description	Access	Default
15:4	Reserved		RO	0
3	Training Failure	0: No Failure 1: Failure	RO	

Table 146 • **KR Training Status (1x0097) *(continued)***

Bit	Name	Description	Access	Default
2	Startup protocol status	0: Not training 1: Actively training	RO	
1	Frame Lock	0: No frame lock 1: Frame lock	RO	
0	Receiver Status	0: Not trained 1: Trained	RO	

Table 147 • **KR Training LP Coeff Update (1x0098)**

Bit	Name	Description	Access	Default
15:14	Reserved		RO	0
13	Preset	0: Normal operation 1: Preset coefficients	RO[1]	
12	Initialize	0: Normal operation 1: Initialize coefficients	RO[1]	
11:6	Reserved		RO	0
5:4	Coefficient (+1) update		RO[1]	
3:2	Coefficient (0) update		RO[1]	
1:0	Coefficient (-1) update		RO[1]	

1. RO when 1x0096.1 = 1. RW when 1x0096.1 = 0.

Table 148 • **KR Training LP Status Report (1x0099)**

Bit	Name	Description	Access	Default
15	Receiver ready	0: LP receiver is requesting that training continue 1: LP receiver has determined training is complete and is prepared to receive data	RO	
14:6	Reserved		RO	0
5:4	Coefficient (+1) status		RO	
3:2	Coefficient (0) status		RO	
1:0	Coefficient (-1) status		RO	

Table 149 • **KR Training LD Coeff Update (1x009A)**

Bit	Name	Description	Access	Default
15:14	Reserved		RO	0
13	Preset	0: Normal operation 1: Preset coefficients	RO	
12	Initialize	0: Normal operation 1: Initialize coefficients	RO	

Table 149 • **KR Training LD Coeff Update (1x009A) *(continued)***

Bit	Name	Description	Access	Default
11:6	Reserved		RO	0
5:4	Coefficient (+1) update		RO	
3:2	Coefficient (0) update		RO	
1:0	Coefficient (-1) update		RO	

Table 150 • **KR Training LD Status Report (1x009B)**

Bit	Name	Description	Access	Default
15	Receiver ready	0: LD receiver is requesting that training continue 1: LD receiver has determined training is complete and is prepared to receive data	RO	
14:6	Reserved		RO	0
5:4	Coefficient (+1) status		RO	
3:2	Coefficient (0) status		RO	
1:0	Coefficient (-1) status		RO	

Table 151 • **KR Training Status (from Firmware) (1x8097)**

Bit	Name	Description	Access	Default
15:4	Reserved		RO	0
3	Training Failure	0: No Failure 1: Failure	RW	0
2	Startup protocol status	0: Not training 1: Actively training	RW	0
1	Reserved		RO	0
0	Receiver Status	0: Not trained 1: Trained	RW	0

Table 152 • **KR Training LD Coeff Update (from Firmware) (1x809A)**

Bit	Name	Description	Access	Default
15:14	Reserved		RO	0
13	Preset	0: Normal operation 1: Preset coefficients	RW	0
12	Initialize	0: Normal operation 1: Initialize coefficients	RW	0
11:6	Reserved		RO	0
5:4	Coefficient (+1) update		RW	0
3:2	Coefficient (0) update		RW	0
1:0	Coefficient (-1) update		RW	0

Table 153 • **KR Training Control 2 (1x8201)**

Bit	Name	Description	Access	Default
15:8	Reserved		RO	0
7	Local Receiver ready	0: Local receiver still training 1: Local receiver is trained.	RW	0
6	Tx prbs11 invert	0: no inversion 1: Invert transmitted prbs11 training pattern	RW	0
5	Rx prbs11 invert	0: no inversion 1: Invert received prbs11 training pattern	RW	0
4	Training Done	0: Actively training 1: Training done	RW	0
3	wait_timer_start	1: Initialize timer to maxval, and start counting down	RW SC	0
2	max_wait_timer_start	1: Initialize timer to maxval, and start counting down	RW SC	0
1	tr_coef_ready	0: LD Coeff update reg is not ready to transmit 1: LD Coeff update register (1x809A) is stable and ready for transmission	RW	0
0	Enable training pattern error detector	0: Disabled 1: Enabled	RW	0

Table 154 • **KR Training Status 2 (1x8208)**

Bit	Name	Description	Access	Default
15:5	Reserved		RO	0
4	frame_transmit_done	1: Training frame has completed transmission	RO/LH	0
3	wait_timer_done	0: Timer was never started, or is still counting down 1: Timer counted down to zero	RO/LH	0
2	max_wait_timer_done	0: Timer was never started, or is still counting down 1: Timer counted down to zero	RO/LH	0
1	DME violation detect	0: No DME violation detected 1: A DME violation has been detected	RO/LH	0
0	BER Busy	0: Idle 1: Rx Training is actively counting frames and bit errors within training pattern	RO	0

Table 155 • **KR Training Pattern Error Count (1x8209)**

Bit	Name	Description	Access	Default
15:0	Bit Error Count		RO	0

Table 156 • **KR Training Frames Counted (1x820A)**

Bit	Name	Description	Access	Default
15:0	Frames counted		RO	0

Table 157 • **KR Training Frames to Count (1x820B)**

Bit	Name	Description	Access	Default
15:0	Frames to count		RW	0

Table 158 • **KR Training wait_timer Setting (1x820C)**

Bit	Name	Description	Access	Default
15:0	wait_timer		RW	0x19F1

Table 159 • **KR Training max_wait_timer Setting 1 (1x820D)**

Bit	Name	Description	Access	Default
15:0	max_wait_timer[15:0]	Lower 16 bits of 32-bit programmable timer	RW	0x0BE4

Table 160 • **KR Training max_wait_timer Setting 2 (1x820E)**

Bit	Name	Description	Access	Default
15:0	max_wait_timer[31:16]	Upper 16 bits of 32-bit programmable timer	RW	0x0254

Table 161 • **KR FEC Ability (1x00AA)**

Bit	Name	Description	Access	Default
15:2	Reserved		RO	0
1	FEC error indication ability	0: This PHY device is not able to report FEC decoding errors to the PCS layer. 1: This PHY device is able to report FEC decoding errors to the PCS layer.	RO	1
0	FEC ability	0: This PHY device does not support FEC. 1: This PHY device supports FEC.	RO	1

Table 162 • **KR FEC Control 1 (1x00AB)**

Bit	Name	Description	Access	Default
15:2	Reserved		RO	0

Table 162 • **KR FEC Control 1 (1x00AB) *(continued)***

Bit	Name	Description	Access	Default
1	FEC enable error indication	0: Decoding errors have no effect on PCS sync bits 1: Enable decoder to indicate errors to PCS sync bits	RW	1
0	FEC enable	0: Disable FEC 1: Enable FEC	RW	0

Table 163 • **KR FEC Corrected Lower (1x00AC)**

Bit	Name	Description	Access	Default
15:0	FEC corrected blocks lower		RO CR	0

Table 164 • **KR FEC Corrected Upper (1x00AD)**

Bit	Name	Description	Access	Default
15:0	FEC corrected blocks upper		RO CR	0

Table 165 • **KR FEC Uncorrected Lower (1x00AE)**

Bit	Name	Description	Access	Default
15:0	FEC uncorrected blocks lower		RO CR	0

Table 166 • **KR FEC Uncorrected Upper (1x00AF)**

Bit	Name	Description	Access	Default
15:0	FEC uncorrected blocks upper		RO CR	0

Table 167 • **KR FEC Control 2 (1x8300)**

Bit	Name	Description	Access	Default
15:2	Reserved		RO	0
1	fec_inframe	0: FEC has not achieved lock 1: FEC has achieved lock	RO/LL	
0	fec_rstmon	0: no effect 1: reset FEC counters	RW	0

Table 168 • **PMA_reset_LH (1x8000)**

Bit	Name	Description	Access	Default
15	Latch High of pma_ieee_reset		RO/LH	0
14:0	Reserved		RO	0

Table 169 • **PMA_TXSTAT: PMA Tx Status (1x8001)**

Bit	Name	Description	Access	Default
15:5	Reserved	Reserved (Ignore when read)	RO	0
4	Tx CMU Loss Of Lock Error	0: Tx CMU Lock Error 1: Tx CMU Lock	RO/LL	
3	FIFO Error	0: FIFO Overflow 1: FIFO Normal Only valid when in loopback K (ignore for normal operation)	RO/LL	
2:1	Reserved	Reserved (Ignore when read)	RO	0
0	Tx CMU Loss Of Lock Error	0: Tx CMU Lock Error 1: Tx CMU Lock	RO	

Table 170 • **PMA_RXSTAT: PMA Rx Status (1x8002)**

Bit	Name	Description	Access	Default
15:3	Reserved	Reserved (Ignore when read)	RO	0
2	DC Offset Sign Output	0: DC Offset Negative 1: DC Offset Positive	RO	
1	Rx Loss of Lock Error	0: Rx CRU Lock Error 1: Rx CRU Lock	RO/LL	
0	Rx Loss of Lock Error	0: Rx CRU Lock Error 1: Rx CRU Lock	RO	

Table 171 • **PMA_RXEDCCTRL: PMA Rx EDC Control (1x8003)**

Bit	Name	Description	Access	Default
15:14	Reserved	Reserved (Ignore when read)	RO	0
4:1	Reserved	Reserved (Ignore when read)	RO	0
0	Rx CRU Lock to Ref	Rx CRU Lock to Ref 0: CRU to lock to data 1: Force CRU to lock to reference	RW	0

Table 172 • **PMA_RXDATACTRL: PMA Rx Data Control (1x8004)**

Bit	Name	Description	Access	Default
15:5	Reserved	Reserved (Ignore when read)	RO	0
4	Rx Receive Data MSB Select	Swaps MSB of 64-bit bus 0: Disabled (MSB first). Bit 63 is MSB 1: Enabled (LSB first). Bit 0 is MSB	RW	1
3	Rx Receive Manual Data Squelch	Squelches 64-bit bus 0: Normal 1: Squelched	RW	0
2	Rx Receive Data Polarity Invert	Inverts Polarity on 64-bit bus 0: Normal 1: Inverted	RW	0
1:0	Reserved	Reserved (Ignore when read)	RO	0

Table 173 • **PMA_FIFOCTRL: PMA FIFO Control (1x8011)**

Bit	Name	Description	Access	Default
15:1	Reserved	Reserved (Ignore when read)	RO	0
0	TXFIFO_SYNCH INHIBIT	FIFO Synch Inhibit 0: Disabled 1: Enabled	RW	0

Table 174 • **PMA_TXDATACTRL: PMA Tx Data Control (1x8012)**

Bit	Name	Description	Access	Default
15:5	Reserved	Reserved (Ignore when read)	RO	0
4	PMA_Serial_Loopback	0: Enables loopback K. 1: Disable loopback K.	RW	1
3	TXOUT_INV	Tx Transmit Data Polarity Invert 0: Normal 1: Inverted	RW	0
2	TXOUT_MSBSEL	Tx Transmit Data MSB Select 0: No bit swapping enabled (MSB first) Bit 63 is MSB 1: Bit swapping enabled (LSB first) Bit 0 is MSB	RW	1
1	Tx Transmit Manual Data Squelch	Tx Transmit Manual Data Squelch 0: Normal 1: Squelched	RW	0
0	Reserved	Reserved (Ignore when read)	RO	1

Table 175 • **PMA_TXOUTCTRL1: PMA Tx Output Driver Control 1 (1x8013)**

Bit	Name	Description	Access	Default
15:12	Reserved	Factory Test Only. Do Not Modify	RW	0
11:8	TXOUT_SLEW_CTRL	Tx Output Driver Slew Rate Control 0: Minimum F: Maximum	RW	0xA
7:5	Reserved	Factory Test Only. Do Not Modify	RW	0
4:0	C(-1) Tap Control	Tx Output Driver C(-1) Coefficient Control 00000: Minimum (-4mA) 11111: Maximum (+4mA)	RW	01111

Table 176 • **PMA_TXOUTCTRL2: PMA Tx Output Driver Control 2 (1x8014)**

Bit	Name	Description	Access	Default
15:13	Reserved	Factory Test Only. Do Not Modify	RW	0
12:8	C(0) Tap Control	Tx Output Driver C(0) Coefficient Control 00000: Minimum (0mA) 11111: Maximum (+16mA)	RW	10011
7:6	Reserved	Factory Test Only. Do Not Modify	RW	0
5:0	C(+1) Tap Control	Tx Output Driver C(+1) Coefficient Control 000000: Minimum (-0.25mA) 111111: Maximum (-16mA)	RW	0

Table 177 • **PMA_TXRATECTRL: PMA Tx Rate Control (1x8015)**

Bit	Name	Description	Access	Default
15:8	Reserved	Reserved (Ignore when read)	RO	0
7:5	Reserved	Reserved (Ignore when read)	RO	001
4:1	Reserved	Reserved (Ignore when read)	RO	0000

Table 178 • **PMA_TXRATECTRL: PMA Tx Rate Control (1x8017)**

Bit	Name	Description	Access	Default
15:6	Reserved	Reserved (Ignore when read)	RO	0
5:4	CMU Varclk Select Bit	CMU Varclk Select Bit 00: /66 01: /64 10: /16 11: /48	RW	00

Table 178 • **PMA_TXRATECTRL: PMA Tx Rate Control (1x8017) *(continued)***

Bit	Name	Description	Access	Default
3:1	CMU Reference Clock Select Bit	CMU Reference Clock Select Bit 00x: CMU0 Refclk Path 01x: CMU1 Refclk Path 1x0: Rx CDR 1x1: XAUI CDR	RW	010
0	Reserved	Reserved (Ignore when read)	RO	0

Table 179 • **PMA_TXRATECTRL: PMA Tx Rate Control (1x8018)**

Bit	Name	Description	Access	Default
15:8	Reserved	Reserved (Ignore when read)	RO	0
7:6	Tx Transmit Slew Control	Selects proper slew rate for 10G and 1G data rates 00: 10G 01: reserved 10: reserved 11: 1G	RW	00
5:2	Reserved	Reserved (Ignore when read)	RO	0

Table 180 • **PMA_RXRATECTRL: PMA Rx Rate Control (1x8019)**

Bit	Name	Description	Access	Default
15:7	Reserved	Reserved (Ignore when read)	RO	0
6:5	Rx Reference Clock Select	Selects Rx Reference Clock Source x0: CRU0 clock path x1: CRU1 clock path	RW	00
4:3	Rx Reference Clock Rate	Selects Rx Reference Clock Rate 00: /64 01: /66 1x: /60	RW	01
2:1	Rx Data Rate	Selects Rx Data Rate 00: 10G 01: reserved 1x: 1G	RW	00
0	Reserved	Reserved (Ignore when read)	RO	0

Table 181 • **Factory Test Register (1x8030)**

Bit	Name	Description	Access	Default
15:12	Reserved	Factory test only.	RO	0
11:0	Reserved	Factory test only.	RO	0

Table 182 • **Factory Test Register (1x8031)**

Bit	Name	Description	Access	Default
15:2	Reserved	Factory test only.	RO	0
1:0	Reserved	Factory test only.	RO	0

Table 183 • **Factory Test Register (1x8034)**

Bit	Name	Description	Access	Default
15:0	Reserved	Factory test only. Do not modify this bit group.	RW	0

Table 184 • **Factory Test Register (1x8035)**

Bit	Name	Description	Access	Default
15:3	Reserved	Factory test only. Do not modify this bit group.	RW	0
2	Reserved	Factory test only. Do not modify this bit group.	RW	0
1:0	Reserved	Factory test only. Do not modify this bit group.	RW	0

Table 185 • **Factory Test Register (1x8036)**

Bit	Name	Description	Access	Default
15:0	Reserved	Factory test only. Do not modify this bit group.	RW	0

Table 186 • **Factory Test Register (1x8037)**

Bit	Name	Description	Access	Default
15:0	Reserved	Factory test only. Do not modify this bit group.	RW	0

Table 187 • **Factory Test Register (1x8038)**

Bit	Name	Description	Access	Default
15:0	Reserved	Factory test only. Do not modify this bit group.	RW	0

Table 188 • **Factory Test Register (1x8039)**

Bit	Name	Description	Access	Default
15:0	Reserved	Factory test only. Do not modify this bit group.	RW	0

Table 189 • **Factory Test Register (1x803A)**

Bit	Name	Description	Access	Default
15:0	Reserved	Factory test only. Do not modify this bit group.	RW	0

Table 190 • **Factory Test Register (1x803B)**

Bit	Name	Description	Access	Default
15:0	Reserved	Factory test only. Do not modify this bit group.	RW	0

Table 191 • **LOS Status (1x8141)**

Bit	Name	Description	Access	Default
15:2	Reserved	Reserved (Ignore when read)	RO	0
1	Hardware LOS Status	Hardware LOS detect using amplitude measurement method. Status is valid only when hardware LOS detection is enabled in 1xB0C0.2. 0: No LOS condition detected. 1: LOS condition detected.	RO	
0	Software EDC CRU LOS	Indicates when the software has detected a loss-of-signal condition at the input to the EDC's CRU. This is the signal on the RXIN input to the EDC. The software contains this LOS detection only in copper connect applications where there is no optics module present to drive the chip's LOPC input. 0: No LOS condition detected. 1: LOS condition detected.	RO	

Table 192 • **LOS_Detection_Source (1x8142)**

Bit	Name	Description	Access	Default
15:2	Reserved	Reserved (Ignore when read)	RO	0
1:0	LOS Detection Source	Selects the source of the LOS signal that drive the Rx WIS framer 00: hardware LOS detection logic 01: Software LOS detection 10: Continuously force LOS alarm state 11:Squelch LOS alarm state	RW	00

Table 193 • **Factory Test Register (1x8151)**

Bit	Name	Description	Access	Default
15:1	Reserved	Factory test only.	RO	0

Table 193 • **Factory Test Register (1x8151) *(continued)***

Bit	Name	Description	Access	Default
0	Reserved	Factory test only.	RW	1

Table 194 • **Driver Coeff PRESET Settings for CM1 (1x8210)**

Bit	Name	Description	Access	Default
15:8	Reserved		RO	0
7:0	cm1 Training PRESET setting		RW	0x0F

Table 195 • **Driver Coeff PRESET Settings for C0 and CP1 (1x8211)**

Bit	Name	Description	Access	Default
15:8	c0 Training PRESET setting		RW	0x1F
7:0	cp1 Training PRESET setting		RW	0x00

Table 196 • **Driver Coeff INITIALIZE Settings for CM1 (1x8212)**

Bit	Name	Description	Access	Default
15:8	Reserved		RO	0
7:0	cm1 Training INITIALIZE setting		RW	0x0B

Table 197 • **Driver Coeff INITIALIZE Settings for C0 and CP1 (1x8213)**

Bit	Name	Description	Access	Default
15:8	c0 Training INITIALIZE setting		RW	0x1F
7:0	cp1 Training INITIALIZE setting		RW	0x1B

Table 198 • **Driver Coeff Step Size (1x8214)**

Bit	Name	Description	Access	Default
15:6	Reserved		RO	0
5:4	cp1 step size		RW	0x1
3:2	c0 step size		RW	0x1
1:0	cm1 step size		RW	0x1

Table 199 • **RX_ALARM Control Register (1x9000)**

Bit	Name	Description	Access	Default
15:11	Reserved	For future use.	RO	0
10	Vendor Specific	0: Disable 1: Enable	RW	0
9	WIS Local Fault Enable	0: Disable 1: Enable	RW	1
8:5	Vendor Specific	0: Disable 1: Enable	RW	0
4	PMA/PMD Receiver Local Fault Enable	0: Disable 1: Enable	RW	1
3	PCS Receive Local Fault Enable	0: Disable 1: Enable	RW	1
2:1	Vendor Specific	0: Disable 1: Enable	RW	0
0	PHY XS Receive Local Fault Enable	0: Disable 1: Enable	RW	0

Table 200 • **TX_ALARM Control Register (1x9001)**

Bit	Name	Description	Access	Default
15:11	Reserved	For future use.	RO	0
10:5	Vendor Specific	0: Disable 1: Enable	RW	0
4	PMA/PMD Transmitter Local Fault Enable	0: Disable 1: Enable	RW	1
3	PCS Transmit Local Fault Enable	0: Disable 1: Enable	RW	1
2:1	Vendor Specific	0: Disable 1: Enable	RW	0
0	PHY XS Transmit Local Fault Enable	0: Disable 1: Enable	RW	1

Table 201 • **RX_ALARM Status Register (1x9003)**

Bit	Name	Description	Access	Default
15:11	Reserved	Ignore when read.	RO	0
10	Vendor Specific	For future use.	RO	0
9	WIS Local Fault	0: No WIS Local Fault 1: WIS Local Fault	RO/LH	
8:5	Vendor Specific	For future use.	RO	0

Table 201 • **RX_ALARM Status Register (1x9003)** ***(continued)***

Bit	Name	Description	Access	Default
4	PMA/PMD Receiver Local Fault	0: No PMA/PMD Receiver Local Fault 1: PMA/PMD Receiver Local Fault link to 1.8.10	RO/LH	
3	PCS Receive Local Fault	0: No PCS Receive Local Fault 1: PCS Receive Local Fault link to 3.8.10	RO/LH	
2:1	Vendor Specific	For future use.	RO	0
0	PHY XS Receive Local Fault	0: No PHY XS Receive Local Fault 1: PHY XS Receive Local Fault link to 4.8.10	RO/LH	

Table 202 • **TX_ALARM Status Register (1x9004)**

Bit	Name	Description	Access	Default
15:11	Reserved	Ignore when read.	RO	0
10:5	Vendor Specific	For future use.	RO	0
4	PMA/PMD Transmitter Local Fault	0: No PMA/PMD Transmitter Local Fault 1: PMA/PMD Transmitter Local Fault link to 1.8.11	RO/LH	
3	PCS Transmit Local Fault	0: No PCS Transmit Local Fault 1: PCS Transmit Local Fault link to 3.8.11	RO/LH	
2:1	Vendor Specific	For future use.	RO	0
0	PHY XS Transmit Local Fault	0: No PHY XS Transmit Local Fault 1: PHY XS Transmit Local Fault link to 4.8.11	RO/LH	

Table 203 • **Rx Clock Output Control (1xA008)**

Bit	Name	Description	Access	Default
15:5	Reserved		RO	0
4	PMA Rx Clock Output Swing	0: Half amplitude swing 1: Full amplitude swing	RW	0
3	Enable Rx Clock Output	0: Rx Clock Output Disable 1: Rx Clock Output Enable	RW	0
2:0	Rx Clock Output Select	000: RESERVED 001: Rx CDR /64 010: Tx CMU /64 011: Tx CMU /66 100: XAUI CMU VARCLK 101: RESERVED 110: Rx CDR /60 111: RESERVED	RW	000

Table 204 • **Tx Clock Output Control (1xA009)**

Bit	Name	Description	Access	Default
15:5	Reserved		RO	0
4	PMA Tx Clock Output Swing	0: Half amplitude swing 1: Full amplitude swing	RW	0
3	Enable Tx Clock Output	0: Tx Clock Output Disable 1: Tx Clock Output Enable	RW	0
2:0	Tx Clock Output Select	000:Tx CMU /64 001: Tx CMU /66 010: RESERVED 011: Rx CDR /64 10x: Tx CMU REFCLK copy 110: Rx CDR CRU copy 111: XAUI recovered clock	RW	000

Table 205 • **Vendor Specific PMA Control 2 (1xA100)**

Bit	Name	Description	Access	Default
15	wis_intb_activeh	0: WIS_INTB is active low 1: WIS_INTB is active high	RW	0
14	wis_inta_activeh	0: WIS_INTA is active low 1: WIS_INTA is active high	RW	0
13	Reserved		RO	0
12	Disable low pwr rst timer	0: Enable low power reset timer 1: Disable low power reset timer	RW	0
11	Reserved		RO	0
10	Reserved		RO	0
9	Suppress LOL detection	0: Allow LOL detection 1: Suppress LOL detection	RW	0
8	TX_LED_BLINK_TIME	Tx data activity LED blink time 0: 50ms interval 1: 100ms interval	RW	1
7	RX_LED_BLINK_TIME	Rx data activity LED blink time 0: 50ms interval 1: 100ms interval	RW	1
6:5	TX_LED_MODE	Tx LED mode control 00: Display Tx link status 01: Reserved 10: Display combination of Tx link and data activity status 11: Reserved.	RW	10
4:3	RX_LED_MODE	Rx LED mode control 00: Display Rx link status 01: Reserved 10: Display combination of Rx link and data activity status 11: Reserved.	RW	10

Table 205 • **Vendor Specific PMA Control 2 (1xA100)** ***(continued)***

Bit	Name	Description	Access	Default
2	Override system loopback data	0: Data sent out XFI output matches default. 1: Use PMA system loopback data select to select XFI output data.	RW	0
1:0	PMA system loopback data select	When Override system loopback data (1xA100.2) is set and the data channel is in 10G mode, the data transmitted from Tx PMA is determined by these register bits. The data transmitted is 00: repeating 0x00FF pattern 01: continuously send 0's 10: continuously send 1's 11: data from Tx WIS block	RW	0

Table 206 • **Vendor Specific PMA Status 2 (1xA101)**

Bit	Name	Description	Access	Default
15:4	Reserved	Value always 0, writes ignored.	RO	0
3	WAN_ENABLED status	0: Not in Wan Mode 1: WAN Mode	RO	0
2	WIS_INTA pin status	0: WIS_INTA pin is low 1: WIS_INTA pin is high	RO	
1	WIS_INTB pin status	0: WIS_INTB pin is low 1: WIS_INTB pin is high	RO	
0	PMTICK pin status	0: PMTICK pin is low 1: PMTICK pin is high	RO	

Table 207 • **Vendor Specific LOPC Status (1xA200)**

Bit	Name	Description	Access	Default
15:3	Reserved	Value always 0, writes ignored.	RO	0
2	Present state of the LOPC pin, taking into account the lopc_invert regbit	0: LOPC pin is low when lopc_invert=0, LOPC is high when lopc_invert=1 1: LOPC pin is high when lopc_invert=0, LOPC is low when lopc_invert=1	RO	
1	Present state of the LOPC pin. Does not take into account the lopc_invert regbit	0: LOPC pin is low 1: LOPC pin is high	RO	
0	Interrupt pending bit	0: An interrupt event has not occurred since the last time this bit was read 1: An interrupt event determined by lopc_intr_mode has occurred	RO CR	0

Table 208 • **Vendor Specific LOPC Control (1xA201)**

Bit	Name	Description	Access	Default
15:3	Reserved	Value always 0, writes ignored.	RO	0
2	LOPC state inversion select	0: The part is in a LOPC alarm state when the LOPC pin is logic low. 1: The part is in a LOPC alarm state when the LOPC pin is logic high.	RW	0
1:0	lopc_intr_pend bit select	This bit group determines how the LOPC interrupt pending register in 1xA200.0 is asserted. 00: interrupt generation is disable 01: lopc_intr_pend is set on a rising edge of the LOPC pin, regardless of the lopc_invert setting 10: lopc_intr_pend is set on a falling edge of the LOPC pin, regardless of the lopc_invert setting 11: lopc_intr_pend is set on both edges of the LOPC pin	RW	0

Table 209 • **Reset (1xAE00)**

Bit	Name	Description	Access	Default
15:13	Reserved	Value always 0, writes ignored.	RO	0
12	Tx 1G reset	0: Normal operation 1: Tx 1G reset	RW SC	0
11	Rx 1G reset	0: Normal operation 1: Rx 1G reset	RW SC	0
10	PMA block reset	0: Normal operation 1: PMA block reset	RW SC	0
9	PMA FIFO reset	0: Normal operation 1: PMA FIFO reset	RW SC	0
8	Tx WIS reset	0: Normal operation 1: WIS Tx path reset	RW SC	0
7	Tx WIS FIFO reset	0: Normal operation 1: Tx WIS FIFO reset	RW SC	0
6	Tx WIS FIFO pointer reset	0: Normal operation 1: Tx WIS FIFO pointer reset	RW SC	0
5	Reset WIS interrupt tree	0: Normal operation 1: Reset WIS interrupt tree	RW SC	0
4	Rx WIS FIFO reset	0: Normal operation 1: Rx WIS FIFO reset	RW SC	0
3	Rx WIS reset	0: Normal operation 1: WIS Rx path reset	RW SC	0
2	PCS Tx reset	0: Normal operation 1: PCS Tx path reset	RW SC	0
1	PCS Rx reset	0: Normal operation 1: PCS Rx path reset	RW SC	0

Table 209 • **Reset (1xAE00)** ***(continued)***

Bit	Name	Description	Access	Default
0	Reserved		RO	0

Table 210 • **WIS_CTRL1: WIS Control 1 (2x0000)**

Bit	Name	Description	Access	Default
15	SOFT_RST	Reset all MMDs. 0: Normal operation. 1: Resets the entire channel.	RW SC	0
14	LPBK_J	Enables WIS system loopback (loopback†J). 0: Disable. 1: Enable.	RW	0
13	SPEED_SEL_A	WIS speed capability. 0: Unspecified 1: Operates at 10 Gbps or above.	RO	1
12	Reserved	Reserved	RO	0
11	LOW_PWR_WIS	Enter low power mode. 0: Normal Operation. The internal TXEN signal will not be set to 0 due to the Low Power register bit. 1: Low Power Mode. Power dissipated in the core datapath, XAUI interface and PMA interface is reduced. The appropriate PMA connected to this channel is powered down when this bit is set. The PMA connected to this channel is a function of the datapath failover crosspoint control in global registers 1Ex0003.1 and 1Ex003.0. The internal TXEN signal will be 0. The TXEN signal can be routed out a GPIO pin to shut off the optics module's Tx driver if desired. The inverted TXEN signal may also be transmitted from a GPIO pin.	RW	0
10:7	Reserved	Reserved	RO	0
6	SPEED_SEL_B	WIS speed capability. 0: Unspecified 1: Operates at 10 Gbps or above.	RO	1
5:2	SPEED_SEL_C	WIS speed selection. WIS speed selection. 1xxx: Reserved. x1xx: Reserved. xx1x: Reserved. 0001: Reserved. 0000: 10 Gbps.	RO	0
1:0	Reserved	Reserved	RO	0

Table 211 • **WIS_STAT1: WIS Status 1 (2x0001)**

Bit	Name	Description	Access	Default
15:8	Reserved		RO	00000000
7	FAULT	WIS fault status. The alarm conditions that cause the WIS fault status to be asserted are configured in the WIS_FAULT_MASK (2xEE07). Based on the 2xEE07 setting, the WIS fault status can be asserted when the following alarm conditions exist: OOF, LOS, LOF, LOP-P, AIS-L, AIS-P, LCD-P, PLM-P, RDI-L, far-end AIS-P and far-end PLM-P. 0: No faults asserted. 1: Fault asserted.	RO/LH	0
6:3	Reserved	Reserved	RO	0000
2	LNK_STAT	WIS receive link status. Link up means no AIS-P, AIS-L, PLM-P, or SEF alarms 0: WIS link down. (AIS-P=1 OR AIS-L=1 OR PLM-P=1 OR WIS SEF=1 or LOP-P=1) 1: WIS link up. (AIS-P=0 AND AIS-L=0 AND PLM-P=0 AND SEF=0 AND LOP-P=0)	RO/LL	
1	LOW_PWR_ABILITY	Low power mode support ability. 0: Supported. 1: Not supported.	RO	1
0	Reserved	Reserved	RO	0

Table 212 • **WIS_DEVID1: WIS Device Identifier 1 (2x0002)**

Bit	Name	Description	Access	Default
15:0	DEV_ID_MSW	Upper 16 bits of a 32-bit unique WIS device identifier. Bits 3-18 of the device manufacturers OUI.	RO	0x0007

Table 213 • **WIS_DEVID2: WIS Device Identifier 2 (2x0003)**

Bit	Name	Description	Access	Default
15:0	DEV_ID_LSW	Lower 16 bits of a 32-bit unique WIS device identifier. Bits 19-24 of the device manufacturers OUI. Six-bit model number, and a four-bit revision number.	RO	0x0400

Table 214 • **WIS_SPEED: WIS Speed Capability (2x0004)**

Bit	Name	Description	Access	Default
15:1	Reserved	Reserved	RO	0

Table 214 • **WIS_SPEED: WIS Speed Capability (2x0004) *(continued)***

Bit	Name	Description	Access	Default
0	RATE_ABILITY	WIS rate capability 0: Not capable of 10Gbps. 1: Capable of 10Gbps.	RO	1

Table 215 • **WIS_DEVPKG1: WIS Devices in Package 1 (2x0005)**

Bit	Name	Description	Access	Default
15:6	Reserved		RO	0
5	DTE_XS_PRES	Indicates whether DTE XS is present in the package 0: Not present. 1: Present.	RO	0
4	PHY_XS_PRES	Indicates whether PHY XS is present in the package 0: Not present. 1: Present.	RO	1
3	PCS_PRES	Indicates whether PCS is present in the package 0: Not present. 1: Present.	RO	1
2	WIS_PRES	Indicates whether WIS is present in the package 0: Not present. 1: Present.	RO	1
1	PMD_PMA_PRES	Indicates whether PMA/PMD is present in the package 0: Not present. 1: Present.	RO	1
0	CLS22_PRES	Indicates whether Clause 22 registers are present in the package 0: Not present. 1: Present.	RO	0

Table 216 • **WIS_DEVPKG2: WIS Devices in Package 2 (2x0006)**

Bit	Name	Description	Access	Default
15	Vendor specific device 2 present		RO	0
14	Vendor specific device 1 present		RO	0
13:0	Reserved		RO	0

Table 217 • **WIS_CTRL2: WIS Control 2 (2x0007)**

Bit	Name	Description	Access	Default
15:6	Reserved		RO	0

Table 217 • **WIS_CTRL2: WIS Control 2 (2x0007) *(continued)***

Bit	Name	Description	Access	Default
5	TEST_PRBS31_ANA	Enable WIS PRBS31 test pattern checking function 0: Disable 1: Enable	RW	0
4	TEST_PRBS31_GEN	Enable WIS PRBS31 test pattern generation function 0: Disable 1: Enable	RW	0
3	TEST_PAT_SEL	Selects the pattern type sent by the transmitter when TEST_PAT_GEN (2x0007.1) is low. 0: Mixed frequency test pattern 1: Square wave	RW	0
2	TEST_PAT_ANA	Enables the WIS test pattern checker. Doing so prevents the loss of code-group delineation (LCD-P) alarm from being set while the WIS is receiving the mixed frequency test pattern. 0: Disable 1: Enable	RW	0
1	TEST_PAT_GEN	Enable WIS test pattern generation 0: Disable 1: Enable	RW	0
0	WAN_MODE	Enable 10GBASE-W logic and sets the speed of the WIS-PMA interface to 9.95328 Gbps. The proper reference clock frequency must be provided to set the data rate. Note: there are multiple ways to enable WAN mode. 0: Disable 1: Enable	RW	0

Table 218 • **WIS_STAT2: WIS Status 2 (2x0008)**

Bit	Name	Description	Access	Default
15:14	DEV_PRES	Reflects the presence of a MMD responding at this address 00: No device responding at this address 01: No device responding at this address 10: Device responding at this address 11: No device responding at this address	RO	10
13:2	Reserved	Reserved	RO	0
1	PRBS31_ABILITY	Indicates if WIS supports PRBS31 pattern testing 0: Not supported. 1: Supported.	RO	1
0	BASE_R_ABILITY	Indicates if WIS supports a bypass to allow support of 10GBASE-R 0: Not supported. 1: Supported.	RO	1

Table 219 • **WIS_TSTPAT_CNT: WIS Test Pattern Error Counter (2x0009)**

Bit	Name	Description	Access	Default
15:0	TSTPAT_CNT	PRBS31 test pattern error counter. The saturating counter clears when read. The error count is not valid until the SYNC bit in 2xEC51.0 is asserted. The error count can be incremented while the checker is acquiring sync. To clear the invalid error count when sync is achieved, read 2x0009. After the count begins to increment, the counting is not affected by changes to the pattern synchronization.	RO CR	0

Table 220 • **WIS_PKGID1: WIS Package Identifier 1 (2x000E)**

Bit	Name	Description	Access	Default
15:0	PKG_ID_MSW	Upper 16 bits of a 32-bit unique WIS package identifier. Bits 3-18 of the device manufacturers OUI. Six-bit model number and a four-bit revision number.	RO	0

Table 221 • **WIS_PKGID2: WIS Package Identifier 2 (2x000F)**

Bit	Name	Description	Access	Default
15:0	PKG_ID_LSW	Lower 16 bits of a 32-bit unique WIS package identifier. Bits 19-24 of the device manufacturers OUI. Six-bit model number and a four-bit revision number.	RO	0

Table 222 • **WIS_STAT3: WIS Status 3 (2x0021)**

Bit	Name	Description	Access	Default
15:12	Reserved	Reserved	RO	0
11	SEF	Severely errored frame 0: No SEF detected 1: SEF detected	RO/LH	
10	FEPLMP_LCDP	Indicates far-end PLM-P/LCD-P defect in WIS Rx 0: No far-end path label mismatch / Loss of code-group delineation 1: far-end path label mismatch / Loss of code-group delineation	RO/LH	
9	FEAISP_LOPP	Indicates far-end AIS-P/LOP-P defect in WIS Rx 0: far-end path Alarm Indication Signal / Path Loss of Pointer 1: No far-end path alarm indication signal / Path loss of pointer	RO/LH	
8	Reserved	Reserved	RO	0

Table 222 • **WIS_STAT3: WIS Status 3 (2x0021) *(continued)***

Bit	Name	Description	Access	Default
7	LOF	Loss of frame 0: Loss of frame flag lowered 1: Loss of frame flag raised	RO/LH	
6	LOS	Loss of signal 0: Loss of signal flag lowered 1: Loss of signal flag raised	RO/LH	
5	RDIL	Line remote defect indication 0: Line remote defect flag lowered 1: Line remote defect flag raised	RO/LH	
4	AISL	Line alarm indication signal 0: Line alarm indication flag lowered 1: Line alarm indication flag raised	RO/LH	
3	LCDP	Path loss of code-group delineation 0: Path loss of code-group delineation flag lowered 1: Path loss of code-group delineation flag raised	RO/LH	
2	PLMP	Path label mismatch 0: Path label mismatch flag lowered 1: Path label mismatch flag raised	RO/LH	
1	AISP	Path alarm indication signal 0: Path alarm indication signal lowered 1: Path alarm indication signal raised	RO/LH	
0	LOPP	Loss of pointer 0: Loss of pointer flag lowered 1: Loss of pointer flag raised	RO/LH	

Table 223 • **WIS_REI_CNT: WIS Far-End Path Block Error Count (2x0025)**

Bit	Name	Description	Access	Default
15:0	Far end path block error count.	Counter wraps around to 0 when it is incremented beyond its maximum error count of 65,535. Cleared on channel reset.	RO	0

Table 224 • **WIS_TXJ1: WIS Tx J1s (Octets 13-0) (2x0027-002D)**

Bit	Name	Description	Access	Default
15:8	TX_J1_ODD	Contains one of the odd numbered transmitted path trace message octets, numbered 13-1. Transmitted path trace octet 1 is in address 2x0027. Octet 3 is in address 2x0028. Octet 13 is in address 2x002D. Octets 14-15 are located in address 2x002E. Octets 16-63 are located in address 2xEA00-EA17. In a one-byte message, octet 0 is transmitted. In a 16-byte message, octet 0 is transmitted first; octet 15 is transmitted last. In a 64-byte trace message, octet 0 is transmitted first; octet 63 is transmitted last.	RW	0

Table 224 • **WIS_TXJ1: WIS Tx J1s (Octets 13-0) (2x0027-002D) *(continued)***

Bit	Name	Description	Access	Default
7:0	TX_J1_EVEN	Contains one of the even numbered transmitted path trace message octets, numbered 12-0. Transmitted path trace octet 0 is in address 2x0027. Octet 2 is in address 2x0028. Octet 12 is in address 2x002D. Octets 14-15 are located in address 2x002E. Octets 16-63 are located in address 2xEA00-EA17. In a one-byte message, octet 0 is transmitted. In a 16-byte message, octet 0 is transmitted first; octet 15 is transmitted last. In a 64-byte trace message, octet 0 is transmitted first; octet 63 is transmitted last.	RW	0

Table 225 • **WIS_TXJ1B: WIS Tx J1s (Octets 15-14) (2x002E)**

Bit	Name	Description	Access	Default
15:8	TX_J1_octet_15	Contains octet 15 of the transmitted path trace message. Octets 0-13 are located in address 2x007-002D. Octets 16-63 are located in address 2xEA00-EA17. In a one-byte message, octet 0 is transmitted. In a 16-byte message, octet 0 is transmitted first; octet 15 is transmitted last. In a 64-byte trace message, octet 0 is transmitted first; octet 63 is transmitted last.	RW	0x89
7:0	TX_J1_octet_14	Contains octet 14 of the transmitted path trace message. Octets 0-13 are located in address 2x007-002D. Octets 16-63 are located in address 2xEA00-EA17. In a one-byte message, octet 0 is received. In a 16-byte message, octet 0 is received first; octet 15 is received last. In a 64-byte trace message, octet 0 is received first; octet 63 is received last.	RW	0

Table 226 • **WIS_RXJ1: WIS Rx J1s (Octets 15-0) (2x002F-0036)**

Bit	Name	Description	Access	Default
15:8	RX_J1_ODD	Contains one of the odd numbered received path trace message octets numbered 15-1. Received path trace octet 1 is in address 2x002F. Octet 3 is in address 2x0030. Octet 15 is in address 2x0036. Octets 16-63 are located in addresses 2xEB00-2xEB17. In a one-byte message, octet 0 is received. In a 16-byte message, octet 0 is received first; octet 15 is received last. In a 64-byte trace message, octet 0 is received first; octet 63 is received last.	RO	

Table 226 • **WIS_RXJ1: WIS Rx J1s (Octets 15-0) (2x002F-0036) *(continued)***

Bit	Name	Description	Access	Default
7:0	RX_J1_EVEN	Contains one of the even numbered received path trace message octets numbered 14-0. Received path trace octet 0 is in address 2x002F. Octet 2 is in address 2x0030. Octet 14 is in address 2x0036. Octets 16-63 are located in addresses 2xEB00-2xEB17. In a one-byte message, octet 0 is received. In a 16-byte message, octet 0 is received first; octet 15 is received last. In a 64-byte trace message, octet 0 is received first; octet 63 is received last.	RO	

Table 227 • **WIS_REIL_CNT1: WIS Far-End Line BIP Errors 1 (2x0037)**

Bit	Name	Description	Access	Default
15:0	REIL_ERR_CNT_MSW	Most significant word of the WIS far end line BIP error counter Whenever the most significant 16-bit register of the counter is read, the 32-bit counter value is latched into the register pair, with the most significant bits appearing in 2x0037 and the least significant bits appearing in 2x0038. Subsequent reads from 2x0038 will return the least significant 16 bits of the latched value, but will not change the register contents.	RO	0

Table 228 • **WIS_REIL_CNT0: WIS Far-End Line BIP Errors 0 (2x0038)**

Bit	Name	Description	Access	Default
15:0	REIL_ERR_CNT_LSW	Least significant word of the WIS far end line BIP error counter Whenever the most significant 16-bit register of the counter is read, the 32-bit counter value is latched into the register pair, with the most significant bits appearing in 2x0037 and the least significant bits appearing in 2x0038. Subsequent reads from 2x0038 will return the least significant 16 bits of the latched value, but will not change the register contents.	RO	0

Table 229 • **WIS_B2_CNT1: WIS L-BIP Error Count 1 (2x0039)**

Bit	Name	Description	Access	Default
15:0	B2_CNT_MSW	Most significant word of the WIS line BIP error counter Whenever the most significant 16-bit register of the counter is read, the 32-bit counter value is latched into the register pair, with the most significant bits appearing in 2x0039 and the least significant bits appearing in 2x003A. Subsequent reads from 2x003A will return the least significant 16 bits of the latched value, but will not change the register contents.	RO	0

Table 230 • **WIS_B2_CNT0: WIS L-BIP Error Count 0 (2x003A)**

Bit	Name	Description	Access	Default
15:0	B2_CNT_LSW	Least significant word of the WIS line BIP error counter Whenever the most significant 16-bit register of the counter is read, the 32-bit counter value is latched into the register pair, with the most significant bits appearing in 2x0039 and the least significant bits appearing in 2x003A. Subsequent reads from 2x003A will return the least significant 16 bits of the latched value, but will not change the register contents.	RO	0

Table 231 • **WIS_B3_CNT: WIS P-BIP Block Error Count (2x003B)**

Bit	Name	Description	Access	Default
15:0	B3_CNT	Path block error count Counter wraps around to 0 when it is incremented beyond its maximum error count of 65,535. Cleared on channel's WIS reset.	RO	0

Table 232 • **WIS_B1_CNT: WIS S-BIP Error Count (2x003C)**

Bit	Name	Description	Access	Default
15:0	B1_CNT	Section BIP error count Counter wraps around to 0 when it is incremented beyond its maximum error count of 65,535. Cleared on channel's WIS reset.	RO	0

Table 233 • **WIS_TXJ0: WIS Tx J0s (Octets 13-0) (2x0040-0046)**

Bit	Name	Description	Access	Default
15:8	TX_J0_ODD	Contains one of the odd numbered transmitted section trace message octets, numbered 13-1. Transmitted section trace octet 1 is in address 2x0040. Octet 3 is in address 2x0041. Octet 13 is in address 2x0046. Octets 14-15 are located in address 2x0047. Octets 16-63 are located in addresses 2xE800-2xE817. In a one-byte message, octet 0 is transmitted. In a 16-byte message, octet 0 is transmitted first; octet 15 is transmitted last. In a 64-byte trace message, octet 0 is transmitted first; octet 63 is transmitted last.	RW	0
7:0	TX_J0_EVEN	Contains one of the even numbered transmitted section trace message octets, numbered 12-0. Transmitted section trace octet 0 is in address 2x0040. Octet 2 is in address 2x0041. Octet 12 is in address 2x0046. Octets 14-15 are located in address 2x0047. Octets 16-63 are located in addresses 2xE800-2xE817. In a one-byte message, octet 0 is transmitted. In a 16-byte message, octet 0 is transmitted first; octet 15 is transmitted last. In a 64-byte trace message, octet 0 is transmitted first; octet 63 is transmitted last.	RW	0

Table 234 • **WIS_TXJ0B: WIS Tx J0s (Octets 15-14) (2x0047)**

Bit	Name	Description	Access	Default
15:8	TX_J0_octet_15	Contains octet 15 of the transmitted section trace message. Octets 0-13 are located in addresses 2x0040-2x0046. Octets 16-63 are located in addresses 2xE800-2xE817. In a one-byte message, octet 0 is transmitted. In a 16-byte message, octet 0 is transmitted first; octet 15 is transmitted last. In a 64-byte trace message, octet 0 is transmitted first; octet 63 is transmitted last.	RW	0x89
7:0	TX_J0_octet_14	Contains octet 14 of the transmitted section trace message. Octets 0-13 are located in addresses 2x0040-2x0046. Octets 16-63 are located in addresses 2xE800-2xE817. In a one-byte message, octet 0 is transmitted. In a 16-byte message, octet 0 is transmitted first; octet 15 is transmitted last. In a 64-byte trace message, octet 0 is transmitted first; octet 63 is transmitted last.	RW	0

Table 235 • **WIS_RXJ0: WIS Rx J0s (2x0048-004F)**

Bit	Name	Description	Access	Default
15:8	RX_J0_ODD	Contains one of the odd numbered received section trace message octets numbered 15-1. Received section trace octet 1 is in address 2x0048. Octet 3 is in address 2x0049. Octet 15 is in address 2x004F. Octets 16-63 are located in addresses 2xE900-2xE917. In a one-byte message, octet 0 is received. In a 16-byte message, octet 0 is received first; octet 15 is received last. In a 64-byte trace message, octet 0 is received first; octet 63 is received last.	RO	
7:0	RX_J0_EVEN	Contains one of the even numbered received section trace message octets numbered 14-0. Received section trace octet 0 is in address 2x0048. Octet 2 is in address 2x0049. Octet 14 is in address 2x004F. Octets 16-63 are located in addresses 2xE900-2xE917. In a one-byte message, octet 0 is received. In a 16-byte message, octet 0 is received first; octet 15 is received last. In a 64-byte trace message, octet 0 is received first; octet 63 is received last.	RO	

Table 236 • **EWIS_TXCTRL1: WIS Vendor Specific Tx Control 1 (2xE5FF)**

Bit	Name	Description	Access	Default
15:1	Reserved	Reserved	RO	0
0	TX_SS	Contents of SS bits in transmitted H1 overhead bytes 2-192. (State of SS bits in the first H1 byte is determined by 2xE615.) 0: SS bits set to 2'b00. 1: SS bits set to 2'b10.	RW	0

Table 237 • **EWIS_TXCTRL2: WIS Vendor Specific Tx Control 2 (2xE600)**

Bit	Name	Description	Access	Default
15	REIL_TXBLK_MODE	Selects use of B2 block error count or bit error count mode to generate the M0/M1 bytes for REI-L back reporting 0: Bit error mode 1: Block error mode	RW	0
14	REIP_TXBLK_MODE	Selects use of B3 block error count or bit error count mode to generate the G1 byte for REI-P back reporting 0: Bit error mode 1: Block error mode	RW	0
13	Reserved	Factory test only. Do not modify this bit group.	RW	0
12	SCR	Enable transmit WIS scrambler 0: Disable 1: Enable	RW	1

Table 237 • **EWIS_TXCTRL2: WIS Vendor Specific Tx Control 2 (2xE600)** ***(continued)***

Bit	Name	Description	Access	Default
11	FRC_TX_TIMP	Force transmission of a TIM-P condition within the G1 byte 0: Normal operation. 1: Force TIM-P	RW	0
10	ERDI_TX_MODE	Selects ERDI as the transmit WIS G1 byte mode 0: RDI mode 1: ERDI mode	RW	1
9	SDH_TX_MODE	Selects the format of the WIS frame structure 0: SONET mode 1: SDH mode	RW	1
8	Reserved	Factory test only. Do not modify this bit group.	RW	0
7:4	SQ_WV_PW	Select the transmit WIS square wave test pattern length 0000 - 0011: Invalid 0100: 4 zeros and 4 ones 0101: 5 zeros and 5 ones 0110: 6 zeros and 6 ones 0111: 7 zeros and 7 ones 1000: 8 zeros and 8 ones 1001: 9 zeros and 9 ones 1010: 10 zeros and 10 ones 1011: 11 zeros and 11 ones 1100 - 1111: Invalid	RW	0100
3	Reserved	Factory test only. Do not modify this bit group.	RW	0
2	FRC_TX_RDI	Force transmission of RDI-L in the K2 byte 0: Normal operation. 1: Force RDI-L	RW	0
1	FRC_TX_AISL	Force transmission of AIS-L in the K2 byte. AIS-L will take precedence over RDI-L if both are asserted. 0: Normal operation. 1: Force AIS-L	RW	0
0	Reserved	Reserved	RO	0

Table 238 • **Factory Test Register (2xE601)**

Bit	Name	Description	Access	Default
15:2	Reserved	Factory test only.	RO	0
1	Reserved	Factory test only. Do not modify this bit group.	RW	0
0	Reserved	Factory test only. Do not modify this bit group.	RW SC	0

Table 239 • **Factory Test Register (2xE602)**

Bit	Name	Description	Access	Default
15:8	Reserved	Factory test only.	RO	0

Table 239 • **Factory Test Register (2xE602) *(continued)***

Bit	Name	Description	Access	Default
7:0	Reserved	Factory test only. Do not modify this bit group.	RW	0

Table 240 • **Factory Test Register (2xE603)**

Bit	Name	Description	Access	Default
15:0	Reserved	Factory test only. Do not modify this bit group.	RW	0

Table 241 • **Factory Test Register (2xE604)**

Bit	Name	Description	Access	Default
15:0	Reserved	Factory test only. Do not modify this bit group.	RW	0

Table 242 • **Factory Test Register (2xE605)**

Bit	Name	Description	Access	Default
15:0	Reserved	Factory test only. Do not modify this bit group.	RW	0

Table 243 • **Factory Test Register (2xE606)**

Bit	Name	Description	Access	Default
15:0	Reserved	Factory test only. Do not modify this bit group.	RW	0

Table 244 • **EWIS_TX_A1_A2: E-WIS Tx A1/A2 Octets (2xE611)**

Bit	Name	Description	Access	Default
15:8	TX_A1	A1 byte to be transmitted when the TOSI data is inactive.	RW	0xF6
7:0	TX_A2	A2 byte to be transmitted when the TOSI data is inactive.	RW	0x28

Table 245 • **EWIS_TX_Z0_E1: E-WIS Tx Z0/E1 Octets (2xE612)**

Bit	Name	Description	Access	Default
15:8	TX_Z0	Z0 byte to be transmitted when the TOSI data is inactive	RW	0xCC
7:0	TX_E1	E1 byte to be transmitted when the TOSI data is inactive	RW	0x00

Table 246 • **EWIS_TX_F1_D1: E-WIS Tx F1/D1 Octets (2xE613)**

Bit	Name	Description	Access	Default
15:8	TX_F1	F1 byte to be transmitted when the TOSI data is inactive	RW	0x00
7:0	TX_D1	D1 byte to be transmitted when the TOSI data is inactive	RW	0x00

Table 247 • **EWIS_TX_D2_D3: E-WIS Tx D2/D3 Octets (2xE614)**

Bit	Name	Description	Access	Default
15:8	TX_D2	D2 byte to be transmitted when the TOSI data is inactive	RW	0x00
7:0	TX_D3	D3 byte to be transmitted when the TOSI data is inactive	RW	0x00

Table 248 • **EWIS_TX_C2_H1: E-WIS Tx C2/H1 Octets (2xE615)**

Bit	Name	Description	Access	Default
15:8	TX_C2	C2 byte to be transmitted	RW	0x1A
7:0	TX_H1	H1 byte to be transmitted	RW	0x62

Table 249 • **EWIS_TX_H2_H3: E-WIS Tx H2/H3 Octets (2xE616)**

Bit	Name	Description	Access	Default
15:8	TX_H2	H2 byte to be transmitted when the TOSI data is inactive	RW	0x0A
7:0	TX_H3	H3 byte to be transmitted when the TOSI data is inactive	RW	0x00

Table 250 • **EWIS_TX_G1_K1: E-WIS Tx G1/K1 Octets (2xE617)**

Bit	Name	Description	Access	Default
15:8	Reserved	Factory test only. Do not modify this bit group.	RW	0x00
7:0	TX_K1	K1 byte to be transmitted when the TOSI data is inactive	RW	0x00

Table 251 • **EWIS_TX_K2_F2: E-WIS Tx K2/F2 Octets (2xE618)**

Bit	Name	Description	Access	Default
15:8	TX_K2	K2 byte to be transmitted when the TOSI data is inactive	RW	0x00
7:0	TX_F2	F2 byte to be transmitted	RW	0x00

Table 252 • **EWIS_TX_D4_D5: E-WIS Tx D4/D5 Octets (2xE619)**

Bit	Name	Description	Access	Default
15:8	TX_D4	D4 byte to be transmitted when the TOSI data is inactive	RW	0x00
7:0	TX_D5	D5 byte to be transmitted when the TOSI data is inactive	RW	0x00

Table 253 • **EWIS_TX_D6_H4: E-WIS Tx D6/H4 Octets (2xE61A)**

Bit	Name	Description	Access	Default
15:8	TX_D6	D6 byte to be transmitted when the TOSI data is inactive	RW	0x00
7:0	TX_H4	H4 byte to be transmitted	RW	0x00

Table 254 • **EWIS_TX_D7_D8: E-WIS Tx D7/D8 Octets (2xE61B)**

Bit	Name	Description	Access	Default
15:8	TX_D7	D7 byte to be transmitted when the TOSI data is inactive	RW	0x00
7:0	TX_D8	D8 byte to be transmitted when the TOSI data is inactive	RW	0x00

Table 255 • **EWIS_TX_D9_Z3: E-WIS Tx D9/Z3 Octets (2xE61C)**

Bit	Name	Description	Access	Default
15:8	TX_D9	D9 byte to be transmitted when the TOSI data is inactive	RW	0x00
7:0	TX_Z3	Z3 byte to be transmitted	RW	0x00

Table 256 • **EWIS_TX_D10_D11: E-WIS Tx D10/D11 Octets (2xE61D)**

Bit	Name	Description	Access	Default
15:8	TX_D10	D10 byte to be transmitted when the TOSI data is inactive	RW	0x00
7:0	TX_D11	D11 byte to be transmitted when the TOSI data is inactive	RW	0x00

Table 257 • **EWIS_TX_D12_Z4: E-WIS Tx D12/Z4 Octets (2xE61E)**

Bit	Name	Description	Access	Default
15:8	TX_D12	D12 byte to be transmitted when the TOSI data is inactive	RW	0x00
7:0	TX_Z4	Z4 byte to be transmitted	RW	0x00

Table 258 • **EWIS_TX_S1_Z1: E-WIS Tx S1/Z1 Octets (2xE61F)**

Bit	Name	Description	Access	Default
15:8	TX_S1	S1 byte to be transmitted when the TOSI data is inactive	RW	0x0F
7:0	TX_Z1	Z1 byte to be transmitted when the TOSI data is inactive	RW	0x00

Table 259 • **EWIS_TX_Z2_E2: E-WIS Tx Z2/E2 Octets (2xE620)**

Bit	Name	Description	Access	Default
15:8	TX_Z2	Z2 byte to be transmitted when the TOSI data is inactive	RW	0x00
7:0	TX_E2	E2 byte to be transmitted when the TOSI data is inactive	RW	0x00

Table 260 • **EWIS_TX_N1: E-WIS Tx N1 Octet (2xE621)**

Bit	Name	Description	Access	Default
15:8	TX_N1	N1 byte to be transmitted	RW	0x00
7:0	Reserved	Reserved	RO	0x00

Table 261 • **Reserved (2xE622)**

Bit	Name	Description	Access	Default
15:8	Reserved	Reserved Factory test only.	RO	0x00
7:0	Reserved	Reserved Factory test only.	RO	0x00

Table 262 • **EWIS_TX_MSGLEN: E-WIS Tx Trace Message Length Control (2xE700)**

Bit	Name	Description	Access	Default
15:4	Reserved	Reserved	RO	0
3:2	J0_TXLEN	Selects length of transmitted section trace message. 00: 16-byte trace length 01: 64-byte trace length 10: 1-byte trace length 11: 1-byte trace length	RW	0
1:0	J1_TXLEN	Selects length of transmitted path trace message. 00: 16-byte trace length 01: 64-byte trace length 10: 1-byte trace length 11: 1-byte trace length	RW	0

Table 263 • **EWIS_TXJ0: E-WIS Tx J0s 16-63 (2xE800-E817)**

Bit	Name	Description	Access	Default
15:8	J0_TX64_ODD	Contains one octet of the transmitted section trace message for octets 17-63. Octet 17 is in 2xE800, octet 19 is in 2xE801, and so on. Octets 0-15 are located in addresses 2x0040-2x0047. In a one-byte message, octet 0 is transmitted. In a 16-byte message, octet 0 is transmitted first; octet 15 is transmitted last. In a 64-byte trace message, octet 0 is transmitted first; octet 63 is transmitted last.	RW	0
7:0	J0_TX64_EVEN	Contains one octet of the transmitted section trace message for octets 16-62. Octet 16 is in 2xE800, octet 18 is in 2xE801, and so on. Octets 0-15 are located in addresses 2x0040-2x0047. In a one-byte message, octet 0 is transmitted. In a 16-byte message, octet 0 is transmitted first; octet 15 is transmitted last. In a 64-byte trace message, octet 0 is transmitted first; octet 63 is transmitted last.	RW	0

Table 264 • **EWIS_RXJ0: E-WIS Rx J0s 16-63 (2xE900-E917)**

Bit	Name	Description	Access	Default
15:8	J0_RX64_ODD	Contains one octet of the received section trace message for octets 17-63. Octet 17 is in 2xE900, octet 19 is in 2xE901, and so on. Octets 0-15 are located in addresses 2x0048-2x004F. In a one-byte message, octet 0 is received. In a 16-byte message, octet 0 is received first; octet 15 is received last. In a 64-byte trace message, octet 0 is received first; octet 63 is received last.	RO	
7:0	J0_RX64_EVEN	Contains one octet of the received section trace message for octets 16-62. Octet 16 is in 2xE900, octet 18 is in 2xE901, and so on. Octets 0-15 are located in addresses 2x0048-2x004F. In a one-byte message, octet 0 is received. In a 16-byte message, octet 0 is received first; octet 15 is received last. In a 64-byte trace message, octet 0 is received first; octet 63 is received last.	RO	

Table 265 • **EWIS_TXJ1: E-WIS Tx WIS J1s 16-63 (2xEA00-EA17)**

Bit	Name	Description	Access	Default
15:8	J1_TX64_ODD	Contains one octet of the transmitted path trace message for octets 17-63. Octet 17 is in 2xEA00, octet 19 is in 2xEA01, and so on. Octets 0-15 are located in addresses 2x0027-2x002E. In a one-byte message, octet 0 is transmitted. In a 16-byte message, octet 0 is transmitted first; octet 15 is transmitted last. In a 64-byte trace message, octet 0 is transmitted first; octet 63 is transmitted last.	RW	0
7:0	J1_TX64_EVEN	Contains one octet of the transmitted path trace message for octets 16-62. Octet 16 is in 2xEA00, octet 18 is in 2xEA01, and so on. Octets 0-15 are located in addresses 2x0027-2x002E. In a one-byte message, octet 0 is transmitted. In a 16-byte message, octet 0 is transmitted first; octet 15 is transmitted last. In a 64-byte trace message, octet 0 is transmitted first; octet 63 is transmitted last.	RW	0

Table 266 • **EWIS_RXJ1: E-WIS Rx J1s 16-63 (2xEB00-EB17)**

Bit	Name	Description	Access	Default
15:8	J1_RX64_ODD	Contains one octet of the received path trace message for octets 17-63. Octet 17 is in 2xEB00, octet 19 is in 2xEB01, and so on. Octets 0-15 are located in addresses 2x002F-2x0036. In a one-byte message, octet 0 is received. In a 16-byte message, octet 0 is received first; octet 15 is received last. In a 64-byte trace message, octet 0 is received first; octet 63 is received last.	RO	

Table 266 • **EWIS_RXJ1: E-WIS Rx J1s 16-63 (2xEB00-EB17) *(continued)***

Bit	Name	Description	Access	Default
7:0	J1_RX64_EVEN	Contains one octet of the received path trace message for octets 16-62. Octet 16 is in 2xEB00, octet 18 is in 2xEB01, and so on. Octets 0-15 are located in addresses 2x002F-2x0036. In a one-byte message, octet 0 is received. In a 16-byte message, octet 0 is received first; octet 15 is received last. In a 64-byte trace message, octet 0 is received first; octet 63 is received last.	RO	

Table 267 • **EWIS_RX_FRM_CTRL1: E-WIS Rx Framer Control 1 (2xEC00)**

Bit	Name	Description	Access	Default
15	Reserved	Reserved	RO	0
14:10	HUNT_A1	The number of consecutive A1 octets the receive framer must find before it can exit the HUNT state. 0: Undefined 1-16: 1-16 17-31: Undefined	RW	0x04
9:5	PRESYNC_A1	The number of consecutive A1 octets in the presync pattern preceding the first A2 octet. 0: 1 1-16: 1-16 17-31: 16	RW	0x10
4:0	PRESYNC_A2	The number of consecutive A2 octets in the presync pattern following the last A1 octet. 0: Only the four MSB of the first A2 byte are compared 1-16: 1-16 17-31: 16	RW	0x10

Table 268 • **EWIS_RX_FRM_CTRL2: E-WIS Rx Framer Control 2 (2xEC01)**

Bit	Name	Description	Access	Default
15:13	Reserved	Reserved	RO	0
12:8	SYNC_PAT	Synchronization pattern to be used after the presync pattern has been detected. 0: Sync pattern is A1 plus 4 most significant bits of A2 1: Sync pattern is 2 A1s plus 1 A2 (A1A1A2) 2-16: Sync pattern is the number of consecutive A1s followed by the same number of A2s (I.e. the sync pattern is A1A1A2A2 when 2 is the setting) 17-31: Undefined	RW	0x02

Table 268 • **EWIS_RX_FRM_CTRL2: E-WIS Rx Framer Control 2 (2xEC01) *(continued)***

Bit	Name	Description	Access	Default
7:4	SYNC_ENTRY_CNT	Number of consecutive frame boundaries to be detected after finding the presync pattern before the framer can enter the SYNC state. 0: 1 1-15: 1-15	RW	0x4
3:0	SYNC_EXIT_CNT	Number of consecutive frame boundary location errors tolerated/detected before exiting the SYNC state. 0: 1 1-15: 1-15	RW	0x4

Table 269 • **EWIS_LOF_CTRL1: E-WIS Loss of Frame Control 1 (2xEC02)**

Bit	Name	Description	Access	Default
15:12	Reserved		RO	0
11:6	LOF_T1	Defines the number of frames periods (nominally 125 µS) during which OOF must persist to trigger LOF. This is not a count of continuous frames. An integrating counter is used. 0x0: Undefined 0x1: 1 frame time (125µs) 0x2: 2 frame times (250µs) ... 0x18: 24 frame times (3ms) 0x3F: 63 frame times (7.875ms)	RW	0x18
5:0	LOF_T2	Defines the number of consecutive frame periods (nominally 125 µS) during which OOF status must not be true in order to clear loss of frame set count (the counter associated with 2xEC02[11:6]). 0x0: Undefined 0x1: 1 frame time (125µs) 0x2: 2 frame times (250µs) ... 0x18: 24 frame times (3ms) 0x3F: 63 frame times (7.875ms)	RW	0x18

Table 270 • **EWIS_LOF_CTRL2: E-WIS Loss of Frame Control 2 (2xEC03)**

Bit	Name	Description	Access	Default
15:7	Reserved	Reserved	RO	0

Table 270 • **EWIS_LOF_CTRL2: E-WIS Loss of Frame Control 2 (2xEC03) *(continued)***

Bit	Name	Description	Access	Default
6:1	LOF_T3	Defines number of consecutive frames (normally 125 µS) for which the receive framer must be in its sync state in order to clear the LOF status 0x0: Undefined 0x1: 1 frame time (125µs) 0x2: 2 frame times (250µs) ... 0x18: 24 frame times (3ms) 0x3F: 63 frame times (7.875ms)	RW	0x18
0	Reserved	Reserved	RO	0

Table 271 • **EWIS_RX_CTRL1: E-WIS Rx Control 1 (2xEC10)**

Bit	Name	Description	Access	Default
15:2	Reserved	Reserved	RO	0
1	DSCR_ENA	Enable the WIS descrambler 0: Disable 1: Enable	RW	1
0	B3_CALC_MODE	Selects whether or not the fixed stuff bytes are included in the receive Path BIP error calculation 0: The fixed stuff bytes are excluded from the B3 calculation. 1: The fixed stuff bytes are included in the B3 calculation.	RW	1

Table 272 • **EWIS_RX_MSGLEN: E-WIS Rx Trace Message Length Control (2xEC20)**

Bit	Name	Description	Access	Default
15:4	Reserved	Reserved	RO	0
3:2	J0_RX_LEN	Selects the expected length of the received Section trace message. 00: 16-byte trace length 01: 64-byte trace length 10: 1-byte trace length 11: 1-byte trace length	RW	0
1:0	J1_RX_LEN	Selects the length of the expected path trace message. 00: 16-byte trace length 01: 64-byte trace length 10: 1-byte trace length 11: 1-byte trace length	RW	0

Table 273 • **EWIS_RX_ERR_FRC1: E-WIS Rx Error Force Control 1 (2xEC30)**

Bit	Name	Description	Access	Default
15:13	Reserved		RO	0
12	FRC_LOPC	Force a Loss of Optical Carrier (LOPC) condition. The LOPC alarm state is asserted in 2xEE03.11 when this bit is set. The LOPC status in 1xA200 is not modified when this bit is set. 0: Normal operation 1: Force LOPC	RW	0
11	FRC_LOS	Force a Loss of Signal (LOS) condition in the WIS receive data path 0: Normal operation 1: Forced receive LOS	RW	0
10	FRC_OOF	Force the receive framer into the out-of-frame (OOF) state 0: Normal operation. 1: Force receive OOF	RW	0
9	Reserved		RO	0
8	RXLOF_ON_LOPC	Selects whether or not the LOPC input has any effect on alarm conditions detected by the device 0: A LOPC condition does not effect the state of the LOF or SEF status, nor the state of the receive path framer. 1: LOF and SEF are asserted and the receive path framer is put into its out-of-frame state during a LOPC condition.	RW	0
7:4	APS_THRES	The number of consecutive frames required to qualify the setting and clearing of AIS-L and RDI-L flags received in the K1/K2 overhead bytes. 3-15: Threshold value All others: Reserved	RW	0101
3	FRC_RX_AISL	Force a Line Alarm Indication Signal (AIS-L) condition in the WIS receive data path 0: Normal operation 1: Device forced into Rx AIS-L condition	RW	0
2	FRC_RX_RDIL	Force a Line Remote Defect Identifier (RDI-L) condition in the WIS receive data path 0: Normal operation 1: Device forced into Rx RDI-L condition	RW	0
1	FRC_RX_AISP	Force a Path Alarm Indication Signal (AIS-P) condition in the WIS receive data path 0: Normal operation 1: Device forced into Rx AIS-P condition	RW	0
0	FRC_RX_LOP	Force a Loss of Pointer (LOP) condition to the starting location of the frame's SPE (synchronous payload envelope) in the WIS receive data path 0: Normal operation 1: Device forced into Rx LOP condition	RW	0

Table 274 • **EWIS_RX_ERR_FRC2: E-WIS Rx Error Force Control 2 (2xEC31)**

Bit	Name	Description	Access	Default
15	FRC_RX_UNEQP	Force a Unequipped Path (UNEQ-P) defect in the WIS receive data path 0: Normal operation 1: Device forced into Rx UNEQ-P condition	RW	0
14	FRC_RX_PLMP	Force a Payload Label Mismatch (PLM-P) defect in the WIS receive data path 0: Normal operation 1: Device forced into Rx PLM-P condition	RW	0
13	FRC_RX_RDIP	Force a far-end Path Remote Defect Identifier condition in the WIS receive data path 0: Normal operation 1: Device forced into Rx far-end RDI-P condition	RW	0
12	FRC_RX_FE_AISP	Force a far-end Path Alarm Indication Signal condition in the WIS receive data path 0: Normal operation 1: Device forced into Rx far-end AIS-P condition	RW	0
11	FRC_RX_FE_UNEQP	Force a far-end Unequipped Path defect in the WIS receive data path 0: Normal operation 1: Device forced into Rx far-end UNEQ-P condition	RW	0
10	FRC_RX_FE_PLMP	Force a far-end Payload Label Mismatch defect in the WIS receive data path 0: Normal operation 1: Device forced into Rx far-end PLM-P condition	RW	0
9	FRC_RX_REIP	Force a Path Remote Error Indication (REI-P) condition in the WIS receive data path. The error is reflected in register 2xEE04.3. 0: Normal operation 1: Device forced into Rx REI-P condition	RW	0
8	FRC_RX_REIL	Force a Line Remote Error Indication (REI-L) condition in the WIS receive data path. The error is reflected in register 2xEE04.4. 0: Normal operation 1: Device forced into Rx REI-L condition	RW	0
7	FRC_RX_SEF	Force a Severely Errored Frame (SEF) condition in the WIS receive data path 0: Normal operation 1: Device forced into Rx SEF condition	RW	0
6	FRC_RX_LOF	Force a Loss of Frame (LOF) condition in the WIS receive data path 0: Normal operation 1: Device forced into Rx LOF condition	RW	0
5	FRC_RX_B1	Force a PMTICK B1 BIP error condition (B1NZ) in the WIS receive data path 0: Normal operation 1: Device forced into PMTICK B1 BIP error condition	RW	0

Table 274 • **EWIS_RX_ERR_FRC2: E-WIS Rx Error Force Control 2 (2xEC31) *(continued)***

Bit	Name	Description	Access	Default
4	FRC_RX_B2	Force a PMTICK B2 BIP error condition (B2NZ) in the WIS receive data path 0: Normal operation 1: Device forced into PMTICK B2 BIP error condition	RW	0
3	FRC_RX_B3	Force a PMTICK B3 BIP error condition (B3NZ) in the WIS receive data path 0: Normal operation 1: Device forced into PMTICK B3 BIP error condition	RW	0
2	FRC_LCDP	Force a Loss of Code-group Delineation (LCD-P) defect in the WIS receive data path 0: Normal operation 1: Device forced into Rx LCD-P condition	RW	0
1	FRC_REIL	Force a far-end line BIP error condition (far-end B2NZ) in the WIS receive data path 0: Normal operation 1: Device forced into Rx far-end line BIP error condition	RW	0
0	FRC_REIP	Force a far-end path BIP error condition (far-end B3NZ) in the WIS receive data path 0: Normal operation 1: Device forced into Rx far-end path BIP error condition	RW	0

Table 275 • **EWIS_MODE_CTRL: E-WIS Mode Control (2xEC40)**

Bit	Name	Description	Access	Default
15	Reserved	Reserved	RO	0
14	PTR_MODE	Selects pointer type interpretation mode 0: SONET mode. All 192 H1 and H2 bytes are used to determine the pointer type. 1: SDH mode. Only the first 64 H1 and H2 bytes are used to determine the pointer type.	RW	0
13	PTR_RULES	Selects pointer increment/decrement rules. 0: Pointer increment/ decrement is declared when 8 of the 10 D/I bits in the H1 and H2 bytes match. 1: Pointer increment/ decrement is declared by majority rules.	RW	0
12	REI_MODE	Selects how REI is extracted from the M0/M1 bytes in the WIS receive data path. 0: SONET mode enabled. Uses M0 only. 1: SDH mode enabled. Uses M0 and M1.	RW	0

Table 275 • **EWIS_MODE_CTRL: E-WIS Mode Control (2xEC40) *(continued)***

Bit	Name	Description	Access	Default
11	RX_SS_MODE	Determines whether the SS bits in the H1 byte are checked when processing the received H1/H2 pointer. 0: SS bits are ignored. 1: SS bits must match 2'b10 to be considered a valid H1 byte	RW	0
10:9	Reserved	Factory test only. Do not modify this bit group.	RW	00
8	RX_ERDI_MODE	Selects how ERDI-P/RDI-P is extracted from the G1 byte in the WIS received data 0: RDI-P is reported in bit 5. Bits 6 and 7 are unused. 1: ERDI is reported in bits 5-7.	RW	1
7:0	C2_EXP	Expected C2 receive octet. A PLM-P alarm is generated if this octet value is not received.	RW	0x1A

Table 276 • **Factory Test Register (2xEC41)**

Bit	Name	Description	Access	Default
15:0	Reserved	Factory test only.	RO	0

Table 277 • **EWIS_PRBS31_ANA_CTRL: E-WIS PRBS31 Analyzer Control (2xEC50)**

Bit	Name	Description	Access	Default
15:2	Reserved	Reserved	RO	0
1	PRBS31_FRC_ERR	Inject a single bit error into the WIS PRBS31 pattern checker. A single bit error will result in the error counter incrementing by 3 (1 error for each tap of the checker). 0: Normal operation. 1: Inject error	RW SC	0
0	PRBS31_FRC_SAT	Force the PRBS31 pattern error counter to a value of 65528. This can be useful for testing the saturating feature of the counter. Forcing the counter to 65528 with this bit has no affect on register 2xEC51.1. 0: Normal operation 1: Force the PRBS31 error counter to a value of 65528.	RW SC	0

Table 278 • **EWIS_PRBS31_ANA_STAT: E-WIS PRBS31 Analyzer Status (2xEC51)**

Bit	Name	Description	Access	Default
15:2	Reserved	Reserved	RO	0

Table 278 • **EWIS_PRBS31_ANA_STAT: E-WIS PRBS31 Analyzer Status (2xEC51)** ***(continued)***

Bit	Name	Description	Access	Default
1	PRBS31_ERR	Status bit indicating if the WIS PRBS31 error counter is nonzero. 0: Counter is zero 1: Counter is nonzero	RO	0
0	PRBS31_ANA_STATE	Indicates when the Rx WIS PRBS31 pattern checker is synchronized to the incoming data. 0: PRBS31 pattern checker is not synchronized to the data. PRBS31 error counter value is not valid. 1: PRBS31 pattern checker is synchronized to the data.	RO	0

Table 279 • **EWIS_PMTICK_CTRL: E-WIS Performance Monitor Control (2xEC60)**

Bit	Name	Description	Access	Default
15:3	PMTICK_DUR	Sets the interval for updating the PMTICK error counters when the PMTICK_SRC bit is 1. The value represents the number of 125µS increments between PMTICK events. 0: Undefined 1: Undefined 2: 250 µS ... 8: 1 mS 8000: 1 sec 8191: 1.024 sec	RW	0x1F40
2	PMTICK_ENA	Enable the PMTICK counters to be updated on a PMTICK event. The source of the PMTICK event is determined by the PMTICK_SRC bit. 0: Disable 1: Enable	RW	0
1	PMTICK_SRC	Selects how the PMTICK counters are updated. The PMTICK counters are updated with the selected source only if the PMTICK enable bit is set. 0: PMTICK counters updated on a rising edge of the (GPIO) PMTICK pin 1: PMTICK counters updated when the PMTICK counter reaches its terminal count (PMTICK_DUR).	RW	1
0	PMTICK_FRC	Force the PMTICK counters to update, regardless of the PMTICK_ENA or PMTICK_SRC settings. 0: Normal operation 1: Forces PMTICK event	RW SC	0

Table 280 • **EWIS_CNT_CFG: E-WIS Counter Configuration (2xEC61)**

Bit	Name	Description	Access	Default
15:12	Reserved	Reserved	RO	0
11	B1_BLK_MODE	Enable block mode (increment once for each errored frame) counting for the B1 BIP PMTICK counter. 0: Bit mode 1: Block mode	RW	0
10	B2_BLK_MODE	Enable block mode (increment once for each errored frame) counting for the B2 BIP PMTICK counter 0: Bit mode 1: Block mode	RW	0
9	B3_BLK_MODE	Enable block mode (increment once for each errored frame) counting for the B3 BIP PMTICK counter 0: Bit mode 1: Block mode	RW	0
8:6	Reserved	Reserved	RO	0
5	REIP_BLK_MODE	Enable block mode (increment once for each errored frame) counting for the REI-P (far-end B3 error count in the G1 byte) PMTICK counter 0: Bit mode 1: Block mode	RW	0
4	REIL_BLK_MODE	Enable block mode (increment once for each errored frame) counting for the REI-L (far-end B2 error count in the M0/M1 byte) PMTICK counter 0: Bit mode 1: Block mode	RW	0
3:0	Reserved		RO	0

Table 281 • **EWIS_CNT_STAT: E-WIS Counter Status (2xEC62)**

Bit	Name	Description	Access	Default
15:3	Reserved	Reserved	RO	0
2	REIP_CNT_STAT	Status bit indicating if the REI-P (far-end B3) PMTICK counter is nonzero 0: Counter is zero 1: Counter is nonzero	RO	0
1	REIL_CNT_STAT	Status bit indicating if the REI-L (far-end B2) PMTICK counter is nonzero 0: Counter is zero 1: Counter is nonzero	RO	0
0	Reserved	Factory test only.	RO	0

Table 282 • **EWIS_REIP_CNT1: E-WIS P-REI Counter 1 (MSW) (2xEC80)**

Bit	Name	Description	Access	Default
15:0	REIP_ERR_CNT_MSW	PMTICK statistical error count of the far-end B3 errors (reported in the G1 byte). 16 MSB are in this register, 16 LSB are in the next register. The count is updated only on a PMTICK event. The counter saturates to all ones.	RO	0

Table 283 • **EWIS_REIP_CNT0: E-WIS P-REI Counter 0 (LSW) (2xEC81)**

Bit	Name	Description	Access	Default
15:0	REIP_ERR_CNT_LSW	PMTICK statistical error count of the far-end B3 errors (reported in the G1 byte). 16 LSB are in this register, 16 MSB are in the previous register. The count is updated only on a PMTICK event. The counter saturates to all ones.	RO	0

Table 284 • **EWIS_REIL_CNT1: E-WIS L-REI Counter 1 (MSW) (2xEC90)**

Bit	Name	Description	Access	Default
15:0	REIL_ERR_CNT_MSW	PMTICK statistical error count of the far-end B2 errors (reported in the M0/M1 bytes). 16 MSB are in this register, 16 LSB are in the next register. The count is updated only on a PMTICK event. The counter saturates to all ones.	RO	0

Table 285 • **EWIS_REIL_CNT0: E-WIS L-REI Counter 0 (LSW) (2xEC91)**

Bit	Name	Description	Access	Default
15:0	REIL_ERR_CNT_LSW	PMTICK statistical error count of the far-end B2 errors (reported in the M0/M1 bytes). 16 LSB are in this register, 16 MSB are in the previous register. The count is updated only on a PMTICK event. The counter saturates to all ones.	RO	0

Table 286 • **B2 Rx debug (2xECA0)**

Bit	Name	Description	Access	Default
15:7	Reserved		RO	0
6:0	Reserved	Factory test only.	RO	0

Table 287 • **EWIS_B1_ERR_CNT1: E-WIS S-BIP Error Counter 1 (MSW) (2xECB0)**

Bit	Name	Description	Access	Default
15:0	B1_ERR_CNT_MSW	PMTICK statistical error count of the B1 BIP errors. 16 MSB are in this register, 16 LSB are in the next register. The count is updated only on a PMTICK event. The counter saturates to all ones.	RO	0

Table 288 • **EWIS_B1_ERR_CNT0: E-WIS S-BIP Error Counter 0 (LSW) (2xECB1)**

Bit	Name	Description	Access	Default
15:0	B1_ERR_CNT_LSW	PMTICK statistical error count of the B1 BIP errors. 16 LSB are in this register, 16 MSB are in the previous register. The count is updated only on a PMTICK event. The counter saturates to all ones.	RO	0

Table 289 • **EWIS_B2_ERR_CNT1: E-WIS L-BIP Error Counter 1 (MSW) (2xECB2)**

Bit	Name	Description	Access	Default
15:0	B2_ERR_CNT_MSW	PMTICK statistical error count of the B2 BIP errors. 16 MSB are in this register, 16 LSB are in the next register. The count is updated only on a PMTICK event. The counter saturates to all 1's.	RO	0

Table 290 • **EWIS_B2_ERR_CNT0: E-WIS L-BIP Error Counter 0 (LSW) (2xECB3)**

Bit	Name	Description	Access	Default
15:0	B2_ERR_CNT_LSW	PMTICK statistical error count of the B2 BIP errors. 16 LSB are in this register, 16 MSB are in the previous register. The count is updated only on a PMTICK event. The counter saturates to all 1's.	RO	0

Table 291 • **EWIS_B3_ERR_CNT1: E-WIS P-BIP Error Counter 1 (MSW) (2xECB4)**

Bit	Name	Description	Access	Default
15:0	B3_ERR_CNT_MSW	PMTICK statistical error count of the B3 BIP errors. 16 MSB are in this register, 16 LSB are in the next register. The count is updated only on a PMTICK event. The counter saturates to all ones.	RO	0

Table 292 • **EWIS_B3_ERR_CNT0: E-WIS P-BIP Error Counter 0 (LSW) (2xECB5)**

Bit	Name	Description	Access	Default
15:0	B3_ERR_CNT_LSW	PMTICK statistical error count of the B3 BIP errors. 16 LSB are in this register, 16 MSB are in the previous register. The count is updated only on a PMTICK event. The counter saturates to all ones.	RO	0

Table 293 • **Framer Debug 1 (2xED00)**

Bit	Name	Description	Access	Default
15:0		Factory test only.	RO	0

Table 294 • **Framer Debug 2 (2xED01)**

Bit	Name	Description	Access	Default
15:0		Factory test only.	RO	0

Table 295 • **Framer Debug 3 (2xED02)**

Bit	Name	Description	Access	Default
15:0		Factory test only.	RO	0

Table 296 • **Framer Debug 4 (2xED03)**

Bit	Name	Description	Access	Default
15:0		Factory test only.	RO	0

Table 297 • **Framer Debug 5 (2xED04)**

Bit	Name	Description	Access	Default
15:0		Factory test only.	RO	0

Table 298 • **Rx SPE Debug Bus 1 (2xED05)**

Bit	Name	Description	Access	Default
15:0		Factory test only.	RO	0

Table 299 • **Rx SPE Debug Bus 1 (2xED06)**

Bit	Name	Description	Access	Default
15:0		Factory test only.	RO	0

Table 300 • **Rx SPE Debug Bus 2 (2xED07)**

Bit	Name	Description	Access	Default
15:0		Factory test only.	RO	0

Table 301 • **Rx SPE Debug Bus 2 (2xED08)**

Bit	Name	Description	Access	Default
15:0		Factory test only.	RO	0

Table 302 • **EWIS_RXTX_CTRL: E-WIS Rx to Tx Control (2xEDFF)**

Bit	Name	Description	Access	Default
15:7	Reserved	Reserved	RO	0
6	RXAISL_ON_LOPC	Select if a LOPC condition contributes to the Rx AIS-L alarm 0: A LOPC condition does not cause the AIS-L alarm to be set. 1: A LOPC condition will cause the AIS-L alarm to be set.	RW	0
5	RXAISL_ON_LOS	Selects if a LOS condition contributes to the Rx AIS-L alarm 0: A LOS condition does not cause the AIS-L alarm to be set. 1: A LOS condition will cause the AIS-L alarm to be set.	RW	0
4	RXAISL_ON_LOF	Select if a LOF condition contributes to the Rx AIS-L alarm 0: A LOF condition does not cause the AIS-L alarm to be set. 1: A LOF condition will cause the AIS-L alarm to be set.	RW	0
3	TXRDIL_ON_LOPC	Select if a RDI-L is reported in the Tx frame's K2 byte when a LOPC condition is detected. 0: RDI-L will not be reported when LOPC is detected. 1: RDI-L will be reported when LOPC is detected.	RW	0

Table 302 • **EWIS_RXTX_CTRL: E-WIS Rx to Tx Control (2xEDFF) *(continued)***

Bit	Name	Description	Access	Default
2	TXRDIL_ON_LOS	Selects whether or not RDI-L is reported in the Tx frame's K2 byte when a LOS condition is detected. 0: RDI-L will not be reported when LOS is detected. 1: RDI-L will be reported when LOS is detected.	RW	0
1	TXRDIL_ON_LOF	Selects whether or not RDI-L is reported in the Tx frame's K2 byte when a LOF condition is detected. 0: RDI-L will not be reported when LOF is detected. 1: RDI-L will be reported when LOF is detected.	RW	0
0	TXRDIL_ON_AISL	Selects whether or not RDI-L is reported in the Tx frame's K2 byte when a Rx AIS-L condition is detected. 0: RDI-L will not be reported when a Rx AIS-L condition is detected. 1: RDI-L will be reported when a Rx AIS-L condition is detected.	RW	0

Table 303 • **EWIS_INTR_PEND1: E-WIS Interrupt Pending 1 (2xEE00)**

Bit	Name	Description	Access	Default
15:12	Reserved	Reserved	RO	0
11	SEF_PEND	Interrupt pending, SEF has changed state since this register was last read 0: SEF condition has not changed state 1: SEF condition has changed state	RO CR	0
10	FEPLMP_LCDP_PEND	Interrupt pending, far-end path label mismatch (PLM-P) / Loss of Code-group Delineation (LCD-P) condition has changed state since this register was last read 0: PLM-P/LCD-P has not changed state 1: PLM-P/LCD-P condition has changed state	RO CR	0
9	FEAISP_LOPP_PEND	Interrupt pending, far-end path Alarm Indication Signal (AIS-P)/ Path Loss of Pointer (LOP) condition has changed state since this register was last read 0: Far-end AIS-P/LOP-P condition has not changed state 1: Far-end AIS-P/LOP-P condition has changed state	RO CR	0
8	Reserved	Reserved	RO	0
7	LOF_PEND	Interrupt pending, Loss of Frame (LOF) condition has changed state since this register was last read 0: LOF condition has not changed state 1: LOF condition has changed state	RO CR	0

Table 303 • **EWIS_INTR_PEND1: E-WIS Interrupt Pending 1 (2xEE00) *(continued)***

Bit	Name	Description	Access	Default
6	LOS_PEND	Interrupt pending, Loss of Signal (LOS) condition has changed state since this register was last read. This bit does not assert if LOPC is active at the LOS changes state. 0: LOS condition has not changed state 1: LOS condition has changed state	RO CR	0
5	RDIL_PEND	Interrupt pending, Line Remote Defect Indication (RDI-L) has changed state since this register was last read. 0: RDI-L condition has not changed state 1: RDI-L condition has changed state	RO CR	0
4	AISL_PEND	Interrupt pending, Line Alarm Indication Signal (AIS-L) has changed state since this register was last read. This bit does not assert if LOPC, LOS, LOF or SEF are asserted at the time AIS-L changes state. 0: AIS-L condition has not changed state 1: AIS-L condition has changed state	RO CR	0
3	LCDP_PEND	Interrupt pending, Loss of Code-group Delineation (LCD-P) has changed state since this register was last read. This bit will not assert if AIS-L, AIS-P, UNEQ-P, or PLM-P are asserted at the time LCD-P changes state. 0: LCD-P condition has not changed state 1: LCD-P condition has changed state	RO CR	0
2	PLMP_PEND	Interrupt pending, Path Label Mismatch (PLM-P) has changed state since this register was last read. This bit will not assert if LOP-P or AIS-P are asserted at the time PLM-P changes state. 0: PLM-P condition has not changed state 1: PLM-P condition has changed state	RO CR	0
1	AISP_PEND	Interrupt pending, Path Alarm Indication Signal (AIS-P) has changed state since this register was last read. This bit will not assert if LOPC, LOS, SEF, LOF, or AIS-L are asserted at the time AIS-P changes state. 0: AIS-P condition has not changed state 1: AIS-P condition has changed state	RO CR	0
0	LOPP_PEND	Interrupt pending, Path Loss of Pointer (LOP-P) has changed state since this register was last read 0: LOP-P condition has not changed state 1: LOP-P condition has changed state	RO CR	0

Table 304 • **EWIS_INTR_MASKA_1: E-WIS Interrupt Mask A 1 (2xEE01)**

Bit	Name	Description	Access	Default
15:12	Reserved	Reserved	RO	0

Table 304 • **EWIS_INTR_MASKA_1: E-WIS Interrupt Mask A 1 (2xEE01)** ***(continued)***

Bit	Name	Description	Access	Default
11	SEF_MASKA	Enable propagation of SEF_PEND to the WIS_INTA (GPIO) pin 0: Disable 1: Enable	RW	0
10	FEPLMP_LCDP_MASKA	Enable propagation of FEPLMP_LCDP_PEND to the WIS_INTA (GPIO) pin 0: Disable 1: Enable	RW	0
9	FEAISP_LOPP_MASKA	Enable propagation of FEAISP_LOPP_PEND to the WIS_INTA (GPIO) pin 0: Disable 1: Enable	RW	0
8	Reserved	Reserved	RO	0
7	LOF_MASKA	Enable propagation of LOF_PEND to the WIS_INTA (GPIO) pin 0: Disable 1: Enable	RW	0
6	LOS_MASKA	Enable propagation of LOS_PEND to the WIS_INTA (GPIO) pin 0: Disable 1: Enable	RW	0
5	RDIL_MASKA	Enable propagation of RDIL_PEND to the WIS_INTA (GPIO) pin 0: Disable 1: Enable	RW	0
4	AISL_MASKA	Enable propagation of AISL_PEND to the WIS_INTA (GPIO) pin 0: Disable 1: Enable	RW	0
3	LCDP_MASKA	Enable propagation of LCDP_PEND to the WIS_INTA (GPIO) pin 0: Disable 1: Enable	RW	0
2	PLMP_MASKA	Enable propagation of PLMP_PEND to the WIS_INTA (GPIO) pin 0: Disable 1: Enable	RW	0
1	AISP_MASKA	Enable propagation of AISP_PEND to the WIS_INTA (GPIO) pin 0: Disable 1: Enable	RW	0
0	LOPP_MASKA	Enable propagation of LOPP_PEND to the WIS_INTA (GPIO) pin 0: Disable 1: Enable	RW	0

Table 305 • **EWIS_INTR_MASKB_1: E-WIS Interrupt Mask B 1 (2xEE02)**

Bit	Name	Description	Access	Default
15:12	Reserved		RO	0
11	SEF_MASKB	Enable propagation of SEF_PEND to the WIS_INTB (GPIO) pin 0: Disable 1: Enable	RW	0
10	FEPLMP_LCDP_MASKB	Enable propagation of FEPLMP_LCDP_PEND to the WIS_INTB (GPIO) pin 0: Disable 1: Enable	RW	0
9	FEAISP_LOPP_MASKB	Enable propagation of FEAISP_LOPP_PEND to the WIS_INTB (GPIO) pin 0: Disable 1: Enable	RW	0
8	Reserved		RO	0
7	LOF_MASKB	Enable propagation of LOF_PEND to the WIS_INTB (GPIO) pin 0: Disable 1: Enable	RW	0
6	LOS_MASKB	Enable propagation of LOS_PEND to the WIS_INTB (GPIO) pin 0: Disable 1: Enable	RW	0
5	RDIL_MASKB	Enable propagation of RDIL_PEND to the WIS_INTB (GPIO) pin 0: Disable 1: Enable	RW	0
4	AISL_MASKB	Enable propagation of AISL_PEND to the WIS_INTB (GPIO) pin 0: Disable 1: Enable	RW	0
3	LCDP_MASKB	Enable propagation of LCDP_PEND to the WIS_INTB (GPIO) pin 0: Disable 1: Enable	RW	0
2	PLMP_MASKB	Enable propagation of PLMP_PEND to the WIS_INTB (GPIO) pin 0: Disable 1: Enable	RW	0
1	AISP_MASKB	Enable propagation of AISP_PEND to the WIS_INTB (GPIO) pin 0: Disable 1: Enable	RW	0
0	LOPP_MASKB	Enable propagation of LOPP_PEND to the WIS_INTB (GPIO) pin 0: Disable 1: Enable	RW	0

Table 306 • **EWIS_INTR_STAT2: E-WIS Interrupt Status 2 (2xEE03)**

Bit	Name	Description	Access	Default
15	MODULE_STAT	GPIO pin state being driven by optics module. 0: Module status pin is low. 1: Module status pin is high.	RO	
14	Reserved		RO	0
13	TXLOL_STAT	PMA CMU Loss of Lock status 0: No PMA CMU lock error 1: PMA CMU lock error	RO	
12	RXLOL_STAT	PMA CRU Loss of Lock status 0: No PMA CRU lock error 1: PMA CRU lock error	RO	
11	LOPC_STAT	Loss of Optical Carrier (LOPC) status 0: The LOPC input pin is deasserted 1: The LOPC input pin is asserted Status reported is function of LOPC polarity inversion register bit 1xA201.2.	RO	
10	UNEQP_STAT	Unequipped Path (UNEQ-P) status 0: UNEQ-P is deasserted 1: UNEQ-P is asserted	RO	
9	FEUNEQP_STAT	Far-end Unequipped Path (UNEQ-P) status 0: Far-end UNEQ-P is deasserted 1: Far-end UNEQ-P is asserted	RO	
8	FERDIP_STAT	Far-end Path Remote Defect Identifier (RDI-P) status 0: Far-end RDI-P is deasserted 1: Far-end RDI-P is asserted	RO	
7	B1_NZ_STAT	PMTICK B1 BIP (B1_ERR_CNT) counter status 0: B1_ERR_CNT is zero 1: B1_ERR_CNT is nonzero	RO	0
6	B2_NZ_STAT	PMTICK B2 BIP (B2_ERR_CNT) counter status 0: B2_ERR_CNT is zero 1: B2_ERR_CNT is nonzero	RO	0
5	B3_NZ_STAT	PMTICK B3 BIP (B3_ERR_CNT) counter status 0: B3_ERR_CNT is zero 1: B3_ERR_CNT is nonzero	RO	0
4	REIL_STAT	Line Remote Error Indication (REI-L) value status 0: The REI-L value in the last received frame reported no errors 1: The REI-L value in the last received frame reported errors	RO	0
3	REIP_STAT	Path Remote Error Indication (REI-P) value status 0: The REI-P value in the last received frame reported no errors 1: The REI-P value in the last received frame reported errors	RO	

Table 306 • **EWIS_INTR_STAT2: E-WIS Interrupt Status 2 (2xEE03) *(continued)***

Bit	Name	Description	Access	Default
2	REIL_NZ_STAT	PMTICK REI-L (REIL_ERR_CNT) counter status 0: REIL_ERR_CNT is zero 1: REIL_ERR_CNT is nonzero	RO	
1	REIP_NZ_STAT	PMTICK REI-P (REIP_ERR_CNT) counter status 0: REIP_ERR_CNT is zero 1: REIP_ERR_CNT is nonzero	RO	0
0	HIGH_BER_STAT	PCS high bit error rate (BER) status. 0: No high BER. 1: The PCS block indicates a high bit error rate.	RO	

Table 307 • **EWIS_INTR_PEND2: E-WIS Interrupt Pending 2 (2xEE04)**

Bit	Name	Description	Access	Default
15	MODULE_PEND	Interrupt pending, Module status input pin state (MODULE_STAT) has changed state since this register was last read. 0: MODULE_STAT has not changed state 1: MODULE_STAT has changed state	RO CR	0
14	PMTICK_PEND	Interrupt pending, a PMTICK event (regardless of the source) has occurred since this register was last read. 0: A PMTICK event has not occurred 1: A PMTICK event occurred	RO CR	0
13	TXLOL_PEND	Interrupt pending, PMA CMU lock signal (TXLOL_STAT) has changed state since this register was last read. 0: TXLOL_STAT has not changed state 1: TXLOL_STAT has changed state	RO CR	0
12	RXLOL_PEND	Interrupt pending, PMA CRU lock signal (RXLOL_STAT) has changed state since this register was last read. 0: RXLOL_STAT has not changed state 1: RXLOL_STAT has changed state	RO CR	0
11	LOPC_PEND	Interrupt pending, Loss of Optical Carrier (LOPC) input pin (LOPC_STAT) has changed state since this register was last read. 0: LOPC_STAT has not changed state 1: LOPC_STAT has changed state	RO CR	0
10	UNEQP_PEND	Interrupt pending, Unequipped Path (UNEQP_STAT) has changed state since this register was last read. This bit does not assert if LOP-P or AIS-P are asserted at the time UNEQ-P changes state. 0: UNEQP_STAT has not changed state 1: UNEQP_STAT has changed state	RO CR	0

Table 307 • **EWIS_INTR_PEND2: E-WIS Interrupt Pending 2 (2xEE04) *(continued)***

Bit	Name	Description	Access	Default
9	FEUNEQP_PEND	Interrupt pending, Far-end Unequipped Path (FEUNEQP_STAT) has changed state since this register was last read 0: FEUNEQP_STAT has not changed state 1: FEUNEQP_STAT has changed state	RO CR	0
8	FERDIP_PEND	Interrupt pending, Far-end Path Remote Defect Identifier (FERDIP_STAT) has changed state since this register was last read 0: FERDIP_STAT has not changed state 1: FERDIP_STAT has changed state	RO CR	0
7	B1_NZ_PEND	Interrupt pending, PMTICK B1 error counter (B1_ERR_CNT) has changed from zero to a nonzero value since this register was last read. This bit will not assert if LOS or LOF are asserted at the time B1_NZ_STAT changes state. 0: B1_NZ_STAT has not changed from a 0 to 1 state 1: B1_NZ_STAT has changed from a 0 to 1 state	RO CR	0
6	B2_NZ_PEND	Interrupt pending, PMTICK B2 error counter (B2_ERR_CNT) has changed from zero to a nonzero value since this register was last read. This bit will not assert if AIS-L is asserted at the time B2_NZ_STAT changes state. 0: B2_NZ_STAT has not changed from a 0 to 1 state 1: B2_NZ_STAT has changed from a 0 to 1 state	RO CR	0
5	B3_NZ_PEND	Interrupt pending, PMTICK B3 error counter (B3_ERR_CNT) has changed from zero to a nonzero value since this register was last read. This bit will not assert if LOP-P or AIS-P are asserted at the time B3_NZ_STAT changes state. 0: B3_NZ_STAT has not changed from a 0 to 1 state 1: B3_NZ_STAT has changed from a 0 to 1 state	RO CR	0
4	REIL_PEND	Interrupt pending, REI-L received a nonzero value since this register was last read. 0: REI-L has not received a nonzero value 1: REI-L has received a nonzero value	RO CR	0
3	REIP_PEND	Interrupt pending, REI-P received a nonzero value since this register was last read. 0: REI-P has not received a nonzero value 1: REI-P has received a nonzero value	RO CR	0
2	REIL_NZ_PEND	Interrupt pending, PMTICK far-end B2 error counter (REIL_ERR_CNT) has changed from a zero to a nonzero value since this register was read. 0: REIL_NZ_STAT has not changed from a 0 to 1 state 1: REIL_NZ_STAT has changed from a 0 to 1 state	RO CR	0

Table 307 • **EWIS_INTR_PEND2: E-WIS Interrupt Pending 2 (2xEE04) *(continued)***

Bit	Name	Description	Access	Default
1	REIP_NZ_PEND	Interrupt pending, PMTICK far-end B3 error counter (REIP_ERR_CNT) has changed from a zero to a nonzero value since this register was read. 0: REIP_NZ_STAT has changed from a 0 to 1 state 1: REIP_NZ_STAT has changed from a 0 to 1 state	RO CR	0
0	HIGH_BER_PEND	Interrupt pending, PCS high bit error rate (BER) condition has changed state since this register was read. 0: No change in PCS high BER condition. 1: PCS high BER condition has changed state.	RO CR	0

Table 308 • **EWIS_INTR_MASKA_2: E-WIS Interrupt Mask A 2 (2xEE05)**

Bit	Name	Description	Access	Default
15	MODULE_STAT_MASKA	Enable propagation of MODULE_PEND to the WIS_INTA (GPIO) pin 0: Disable 1: Enable	RW	0
14	PMTICK_MASKA	Enable propagation of PMTICK_PEND to the WIS_INTA (GPIO) pin 0: Disable 1: Enable	RW	0
13	TXLOL_MASKA	Enable propagation of TXLOL_PEND to the WIS_INTA (GPIO) pin 0: Disable 1: Enable	RW	0
12	RXLOL_MASKA	Enable propagation of RXLOL_PEND to the WIS_INTA (GPIO) pin 0: Disable 1: Enable	RW	0
11	LOPC_MASKA	Enable propagation of LOPC_PEND to the WIS_INTA (GPIO) pin 0: Disable 1: Enable	RW	0
10	UNEQP_MASKA	Enable propagation of UNEQP_PEND to the WIS_INTA (GPIO) pin 0: Disable 1: Enable	RW	0
9	FEUNEQP_MASKA	Enable propagation of FEUNEQP_PEND to the WIS_INTA (GPIO) pin 0: Disable 1: Enable	RW	0
8	FERDIP_MASKA	Enable propagation of FERDIP_PEND to the WIS_INTA (GPIO) pin 0: Disable 1: Enable	RW	0

Table 308 • **EWIS_INTR_MASKA_2: E-WIS Interrupt Mask A 2 (2xEE05)** ***(continued)***

Bit	Name	Description	Access	Default
7	B1_NZ_MASKA	Enable propagation of B1_NZ_PEND to the WIS_INTA (GPIO) pin 0: Disable 1: Enable	RW	0
6	B2_NZ_MASKA	Enable propagation of B2_NZ_PEND to the WIS_INTA (GPIO) pin 0: Disable 1: Enable	RW	0
5	B3_NZ_MASKA	Enable propagation of B3_NZ_PEND to the WIS_INTA (GPIO) pin 0: Disable 1: Enable	RW	0
4	REIL_MASKA	Enable propagation of REIL_PEND to the WIS_INTA (GPIO) pin 0: Disable 1: Enable	RW	0
3	REIP_MASKA	Enable propagation of REIP_PEND to the WIS_INTA (GPIO) pin 0: Disable 1: Enable	RW	0
2	REIL_NZ_MASKA	Enable propagation of REIL_NZ_PEND to the WIS_INTA (GPIO) pin 0: Disable 1: Enable	RW	0
1	REIP_NZ_MASKA	Enable propagation of REIP_NZ_PEND to the WIS_INTA (GPIO) pin 0: Disable 1: Enable	RW	0
0	HIGH_BER_MASKA	Enable propagation of HIGH_BER_PEND to the WIS_INTA (GPIO) pin 0: Disable 1: Enable	RW	0

Table 309 • **EWIS_INTR_MASKB_2: E-WIS Interrupt Mask B 2 (2xEE06)**

Bit	Name	Description	Access	Default
15	MODULE_STAT_MASKB	Enable propagation of MODULE_PEND to the WIS_INTB (GPIO) pin 0: Disable 1: Enable	RW	0
14	PMTICK_MASKB	Enable propagation of PMTICK_PEND to the WIS_INTB pin 0: Disable 1: Enable	RW	0
13	TXLOL_MASKB	Enable propagation of TXLOL_PEND to the WIS_INTB pin 0: Disable 1: Enable	RW	0

Table 309 • **EWIS_INTR_MASKB_2: E-WIS Interrupt Mask B 2 (2xEE06)** ***(continued)***

Bit	Name	Description	Access	Default
12	RXLOL_MASKB	Enable propagation of RXLOL_PEND to the WIS_INTB pin 0: Disable 1: Enable	RW	0
11	LOPC_MASKB	Enable propagation of LOPC_PEND to the WIS_INTB pin 0: Disable 1: Enable	RW	0
10	UNEQP_MASKB	Enable propagation of UNEQP_PEND to the WIS_INTB pin 0: Disable 1: Enable	RW	0
9	FEUNEQP_MASKB	Enable propagation of FEUNEQP_PEND to the WIS_INTB pin 0: Disable 1: Enable	RW	0
8	FERDIP_MASKB	Enable propagation of FERDIP_PEND to the WIS_INTB pin 0: Disable 1: Enable	RW	0
7	B1_NZ_MASKB	Enable propagation of B1_NZ_PEND to the WIS_INTB pin 0: Disable 1: Enable	RW	0
6	B2_NZ_MASKB	Enable propagation of B2_NZ_PEND to the WIS_INTB pin 0: Disable 1: Enable	RW	0
5	B3_NZ_MASKB	Enable propagation of B3_NZ_PEND to the WIS_INTB pin 0: Disable 1: Enable	RW	0
4	REIL_MASKB	Enable propagation of REIL_PEND to the WIS_INTB pin 0: Disable 1: Enable	RW	0
3	REIP_MASKB	Enable propagation of REIP_PEND to the WIS_INTB pin 0: Disable 1: Enable	RW	0
2	REIL_NZ_MASKB	Enable propagation of REIL_NZ_PEND to the WIS_INTB pin 0: Disable 1: Enable	RW	0
1	REIP_NZ_MASKB	Enable propagation of REIP_NZ_PEND to the WIS_INTB pin 0: Disable 1: Enable	RW	0

Table 309 • **EWIS_INTR_MASKB_2: E-WIS Interrupt Mask B 2 (2xEE06) *(continued)***

Bit	Name	Description	Access	Default
0	HIGH_BER_MASKB	Enable propagation of HIGH_BER_PEND to the WIS_INTB pin 0: Disable 1: Enable	RW	0

Table 310 • **WIS_FAULT_MASK (2xEE07)**

Bit	Name	Description	Access	Default
15:11	Reserved		RW	00111
10	WIS_FAULT_ON_FEPLMP	Selects if the far-end PLM-P condition triggers the WIS fault alarm (2x0001.7). 0: No trigger 1: Triggers WIS_FAULT	RW	0
9	WIS_FAULT_ON_FEAISP	Selects if the far-end AIS-P condition triggers the WIS fault alarm (2x0001.7). 0: No trigger 1: Triggers WIS_FAULT	RW	0
8	WIS_FAULT_ON_RDIL	Selects if the RDI-L condition triggers the WIS fault alarm (2x0001.7). 0: No trigger 1: Triggers WIS_FAULT	RW	0
7	WIS_FAULT_ON_SEF	Selects if the SEF condition triggers the WIS fault alarm (2x0001.7). 0: No trigger 1: Triggers WIS_FAULT	RW	1
6	WIS_FAULT_ON_LOF	Selects if the LOF condition triggers the WIS fault alarm (2x0001.7). 0: No trigger 1: Triggers WIS_FAULT	RW	1
5	WIS_FAULT_ON_LOS	Selects if the LOS condition triggers the WIS fault alarm (2x0001.7). 0: No trigger 1: Triggers WIS_FAULT	RW	1
4	WIS_FAULT_ON_AISL	Selects if the AIS-L condition triggers the WIS fault alarm (2x0001.7). 0: No trigger 1: Triggers WIS_FAULT	RW	1
3	WIS_FAULT_ON_LCDP	Selects if the LCD-P condition triggers the WIS fault alarm (2x0001.7). 0: No trigger 1: Triggers WIS_FAULT	RW	1
2	WIS_FAULT_ON_PLMP	Selects if the PLM-P condition triggers the WIS fault alarm (2x0001.7). 0: No trigger 1: Triggers WIS_FAULT	RW	1

Table 310 • **WIS_FAULT_MASK (2xEE07) *(continued)***

Bit	Name	Description	Access	Default
1	WIS_FAULT_ON_AISP	Selects if the AIS-P condition triggers the WIS fault alarm (2x0001.7). 0: No trigger 1: Triggers WIS_FAULT	RW	1
0	WIS_FAULT_ON_LOPP	Selects if the LOP-P condition triggers the WIS fault alarm (2x0001.7). 0: No trigger 1: Triggers WIS_FAULT	RW	1

Table 311 • **EWIS_INTR_PEND2: E-WIS Interrupt Pending 3 (2xEE08)**

Bit	Name	Description	Access	Default
15:5	Reserved		RO	0
4	REIP_THRESH_PEND	Interrupt pending, REIP_THRESH_ERR has been asserted since this register was last read. 0: A counter threshold error has not occurred 1: A counter threshold error occurred	RO CR	0
3	REIL_THRESH_PEND	Interrupt pending, REIL_THRESH_ERR has been asserted since this register was last read. 0: A counter threshold error has not occurred 1: A counter threshold error occurred	RO CR	0
2	B1_THRESH_PEND	Interrupt pending, B1_THRESH_ERR has been asserted since this register was last read. 0: A counter threshold error has not occurred 1: A counter threshold error occurred	RO CR	0
1	B2_THRESH_PEND	Interrupt pending, B2_THRESH_ERR has been asserted since this register was last read. 0: A counter threshold error has not occurred 1: A counter threshold error occurred	RO CR	0
0	B3_THRESH_PEND	Interrupt pending, B3_THRESH_ERR has been asserted since this register was last read. 0: A counter threshold error has not occurred 1: A counter threshold error occurred	RO CR	0

Table 312 • **EWIS_INTR_MASKA_3: E-WIS Interrupt Mask A 3 (2xEE09)**

Bit	Name	Description	Access	Default
15:5	Reserved		RO	0
4	REIP_THRESH_MASKA	Enable propagation of REIP_THRESH_PEND to the WIS_INTA (GPIO) pin 0: Disable 1: Enable	RW	0
3	REIL_THRESH_MASKA	Enable propagation of REIL_THRESH_PEND to the WIS_INTA (GPIO) pin 0: Disable 1: Enable	RW	0

Table 312 • **EWIS_INTR_MASKA_3: E-WIS Interrupt Mask A 3 (2xEE09) *(continued)***

Bit	Name	Description	Access	Default
2	B1_THRESH_MASKA	Enable propagation of B1_THRESH_PEND to the WIS_INTA (GPIO) pin 0: Disable 1: Enable	RW	0
1	B2_THRESH_MASKA	Enable propagation of B2_THRESH_PEND to the WIS_INTA (GPIO) pin 0: Disable 1: Enable	RW	0
0	B3_THRESH_MASKA	Enable propagation of B3_THRESH_PEND to the WIS_INTA (GPIO) pin 0: Disable 1: Enable	RW	0

Table 313 • **EWIS_INTR_MASKB_3: E-WIS Interrupt Mask B 3 (2xEE0A)**

Bit	Name	Description	Access	Default
15:5	Reserved		RO	0
4	REIP_THRESH_MASKB	Enable propagation of REIP_THRESH_PEND to the WIS_INTB (GPIO) pin 0: Disable 1: Enable	RW	0
3	REIL_THRESH_MASKB	Enable propagation of REIL_THRESH_PEND to the WIS_INTB (GPIO) pin 0: Disable 1: Enable	RW	0
2	B1_THRESH_MASKB	Enable propagation of B1_THRESH_PEND to the WIS_INTB (GPIO) pin 0: Disable 1: Enable	RW	0
1	B2_THRESH_MASKB	Enable propagation of B2_THRESH_PEND to the WIS_INTB (GPIO) pin 0: Disable 1: Enable	RW	0
0	B3_THRESH_MASKB	Enable propagation of B3_THRESH_PEND to the WIS_INTB (GPIO) pin 0: Disable 1: Enable	RW	0

Table 314 • **Threshold Error Status (2xEE0B)**

Bit	Name	Description	Access	Default
15:5	Reserved		RO	0

Table 314 • **Threshold Error Status (2xEE0B)** ***(continued)***

Bit	Name	Description	Access	Default
4	REIP_THRESH_ERR	Indicates when the REI-P PMTICK counter exceeds the threshold level defined in REIP_THRESH_ERR. The threshold is compared to an internal error accumulator, not the value captured and stored in REIP_ERR_CNT. 0: Counter does not exceed threshold level. 1: Counter exceeds threshold level.	RO	0
3	REIL_THRESH_ERR	Indicates when the REI-L PMTICK counter exceeds the threshold level defined in REIL_THRESH_ERR. The threshold is compared to an internal error accumulator, not the value captured and stored in REIL_ERR_CNT. 0: Counter does not exceed threshold level. 1: Counter exceeds threshold level.	RO	0
2	B1_THRESH_ERR	Indicates when the B2 PMTICK counter exceeds the threshold level defined in B2_THRESH_ERR. The threshold is compared to an internal error accumulator, not the value captured and stored in B2_ERR_CNT. 0: Counter does not exceed threshold level. 1: Counter exceeds threshold level.	RO	0
1	B2_THRESH_ERR	Indicates when the B1 PMTICK counter exceeds the threshold level defined in B1_THRESH_ERR. The threshold is compared to an internal error accumulator, not the value captured and stored in B1_ERR_CNT. 0: Counter does not exceed threshold level. 1: Counter exceeds threshold level.	RO	0
0	B3_THRESH_ERR	Indicates when the B3 PMTICK counter exceeds the threshold level defined in B3_THRESH_ERR. The threshold is compared to an internal error accumulator, not the value captured and stored in B3_ERR_CNT. 0: Counter does not exceed threshold level. 1: Counter exceeds threshold level.	RO	0

Table 315 • **WIS REI-P Threshold Level 1 (2xEE10)**

Bit	Name	Description	Access	Default
15:0	REIP_THRESH_LVL_MSW	REIP_THRESH_ERR is asserted when the REI-P PMTICK error counter is greater than the REI-P threshold level defined by this register and the next register.	RW	0xFFFF

Table 316 • **WIS REI-P Threshold Level 2 (2xEE11)**

Bit	Name	Description	Access	Default
15:0	REIP_THRESH_LVL_LSW	REIP_THRESH_ERR is asserted when the REI-P PMTICK error counter is greater than the REI-P threshold level defined by this register and the previous register.	RW	0xFFFF

Table 317 • **WIS REI-L Threshold Level 1 (2xEE12)**

Bit	Name	Description	Access	Default
15:0	REIL_THRESH_LVL_MSW	REIL_THRESH_ERR is asserted when the REI-L PMTICK error counter is greater than the REI-L threshold level defined by this register and the next register.	RW	0xFFFF

Table 318 • **WIS REI-L Threshold Level 2 (2xEE13)**

Bit	Name	Description	Access	Default
15:0	REIL_THRESH_LVL_LSW	REIL_THRESH_ERR is asserted when the REI-L PMTICK error counter is greater than the REI-L threshold level defined by this register and the previous register.	RW	0xFFFF

Table 319 • **WIS B1 Threshold Level 1 (2xEE14)**

Bit	Name	Description	Access	Default
15:0	B1_THRESH_LVL_MSW	B1_THRESH_ERR is asserted when the B1 PMTICK error counter is greater than the B1 threshold level defined by this register and the next register.	RW	0xFFFF

Table 320 • **WIS B1 Threshold Level 2 (2xEE15)**

Bit	Name	Description	Access	Default
15:0	B1_THRESH_LVL_LSW	B1_THRESH_ERR is asserted when the B1 PMTICK error counter is greater than the B1 threshold level defined by this register and the previous register.	RW	0xFFFF

Table 321 • **WIS B2 Threshold Level 1 (2xEE16)**

Bit	Name	Description	Access	Default
15:0	B2_THRESH_LVL_MSW	B2_THRESH_ERR is asserted when the B2 PMTICK error counter is greater than the B2 threshold level defined by this register and the next register.	RW	0xFFFF

Table 322 • **WIS B2 Threshold Level 2 (2xEE17)**

Bit	Name	Description	Access	Default
15:0	B2_THRESH_LVL_LSW	B2_THRESH_ERR is asserted when the B2 PMTICK error counter is greater than the B2 threshold level defined by this register and the previous register.	RW	0xFFFF

Table 323 • **WIS B3 Threshold Level 1 (2xEE18)**

Bit	Name	Description	Access	Default
15:0	B3_THRESH_LVL_MSW	B3_THRESH_ERR is asserted when the B3 PMTICK error counter is greater than the B3 threshold level defined by this register and the next register.	RW	0xFFFF

Table 324 • **WIS B3 Threshold Level 2 (2xEE19)**

Bit	Name	Description	Access	Default
15:0	B3_THRESH_LVL_LSW	B3_THRESH_ERR is asserted when the B3 PMTICK error counter is greater than the B3 threshold level defined by this register and the previous register.	RW	0xFFFF

Table 325 • **Factory Test Registers (2xEF00 to 2xEF15)**

Bit	Name	Description	Access	Default
15:0	Reserved	Factory test only. Do not modify this bit group.	RW	0

Table 326 • **PCS_CTRL1: PCS Control 1 (3x0000)**

Bit	Name	Description	Access	Default
15	SOFT_RST	Reset all MMDs. 0: Normal operation. 1: Resets the entire channel.	RW SC	0

Table 326 • **PCS_CTRL1: PCS Control 1 (3x0000) *(continued)***

Bit	Name	Description	Access	Default
14	PCS System loopback. See Loopback G.	0: Disable PCS loopback mode 1: Enable PCS loopback mode XFI outputs 00FF.	RW	0
13	Speed selection	0: Unspecified 1: Operation at 10 Gbps and above	RO	1
12	Reserved	Value always 0, writes ignored.	RO	0
11	LOW_PWR_PCS	0: Normal Operation. The internal TXEN signal will not be set to 0 due to the Low Power register bit. 1: Low Power Mode. Power dissipated in the core datapath, XAUI interface and PMA interface is reduced. The appropriate PMA connected to this channel is powered down when this bit is set. The PMA connected to this channel is a function of the datapath failover crosspoint control in global registers 1Ex0003.1 and 1Ex003.0. The internal TXEN signal will be 0. The TXEN signal can be routed out a GPIO pin to shut off the optics module's Tx driver if that is desirable. TXEN-inverted can also be transmitted from a GPIO pin.	RW	0
10:7	Reserved	Value always 0, writes ignored.	RO	0
6	Speed selection	0: Unspecified 1: Operation at 10 Gbps and above	RO	1
5:2	Speed selection		RO	0000
1:0	Reserved	Value always 0, writes ignored.	RO	0

Table 327 • **PCS Status 1 (3x0001)**

Bit	Name	Description	Access	Default
15:8	Reserved	Ignore when read.	RO	0
7	Fault	0: Fault condition not detected. (PCS receive local fault (3x0008.10) = 0) AND (PCS transmit local fault (3x0008.11) = 0) 1: Fault condition detected. (PCS receive local fault (3x0008.10) = 1) OR (PCS transmit local fault (3x0008.11) = 1)	RO	
6:3	Reserved	Ignore when read.	RO	0
2	PCS receive link status	0: PCS received link down. BLOCK_LOCK=0 OR HIGH_BER=1 pin low 1: PCS receive link up. BLOCK_LOCK=1 AND HI_BER=0.	RO/LL	
1	Low power ability	0: PCS does not support low power mode 1: PCS supports low power mode	RO	1
0	Reserved	Ignore when read.	RO	0

Table 328 • **PCS Device Identifier 1 (3x0002)**

Bit	Name	Description	Access	Default
15:0	DEV_ID_LSW	Upper 16 bits of a 32-bit unique PCS device identifier. Bits 3-18 of the device manufacturer's OUI.	RO	0x0007

Table 329 • **PCS Device Identifier 2 (3x0003)**

Bit	Name	Description	Access	Default
15:0	DEV_ID_MSW	Lower 16 bits of a 32-bit unique PCS device identifier. Bits 19-24 of the device manufacturer's OUI. Six-bit model number, and a four-bit revision number.	RO	0x0400

Table 330 • **PCS Speed Ability (3x0004)**

Bit	Name	Description	Access	Default
15:1	Reserved for Future speeds		RO	0
0	Rate_Ability	PCS rate capability 0: Not capable of 10 Gbps 1: Capable of 10 Gbps	RO	1

Table 331 • **PCS Devices in Package (3x0005)**

Bit	Name	Description	Access	Default
15:6	Reserved		RO	0000000000
5	DTE XS present	Indicates whether DTE XS is present in the package. 0: Not present. 1: Present.	RO	0
4	PHY XS present	Indicates whether PHY XS is present in the package 0: Not present. 1: Present.	RO	1
3	PCS present	Indicates whether PCS is present in the package 0: Not present. 1: Present.	RO	1
2	WIS present	Indicates whether WIS is present in the package 0: Not present. 1: Present.	RO	1

Table 331 • **PCS Devices in Package (3x0005) *(continued)***

Bit	Name	Description	Access	Default
1	PMD/PCS present	Indicates whether PMD/PCS is present in the package 0: Not present. 1: Present.	RO	1
0	Clause 22 registers present	Indicates whether clause 22 registers are present in the package 0: Not present. 1: Present.	RO	0

Table 332 • **PCS Devices in Package (3x0006)**

Bit	Name	Description	Access	Default
15	Vendor specific device 2 present	Vendor specific device 2 present 0: Not present 1: Present	RO	0
14	Vendor specific device 1 present	Vendor specific device 1 present 0: Not present 1: Present	RO	0
13:0	Reserved		RO	0

Table 333 • **PCS Control 2 Register (3x0007)**

Bit	Name	Description	Access	Default
15:2	Reserved		RO	0
1:0	Select WAN mode or 10GBASE-R	Indicates the PCS type selected 11: Reserved 10: 10GBASE-W PCS 01: Reserved 00: 10GBASE-R PCS	RW	0

Table 334 • **PCS Status 2 Register (3x0008)**

Bit	Name	Description	Access	Default
15:14	Device present	Reflects the presence of a MMD responding at this address 00: No device responding at this address 01: No device responding at this address 10: Device responding at this address 11: No device responding at this address	RO	10
13:12	Reserved		RO	00
11	Transmit fault	Indicates a fault condition on the transmit path 0: No faults asserted 1: Fault asserted	RO/LH	

Table 334 • **PCS Status 2 Register (3x0008) *(continued)***

Bit	Name	Description	Access	Default
10	Receive fault	Indicates a fault condition on the receive path 0: No faults asserted 1: Fault asserted	RO/LH	
9:3	Reserved		RO	0
2	10GBASE-W ability	Device capability to support 10GBASE-W 0: Not capable 1: Capable	RO	1
1	10GBASE-X ability	Device capability to support 10GBASE-X 0: Not capable 1: Capable	RO	0
0	10GBASE-R ability	Device capability to support 10GBASE-R 0: Not capable 1: Capable	RO	1

Table 335 • **PCS Package Identifier (3x000E)**

Bit	Name	Description	Access	Default
15:0	PKG_ID_MSW	Upper 16 bits of a 32-bit unique PCS package identifier. Bits 3-18 of the device manufacturer's OUI.	RO	0

Table 336 • **PCS Package Identifier (3x000F)**

Bit	Name	Description	Access	Default
15:0	PKG_ID_LSW	Lower 16 bits of a 32-bit unique PCS package identifier. Bits 19-24 of the device manufacturer's OUI. Six-bit model number, and a four-bit revision number.	RO	0

Table 337 • **10GBASE-X Status (3x0018)**

Bit	Name	Description	Access	Default
15:0	BASE_X_STAT	This device does not implement 10GBASE-X	RO	0

Table 338 • **10GBASE-X Control (3x0019)**

Bit	Name	Description	Access	Default
15:0	BASE_X_CTRL	This device does not implement 10GBASE-X	RO	0

Table 339 • **10GBASE-R PCS Status 1 (3x0020)**

Bit	Name	Description	Access	Default
15:13	Reserved		RO	0
12	10GBASE-R receive lock status	0: 10GBASE-R PCS receive link down BLOCK_LOCK (3x0020.0) = 0 OR BER_HI (3x0020.1) = 1 1: 10GBASE-R PCS receive link up BLOCK_LOCK (3x0020.0) = 1 AND BER_HI (3x0020.1) = 0	RO	
11:3	Reserved		RO	0
2	PRBS31 pattern testing ability	0: PCS does not support PRBS31 pattern testing 1: PCS is able to support PRBS31 pattern testing	RO	1
1	10GBASE-R PCS high BER	0: 10GBASE-R PCS not reporting a high BER. 1: 10GBASE-R PCS reporting a high BER.	RO	
0	10GBASE-R PCS block lock	0: 10GBASE-R PCS is not locked to receive blocks. 1: 10GBASE-R PCS is locked to receive blocks.	RO	

Table 340 • **10GBASE-R PCS Status 2 (3x0021)**

Bit	Name	Description	Access	Default
15	Latched block lock	0: 10GBASE-R PCS does not have block lock 1: 10GBASE-R PCS has block lock	RO/LL	
14	Latched high BER	0: 10GBASE-R PCS has not reported a high BER 1: 10GBASE-R PCS has reported a high BER	RO/LH	
13:8	BER	Nonrollover counter, cleared on read.	RO CR	0
7:0	Errored blocks	Nonrollover errored blocks counter, cleared on read.	RO CR	0

Table 341 • **10GBASE-R PCS Test Pattern Seed A 3 (3x0022)**

Bit	Name	Description	Access	Default
15:0	Test pattern seed A bits 0-15	Bits 15:0 of the 58-bit seed A test pattern. Used during PCS pseudorandom test.	RW	0

Table 342 • **10GBASE-R PCS Test Pattern Seed A 2 (3x0023)**

Bit	Name	Description	Access	Default
15:0	Test pattern seed A bits 16-31	Bits 31:16 of the 58-bit seed A test pattern. Used during PCS pseudorandom test.	RW	0

Table 343 • **10GBASE-R PCS Test Pattern Seed A 2 (3x0024)**

Bit	Name	Description	Access	Default
15:0	Test pattern seed A bits 32-47	Bits 47:32 of the 58-bit seed A test pattern. Used during PCS pseudorandom test.	RW	0

Table 344 • **10GBASE-R PCS Test Pattern Seed A 2 (3x0025)**

Bit	Name	Description	Access	Default
15:10	Reserved		RO	0
9:0	Test pattern seed A bits 48-57	Bits 57:48 of the 58-bit seed A test pattern. Used during PCS pseudorandom test.	RW	0

Table 345 • **10GBASE-R PCS Test Pattern Seed B 3 (3x0026)**

Bit	Name	Description	Access	Default
15:0	Test pattern seed B bits 0-15	Bits 15:0 of the 58-bit seed B test pattern. Used during PCS pseudorandom test.	RW	0

Table 346 • **10GBASE-R PCS Test Pattern Seed B 2 (3x0027)**

Bit	Name	Description	Access	Default
15:0	Test pattern seed B bits 16-31	Bits 31:16 of the 58-bit seed B test pattern. Used during PCS pseudorandom test.	RW	0

Table 347 • **10GBASE-R PCS Test Pattern Seed B 1 (3x0028)**

Bit	Name	Description	Access	Default
15:0	Test pattern seed B bits 32-47	Bits 47:32 of the 58-bit seed B test pattern. Used during PCS pseudorandom test.	RW	0

Table 348 • **10GBASE-R PCS Test Pattern Seed B 0 (3x0029)**

Bit	Name	Description	Access	Default
15:10	Reserved		RO	0
9:0	Test pattern seed B bits 48-57	Bits 57:48 of the 58-bit seed B test pattern. Used during PCS pseudorandom test.	RW	0

Table 349 • **10GBASE-R PCS Test Pattern Control (3x002A)**

Bit	Name	Description	Access	Default
15:6	Reserved		RO	0
5	PRBS31 Receive test pattern enable	Enables PRBS31 test pattern analysis 0: Disable 1: Enable	RW	0
4	PRBS31 transmit test pattern enable	Enables PRBS31 test pattern generation 0: Disable 1: Enable	RW	0
3	Transmit test pattern enable	Enables PCS test pattern generator 0: Disable 1: Enable	RW	0
2	Receive test pattern enable	Enables PCS test pattern analyzer 0: Disable 1: Enable	RW	0
1	Test pattern select	Selects which test pattern to be used during the PCS_TSTPAT_GEN/ANA 0: Pseudorandom 1: Square Wave (generation only)	RW	0
0	Data pattern select	Data to be sent during the pseudorandom pattern test after the loading of seed A or seed B 0: 64-bit encoding for 2 local fault ordered sets 1: 64 zeros	RW	0

Table 350 • **10GBASE-R PCS Test Pattern Counter (3x002B)**

Bit	Name	Description	Access	Default
15:0	Test error counter	If customer reads 3x002B, or both 3x8007 and 3x8008, md_testerr_clr will go high. If customer reads only 3x8007 or 3x8008, it will stop update another register until both are read.	RO CR	0

Table 351 • **Vendor Specific USR Test (3x8000)**

Bit	Name	Description	Access	Default
15:0	User-defined data pattern [15:0]	Bits 15:0 of the 64-bit user pattern to be sent instead of local fault ordered sets during pseudorandom testing. Active when 3x8005.0 is asserted.	RW	0

Table 352 • **Vendor Specific USR Test (3x8001)**

Bit	Name	Description	Access	Default
15:0	User-defined data pattern [31:16]	Bits 31:16 of the 64-bit user pattern to be sent instead of local fault ordered sets during pseudorandom testing. Active when 3x8005.0 is asserted.	RW	0

Table 353 • **Vendor Specific USR Test (3x8002)**

Bit	Name	Description	Access	Default
15:0	User-defined data pattern [47:32]	Bits 47:22 of the 64-bit user pattern to be sent instead of local fault ordered sets during pseudorandom testing. Active when 3x8005.0 is asserted.	RW	0

Table 354 • **Vendor Specific USR Test (3x8003)**

Bit	Name	Description	Access	Default
15:0	User-defined data pattern [63:48]	Bits 63:48 of the 64-bit user pattern to be sent instead of local fault ordered sets during pseudorandom testing. Active when 3x8005.0 is asserted.	RW	0

Table 355 • **Square Wave Pulse Width (3x8004)**

Bit	Name	Description	Access	Default
15:4	Reserved		RO	0
3:0	Square wave pulse width	Pulse width of the generated square wave test pattern. This is the number of consecutive low bit times and the number of consecutive high bit times. Only values of 4 through 11 bits are valid.	RW	0000

Table 356 • **Vendor Specific PCS Control (3x8005)**

Bit	Name	Description	Access	Default
15:12	Reserved		RO	0
11	Tx AN select	0: Select normal PCS path in Tx PCS 1: Select AN path in Tx PCS	RW	0
10	Disable Rx pathdescrambler	Disable Rx block descrambler 0: Enable 1: Disable	RW	0

Table 356 • **Vendor Specific PCS Control (3x8005)** ***(continued)***

Bit	Name	Description	Access	Default
9	Disable Tx path scrambler	Disable Tx block scrambler 0: Enable 1: Disable	RW	0
8	Tx PCS data source selection	0: Data from XGXS 1: Data from PCS BIST generator	RW	0
7	Rx PCS data output selection	0: Data from Rx PCS 1: Data from PCS BIST generator	RW	0
6	Reserved		RO	0
5	Disable Rx block sequence check	0: Blocks errors are generated when an invalid block sequence is encountered in the Rx path 1: Blocks errors are not generated when an invalid block sequence is encountered in the Rx path	RW	0
4	Disable Tx block sequence check	0: Blocks errors are generated when an invalid block sequence is encountered in the Tx path 1: Blocks errors are not generated when an invalid block sequence is encountered in the Tx path	RW	0
3	Loopback F	0: loopback F disabled 1: loopback F enabled	RW	0
2	Reserved		RO	0
1	Reserved		RO	0
0	User test pattern enable	Selects the user test pattern in 3x8000 to 3x8003 for pseudorandom test 0: Standard test pattern 1: User test pattern	RW	0

Table 357 • **Vendor Specific Test Error Counter 0 (3x8007)**

Bit	Name	Description	Access	Default
15:0	Test error counter [15:0]	If customer reads 3x002B, or both 3x8007 and 3x8008, md_testerr_clr will go high. If customer reads only 3x8007 or 3x8008, it will stop update another register until both are read.	RO CR	0

Table 358 • **Vendor Specific Test Error Counter 1 (3x8008)**

Bit	Name	Description	Access	Default
15:0	Test error counter [31:16]	If customer reads 3x002B, or both 3x8007 and 3x8008, md_testerr_clr will go high. If customer reads only 3x8007 or 3x8008, it will stop update another register until both are read.	RO CR	0

Table 359 • **Factory Test Only (3x8009)**

Bit	Name	Description	Access	Default
15:0	Reserved	Factory test only.	RO	0

Table 360 • **Factory Test Only (3x800C)**

Bit	Name	Description	Access	Default
15:0	Reserved	Factory test only.	RO CR	0

Table 361 • **Factory Test Only (3x800D)**

Bit	Name	Description	Access	Default
15:0	Reserved	Factory test only.	RO CR	0

Table 362 • **Factory Test Only (3x800E)**

Bit	Name	Description	Access	Default
15:0	Reserved	Factory test only.	RO CR	0

Table 363 • **Factory Test Only (3x800F)**

Bit	Name	Description	Access	Default
15:0	Reserved	Factory test only.	RO CR	0

Table 364 • **Factory Test Only (3x8010)**

Bit	Name	Description	Access	Default
15:0	Reserved	Factory test only.	RO CR	0

Table 365 • **Factory Test Only (3x8011)**

Bit	Name	Description	Access	Default
15:0	Reserved	Factory test only.	RO CR	0

Table 366 • **Factory Test Only (3x8012)**

Bit	Name	Description	Access	Default
15:0	Reserved	Factory test only.	RO CR	0

Table 367 • **Factory Test Only (3x8013)**

Bit	Name	Description	Access	Default
15:0	Reserved	Factory test only.	RO CR	0

Table 368 • **Factory Test Only (3x8014)**

Bit	Name	Description	Access	Default
15:0	Reserved	Factory test only.	RO CR	0

Table 369 • **Factory Test Only (3x8015)**

Bit	Name	Description	Access	Default
15:0	Reserved	Factory test only.	RO CR	0

Table 370 • **Loopback FIFOs Stat/Ctrl (3x8016)**

Bit	Name	Description	Access	Default
15:4	Reserved		RO	0
3	Loop F FIFO Overflow	Loopback F FIFO overflow status 0: normal operation 1: over/under flow condition	RO/LH	
2	Loop F FIFO Sync Inhibit	Selects whether loopback F FIFO's sync inhibit feature is enabled 0: Disabled 1: Enabled	RW	
1	Loop G FIFO Overflow	Loopback G FIFO overflow status 0: Normal operation 1: Over/under flow condition	RO/LH	
0	Loop G FIFO Sync Inhibit	Selects whether loopback G FIFO's sync inhibit feature is enabled 0: Disabled 1: Enabled	RW	

Table 371 • **Vendor Specific PCS 1G BIST Control (3x8200)**

Bit	Name	Description	Access	Default
15:5	Reserved		RO	0
4	Force single bit error at generator output	1: Force single bit error at generator output	RW SC	0
3	Force single bit error at checker input	1: Force single bit error at checker input	RW SC	0
2	Start Generator	1: Start Generator	RW	0

Table 371 • **Vendor Specific PCS 1G BIST Control (3x8200) *(continued)***

Bit	Name	Description	Access	Default
1	Start Checker	1: Start Checker	RW	0
0	Self-check mode	1: Self-check mode	RW	0

Table 372 • **Vendor Specific PCS 1G BIST Status (3x8201)**

Bit	Name	Description	Access	Default
15:6	Reserved		RO	0
5	Tx FIFO overflow	0: No overflow 1: Tx FIFO overflow	RO/LH	
4	Rx FIFO overflow	0: No overflow 1: Rx FIFO overflow	RO/LH	
3	Checker Status - Sync Error	1: Checker never sync'ed to data once checker was enabled. Valid states of 3x8201[3:0]: 0x0: Checker was never started 0x1: Checker is started and searching for pattern 0x3: Checker has sync'ed to pattern and is checking for errors 0x7: Checker has sync'ed to pattern and has found at least one error and is still checking data 0x2: Checker is stopped. Before being stopped, it sync'ed to the pattern and found no errors 0x6: checker is stopped. Before being stopped, it sync'ed to the pattern and count at least one error 0x8: checker is stopped. Before being stopped, it attempted, but could not sync to a pattern.	RO	0
2	Checker Status - Fail	1: Checker sync'ed to data and found at least 1 error.	RO	0
1	Checker Status - Sync	1: Checker Sync'ed to the data.	RO	0
0	Checker Status - Busy	1: Checker is actively seeking or checking data.	RO	0

Table 373 • **(3xE600)**

Bit	Name	Description	Access	Default
15:3	Reserved		RO	0
2	PR58_INV_DIS	Disable the periodic inversion of the pseudorandom test pattern for both transmit and receive paths 0: Enable 1: Disable	RW	0

Table 373 • **(3xE600) *(continued)***

Bit	Name	Description	Access	Default
1	FAULT_TX_SEL	Selects error types to trigger a transmit fault 0: FIFO over/underflow condition only 1: Character encoding error, block encoding error, FIFO over/underflow condition **Note:** For optimal fault indication coverage, set to 1.	RW	0
0	RX_STAT_SEL	Selects contributing logic for receive link status 0: BLOCK_LOCK = 0 1: BLOCK_LOCK = 0 or HIGH_BER = 1 **Note:** For optimal fault indication coverage, set to 1.	RW	0

Table 374 • **PCS BIST Control 1 (3xE61A)**

Bit	Name	Description	Access	Default
15:3	Reserved		RO	0
2	Clear error count	0: no action 1:clear error count	RW	0
1	Checker start	0:checker not enabled 1:start checker	RW	0
0	Reserved		RO	0

Table 375 • **PCS BIST Control 2 (3xE61B)**

Bit	Name	Description	Access	Default
15:8	Packet length	Set packet length	RW	0x10
7:0	IPG length	Set IPG length	RW	0x14

Table 376 • **PCS BIST Error Counter (3xE61C)**

Bit	Name	Description	Access	Default
15:0	PCS BIST Error Counter	Cleared when 3xE61A.2 is set.	RO	0

Table 377 • **PCS BIST Status (3xE61D)**

Bit	Name	Description	Access	Default
15:5	Reserved		RO	0
4	Sync	Pattern is in sync	RO	0
3	Check fail	Fails error check	RO	0
2	Error counter full	Error counter is full	RO	0
1	Sync error	Sync error with data	RO	0

Table 377 • **PCS BIST Status (3xE61D)** ***(continued)***

Bit	Name	Description	Access	Default
0	Busy	Busy in checking	RO	0

Table 378 • **PCS Interrupt Pending 1 (3xEE00)**

Bit	Name	Description	Access	Default
15:8	Reserved		RO	0
7	FEC fixed error count pending	0: Error counter has not exceeded threshold since the last time this interrupt pending bit was asserted. 1: Error count exceeded threshold. Bit is asserted only when counter changes from [threshold to] threshold.	RO CR	0
6	FEC unfixable error count pending	0: Error counter has not exceeded threshold since the last time this interrupt pending bit was asserted. 1: Error count exceeded threshold. Bit is asserted only when counter changes from [threshold to] threshold.	RO CR	0
5	Tx sequencing error count pending	0: Error counter has not exceeded threshold since the last time this interrupt pending bit was asserted. 1: Error count exceeded threshold. Bit is asserted only when counter changes from [threshold to] threshold.	RO CR	0
4	Rx sequencing error count pending	0: Error counter has not exceeded threshold since the last time this interrupt pending bit was asserted. 1: Error count exceeded threshold. Bit is asserted only when counter changes from [threshold to] threshold.	RO CR	0
3	Tx block encode error count pending	0: Error counter has not exceeded threshold since the last time this interrupt pending bit was asserted. 1: Error count exceeded threshold. Bit is asserted only when counter changes from [threshold to] threshold.	RO CR	0
2	Rx block decode error count pending	0: Error counter has not exceeded threshold since the last time this interrupt pending bit was asserted. 1: Error count exceeded threshold. Bit is asserted only when counter changes from [threshold to] threshold.	RO CR	0
1	Tx character encode error count pending	0: Error counter has not exceeded threshold since the last time this interrupt pending bit was asserted. 1: Error count exceeded threshold. Bit is asserted only when counter changes from [threshold to] threshold.	RO CR	0

Table 378 • **PCS Interrupt Pending 1 (3xEE00) *(continued)***

Bit	Name	Description	Access	Default
0	Rx character decode error count pending	0: Error counter has not exceeded threshold since the last time this interrupt pending bit was asserted. 1: Error count exceeded threshold. Bit is asserted only when counter changes from [threshold to] threshold.	RO CR	0

Table 379 • **PCS Interrupt WIS_INT0 Mask 1 (3xEE01)**

Bit	Name	Description	Access	Default
15:8	Reserved		RO	0
7	FEC fixed error count WIS_INT0 mask	0: Disables the alarm/condition from setting the WIS_INTA interrupt pin. 1: Enables the alarm/condition to set the WIS_INTA interrupt pin.	RW	0
6	FEC unfixable error count WIS_INT0 mask	0: Disables the alarm/condition from setting the WIS_INTA interrupt pin. 1: Enables the alarm/condition to set the WIS_INTA interrupt pin.	RW	0
5	Tx sequencing error count WIS_INT0 mask	0: Disables the alarm/condition from setting the WIS_INTA interrupt pin. 1: Enables the alarm/condition to set the WIS_INTA interrupt pin.	RW	0
4	Rx sequencing error count WIS_INT0 mask	0: Disables the alarm/condition from setting the WIS_INTA interrupt pin. 1: Enables the alarm/condition to set the WIS_INTA interrupt pin.	RW	0
3	Tx block encode error count WIS_INT0 mask	0: Disables the alarm/condition from setting the WIS_INTA interrupt pin. 1: Enables the alarm/condition to set the WIS_INTA interrupt pin.	RW	0
2	Rx block decode error count WIS_INT0 mask	0: Disables the alarm/condition from setting the WIS_INTA interrupt pin. 1: Enables the alarm/condition to set the WIS_INTA interrupt pin.	RW	0
1	Tx character encode error count WIS_INT0 mask	0: Disables the alarm/condition from setting the WIS_INTA interrupt pin. 1: Enables the alarm/condition to set the WIS_INTA interrupt pin.	RW	0
0	Rx character decode error count WIS_INT0 mask	0: Disables the alarm/condition from setting the WIS_INTA interrupt pin. 1: Enables the alarm/condition to set the WIS_INTA interrupt pin.	RW	0

Table 380 • **PCS Interrupt WIS_INT1 Mask 1 (3xEE02)**

Bit	Name	Description	Access	Default
15:8	Reserved		RO	0
7	FEC fixed error count WIS_INT1 mask	0: Disables the alarm/condition from setting the WIS_INTA interrupt pin. 1: Enables the alarm/condition to set the WIS_INTA interrupt pin.	RW	0
6	FEC unfixable error count WIS_INT1 mask	0: Disables the alarm/condition from setting the WIS_INTA interrupt pin. 1: Enables the alarm/condition to set the WIS_INTA interrupt pin.	RW	0
5	Tx sequencing error count WIS_INT1 mask	0: Disables the alarm/condition from setting the WIS_INTA interrupt pin. 1: Enables the alarm/condition to set the WIS_INTA interrupt pin.	RW	0
4	Rx sequencing error count WIS_INT1 mask	0: Disables the alarm/condition from setting the WIS_INTA interrupt pin. 1: Enables the alarm/condition to set the WIS_INTA interrupt pin.	RW	0
3	Tx block encode error count WIS_INT1 mask	0: Disables the alarm/condition from setting the WIS_INTA interrupt pin. 1: Enables the alarm/condition to set the WIS_INTA interrupt pin.	RW	0
2	Rx block decode error count WIS_INT1 mask	0: Disables the alarm/condition from setting the WIS_INTA interrupt pin. 1: Enables the alarm/condition to set the WIS_INTA interrupt pin.	RW	0
1	Tx character encode error count WIS_INT1 mask	0: Disables the alarm/condition from setting the WIS_INTA interrupt pin. 1: Enables the alarm/condition to set the WIS_INTA interrupt pin.	RW	0
0	Rx character decode error count WIS_INT1 mask	0: Disables the alarm/condition from setting the WIS_INTA interrupt pin. 1: Enables the alarm/condition to set the WIS_INTA interrupt pin.	RW	0

Table 381 • **PCS Interrupt Error Status (3xEE03)**

Bit	Name	Description	Access	Default
15:8	Reserved		RO	0
7	FEC fixed error count error status		RO	0
6	FEC unfixable error count error status		RO	0
5	Tx sequencing error count error status		RO	0

Table 381 • **PCS Interrupt Error Status (3xEE03) *(continued)***

Bit	Name	Description	Access	Default
4	Rx sequencing error count error status		RO	0
3	Tx block encode error count error status		RO	0
2	Rx block decode error count error status		RO	0
1	Tx character encode error count error status		RO	0
0	Rx character decode error count error status		RO	0

Table 382 • **Tx Sequencing Error Count Threshold (3xEE04)**

Bit	Name	Description	Access	Default
15:0	Tx sequencing error count threshold		RW	0xFFFF

Table 383 • **Rx Sequencing Error Count Threshold (3xEE05)**

Bit	Name	Description	Access	Default
15:0	Rx sequencing error count threshold		RW	0xFFFF

Table 384 • **Tx Block Encode Error Count Threshold (3xEE06)**

Bit	Name	Description	Access	Default
15:0	Tx block encode error count threshold		RW	0xFFFF

Table 385 • **Rx Block Encode Error Count Threshold (3xEE07)**

Bit	Name	Description	Access	Default
15:0	Rx block encode error count threshold		RW	0xFFFF

Table 386 • **Tx Character Encode Error Count Threshold (3xEE08)**

Bit	Name	Description	Access	Default
15:0	Tx character encode error count threshold		RW	0xFFFF

Table 387 • **Rx Character Encode Error Count Threshold (3xEE09)**

Bit	Name	Description	Access	Default
15:0	Rx character encode error count threshold		RW	0xFFFF

Table 388 • **FEC Fixed Error Count Threshold (3xEE0A)**

Bit	Name	Description	Access	Default
15:0	FEC fixed error count threshold[31:16]		RW	0xFFFF

Table 389 • **FEC Fixed Error Count Threshold (3xEE0B)**

Bit	Name	Description	Access	Default
15:0	FEC fixed error count threshold[15:0]		RW	0xFFFF

Table 390 • **FEC Unfixable Error Count Threshold (3xEE0C)**

Bit	Name	Description	Access	Default
15:0	FEC unfixable error count threshold[31:16]		RW	0xFFFF

Table 391 • **FEC Unfixable Error Count Threshold (3xEE0D)**

Bit	Name	Description	Access	Default
15:0	FEC unfixable error count threshold[15:0]		RW	0xFFFF

Table 392 • **PCS Spare Control/Status (3xEF00 to 3xEF15)**

Bit	Name	Description	Access	Default
15:0	Reserved		RW	0x00

Table 393 • **PHYXS_CTRL1: PHY XS Control 1 (4x0000)**

Bit	Name	Description	Access	Default
15	SOFT_RST	Reset all MMDs. 0: Normal operation. 1: Resets the entire channel.	RW SC	0

Table 393 • **PHYXS_CTRL1: PHY XS Control 1 (4x0000) *(continued)***

Bit	Name	Description	Access	Default
14	LPBK_A	Enable PHY XS Network loopback (Loopback A)[1] 0: Disable 1: Enable	RW	0
13	SPEED_SEL_A	PHY XS Speed capability. 0: Unspecified 1: Operates at 10 Gbps or above	RO	1
12	Reserved	Value always 0, writes ignored.	RO	0
11	LOW_PWR_PHYXS	PHY XS low power mode control 0: Normal Operation. The internal TXEN signal will not be set to 0 due to the Low Power register bit. 1: Low Power Mode. Power dissipated in the core datapath, XAUI interface and PMA interface is reduced. The appropriate PMA connected to this channel is powered down when this bit is set. The PMA connected to this channel is a function of the datapath failover crosspoint control in global registers 1Ex0003.1 and 1Ex003.0. The internal TXEN signal will be 0. The TXEN signal can be routed out a GPIO pin to shut off the optics module's Tx driver if that is desirable. TXEN-inverted can also be transmitted from a GPIO pin.	RW	0
10:7	Reserved	Value always 0, writes ignored.	RO	0
6	SPEED_SEL_B	Speed selection 0: Unspecified 1: Operation at 10 Gbps and above	RO	1
5:2	SPEED_SEL_C	Speed selection	RO	0000
1:0	Reserved	Value always 0, writes ignored.	RO	0

1. When loopback A is enabled, XAUI signal detect has to be disabled by setting 4xE600.1 to 1.

Table 394 • **PHYXS_STAT1: PHY XS Status1 (4x0001)**

Bit	Name	Description	Access	Default
15:8	Reserved	Reserved (ignore when read)	RO	0
7	Fault	PHY XS fault status. Asserted when either the PHY XS FAULT_RX(4x0008.10) or PHY XS FAULT_TX (4x0008.11) is asserted. 0: No faults asserted 1: Fault(s) asserted	RO	
6:3	Reserved	Reserved (ignore when read)	RO	0
2	PHY XS transmit link status	PHY XS transmit link status 0: PHY XS transmit link is down (4x0018.12 = 0) 1: PHY XS transmit link is up (4x0018.12 = 1)	RO/LL	
1	Low power ability	Low power mode support ability 0: Not supported 1: Supported	RO	1
0	Reserved	Reserved (ignore when read)	RO	0

Table 395 • **PHYXS_DEVID1: PHY XS Device Identifier 1 (4x0002)**

Bit	Name	Description	Access	Default
15:0	DEV_ID_LSW	Upper 16 bits of a 32-bit unique PHY XS device identifier. Bits 3-18 of the device manufacturer's OUI. Device Identifier bits 31:16	RO	0x0007

Table 396 • **PHYXS_DEVID2: PHY XS Device Identifier 2 (4x0003)**

Bit	Name	Description	Access	Default
15:0	DEV_ID_MSW	Lower 16 bits of a 32-bit unique PHY XS device identifier. Bits 19-24 of the device manufacturer's OUI. Six-bit model number, and a four-bit revision number. Device Identifier bits 15:0	RO	0x0400

Table 397 • **PHYXS_SPEED: PHY XS Speed Capability (4x0004)**

Bit	Name	Description	Access	Default
15:1	Reserved	Reserved for future speeds (value always 0, writes ignored)	RO	0
0	RATE_ABILITY	PHY XS rate capability 0: Not capable of 10 Gbps 1: Capable of 10 Gbps	RO	1

Table 398 • **PHYXS_DEVPKG1: PHY XS Devices in Package 1 (4x0005)**

Bit	Name	Description	Access	Default
15:6	Reserved	Reserved (ignore when read)	RO	0000000000
5	DTE_XS_PRES	Indicates whether device includes DTS XS. 0: Not present 1: Present	RO	0
4	PHY_XS_PRES	Indicates whether device includes PHY XS. 0: Not present 1: Present	RO	1
3	PCS_PRES	Indicates whether PCS is present in the package 0: Not present 1: Present	RO	1
2	WIS_PRES	Indicates whether device includes WIS. NOTE: the read-only register should be a 1 as WIS is supported, however the default value is 0. Registers 1x0005.2 and 2x0005.2 correctly report the WIS block is present 0: Not present 1: Present	RO	1

Table 398 • **PHYXS_DEVPKG1: PHY XS Devices in Package 1 (4x0005) *(continued)***

Bit	Name	Description	Access	Default
1	PMD_PMA_PRES	Indicates whether PMA/PMD is present in the package 0: Not present 1: Present	RO	1
0	CLS22_PRES	Indicates whether Clause 22 registers are present in the package 0: Not present 1: Present	RO	0

Table 399 • **PHYXS_DEVPKG2: PHY XS Devices in Package 2 (4x0006)**

Bit	Name	Description	Access	Default
15	VS2_PRES	Vendor specific device 2 present 0: Not present 1: Present	RO	0
14	VS1_PRES	Vendor specific device 1 present 0: Not present 1: Present	RO	0
13:0	Reserved	Reserved (ignore when read)	RO	0

Table 400 • **PHYXS_STAT2: PHY XS Status 2 (4x0008)**

Bit	Name	Description	Access	Default
15:14	DEV_PRES	Reflects the presence of a MMD responding at this address 10: Device responding at this address 11: No device responding at this address 10: No device responding at this address 00: No device responding at this address	RO	10
13:12	Reserved	Reserved (ignore when read)	RO	00
11	FAULT_TX	Indicates a fault condition on the transmit path 0: No fault condition. XGXS lanes are aligned, 4x0018.12=1. 1: Fault condition on. XGXS lanes are not aligned, 4x0018.12=0. Linked to 1x9004.0. Read to either register clears both bits if fault condition no longer exists.	RO/LH	
10	FAULT_RX	Indicates a fault condition on the receive path 0: Rx PCS is locked to the data, is not reporting a high bit error rate, and there is no XAUI CMU loss of lock. 1: Rx PCS block is not locked to the data, is reporting a high bit error rate, or there is XAUI CMU loss of lock.	RO/LH	
9:0	Reserved	Reserved (ignore when read)	RO	0

Table 401 • **PHYXS_PKGID1: WIS Package Identifier 1 (4x000E)**

Bit	Name	Description	Access	Default
15:0	PKG_ID_MSW	Upper 16 bits of a 32-bit unique PHY XS package identifier. Bits 3-18 of the device manufacturer's OUI. Six-bit model number and a four-bit revision number.	RO	0

Table 402 • **PHYXS_PKGID2: WIS Package Identifier 2 (4x000F)**

Bit	Name	Description	Access	Default
15:0	PKG_ID_LSW	Lower 16 bits of a 32-bit unique PHY XS package identifier. Bits 19-24 of the device manufacturer's OUI. Six-bit model number and a four-bit revision number.	RO	0

Table 403 • **PHYXS_STAT3: PHY XS Status 3 (4x0018)**

Bit	Name	Description	Access	Default
15:13	Reserved	Reserved (ignore when read)	RO	0
12	LANES_ALIGNED	PHY XGXS lane alignment status 0: Incoming PHY XS transmit path lanes are not aligned. 1: Incoming PHY XS transmit path lanes are aligned.	RO	
11	PATT_ABILITY	PHY XGXS test pattern generation ability 0: PHY XS is not able to generate test patterns. 1: PHY XS is able to generate test patterns.	RO	1
10	LPBK_ABILITY	PHY XGXS loopback ability 0: PHY XS does not have the ability to perform a loopback function 1: PHY XS has the ability to perform a loopback function	RO	1
9:4	Reserved	Reserved (ignore when read)	RO	0
3	LANE3_SYNC	PHY XGXS lane 3 synchronization status 0: Not synchronized 1: Synchronized	RO	
2	LANE2_SYNC	PHY XGXS lane 2 synchronization status 0: Not synchronized 1: Synchronized	RO	
1	LANE1_SYNC	PHY XGXS lane 1 synchronization status 0: Not synchronized 1: Synchronized	RO	
0	LANE0_SYNC	PHY XGXS lane 0 synchronization status 0: Not synchronized 1: Synchronized	RO	

Table 404 • **PHYXS_TSTCTRL1: PHY XGXS Test Control 1 (4x0019)**

Bit	Name	Description	Access	Default
15:3	Reserved	Reserved (ignore when read)	RO	0
2	TST_PATT_GEN_ENA	PHYXS test pattern generator enable 0: Disable 1: Enable	RW	0
1:0	TST_PATT_GEN_SEL1	PHYXS test pattern generator selection. 4x8000.4 is the MSB 4x0019.1:0 are the two LSBs 111: 2^7 PRBS Pattern 110: Fibre channel CJPAT 101: Continuous jitter test pattern 100: Continuous random test pattern 011: Disable pattern generator 010: Mixed frequency test pattern 001: Low frequency test pattern 000: High frequency test pattern. Register 4xE604 defines the Fibre Channel CJPAT format used by the pattern generator.	RW	11

Table 405 • **PHYXS_TSTCTRL2: PHY XS Test Control 2 (4x8000)**

Bit	Name	Description	Access	Default
15:5	Reserved	Reserved (ignore when read)	RO	0
4	TST_PATT_GEN_SEL2	PHYXS test pattern generator selection. 4x8000.4 is the MSB 4x0019.1:0 are the two LSBs 111: 2^7 PRBS Pattern 110: Fibre channel CJPAT 101: Continuous jitter test pattern 100: Continuous random test pattern 011: Disable pattern generator 010: Mixed frequency test pattern 001: Low frequency test pattern 000: High frequency test pattern. Register 4xE604 defines the Fibre Channel CJPAT format used by the pattern generator.	RW	0
3	TST_PATT_CHK_ENA	PHYXS test pattern checker enable. 0: Disable 1: Enable	RW	0

Table 405 • **PHYXS_TSTCTRL2: PHY XS Test Control 2 (4x8000) *(continued)***

Bit	Name	Description	Access	Default
2:0	TST_PATT_CHK_SEL	PHYXS test pattern checker pattern selection. 111: 2^7 PRBS Pattern 110: Fibre channel CJPAT 101: Continuous jitter test pattern 100: Continuous random test pattern 011: Disable pattern generator 010: Mixed frequency test pattern 001: Low frequency test pattern 000: High frequency test pattern. Register 4xE604 defines the Fibre Channel CJPAT format used by the pattern checker.	RW	011

Table 406 • **PHYXS_TSTSTAT: PHY XS Test Pattern Check Status (4x8001)**

Bit	Name	Description	Access	Default
15:4	Reserved	Reserved (ignore when read)	RO	0
3	LANE3_PATT_CHK	Lane 3 test pattern check result 0: Pattern check fail 1: Pattern check pass	RO	0
2	LANE2_PATT_CHK	Lane 2 test pattern check result 0: Pattern check fail 1: Pattern check pass	RO	0
1	LANE1_PATT_CHK	Lane 1 test pattern check result 0: Pattern check fail 1: Pattern check pass	RO	0
0	LANE0_PATT_CHK	Lane 0 test pattern check result 0: Pattern check fail 1: Pattern check pass	RO	0

Table 407 • **Factory Test Register (4x8002)**

Bit	Name	Description	Access	Default
15:5	Reserved	Factory test only.	RO	0
4	Reserved	Factory test only. Do not modify this bit group.	RW SC	0
3	Reserved	Factory test only. Do not modify this bit group.	RW	1
2:0	Reserved	Factory test only. Do not modify this bit group.	RW	100

Table 408 • **Factory Test Register (4x8003)**

Bit	Name	Description	Access	Default
15:0	Reserved	Factory test only.	RO CR	0

Table 409 • **Factory Test Register (4x8004)**

Bit	Name	Description	Access	Default
15:0	Reserved	Factory test only.	RO CR	0

Table 410 • **Factory Test Register (4x8005)**

Bit	Name	Description	Access	Default
15:5	Reserved	Factory test only.	RO	0
4	Reserved	Factory test only. Do not modify this bit group.	RW SC	0
3	Reserved	Factory test only. Do not modify this bit group.	RW	1
2:0	Reserved	Factory test only. Do not modify this bit group.	RW	100

Table 411 • **Factory Test Register (4x8006)**

Bit	Name	Description	Access	Default
15:0	Reserved	Factory test only.	RO CR	0

Table 412 • **Factory Test Register (4x8007)**

Bit	Name	Description	Access	Default
15:0	Reserved	Factory test only.	RO CR	0

Table 413 • **Factory Test Register (4x8008)**

Bit	Name	Description	Access	Default
15:5	Reserved	Factory test only.	RO	0
4	Reserved	Factory test only. Do not modify this bit group.	RW SC	0
3	Reserved	Factory test only. Do not modify this bit group.	RW	1
2:0	Reserved	Factory test only. Do not modify this bit group.	RW	100

Table 414 • **Factory Test Register (4x8009)**

Bit	Name	Description	Access	Default
15:0	Reserved	Factory test only.	RO CR	0

Table 415 • **Factory Test Register (4x800A)**

Bit	Name	Description	Access	Default
15:0	Reserved	Factory test only.	RO CR	0

Table 416 • **PHYXS_TPERR_CTRL: PHY XS Test Pattern Error Counter Control (4x800B)**

Bit	Name	Description	Access	Default
15:5	Reserved	Reserved (ignore when read)	RO	0
4	TP_CNT_CLR	Clear test pattern mismatch error counter 0: Normal operation 1: Clear counter	RW SC	0
3	TP_CNT_ENA	Test pattern mismatch error counter enable 0: Disable 1: Enable	RW	1
2:0	TP_CNT_SEL	Select test pattern mismatch error source 111: Reserved 110: Reserved 101: Reserved 100: Cumulative error count on all lanes 011: Error count on lane 3 010: Error count on lane 2 001: Error count on lane 1 000: Error count on lane 0	RW	100

Table 417 • **PHYXS_TPERR_CNT0: PHY XS Test Pattern Error Counter 0 (LSW) (4x800C)**

Bit	Name	Description	Access	Default
15:0	TP_CNT_LSW	Test pattern mismatch error counter. Lower 16-bits of the saturating (Nonrollover) counter. Both MSW and LSW registers must be read to clear the counter.	RO CR	0

Table 418 • **PHYXS_TPERR_CNT0: PHY XS Test Pattern Error Counter 1 (MSW) (4x800D)**

Bit	Name	Description	Access	Default
15:0	TP_CNT_MSW	Test pattern mismatch error counter. Upper 16-bits of the saturating (Nonrollover) counter. Both MSW and LSW registers must be read to clear the counter.	RO CR	0

Table 419 • **PHYXS_XAUI_CTRL1: PHY XS XAUI Control 1 (4x800E)**

Bit	Name	Description	Access	Default
15:14	Reserved	Reserved (ignore when read)	RO	0

Table 419 • **PHYXS_XAUI_CTRL1: PHY XS XAUI Control 1 (4x800E) *(continued)***

Bit	Name	Description	Access	Default
13	LPBK_B	Loopback B enable (PHY XS shallow system). 0: Disable 1: Enable SFI interface's output driver is enabled. Use register 1xA100.1:0 to select options to transmit all 1's, 0's, 0x00FF pattern, or XAUI data from SFI driver when loopback B is enabled.	RW	0
12	RX_FIFO_RST	Reset PHY XS Rx path FIFOs 0: Resets FIFOs 1: Normal operation	RW SC	1
11:9	Reserved	Factory test only.	RO	1
8:5	TX_SQUELCH_XAUI	Force received XAUI data to zero (bit 8 corresponds to lane 3, and bit 5 corresponds to lane 0). Local fault will be seen at the SFI interface when data is forced to 1. The lane controlled by these bits is not adjusted by the TX_LANE_SWAP register (4x800F.10). 0: Normal operation 1: Force data to zero	RW	0
4	Reserved	Factory test only.	RO	0
3	Reserved	Factory test only. Do not modify this bit group.	RW	0
2:0	Reserved	Factory test only.	RO	0

Table 420 • **PHYXS_XAUI_CTRL2: PHY XS XAUI Control 2 (4x800F)**

Bit	Name	Description	Access	Default
15:13	Reserved	Factory test only. Do not modify this bit group.	RW	0
12	Reserved	Factory test only. Do not modify this bit group.	RW	1
11	XGXS BIST pattern generator	XGXS BIST pattern generator enable 0: Disable 1: Enable	RW	0
10	TX_LANE_SWAP	Enables lane order of incoming XAUI data in the transmit data path to be swapped prior to lane alignment in 10G mode. Swaps lane 0 with lane 3 and swaps lane 1 with lane 2 when enabled. This bit provides the option to use either lane 0 or lane 3 in 1G pass-through operating modes. 0: Enable 1: Disable	RW	1
9	RX_LANE_SWAP	Enables lane order of out going XAUI lanes in the receive data path to be swapped prior to transmission from the XAUI pins. Swaps lane 0 with lane 3 and swaps lane 1 with lane 2 when enabled. This bit provides the option to transmit data on lane 0 or lane 3 in 1G pass-through operating modes. 0: Enable 1: Disable	RW	1

Table 420 • **PHYXS_XAUI_CTRL2: PHY XS XAUI Control 2 (4x800F) *(continued)***

Bit	Name	Description	Access	Default
8:7	Reserved	Factory test only. Do not modify this bit group.	RW	0
6	TX_INV	Disable inversion of the XAUI input data in the transmit path. 0: Enable 1: Disable	RW	1
5	RX_INV	Disable inversion of the XAUI output data in the receive path. 0: Enable 1: Disable	RW	1
4:0	Reserved	Factory test only. Do not modify this bit group.	RW	0

Table 421 • **PHYXS_RXEQ_CTRL: PHY XS XAUI Rx Equalization Control (4x8010)**

Bit	Name	Description	Access	Default
15:12	LANE0_EQ	Equalization setting for XAUI input lane 0 0000: 0 dB 0001: 1.41 dB 0010: 2.24 dB 0011: 2.83 dB 0101: 4.48 dB 0110: 5.39 dB 0111: 6.07 dB 1001: 6.18 dB 1010: 7.08 dB 1011: 7.79 dB 1101: 9.96 dB 1110: 10.84 dB 1111: 11.55 dB	RW	1010
11:8	LANE1_EQ	Equalization setting for XAUI input lane 1 Refer to bits [15:12] for settings	RW	1010
7:4	LANE2_EQ	Equalization setting for XAUI input lane 2 Refer to bits [15:12] for settings	RW	1010
3:0	LANE3_EQ	Equalization setting for XAUI input lane 3 Refer to bits [15:12] for settings	RW	1010

Table 422 • **PHYXS_TXPE_CTRL: PHY XS XAUI Tx Pre-emphasis Control (4x8011)**

Bit	Name	Description	Access	Default
15	Reserved	Reserved (ignore when read)	RO	0
14:13	LANE0_PE	Preemphasis setting for XAUI output lane 0 00: 0 dB 01: ~2.5 dB 10: ~6 dB 11: ~12 dB	RW	10
12	Reserved	Reserved (ignore when read)	RO	0

Table 422 • **PHYXS_TXPE_CTRL: PHY XS XAUI Tx Pre-emphasis Control (4x8011)** ***(continued)***

Bit	Name	Description	Access	Default
11:10	LANE1_PE	Preemphasis setting for XAUI output lane 0 Refer to bits [14:13] for settings	RW	10
9	Reserved	Reserved (ignore when read)	RO	0
8:7	LANE2_PE	Preemphasis setting for XAUI output lane 0 Refer to bits [14:13] for settings	RW	10
6	Reserved	Reserved (ignore when read)	RO	0
5:4	LANE3_PE	Preemphasis setting for XAUI output lane 0 Refer to bits [14:13] for settings	RW	10
3:2	LOS_THRES	The following estimated settings can be used for various LOS_THRES. 11: 80 mV to 205 mV differential peak-peak 10: 70 mV to 195 mV differential peak-peak 01: 60 mV to 185 mV differential peak-peak 00: 50 mV to 175 mV differential peak-peak	RW	0
1	HS_ENA	Enable XAUI output high swing mode 0: Disable 1: Enable Note: Low swing mode is recommended as there is no significant output amplitude difference between high swing mode and low swing mode.	RW	0
0	Reserved	Reserved (ignore when read)	RO	0

Table 423 • **PHYXS_RXLOS_STAT: PHY XS Rx Loss of Signal Status (4x8012)**

Bit	Name	Description	Access	Default
15:12	Reserved	Reserved (ignore when read)	RO	0
11	LANE3_FIFO_ERR	FIFO Overflow in the transmit path XAUI serializer, lane 3. 0: No FIFO Overflow 1: FIFO Overflow **Note:** The FIFO is only used in loopback B mode. Ignore in all other modes.	RO	
10	LANE2_FIFO_ERR	FIFO Overflow in the transmit path XAUI serializer, lane 2. 0: No FIFO Overflow 1: FIFO Overflow **Note:** The FIFO is only used in loopback B mode. Ignore in all other modes.	RO	
9	LANE1_FIFO_ERR	FIFO Overflow in the transmit path XAUI serializer, lane 1. 0: No FIFO Overflow 1: FIFO Overflow **Note:** The FIFO is only used in loopback B mode. Ignore in all other modes.	RO	

Table 423 • **PHYXS_RXLOS_STAT: PHY XS Rx Loss of Signal Status (4x8012) *(continued)***

Bit	Name	Description	Access	Default
8	LANE0_FIFO_ERR	FIFO Overflow in the transmit path XAUI serializer, lane 0. 0: No FIFO Overflow 1: FIFO Overflow **Note:** The FIFO is only used in loopback B mode. Ignore in all other modes.	RO	
7:6	Reserved	Reserved (ignore when read)	RO	0
5	GLBL_SYNC	PHY XS code group synchronization status 0: At least one lane is not in sync 1: All lanes are in sync	RO	
4	XS_LOL	PHY XS PLL loss of lock 0: PLL in lock 1: PLL loss of lock	RO	
3	LANE3_LOSN	Loss of signal status for lane 3 XAUI input. Active low alarm condition.[1] 0: Lane 3 loss of signal 1: Lane 3 signal present	RO	
2	LANE2_LOSN	Loss of signal status for lane 2 XAUI input. Active low alarm condition.[1] 0: Lane 2 loss of signal 1: Lane 2 signal present	RO	
1	LANE1_LOSN	Loss of signal status for lane 1 XAUI input. Active low alarm condition.[1] 0: Lane 1 loss of signal 1: Lane 1 signal present	RO	
0	LANE0_LOSN	Loss of signal status for lane 0 XAUI input. Active low alarm condition.[1] 0: Lane 0 loss of signal 1: Lane 0 signal present	RO	

1. While there is no issue on the actual data path, this real time detection signal can chatter when the amplitude of the input signal is larger than 1200 mV or the equivalent frequency is above 1.6 GHz.

Table 424 • **PHYXS_RXSD_STAT: PHY XS Rx Signal Detect Status (4xE600)**

Bit	Name	Description	Access	Default
15:2	Reserved	Reserved (ignore when read)	RO	0
1	GLBL_SIG_DET	Disable signal detect function of all XAUI inputs 0: Enabled 1: Disabled.	RW	0
0	SIG_DET	Global signal detect status 0: No signal detected in at least one lane. 1: Signal detected in all lanes.	RO	

Table 425 • **Factory Test Register (4xE601)**

Bit	Name	Description	Access	Default
15:9	Reserved	Factory test only.	RO	0
8	Reserved	Factory test only. Do not modify this bit group.	RW	0
7:6	Reserved	Factory test only. Do not modify this bit group.	RW	01
5:4	Reserved	Factory test only. Do not modify this bit group.	RW	01
3:2	Reserved	Factory test only. Do not modify this bit group.	RW	01
1:0	Reserved	Factory test only. Do not modify this bit group.	RW	01

Table 426 • **PHYXS_TXPD_CTRL: PHY XS XAUI Tx Power Down Control (4xE602)**

Bit	Name	Description	Access	Default
15	Reserved	Reserved (ignore when read)	RO	0
14	LANE3_TX_PD	Power down XAUI input lane 3 in the transmit data path. 0: Powered up 1: Powered down. The lane number powered down is not a function of lane swap control (4x800F.10).	RW	0
13	LANE2_TX_PD	Power down XAUI input lane 2 in the transmit data path. 0: Powered up 1: Powered down. The lane number powered down is not a function of lane swap control (4x800F.10).	RW	0
12	LANE1_TX_PD	Power down XAUI input lane 1 in the transmit data path. 0: Powered up 1: Powered down. The lane number powered down is not a function of lane swap control (4x800F.10).	RW	0
11	LANE0_TX_PD	Power down XAUI input lane 0 in the transmit data path. 0: Powered up 1: Powered down. The lane number powered down is not a function of lane swap control (4x800F.10).	RW	0
10:9	LPBK_B_CLK	Select which of the 4 recovered clocks will be used for loopback B 11: Lane 3 10: Lane 2 01: Lane 1 00: Lane 0	RW	00

Table 426 • **PHYXS_TXPD_CTRL: PHY XS XAUI Tx Power Down Control (4xE602)** ***(continued)***

Bit	Name	Description	Access	Default
8	LPBK_B_CLKSEL	1 of 4 XAUI lane recovered clocks are used to retime the XAUI transmitted data when loopback B is enabled. This bit enables automatic selection of the best recovered clock used to retime the data. 0: Manual select (see bits 10:9) 1: Auto select	RW	1
7:6	Reserved	Factory test only.	RO	0
5:4	Reserved	Factory test only.	RO	0
3:2	Reserved	Factory test only.	RO	0
1:0	Reserved	Factory test only.	RO	0

Table 427 • **PHYXS_RXPD_CTRL: PHY XS XAUI Rx Power Down Control (4xE603)**

Bit	Name	Description	Access	Default
15:10	Reserved	Reserved (ignore when read)	RO	0
9	Reserved	Factory test only. Do not modify this bit group.	RW	0
8	Reserved	Factory test only. Do not modify this bit group.	RW	1
7	LANE3_RX_PD	Power down XAUI output lane 3 in the receive data path. 0: Powered up 1: Powered down. The lane number powered down is not a function of lane swap control (4x800F.9).	RW	0
6	LANE2_RX_PD	Power down XAUI output lane 2 in the receive data path. 0: Powered up 1: Powered down. The lane number powered down is not a function of lane swap control (4x800F.9).	RW	0
5	LANE1_RX_PD	Power down XAUI output lane 1 in the receive data path. 0: Powered up 1: Powered down. The lane number powered down is not a function of lane swap control (4x800F.9).	RW	0
4	LANE0_RX_PD	Power down XAUI output lane 0 in the receive data path. 0: Powered up 1: Powered down. The lane number powered down is not a function of lane swap control (4x800F.9).	RW	0
3	LANE3_RX_SQU	Force PHY XS Rx lane 3 XAUI output to zero 0: Output normal 1: Output squelched The lane number powered down is not a function of lane swap control (4x800F.9).	RW	0

Table 427 • **PHYXS_RXPD_CTRL: PHY XS XAUI Rx Power Down Control (4xE603)** ***(continued)***

Bit	Name	Description	Access	Default
2	LANE2_RX_SQU	Force PHY XS Rx lane 2 XAUI output to zero 0: Output normal 1: Output squelched The lane number powered down is not a function of lane swap control (4x800F.9).	RW	0
1	LANE1_RX_SQU	Force PHY XS Rx lane 1 XAUI output to zero 0: Output normal 1: Output squelched The lane number powered down is not a function of lane swap control (4x800F.9).	RW	0
0	LANE0_RX_SQU	Force PHY XS Rx lane 0 XAUI output to zero 0: Output normal 1: Output squelched The lane number powered down is not a function of lane swap control (4x800F.9).	RW	0

Table 428 • **FC_CJPAT_SEL (4xE604)**

Bit	Name	Description	Access	Default
15:2	Reserved	Factory Test Only. Do Not Modify	RW	0
1	FC_CJPAT_CHK_MODE31	Selects 10G Fibre Channel (10GFC) spec revision supported by the FC CJPAT data pattern checker in the PHY XS block. 0: Revision 3.5. 1: Revision 3.1.	RW	1
0	FC_CJPAT_GEN_MODE31	Selects 10G Fibre Channel (10GFC) spec revision supported by the FC CJPAT data pattern generator in the PHY XS block. 0: Revision 3.5. 1: Revision 3.1.	RW	1

Table 429 • **Factory Test Registers (4xE610 to 4xEF15)**

Bit	Name	Description	Access	Default
15:0	Reserved	Factory test only. Do not modify this bit group.	RW	0x00

Table 430 • **Auto-Negotiation Control (7x0000)**

Bit	Name	Description	Access	Default
15	Reset	0: No effect 1: Resets AN blocks	RW SC	0
14:13	Reserved	Reserved (ignore when read)	RO	0
12	AN Enable	0: Disable AN 1: Enable AN	RW	0
11:10	Reserved	Reserved (ignore when read)	RO	0

Table 430 • **Auto-Negotiation Control (7x0000) *(continued)***

Bit	Name	Description	Access	Default
9	AN Restart	0: No effect 1: Restart AN	RW SC	0
8:0	Reserved	Reserved (ignore when read)	RO	0

Table 431 • **AN Status (7x0001)**

Bit	Name	Description	Access	Default
15:10	Reserved	Reserved (ignore when read)	RO	0
9	Parallel detection fault	0: Fault has not been detected via parallel detection function 1: Fault detected via parallel detection function	RO/LH	0
8	Reserved	Reserved (ignore when read)	RO	0
7	Extended next page status	0: Extended next page is not allowed 1: Extended next page is used	RO	0
6	Page received	0: A page has not been received 1: A page has been received	RO/LH	0
5	Auto-Negotiation complete	0: AN process not completed 1: AN process completed	RO	0
4	Remote fault	0: no remote fault condition detected 1: remote fault condition detected	RO/LH	0
3	Auto-Negotiation ability	0: PHY is not able to perform AN 1: PHY is able to perform AN	RO	1
2	Link status	0: Link is down 1: Link is up	RO/LL	1
1	Reserved	Reserved (ignore when read)	RO	0
0	Link partner Auto-Negotiation ability	0: LP is not able to perform AN 1: LP is able to perform AN	RO	0

Table 432 • **AN Advertisement Register 1 (7x0010)**

Bit	Name	Description	Access	Default
15	Next page	See IEEE 802.3ap	RW	0
14	Ack (always 0)	See IEEE 802.3ap	RO	0
13	Remote fault	See IEEE 802.3ap	RW	0
12:5	D[12:5]	See IEEE 802.3ap	RW	0
4:0	Selector field	See IEEE 802.3ap	RW	0

Table 433 • **AN Advertisement Register 2 (7x0011)**

Bit	Name	Description	Access	Default
15:0	D[31:16]	See IEEE 802.3ap	RW	0

Table 434 • **AN Advertisement Register 3 (7x0012)**

Bit	Name	Description	Access	Default
15:0	D[47:32]	See IEEE 802.3ap	RW	0

Table 435 • **AN LP Base Page Ability Register 1 (7x0013)**

Bit	Name	Description	Access	Default
15:0	D[15:0]	See IEEE 802.3ap	RO	0

Table 436 • **AN LP Base Page Ability Register 2 (7x0014)**

Bit	Name	Description	Access	Default
15:0	D[31:16]	See IEEE 802.3ap	RO	0

Table 437 • **AN LP Base Page Ability Register 3 (7x0015)**

Bit	Name	Description	Access	Default
15:0	D[47:32]	See IEEE 802.3ap	RO	0

Table 438 • **AN XNP Transmit Register 1 (7x0016)**

Bit	Name	Description	Access	Default
15	Next page	See IEEE 802.3ap	RW	0
14	Reserved	See IEEE 802.3ap	RO	0
13	Message page	See IEEE 802.3ap	RW	0
12	Ack 2	See IEEE 802.3ap	RW	0
11	Toggle	See IEEE 802.3ap	RO	0
10:0	Message code field	See IEEE 802.3ap	RW	0

Table 439 • **AN XNP Transmit Register 2 (7x0017)**

Bit	Name	Description	Access	Default
15:0	Unformatted code field 1	See IEEE 802.3ap	RW	0

Table 440 • **AN XNP Transmit Register 3 (7x0018)**

Bit	Name	Description	Access	Default
15:0	Unformatted code field	See IEEE 802.3ap	RW	0

Table 441 • **AN LP XNP Ability Register 1 (7x0019)**

Bit	Name	Description	Access	Default
15	Next page	See IEEE 802.3ap	RO	0
14	Ack	See IEEE 802.3ap	RO	0
13	Message page	See IEEE 802.3ap	RO	0
12	Ack 2	See IEEE 802.3ap	RO	0
11	Toggle	See IEEE 802.3ap	RO	0
10:0	Message code field	See IEEE 802.3ap	RO	0

Table 442 • **AN LP XNP Ability Register 2 (7x001A)**

Bit	Name	Description	Access	Default
15:0	Unformatted code field 1	See IEEE 802.3ap	RO	0

Table 443 • **AN LP XNP Ability Register 3 (7x001B)**

Bit	Name	Description	Access	Default
15:0	Unformatted code field 2	See IEEE 802.3ap	RO	0

Table 444 • **BPS (7x0030)**

Bit	Name	Description	Access	Default
15:5	Reserved	Reserved (ignore when read)	RO	0
4	10GBASE-KR FEC	0: PMA/PMD is not negotiated to perform 10GBASE-KR FEC 1: PMA/PMD is negotiated to perform 10GBASE-KR FEC	RO	0
3	10GBASE-KR	0: PMA/PMD is not negotiated to perform 10GBASE-KR 1: PMA/PMD is negotiated to perform 10GBASE-KR	RO	0
2	10GBASE-KX4	0: PMA/PMD is not negotiated to perform 10GBASE-KX4 1: PMA/PMD is negotiated to perform 10GBASE-KX4	RO	0
1	1000BASE-KX	0: PMA/PMD is not negotiated to perform 1000BASE-KX 1: PMA/PMD is negotiated to perform 1000BASE-KX	RO	0
0	BP AN ability	0: No 10GBASE-KR, 10GBASE-KX4 or 1000BASE-KX PHY type is implemented 1: A 10GBASE-KR, 10GBASE-KX4 or 1000BASE-KX PHY type is implemented	RO	1

Table 445 • **Factory Test Register (7x8001)**

Bit	Name	Description	Access	Default
15:10	Reserved	Factory test only.	RO	0
9	Reserved	Factory test only. Do not modify this bit group.	RW	0
8	Reserved	Factory test only.	RO	0
7:4	Reserved	Factory test only. Do not modify this bit group.	RW	0
3:2	Reserved	Factory test only. Do not modify this bit group.	RW	1
1	Reserved	Factory test only.	RO	0
0	Reserved	Factory test only. Do not modify this bit group.	RW	0

Table 446 • **Factory Test Register (7x8013)**

Bit	Name	Description	Access	Default
15:0	Reserved	Factory test only. Do not modify this bit group.	RW	0

Table 447 • **Factory Test Register (7x8014)**

Bit	Name	Description	Access	Default
15:0	Reserved	Factory test only. Do not modify this bit group.	RW	0

Table 448 • **Factory Test Register (7x8015)**

Bit	Name	Description	Access	Default
15:0	Reserved	Factory test only. Do not modify this bit group.	RW	0

Table 449 • **Factory Test Register (7x8019)**

Bit	Name	Description	Access	Default
15	Reserved	Factory test only. Do not modify this bit group.	RW	0
14	Reserved	Factory test only.	RO	0
13:0	Reserved	Factory test only. Do not modify this bit group.	RW	0

Table 450 • **Factory Test Register (7x801A)**

Bit	Name	Description	Access	Default
15:0	Reserved	Factory test only. Do not modify this bit group.	RW	0

Table 451 • **Factory Test Register (7x801B)**

Bit	Name	Description	Access	Default
15:0	Reserved	Factory test only. Do not modify this bit group.	RW	0

Table 452 • **Factory Test Register (7x8030)**

Bit	Name	Description	Access	Default
15:5	Reserved	Factory test only.	RO	0
4:1	Reserved	Factory test only. Do not modify this bit group.	RW	0
0	Reserved	Factory test only.	RO	1

Table 453 • **Factory Test Register (7x8040)**

Bit	Name	Description	Access	Default
15:0	Reserved	Factory test only. Do not modify this bit group.	RO	0

Table 454 • **Factory Test Register (7x8041)**

Bit	Name	Description	Access	Default
15:0	Reserved	Factory test only. Do not modify this bit group.	RO	0

Table 455 • **Factory Test Register (7x8042)**

Bit	Name	Description	Access	Default
15:0	Reserved	Factory test only. Do not modify this bit group.	RO	0

Table 456 • **Factory Test Register (7x8043)**

Bit	Name	Description	Access	Default
15:0	Reserved	Factory test only. Do not modify this bit group.	RO	0

Table 457 • **Factory Test Register (7x8044)**

Bit	Name	Description	Access	Default
15:0	Reserved	Factory test only. Do not modify this bit group.	RO	0

Table 458 • **Factory Test Register (7x8045)**

Bit	Name	Description	Access	Default
15:0	Reserved	Factory test only. Do not modify this bit group.	RO	0

Table 459 • **Factory Test Register (7x8046)**

Bit	Name	Description	Access	Default
15:0	Reserved	Factory test only. Do not modify this bit group.	RO	0

Table 460 • **Factory Test Register (7x8047)**

Bit	Name	Description	Access	Default
15:0	Reserved	Factory test only. Do not modify this bit group.	RO	0

Table 461 • **Factory Test Register (7x8048)**

Bit	Name	Description	Access	Default
15:0	Reserved	Factory test only. Do not modify this bit group.	RO	0

Table 462 • **AN Vendor Status (7x8100)**

Bit	Name	Description	Access	Default
15:3	Reserved	Reserved (ignore when read)	RO	0
2:1	link_HCD	Negotiated rate: 00: NULL 01: KR_10G 10: KX4_10G 11: KX_1G	RO	0
0	Reserved	Reserved (ignore when read)	RO	0

Table 463 • **AN break_link_timer Setting 1 (7x810E)**

Bit	Name	Description	Access	Default
15:0	maxval[15:0]	Lower 16 bits of 32-bit programmable timer	RW	0x7C6D

Table 464 • **AN break_link_timer Setting 2 (7x810F)**

Bit	Name	Description	Access	Default
15:0	maxval[31:16]	Upper 16 bits of 32-bit programmable timer	RW	0x004D

Table 465 • **AN an_wait_timer Setting 1 (7x8110)**

Bit	Name	Description	Access	Default
15:0	maxval[15:0]	Lower 16 bits of 32-bit programmable timer	RW	0xC346

Table 466 • **AN an_wait_timer Setting 2 (7x8111)**

Bit	Name	Description	Access	Default
15:0	maxval[31:16]	Upper 16 bits of 32-bit programmable timer	RW	0x0023

Table 467 • **AN link_fail_inhibit_short_timer Setting 1 (7x8112)**

Bit	Name	Description	Access	Default
15:0	maxval[15:0]	Lower 16 bits of 32-bit programmable timer	RW	0xA4E9

Table 468 • **AN link_fail_inhibit_short_timer Setting 2 (7x8113)**

Bit	Name	Description	Access	Default
15:0	maxval[31:16]	Upper 16 bits of 32-bit programmable timer	RW	0x0035

Table 469 • **AN link_fail_inhibit_long_timer Setting 1 (7x8114)**

Bit	Name	Description	Access	Default
15:0	maxval[15:0]	Lower 16 bits of 32-bit programmable timer	RW	0x01C5

Table 470 • **AN link_fail_inhibit_long_timer Setting 2 (7x8115)**

Bit	Name	Description	Access	Default
15:0	maxval[31:16]	Upper 16 bits of 32-bit programmable timer	RW	0x025A

Table 471 • **AN page_detect_timer Setting 1 (7x8116)**

Bit	Name	Description	Access	Default
15:0	maxval[15:0]	Lower 16 bits of 32-bit programmable timer	RW	0

Table 472 • **AN page_detect_timer Setting 2 (7x8117)**

Bit	Name	Description	Access	Default
15:0	maxval[31:16]	Upper 16 bits of 32-bit programmable timer	RW	0

Table 473 • **AN link_status_10G_timer Setting 1 (7x8118)**

Bit	Name	Description	Access	Default
15:0	maxval[15:0]	Lower 16 bits of 32-bit programmable timer	RW	0

Table 474 • **AN link_status_10G_timer Setting 2 (7x8119)**

Bit	Name	Description	Access	Default
15:0	maxval[31:16]	Upper 16 bits of 32-bit programmable timer	RW	0

Table 475 • **AN link_status_3G_timer Setting 1 (7x811A)**

Bit	Name	Description	Access	Default
15:0	maxval[15:0]	Lower 16 bits of 32-bit programmable timer	RW	0

Table 476 • **Reserved (7x811B)**

Bit	Name	Description	Access	Default
15:0	maxval[31:16]	Upper 16 bits of 32-bit programmable timer	RW	0

Table 477 • **Reserved (7x811C)**

Bit	Name	Description	Access	Default
15:0	maxval[15:0]	Lower 16 bits of 32-bit programmable timer	RW	0

Table 478 • **AN link_status_1G_timer Setting 2 (7x811D)**

Bit	Name	Description	Access	Default
15:0	maxval[31:16]	Upper 16 bits of 32-bit programmable timer	RW	0

Table 479 • **Factory Test Register (7x811E)**

Bit	Name	Description	Access	Default
15:8	Reserved	Factory test only.	RO	0
7	Reserved	Factory test only. Do not modify this bit group.	RW	0
6:0	Reserved	Factory test only. Do not modify this bit group.	RW SC	0

Table 480 • **Factory Test Register (7x811F)**

Bit	Name	Description	Access	Default
15:7	Reserved	Factory test only.	RO	0
6:0	Reserved	Factory test only.	RO/LH	0

Table 481 • **AN Hardware Arbitration State Machine State (7x8120)**

Bit	Name	Description	Access	Default
15	base_page	0: Transmitting next_page codewords 1: Transmitting base_page codewords	RO	0
14	np_rx	1: NP bit is set in received codeword	RO	0
13:12	Reserved	Reserved (ignore when read)	RO	0
11	training_required	1: HCD is KR_10G, and Link training is required	RO	0
10	RATE_DETECT	0: ASM is not in this state 1: ASM is in this state	RO	0
9	NXTPG_WAIT	0: ASM is not in this state 1: ASM is in this state	RO	0
8	AN_GOOD	0: ASM is not in this state 1: ASM is in this state	RO	0
7	PARLL_DET_FAULT	0: ASM is not in this state 1: ASM is in this state	RO	0
6	AN_GOOD_CHECK	0: ASM is not in this state 1: ASM is in this state	RO	0
5	COMPLETE_ACKNOWLEDGE	0: ASM is not in this state 1: ASM is in this state	RO	0
4	LINK_STATUS_CHECK	0: ASM is not in this state 1: ASM is in this state	RO	0
3	ACKNOWLEDGE_DETECT	0: ASM is not in this state 1: ASM is in this state	RO	0
2	ABILITY_DETECT	0: ASM is not in this state 1: ASM is in this state	RO	0
1	TRANSMIT_DISABLE	0: ASM is not in this state 1: ASM is in this state	RO	0
0	AN_ENABLE	0: ASM is not in this state 1: ASM is in this state	RO	0

Table 482 • **Factory Test Register (7x8200)**

Bit	Name	Description	Access	Default
15:13	Reserved	Factory test only. Do not modify this bit group.	RW	0
12	Reserved	Factory test only.	RO	0
11:10	Reserved	Factory test only. Do not modify this bit group.	RW	0

Table 482 • **Factory Test Register (7x8200)** ***(continued)***

Bit	Name	Description	Access	Default
9	Reserved	Factory test only.	RO	0
8:7	Reserved	Factory test only. Do not modify this bit group.	RW	0
6	Reserved	Factory test only.	RO	0
5:0	Reserved	Factory test only. Do not modify this bit group.	RW	0

Table 483 • **Factory Test Register (7x8201)**

Bit	Name	Description	Access	Default
15:8	Reserved	Factory test only.	RO	0
7:5	Reserved	Factory test only.	RO/LH	0
4	Reserved	Factory test only.	RO	1
3:1	Reserved	Factory test only.	RO/LH	0
0	Reserved	Factory test only.	RO	0

Table 484 • **Factory Test Register (7x8203)**

Bit	Name	Description	Access	Default
15:0	Reserved	Factory test only. Do not modify this bit group.	RW	0

Table 485 • **Factory Test Register (7x8204)**

Bit	Name	Description	Access	Default
15:0	Reserved	Factory test only. Do not modify this bit group.	RW	0

Table 486 • **Factory Test Register (7x8205)**

Bit	Name	Description	Access	Default
15:0	Reserved	Factory test only. Do not modify this bit group.	RW	0

Table 487 • **Factory Test Register (7x8220)**

Bit	Name	Description	Access	Default
15:13	Reserved	Factory test only.	RO	0
12	Reserved	Factory test only. Do not modify this bit group.	RW	0
11	Reserved	Factory test only.	RO	0
10:0	Reserved	Factory test only. Do not modify this bit group.	RW	0

Table 488 • **Factory Test Register (7xEF00)**

Bit	Name	Description	Access	Default
15:0	Reserved	Factory test only. Do not modify this bit group.	RW	0x00

Table 489 • **Factory Test Register (7xEF01)**

Bit	Name	Description	Access	Default
15:0	Reserved	Factory test only. Do not modify this bit group.	RW	0x00

Table 490 • **Factory Test Register (7xEF02)**

Bit	Name	Description	Access	Default
15:0	Reserved	Factory test only. Do not modify this bit group.	RW	0x00

Table 491 • **Factory Test Register (7xEF03)**

Bit	Name	Description	Access	Default
15:0	Reserved	Factory test only. Do not modify this bit group.	RW	0x00

Table 492 • **Factory Test Register (7xEF10)**

Bit	Name	Description	Access	Default
15:0	Reserved	Factory test only.	RO	0x00

Table 493 • **Factory Test Register (7xEF11)**

Bit	Name	Description	Access	Default
15:0	Reserved	Factory test only.	RO	0x00

Table 494 • **Factory Test Register (7xEF12)**

Bit	Name	Description	Access	Default
15:0	Reserved	Factory test only.	RO	0x00

Table 495 • **Factory Test Register (7xEF13)**

Bit	Name	Description	Access	Default
15:0	Reserved	Factory test only.	RO	0x00

4.3 EDC Registers

This section provides information about the EDC registers.

Table 496 • **DC_AGC_LOS Config1 (1xB0C0)**

Bit	Name	Description	Access	Default
15	Suppress_Coarse_Adj_on_LOS_Clear	Selects how DC offset correction resumes operation when LOPC/LOS alarms clear. Applicable alarms defined in DC_Offset_Alarm_Mode(1xB0C0.6:4). This setting is ignored if Force_DCx_Fine_Adj=1. 0: DC offset correction performed using coarse resolution mode when correction resumes after the LOPC/LOS alarms clear. 1: DC offset correction performed using fine resolution mode when correction resumes after the LOPC/LOS alarms clear. This guarantees there will be no big jumps in the offset at the expense of taking longer to reach the optimal setting.	RW	0
14	Force_DC2_Fine_Adj	Forces the DC offset correction to operate in fine resolution adjustment mode at times when the algorithm would normally make coarse adjustments. Use of this function will slow down the offset correction performance when alarm conditions clear. For more information, see DC_Offset_Alarm_Mode. 0: DC offset correction makes coarse adjustments when correction mode is first enabled. 1: DC offset correction performed using fine resolution at all times	RW	0
13	Force_DC1_Fine_Adj	Forces the DC offset correction to operate in fine resolution adjustment mode at times when the algorithm would normally make coarse adjustments. Use of this function will slow down the offset correction performance when alarm conditions clear. For more information, see DC_Offset_Alarm_Mode. 0: DC offset correction makes coarse adjustments when correction mode is first enabled 1: DC offset correction performed using fine resolution at all times	RW	0

Table 496 • **DC_AGC_LOS Config1 (1xB0C0)** ***(continued)***

Bit	Name	Description	Access	Default
12	Force_DC0_Fine_Adj	Forces the DC offset correction to operate in fine resolution adjustment mode at times when the algorithm would normally make coarse adjustments. Use of this function will slow down the offset correction performance when alarm conditions clear. For more information, see DC_Offset_Alarm_Mode. 0: DC offset correction makes coarse adjustments when correction mode is first enabled. 1: DC offset correction performed using fine resolution at all times	RW	0
11	Reserved	Reserved (Ignore when read)	RO	0
10	Skip_DC2_Adj	Selects if DC offset correction is skipped at node 2 when DC offset correction is enabled. Use of this bit serves a function only when DC_Offset_Adj_Enable=1 and DC_Offset_Adj_Suspend=0. 0: DC2 offset correction permitted. 1: DC2 offset correction skipped (i.e. disabled)	RW	0
9	Skip_DC1_Adj	Selects if DC offset correction is skipped at node 1 when DC offset correction is enabled. Use of this bit serves a function only when DC_Offset_Adj_Enable=1 and DC_Offset_Adj_Suspend=0. 0: DC1 offset correction permitted. 1: DC1 offset correction skipped (i.e. disabled)	RW	0
8	Skip_DC0_Adj	Selects if DC offset correction is skipped at node 0 when DC offset correction is enabled. Use of this bit serves a function only when DC_Offset_Adj_Enable=1 and DC_Offset_Adj_Suspend=0. 0: DC0 offset correction permitted. 1: DC0 offset correction skipped (i.e. disabled)	RW	0
7	Reserved	Reserved (Ignore when read)	RO	0
6:04	DC_Offset_Alarm_Mode	Selects the alarm conditions that will halt the DC offset correction logic when the alarm(s) are set. When those same alarm(s) are cleared, coarse adjustments to the DC offsets are made to reach the optimal setting faster. 111: reserved’110: reserved 101: LOPC and software LOS detection 100: LOPC and hardware LOS detection 011: software LOS detection 010: hardware LOS detection 001: LOPC 000: Never. DC offset correction will continue to make fine resolution adjustments to the offsets even when LOPC and LOS alarms are present.	RW	1

Table 496 • **DC_AGC_LOS Config1 (1xB0C0)** ***(continued)***

Bit	Name	Description	Access	Default
3	AGC_Enable	selects when the hardware AGC adjustment logic and LOS detection logic is enabled 0: disabled 1: enabled The difference between AGC adjustments disabled and suspended is the manner in which the AGC resumes operation. Switching from AGC adjustments disabled to enabled causes the gain to be initialized to Init_VGA_Gain, then perform a search for the best setting.	RW	1
2	AGC_Suspend	suspends the LOS detection logic and AGC logic from making adjustments to the gain. Bit valid only if AGC_Enable =1 0: AGC adjustments enabled 1: adjustments to AGC suspended The difference between AGC adjustments disabled and suspended is the manner in which the AGC resumes operation. When exiting the suspend AGC adjustments state, the logic resumes making 1-step adjustments to the present state of the gain.	RW	0
1	DC_Offset_Adj_Enable	selects when the hardware DC offset correction logic is enabled 0: disabled 1: enabled The difference between DC offset correction disabled and suspended is the manner in which the correction logic resumes operation. Switching from the DC offset correction disabled to enabled state causes the offset settings to jump to 0x00 and then make coarse adjustments to the optimal setting.	RW	1
0	DC_Offset_Adj_Suspend	suspends the DC offset correction logic from making adjustments to all offset settings. Bit valid only if DC_Offset_Adj_Enable =1 0: DC offset correction enabled 1: DC offset correction suspended The difference between DC offset correction disabled and suspended is the manner in which the correction logic resumes operation. When exiting the suspend offset correction state, offset correction resumes making fine (1-step) adjustments to the offsets from their present state.	RW	0

Table 497 • **DC_OFF_Timer1 (1xB0C1)**

Bit	Name	Description	Access	Default
15:05	Reserved	Reserved (Ignore when read)	RO	0

Table 497 • **DC_OFF_Timer1 (1xB0C1) *(continued)***

Bit	Name	Description	Access	Default
4:00	DCoffset_Correction_Timer 2	Duration of time given for the DC offset correction logic to react to a new offset settings before making another adjustment. Delay equals this number of 78.125MHz clock cycles. default is ~10mS. 0x0 to 0x2 is invalid.	RW	0x0B

Table 498 • **DC_OFF_Timer2 (1xB0C2)**

Bit	Name	Description	Access	Default
15:00	DCoffset_Correction_Timer 1	Duration of time given for the DC offset correction logic to react to a new offset settings before making another adjustment. Delay equals this number of 78.125MHz clock cycles. default is ~10mS. 0x0 to 0x2 is invalid.	RW	0xEBC2

Table 499 • **AGC_Config2 (1xB0C3)**

Bit	Name	Description	Access	Default
15	Reserved	Reserved (Ignore when read)	RO	0
14:8	AGC_Gain_Limit	Defines maximum value the AGC logic will set the VGA gain (i.e. max allowed gain for chip is 0x7F, but never allowing the gain to exceed this register setting may improve performance). VGA gain limit in AGC circuit	RW	0x5F
7	Reserved	Reserved (Ignore when read)	RO	0
6:00	Init_VGA_Gain	Initial VGA gain setting used by AGC circuit when restarting the algorithm. Algorithm restarts when alarm conditions defined in DC_Offset_Alarm_Mode are cleared.	RW	0x17

Table 500 • **AGC_Config3 (1xB0C4)**

Bit	Name	Description	Access	Default
15:10	Reserved	Reserved (Ignore when read)	RO	0
9:00	Peak_Det_Stabilize_Time	Used when measuring input amplitude. Defines period of time given for the peak detector circuit to become valid. Delay equals this number of 78.125 MHz clock cycles. 0x0 to 0x2 is invalid.	RW	0x06C

Table 501 • **AGC_Config4 (1xB0C5)**

Bit	Name	Description	Access	Default
15:14	Reserved	Reserved (Ignore when read)	RO	0
13:08	Ampl_Tolerance	This defines the hysteresis built into the AGC adjustment circuit. The VGA gain will not be adjusted as long as the measured input amplitude is Inp_Ampl_Target +/- Ampl_Tolerance. amplitude tolerance	RW	0x04
7:00	Inp_Ampl_Target	This is the target amplitude desired to be measured at the peak detector when measuring input amplitude. The VGA gain is adjusted to achieve this target setting. target amplitude setting	RW	0x6E

Table 502 • **LOS_Config2 (1xB0C6)**

Bit	Name	Description	Access	Default
15:08	LOS_Alarm_Ampl_Thresh	LOS is declared when the input amplitude is < LOS_Alarm_Ampl_Thresh - AND- the VGA gain is	RW	

Table 503 • **FFE DAC 0 Control (1xB000)**

Bit	Name	Description	Access	Default
15:8	Reserved	Reserved (Ignore when read)	RO	0
7	Sign	Sign 0: 0 1: 1	RW	0
6:0	Control	Control 0x7F: Maximum 0x00: Minimum	RW	0x00

Table 504 • **FFE DAC 1 Control (1xB002)**

Bit	Name	Description	Access	Default
15:8	Reserved	Reserved (Ignore when read)	RO	0
7	Sign	Sign 0: 0 1: 1	RW	0
6:0	Control	Control 0x7F: Maximum 0x00: Minimum	RW	0x00

Table 505 • **FFE DAC 2 Control (1xB004)**

Bit	Name	Description	Access	Default
15:8	Reserved	Reserved (Ignore when read)	RO	0
7	Sign	Sign 0: 0 1: 1	RW	0
6:0	Control	Control 0x7F: Maximum 0x00: Minimum	RW	0x00

Table 506 • **FFE DAC 3 Control (1xB006)**

Bit	Name	Description	Access	Default
15:8	Reserved	Reserved (Ignore when read)	RO	0
7	Sign	Sign 0: 0 1: 1	RW	1
6:0	Control	Control 0x7F: Maximum 0x00: Minimum	RW	0x4D

Table 507 • **FFE DAC 4 Control (1xB008)**

Bit	Name	Description	Access	Default
15:8	Reserved	Reserved (Ignore when read)	RO	0
7	Sign	Sign 0: 0 1: 1	RW	0
6:0	Control	Control 0x7F: Maximum 0x00: Minimum	RW	0x7F

Table 508 • **FFE DAC 5 Control (1xB00A)**

Bit	Name	Description	Access	Default
15:8	Reserved	Reserved (Ignore when read)	RO	0
7	Sign	Sign 0: 0 1: 1	RW	0
6:0	Control	Control 0x7F: Maximum 0x00: Minimum	RW	0x7F

Table 509 • **FFE DAC 6 Control (1xB00C)**

Bit	Name	Description	Access	Default
15:8	Reserved	Reserved (Ignore when read)	RO	0
7	Sign	Sign 0: 0 1: 1	RW	1
6:0	Control	Control 0x7F: Maximum 0x00: Minimum	RW	0x39

Table 510 • **FFE DAC 7 Control (1xB00E)**

Bit	Name	Description	Access	Default
15:8	Reserved	Reserved (Ignore when read)	RO	0
7	Sign	Sign 0: 0 1: 1	RW	0
6:0	Control	Control 0x7F: Maximum 0x00: Minimum	RW	0x00

Table 511 • **FFE DAC 8 Control (1xB010)**

Bit	Name	Description	Access	Default
15:8	Reserved	Reserved (Ignore when read)	RO	0
7	Sign	Sign 0: 0 1: 1	RW	0
6:0	Control	Control 0x7F: Maximum 0x00: Minimum	RW	0x00

Table 512 • **DFE DAC 0 Control (1xB018)**

Bit	Name	Description	Access	Default
15:8	Reserved	Reserved (Ignore when read)	RO	0
7	Sign	Sign 0: 0 1: 1	RW	0
6:0	Control	Control 0x7F: Maximum 0x00: Minimum	RW	0x00

Table 513 • **DFE DAC 1 Control (1xB01A)**

Bit	Name	Description	Access	Default
15:8	Reserved	Reserved (Ignore when read)	RO	0
7	Sign	Sign 0: 0 1: 1	RW	0
6:0	Control	Control 0x7F: Maximum 0x00: Minimum	RW	0x00

Table 514 • **DFE DAC 2 Control (1xB01C)**

Bit	Name	Description	Access	Default
15:8	Reserved	Reserved (Ignore when read)	RO	0
7	Sign	Sign 0: 0 1: 1	RW	0
6:0	Control	Control 0x7F: Maximum 0x00: Minimum	RW	0x00

Table 515 • **DFE DAC 3 Control (1xB01E)**

Bit	Name	Description	Access	Default
15:8	Reserved	Reserved (Ignore when read)	RO	0
7	Sign	Sign 0: 0 1: 1	RW	0
6:0	Control	Control 0x7F: Maximum 0x00: Minimum	RW	0x00

4.3.1 Hardware DC Offset Correction Logic

The following registers are associated with the hardware DC offset correction logic. The offset correction logic is enabled by default. The circuitry starts modifying these values immediately in search of an optimal location, which makes it impossible to read the default setting. The value continues to change until the device reaches its optimal setting.

To disable the hardware offset correction logic and are not run firmware, make sure these registers are set to the proper value of their system. If they have not yet characterized what those values should be, set these registers back to the default values listed.

Table 516 • **FFE 0 Offset Control (1xB020)**

Bit	Name	Description	Access	Default
15:6	Reserved	Reserved (Ignore when read)	RO	0

Table 516 • **FFE 0 Offset Control (1xB020) *(continued)***

Bit	Name	Description	Access	Default
5	Disable	Disable 0: Enable 1: Disable	RW	0
4	Sign	Sign 0: 0 1: 1	RW	0
3:0	Magnitude	Magnitude 1111: Maximum 0000: Minimum	RW	0000

For more information about the default values, see Hardware DC Offset Correction Logic, page 293.

Table 517 • **FFE 1 Offset Control (1xB022)**

Bit	Name	Description	Access	Default
15:6	Reserved	Reserved (Ignore when read)	RO	0
5	Disable	Disable 0: Enable 1: Disable	RW	0
4	Sign	Sign 0: 0 1: 1	RW	0
3:0	Magnitude	Magnitude 1111: Maximum 0000: Minimum	RW	0000

For more information about the default values, see Hardware DC Offset Correction Logic, page 293.

Table 518 • **FFE 2 Offset Control (1xB024)**

Bit	Name	Description	Access	Default
15:6	Reserved	Reserved (Ignore when read)	RO	0
5	Disable	Disable 0: Enable 1: Disable	RW	0
4	Sign	Sign 0: 0 1: 1	RW	0
3:0	Magnitude	Magnitude 1111: Maximum 0000: Minimum	RW	0000

For more information about the default values, see Hardware DC Offset Correction Logic, page 293.

Table 519 • **FFE 3 Offset Control (1xB026)**

Bit	Name	Description	Access	Default
15:6	Reserved	Reserved (Ignore when read)	RO	0

Table 519 • **FFE 3 Offset Control (1xB026) *(continued)***

Bit	Name	Description	Access	Default
5	Disable	Disable 0: Enable 1: Disable	RW	0
4	Sign	Sign 0: 0 1: 1	RW	0
3:0	Magnitude	Magnitude 1111: Maximum 0000: Minimum	RW	0000

For more information about the default values, see Hardware DC Offset Correction Logic, page 293.

Table 520 • **FFE 4 Offset Control (1xB028)**

Bit	Name	Description	Access	Default
15:6	Reserved	Reserved (Ignore when read)	RO	0
5	Disable	Disable 0: Enable 1: Disable	RW	0
4	Sign	Sign 0: 0 1: 1	RW	0
3:0	Magnitude	Magnitude 1111: Maximum 0000: Minimum	RW	0000

For more information about the default values, see Hardware DC Offset Correction Logic, page 293.

Table 521 • **FFE 5 Offset Control (1xB02A)**

Bit	Name	Description	Access	Default
15:6	Reserved	Reserved (Ignore when read)	RO	0
5	Disable	Disable 0: Enable 1: Disable	RW	0
4	Sign	Sign 0: 0 1: 1	RW	0
3:0	Magnitude	Magnitude 1111: Maximum 0000: Minimum	RW	0000

For more information about the default values, see Hardware DC Offset Correction Logic, page 293.

Table 522 • **FFE 6 Offset Control (1xB02C)**

Bit	Name	Description	Access	Default
15:6	Reserved	Reserved (Ignore when read)	RO	0

Table 522 • **FFE 6 Offset Control (1xB02C)** ***(continued)***

Bit	Name	Description	Access	Default
5	Disable	Disable 0: Enable 1: Disable	RW	0
4	Sign	Sign 0: 0 1: 1	RW	0
3:0	Magnitude	Magnitude 1111: Maximum 0000: Minimum	RW	0000

For more information about the default values, see Hardware DC Offset Correction Logic, page 293.

Table 523 • **FFE 7 Offset Control (1xB02E)**

Bit	Name	Description	Access	Default
15:6	Reserved	Reserved (Ignore when read)	RO	0
5	Disable	Disable 0: Enable 1: Disable	RW	0
4	Sign	Sign 0: 0 1: 1	RW	0
3:0	Magnitude	Magnitude 1111: Maximum 0000: Minimum	RW	0000

For more information about the default values, see Hardware DC Offset Correction Logic, page 293.

Table 524 • **FFE 8 Offset Control (1xB030)**

Bit	Name	Description	Access	Default
15:6	Reserved	Reserved (Ignore when read)	RO	0
5	Disable	Disable 0: Enable 1: Disable	RW	0
4	Sign	Sign 0: 0 1: 1	RW	0
3:0	Magnitude	Magnitude 1111: Maximum 0000: Minimum	RW	0000

For more information about the default values, see Hardware DC Offset Correction Logic, page 293.

Table 525 • **DFE 0 Offset Control (1xB038)**

Bit	Name	Description	Access	Default
15:6	Reserved	Reserved (Ignore when read)	RO	0

Table 525 • **DFE 0 Offset Control (1xB038) *(continued)***

Bit	Name	Description	Access	Default
5	Disable	Disable 0: Enable 1: Disable	RW	0
4:0	Reserved	Factory test only. Do not modify this bit group.	RW	0

For more information about the default values, see Hardware DC Offset Correction Logic, page 293.

Table 526 • **DFE 1 Offset Control (1xB03A)**

Bit	Name	Description	Access	Default
15:6	Reserved	Reserved (Ignore when read)	RO	0
5	Disable	Disable 0: Enable 1: Disable	RW	0
4:0	Reserved	Factory test only. Do not modify this bit group.	RW	0

For more information about the default values, see Hardware DC Offset Correction Logic, page 293.

Table 527 • **DFE 2 Offset Control (1xB03C)**

Bit	Name	Description	Access	Default
15:6	Reserved	Reserved (Ignore when read)	RO	0
5	Disable	Disable 0: Enable 1: Disable	RW	0
4:0	Reserved	Factory test only. Do not modify this bit group.	RW	0

For more information about the default values, see Hardware DC Offset Correction Logic, page 293.

Table 528 • **DFE 3 Offset Control (1xB03E)**

Bit	Name	Description	Access	Default
15:6	Reserved	Reserved (Ignore when read)	RO	0
5	Disable	Disable 0: Enable 1: Disable	RW	0
4:0	Reserved	Factory test only. Do not modify this bit group.	RW	0

For more information about the default values, see Hardware DC Offset Correction Logic, page 293.

Table 529 • **DC Sense Mux (1xB040)**

Bit	Name	Description	Access	Default
15:8	Reserved	Reserved (Ignore when read)	RO	0
7:6	Rx EDC DCOUT SELECT	Selects Node to output on DCOUT 00: High-Z 01: FP 10: FN 11: (FP+FN)/2	RW	00

Table 529 • **DC Sense Mux (1xB040) *(continued)***

Bit	Name	Description	Access	Default
5	Enable Peak Detector	0: Disable 1: Enable	RW	0
4	Sign	0: 0 1: 1	RW	0
3	Control	0: Offsets 1: Peak Detector	RW	0
2:0	Control	1xx: latch 011: 2nd summing node 010: 1st summing node 001: output of VGA 000: none	RW	000

For more information about the default values, see Hardware DC Offset Correction Logic, page 293.

Table 530 • **Peak Detect (1xB042)**

Bit	Name	Description	Access	Default
15:8	Reserved	Reserved (Ignore when read)	RO	0
7:0	Magnitude	11111111: Maximum 00000000: Minimum	RW	00000000

For more information about the default values, see Hardware DC Offset Correction Logic, page 293.

Table 531 • **VGA0 Gain (1xB044)**

Bit	Name	Description	Access	Default
15:7	Reserved	Reserved (Ignore when read)	RO	0
6:0	Magnitude	1111111: Maximum 0000000: Minimum	RW	0011110

For more information about the default values, see Hardware DC Offset Correction Logic, page 293.

Table 532 • **VGA0 Boost (1xB046)**

Bit	Name	Description	Access	Default
15:4	Reserved	Reserved (Ignore when read)	RO	0
3:0	Magnitude	1111: Maximum 0000: Minimum	RW	1000

For more information about the default values, see Hardware DC Offset Correction Logic, page 293.

Table 533 • **VGA1 Gain (1xB048)**

Bit	Name	Description	Access	Default
15:6	Reserved	Reserved (Ignore when read)	RO	0
5:0	Magnitude	111111: Maximum 000000: Minimum	RW	010100

For more information about the default values, see Hardware DC Offset Correction Logic, page 293.

Table 534 • **VGA1 Boost (1xB04A)**

Bit	Name	Description	Access	Default
15:0	Reserved	Reserved (Ignore when read)	RO	0

For more information about the default values, see Hardware DC Offset Correction Logic, page 293.

Table 535 • **VGA0 Offset (1xB04C)**

Bit	Name	Description	Access	Default
15:8	Reserved	Reserved (Ignore when read)	RO	0
7	Sign	0: 0 1: 1	RW	0
6:0	Magnitude	1111111: Maximum 0000000: Minimum	RW	0000000

For more information about the default values, see Hardware DC Offset Correction Logic, page 293.

Table 536 • **VGA1 Offset (1xB04E)**

Bit	Name	Description	Access	Default
15:8	Reserved	Reserved (Ignore when read)	RO	0
7	Sign	0: 0 1: 1	RW	0
6:0	Magnitude	1111111: Maximum 0000000: Minimum	RW	0000000

For more information about the default values, see Hardware DC Offset Correction Logic, page 293.

Table 537 • **Latch Offset (1xB050)**

Bit	Name	Description	Access	Default
15:8	Reserved	Reserved (Ignore when read)	RO	0
7	Sign	0: 0 1: 1	RW	0
6:0	Magnitude	1111111: Maximum 0000000: Minimum	RW	0000000

Table 538 • **Evalue (1xB058)**

Bit	Name	Description	Access	Default
15:0	Reserved	Reserved (Ignore when read)	RO	0

Table 539 • **Pattern (1xB05A)**

Bit	Name	Description	Access	Default
15:0	Reserved	Reserved (Ignore when read)	RW	0

Table 540 • **Mask (1xB05C)**

Bit	Name	Description	Access	Default
15:0	Reserved	Reserved (Ignore when read)	RW	0

Table 541 • **Count (1xB05E)**

Bit	Name	Description	Access	Default
15:0	Reserved	Reserved (Ignore when read)	RO	0

Table 542 • **Error Sample Timing Fine Control (1xB060)**

Bit	Name	Description	Access	Default
15:0	Reserved	Reserved (Ignore when read)	RW	0

Table 543 • **Error Sample Timing Coarse Control (1xB062)**

Bit	Name	Description	Access	Default
15:0	Reserved	Reserved (Ignore when read)	RO	0

Table 544 • **Eoff (1xB064)**

Bit	Name	Description	Access	Default
15:0	Reserved	Reserved (Ignore when read)	RO	0

Table 545 • **EPTR (1xB066)**

Bit	Name	Description	Access	Default
15:0	Control		RW	FFFF

Table 546 • **ENTR (1xB068)**

Bit	Name	Description	Access	Default
15:0	Control		RW	FFFF

Table 547 • **EDC Control Misc (1xB06A)**

Bit	Name	Description	Access	Default
15:2	Reserved	Reserved (Ignore when read)	RO	0

Table 547 • **EDC Control Misc (1xB06A) *(continued)***

Bit	Name	Description	Access	Default
1	Selmdb	0: 0 1: 1	RW	0
0	Reserved	Reserved (Ignore when read)	RO	0

Table 548 • **Ncounto1 (1xB070)**

Bit	Name	Description	Access	Default
15:0	Reserved	Reserved (Ignore when read)	RO	0

Table 549 • **Ncounto2 (1xB072)**

Bit	Name	Description	Access	Default
15:0	Reserved	Reserved (Ignore when read)	RO	0

Table 550 • **Ecounto1 (1xB074)**

Bit	Name	Description	Access	Default
15:0	Reserved	Reserved (Ignore when read)	RO	0

Table 551 • **Ecounto2 (1xB076)**

Bit	Name	Description	Access	Default
15:0	Reserved	Reserved (Ignore when read)	RO	0

Table 552 • **Ucounto1 (1xB078)**

Bit	Name	Description	Access	Default
15:0	Reserved	Reserved (Ignore when read)	RO	0

Table 553 • **Dcounto1 (1xB07A)**

Bit	Name	Description	Access	Default
15:0	Reserved	Reserved (Ignore when read)	RO	0

Table 554 • **(1Ex8000)**

Bit	Name	Description	Access	Default
15	I2C speed select	0: 400 kHz 1: 100 kHz	RW	0
14	Interface select	0: MDIO/I2C slave interface 1: µP interface	RW	0
13	Reserved	Do not modify	RW	0
12	Reset sequence disable	0: Enable reset sequence 1: Disable reset sequence	RW	0
11:5	Reserved	Do not modify	RW	0
4	Command	0: Read 1: Write	RW	0
3:2	MDIO/I2C slave interfaces command status		RO	0
1:0	µP interfaces command status		RO	0

5 Electrical Specifications

This section provides the DC characteristics, AC characteristics, recommended operating conditions, and stress ratings for the VSC8484 device.

5.1 DC Characteristics

This section contains the DC specifications for the VSC8484 device.

5.1.1 Low-Speed Inputs and Outputs

The following table lists the DC specifications for the LVTTL inputs and outputs for the VSC8484 device. When VDDMDIO is set to 1.2 V, 1.5 V, 1.8 V, 2.5 V, or 3.3 V as the VDDTTL, the following specifications apply to MDIO as well.

Table 555 • **MDIO and LVTTL Inputs and Outputs**

Parameter	Symbol	Minimum	Maximum	Unit	Condition
Output high voltage, LVTTL[1]	V_{OH_TTL}	2.4 1.8 1.35 0.95 0.65	V_{DDTTL}	V	V_{DDTTL} = 3.3 V and I_{OH} = –4 mA V_{DDTTL} = 2.5 V and I_{OH} = –4 mA V_{DDTTL} = 1.8 V and I_{OH} = –2 mA V_{DDTTL} = 1.5 V and I_{OH} = –2 mA V_{DDTTL} = 1.2 V and I_{OH} = –1 mA
Output high voltage, open drain	V_{OH_OD}	2.4 1.8 1.4 1.05 0.85	V_{DDTTL}	V	V_{DDTTL}/V_{DDMDIO} = 3.3 V and I_{OH} = 100 µA V_{DDTTL}/V_{DDMDIO} = 2.5 V and I_{OH} = 100 µA V_{DDTTL}/V_{DDMDIO} = 1.8 V and I_{OH} = 100 µA V_{DDTTL}/V_{DDMDIO} = 1.5 V and I_{OH} = 100 µA V_{DDTTL}/V_{DDMDIO} = 1.2 V and I_{OH} = 100 µA
Output low voltage (LVTTL, open drain)	V_{OL}		0.5 0.5 0.4 0.25 0.2	V	V_{DDTTL}/V_{DDMDIO} = 3.3 V and I_{OL} = 4 mA V_{DDTTL}/V_{DDMDIO} = 2.5 V and I_{OL} = 4 mA V_{DDTTL}/V_{DDMDIO} = 1.8 V and I_{OL} = 2 mA V_{DDTTL}/V_{DDMDIO} = 1.5 V and I_{OL} = 2 mA V_{DDTTL}/V_{DDMDIO} = 1.2 V and I_{OL} = 1 mA
Input high voltage	V_{IH}	2.0 1.7 1.2 1.05 0.90	V_{DDTTL}	V	V_{DDTTL}/V_{DDMDIO} = 3.3 V V_{DDTTL}/V_{DDMDIO} = 2.5 V V_{DDTTL}/V_{DDMDIO} = 1.8 V V_{DDTTL}/V_{DDMDIO} = 1.5 V V_{DDTTL}/V_{DDMDIO} = 1.2 V
Input low voltage	V_{IL}		0.8 0.8 0.6 0.45 0.36	V	V_{DDTTL}/V_{DDMDIO} = 3.3 V V_{DDTTL}/V_{DDMDIO} = 2.5 V V_{DDTTL}/V_{DDMDIO} = 1.8 V V_{DDTTL}/V_{DDMDIO} = 1.5 V V_{DDTTL}/V_{DDMDIO} = 1.2 V
Input high current	I_{IH}		500	µA	$V_{IH} = V_{DDTTL}/V_{DDMDIO}$
Input low current	I_{IL}	–50		µA	V_{IL} = 0 V

1. The V_{REF} of the downstream logic might need adjustment to interface with HSTL-12 logic.

5.1.2 Reference Clock

The following table lists the DC specifications for the reference clock for the VSC8484 device.

Table 556 • **Reference Clock**

Parameter	Symbol	Minimum	Maximum	Unit	Condition
DC common-mode voltage	V_{ICM_DC}	0.65	1.0	V	DC-coupled LVPECL inputs
Single-ended input swing	ΔV_{I_SE}	250	1200	mV_{p-p}	CML or LVPECL reference clock input
Differential input swing	ΔV_{I_DIFF}	350	2400	mV_{p-p}	CML or LVPECL reference clock input

5.1.3 MDIO Interface

The following table lists the DC specifications for the MDIO interface of the VSC8484 device.

Table 557 • **MDIO Interface**

Parameter	Symbol	Minimum	Maximum	Unit	Condition
Input high voltage[1]	V_{IH}	0.95	V_{DDMDIO}	V	V_{DDMDIO} = 1.2 V
Input low voltage	V_{IL}	0	0.36	V	
Output high voltage[2]	V_{OH}	1.0	V_{DDMDIO}	V	I_{OH} = –100 µA
Output low voltage	V_{OL}	0	0.2	V	I_{OL} = 100 µA
Output high current during tristate	I_{OZH}	–100	100	µA	V_I = 1.2 V
Output low current	I_{OL}	4.0		mA	V_I = 0.2 V
Input capacitance	C_{IN}		10	pF	
Bus loading	C_L		470	pF	

1. Maximum input high voltage must not exceed V_{DDMDIO}.
2. Output is open drain and pulled up to V_{DDMDIO} through a 4.7 kΩ resistor.

5.2 AC Characteristics

This section contains the AC specifications for the VSC8484 device. The specifications apply to all channels.

5.2.1 Receiver Specifications

This section includes the receiver specifications.

The specifications in the following table correspond to SFI point D. Point D assumes that the input is from a compliant point C output and a compliant SFI or XFI channel according to the SFP+ standard (SFF-8431) or the XFP multisource agreement (INF-8077i). A 4.5 dB channel loss is used for the test setup.

Table 558 • **SFI Input Receiver (SFI Point D)**

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Condition
RXIN input data rate, 10 Gbps		9.95	10.3125	10.6	Gbps	10 Gbps mode
RXIN input data rate, 1.25 Gbps			1.25		Gbps	1.25 Gbps mode

Table 558 • **SFI Input Receiver (SFI Point D) *(continued)***

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Condition
RXIN linear mode differential input data swing	$\Delta VRXIN_{LINEAR}$	180		600	mV	Voltage modulation amplitude (VMA)
RXIN limiting mode differential input data swing	$\Delta VRXIN_{LIMITING}$	300		850	mV	Measured peak-to-peak
RXIN AC common-mode voltage	V_{CM}			15	mV (RMS)	
Differential input S-parameter, 0.01 GHz to 2.8 GHz[1]	SDD11		–12		dB	0.01 GHz to 2.8 GHz
Differential input S-parameter, 2.8 GHz to 11 GHz[1]	SDD11		See note[2]		dB	2.8 GHz to 11 GHz
Differential to common-mode conversion[3]	SCD11		–15		dB	0.01 GHz to 11 GHz

1. Reference differential impedance is 100 Ω.
2. Return loss value is given by the equation SDD11(dB) = –8.15 + 13.33 Log_{10}(f/5.5), with f in GHz.
3. The test set common-mode reference impedance is 25 Ω.

Table 559 • **Receive Path Input**

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Condition
Input amplitude, without offset optimization	$\|V_{ID_RXIN}\|$	90			mV	AC-coupled, both sides driven. BER 1×10E^{-12}.
Back-to-back optical sensitivity with PIN	S_{PIN}		–19		dBm	40 km EML with PIN. BER 1×10E^{-12}.
Dispersion penalty with PIN	DP_{PIN}		1		dBm	Up to ±1600 ps/nm dispersion, 40 km EML.
Back-to-back optical sensitivity with APD	S_{APD}		–26		dBm	80 km EML with APD. BER 1×10E^{-12}. 10.7 Gbps with offset optimized.
Dispersion penalty with APD	DP_{APD}		1		dBm	Up to ±2000 ps/nm dispersion 80 km EML. 10.7 Gbps with offset optimized.
OSNR penalty per 0.1 nm, 10.709 Gbps	$OSNR_{RATE_PEN}$		0		dB	OSNR penalty measured for < 3.3x10E^{-5} BER. Up to ±1500 ps/nm dispersion. Optimized decision threshold and EDC feature enabled.

Table 559 • **Receive Path Input *(continued)***

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Condition
OSNR penalty per 0.1 nm, 11.3 Gbps	$OSNR_{RATE_PEN}$		0.5		dB	OSNR penalty measured for < 3.3x10E^{-5} BER. Up to ±1500 ps/nm dispersion. Optimized decision threshold and EDC feature enabled.
OSNR variation vs. fiber dispersion at BER < 3.3 x 10E^{-5} (±1500 ps/nm)	$OSNR_{DISP_VAR}$			3	dB	Up to ±1500 ps/nm.
OSNR variation vs. fiber dispersion at BER < 3.3 x 10E^{-5} (±1200 ps/nm)	$OSNR_{DISP_VAR}$			1.8	dB	Up to ±1200 ps/nm.
OSNR variation vs. fiber dispersion at BER < 3.3 x 10E^{-5} (±800 ps/nm)	$OSNR_{DISP_VAR}$			1.5	dB	Up to ±800 ps/nm.
OSNR variation over temperature –5 °C to 75 °C	$OSNR_{TEMP_VAR}$			0.5	dB	OSNR 12 dB to 17 dB. Dispersion = 0 ps/nm.
BER variation over Rx power (BER high/BER low)	BER_{PWR_VAR}	5		10		15 dB OSNR. Rx power = –20 dBm to –6 dBm.
BER vs. input power	BER_{PWR}			3.30E^{-5}		0 ps/nm and 13 dB OSNR for –20 dBm to –6 dBm Rx power.

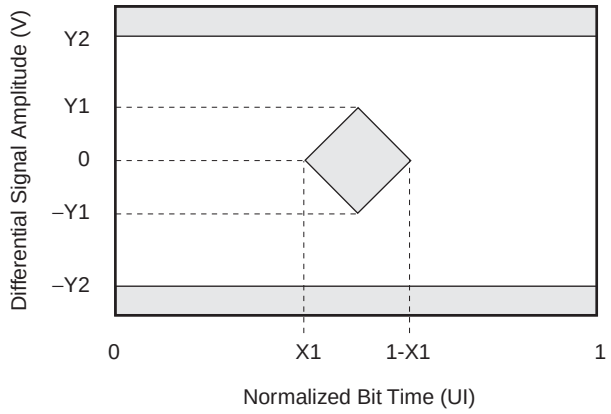
Table 560 • **1.25 Gbps SFI Input Jitter**

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Condition
Total jitter tolerance	TJT			0.749	UI	1.25 Gbps. Measured peak-to-peak.
Deterministic jitter	DJ			0.462	UI	1.25 Gbps. Measured peak-to-peak.
Eye mask X1	X1		0.35		UI	1.25 Gbps. Measured peak-to-peak. See Figure 41, page 307.
Eye mask Y1	Y1	125			mV	1.25 Gbps. Measured peak-to-peak. See Figure 41, page 307.
Eye mask Y2	Y2			600	mV	1.25 Gbps. Measured peak-to-peak. See Figure 41, page 307.

Table 561 • **SONET 10G Input Jitter**

Parameter	Symbol	Minimum	Condition
Sinusoidal jitter tolerance, 9.95 Gbps to 10.3 Gbps	SJT	2× jitter mask	GR-253 and 10 GbE masks according to SONET OC-192 and IEEE 802.3ae standards

Figure 41 • **Receive Path Input Compliance Mask**



The following table lists the CRU input specifications for the VSC8484 device. The test is done with a 4.5 dB channel loss and dynamic EDC enabled.

Table 562 • **10-Gigabit Serial Data Input for CRU**

Parameter	Symbol	Minimum	Maximum	Unit	Condition
Total jitter tolerance	TOL_{JIT_P-P}		0.70	UI	Calibrated and measured at point C", as specified in SFF-8431 revision 4.1
99% jitter	$99\%_{JIT_p-p}$		0.42	UI	Calibrated and measured at point C", as specified in SFF-8431 revision 4.1
Pulse width shrinkage jitter	$DDPWS_{JIT_p-p}$		0.3	UI	Calibrated and measured at point C", as specified in SFF-8431 revision 4.1
Sinusoidal jitter, Datacom, SFI	$S_{J_DAT_SFI}$		See Figure 43, page 308		SFF-8431 revision 4.1 Datacom mask
Eye mask X1	X1		0.35	UI	Calibrated and measured at point C", as specified in SFF-8431 revision 4.1
Eye mask Y1	Y1	150		mV	Calibrated and measured at point C", as specified in SFF-8431 revision 4.1
Eye mask Y2	Y2		425	mV	Calibrated and measured at point C", as specified in SFF-8431 revision 4.1

Figure 42 • **10-Gigabit Data Input Compliance Mask (SFP+)**

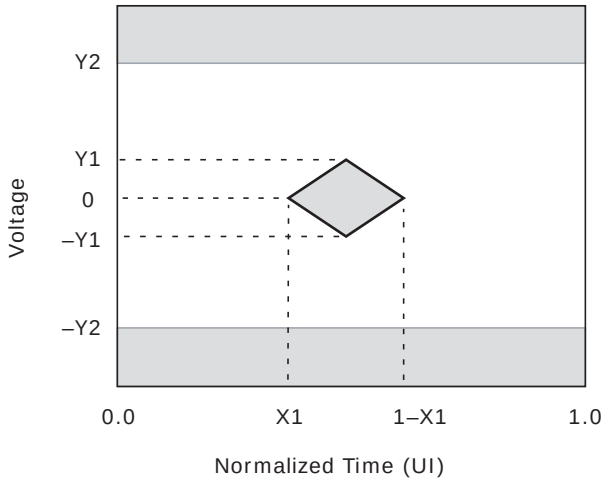
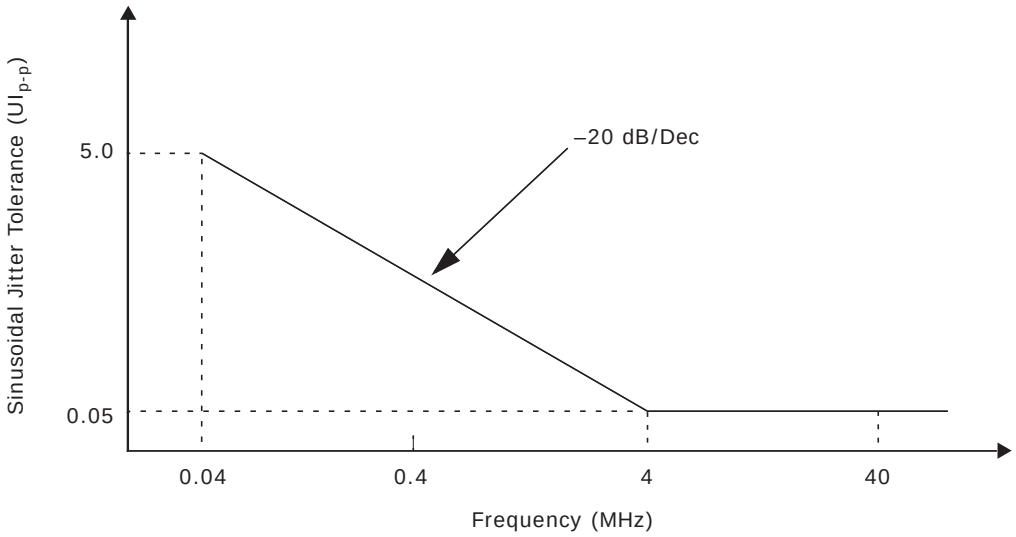


Figure 43 • **SFI Datacom Sinusoidal Jitter Tolerance**



5.2.2 Transmitter Specifications

This section includes the transmitter specifications.

The specifications in the following table correspond to SFI point B. Point B is after a standard-compliant SFI or XFI channel, as defined in the SFP+ standard (SFF-8431) or the XFP multisource agreement (INF-8077i). A 4.5 dB channel loss is used for the test setup.

Table 563 • **SFI Output Driver (SFI Point B)**

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Condition
Termination mismatch	ΔZ_M			5	%	
DC common-mode voltage	V_{CM}	0		3.6	V	
AC common-mode voltage	V_{OCM_AC}			15	mV (RMS)	
Differential output S-parameter, 0.01 GHz to 2.0 GHz[1]	SDD22		–12		dB	0.01 GHz to 2.0 GHz

Table 563 • **SFI Output Driver (SFI Point B)** ***(continued)***

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Condition
Differential output S-parameter, 2.0 GHz to 11.1 GHz[1]	SDD22		See note[2]		dB	2.0 GHz to 11.1 GHz
Common-mode output S-parameter, 0.01 GHz to 2.5 GHz	SCC22		See note[3]		dB	0.01 GHz to 2.5 GHz
Common-mode output S-parameter, 2.5 GHz to 11.1 GHz	SCC22		–3		db	2.5 GHz to 11.1 GHz

1. Reference differential impedance is 100 Ω.
2. Reflection coefficient given by the equation SDD22(dB) = –6.68 + 12.1 Log_{10}(f/5.5), with f in GHz.
3. S-parameter equation SCC22(dB) = -7 + 1.6 × f, with f in GHz.

The jitter performance specifications in the following table correspond to point B. The test is done with a 4.5 dB channel loss.

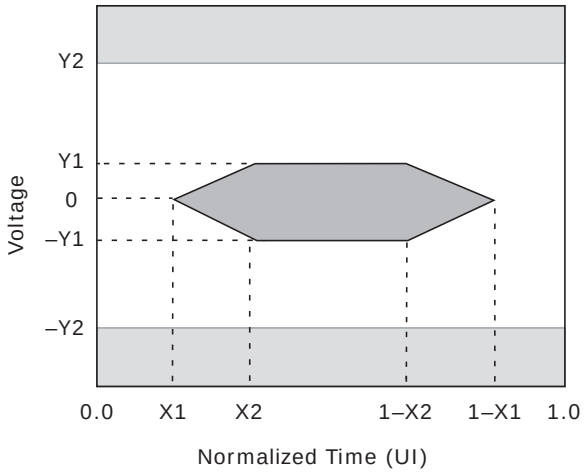
Table 564 • **SFI Output Specifications for Jitter Performance (SFI Point B)**

Parameter	Symbol	Minimum	Maximum	Unit	Condition
Total jitter	TJ		0.28	UI	Calibrated and measured at point B, as specified in SFF-8431 revision 4.1.
Data-dependant jitter	DDJ		0.1	UI	Calibrated and measured at point B, as specified in SFF-8431 revision 4.1.
Uncorrelated jitter	UJ		0.023	UI (RMS)	Calibrated and measured at point B, as specified in SFF-8431 revision 4.1.
Eye mask X1	X1		0.12	UI	Measured at 5e-5 mask hit ratio. See Figure 44, page 310.
Eye mask X2	X2		0.33	UI	Measured at 5e-5 mask hit ratio. See Figure 44, page 310.
Eye mask Y1	Y1	95		mV	Measured at 5e-5 mask hit ratio. See Figure 44, page 310.
Eye mask Y2	Y2		350	mV	See Figure 44, page 310.

Note: For optimal channel jitter performance, set the Tx output driver slew rate control register to the maximum slew rate.

The following illustration shows the compliance mask associated with the Tx SFI transmit differential output.

Figure 44 • **SFI Transmit Differential Output Compliance Mask**



The following table shows the transmit path output specifications for SFP+ point B.

Table 565 • **Transmit Path SFP+ Direct Attach Copper Output**

Parameter	Symbol	Minimum	Maximum	Unit	Condition
SFP+ direct attach copper voltage modulation amplitude, peak-to-peak	V_{MA}	300		mV	See SFF-8431 section D.7.
SFP+ direct attach copper transmitter Qsq	Q_{sq}	63.1			Qsq = 1/RN if the one level and zero level noises are identical. See SFF-8431 section D.8.
SFP+ direct attach copper output AC common-mode voltage			12	mV (RMS)	See SFF-8431 section D.15.
SFP+ direct attach copper host output TWDPc	TWDPc		10.7	dB	Host electrical output measured using SFF-8431 Appendix G, including copper direct attach stressor.

The following table provides the AC specifications for the KR output driver.

Table 566 • **Transmit Path KR Output**

Parameter	Minimum	Maximum	Unit	Condition
Signaling speed	10.3125 – 100 ppm	10.3125 + 100 ppm	Gbps	
Differential peak-to-peak output voltage		1200	mV	
Differential peak-to-peak output voltage with Tx disabled		30	mV	
Common-mode voltage limits	0	1.9	V	

Table 566 • **Transmit Path KR Output *(continued)***

Parameter	Minimum	Maximum	Unit	Condition
Differential output return loss, 0.05 GHz to 2.5 GHz		–9	dB	0.05 GHz to 2.5 GHz
Differential output return loss, 2.5 GHz to 7.5 GHz		–9 + 12 × log(*f*/2.5)	dB	2.5 GHz to 7.5 GHz
Common-mode output return loss, 0.05 GHz to 2.5 GHz		–6	dB	0.05 GHz to 2.5 GHz
Common-mode output return loss, 2.5 GHz to 7.5 GHz		–6 + 12 × log(*f*/2.5G)	dB	2.5 GHz to 7.5 GHz
Transition time (20% to 80%)	24	47	ps	

The following table provides the jitter specifications for the KR output driver.

Table 567 • **Transmit Path KR Output Jitter**

Parameter	Symbol	Maximum	Unit	Condition
Random jitter	RJ	0.15	UI	BER $1E^{-12}$
Deterministic jitter	DJ	0.15	UI	
Duty cycle distortion	DCD	0.035	UI	
Total jitter	TJ	0.28	UI	

The following table shows the transmit path SONET jitter specifications for point A, measured with register optimization.

Table 568 • **Transmit Path SONET Output Jitter**

Parameter	Symbol	Maximum	Unit	Condition
Total jitter	TJ	150	mUI	20 kHz to 80 MHz
		80	mUI	4 MHz to 80 MHz

The following table lists the XAUI input specifications for the VSC8484 device.

Table 569 • **XAUI Input**

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Condition
Input baud rate	f	3.125 – 100 ppm		3.1875 + 100 ppm	Gbps	
Unit interval	UI		320		ps	3.125 Gbps – 100 ppm to 3.1875 Gbps + 100 ppm
Differential input amplitude	V_{IN_DIFF}	75		1600	mV	AC-coupled, measured peak-to-peak each side (both sides driven)
Differential return loss[1]	RLI_{DIFF}		–10		dB	100 Ω differential reference impedance

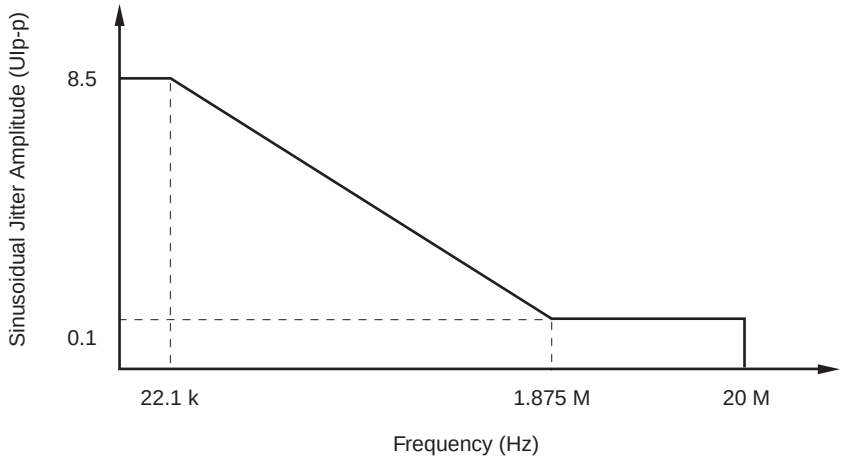
Table 569 • **XAUI Input *(continued)***

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Condition
Common-mode return loss	RLI_{CM}		–6		dB	100 MHz to 2.5 GHz, 25 Ω reference impedance
Differential skew	SK_{DIFF}			75	ps	Between true and complement inputs
Jitter tolerance, total	TOL_{TJ}	0.65			UI	Measured peak-to-peak, see IEEE 802.3ae-2002, clause 47.3.4
Jitter tolerance, deterministic	TOL_{DJ}	0.37			UI	Measured peak-to-peak, see IEEE 802.3ae-2002, clause 47.3.4
Jitter tolerance, deterministic plus random jitter	TOL_{DJ+RJ}	0.55			UI	Measured peak-to-peak, see IEEE 802.3ae-2002, clause 47.3.4

1. Limited sample size tested under nominal conditions.

The following illustration shows the sinusoidal jitter tolerance for the XAUI receiver input.

Figure 45 • **XAUI Receiver Input Sinusoidal Jitter Tolerance**



The following table lists the XAUI output specifications for the VSC8484 device.

Table 570 • **XAUI Output**

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Condition
Output baud rate	f	3.125 – 100 ppm		3.1875 + 100 ppm	Gbps	
Unit interval	UI		320		ps	3.125 Gbps – 100 ppm to 3.1875 Gbps + 100 ppm.
Differential output voltage	XV_{OUT_DIFF}	100		800	mV	Single-ended, AC-coupled. Measured peak-to-peak at far end, both sides driven with no offset applied. HISWNG = 0.
Output impedance[1]	Z_{OUT}		100		Ω	Differential.

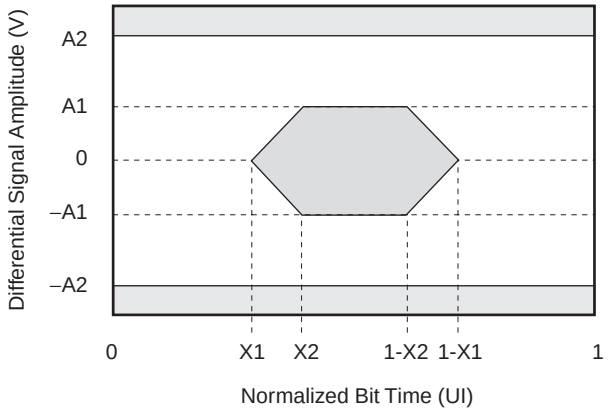
Table 570 • **XAUI Output *(continued)***

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Condition
Differential output return loss[1]	RLO_{DIFF}		–10		dB	100 MHz to 781.25 MHz, reducing 20 dB per decade up to 3.5 GHz. Includes on-device circuitry, packaging, and off-device components. 100 Ω test source.
Common-mode output return loss[1]	RLO_{CM}		–6		dB	100 MHz to 2.5 GHz over valid output levels. Includes on-device circuitry, packaging, and off-device components. 25 Ω test source.
Total jitter	TJ			0.55	UI	Measured peak-to-peak, no preemphasis at far end template.
Deterministic jitter	DJ			0.37	UI	Measured peak-to-peak, no preemphasis at far end template.
Eye mask X1	X1			0.275	UI	Measured at far end template. See Figure 46, page 313.
Eye mask X2	X2			0.40	UI	Measured at far end template. See Figure 46, page 313.
Eye mask A1	A1	100			mV	HISWNG = 0. Measured at far end template. See Figure 46, page 313.
Eye mask A2	A2			800	mV	HISWNG = 0. Measured at far end template. See Figure 46, page 313.

1. Limited sample size tested under nominal conditions.

The following illustration shows the compliance mask for the XAUI output.

Figure 46 • **XAUI Output Compliance Mask**



5.2.3 Timing and Reference Clock

The following table lists the timing clock specifications for the VSC8484 device.

Table 571 • **Reset**

Parameter	Symbol	Minimum	Unit	Condition
Minimum reset pulse width	T_{RESET}	0.1	µs	All power supplies are stable

The following table lists the reference clock specifications (XREFCK, SREFCK, WREFCK) for the VSC8484 device.

Table 572 • **Reference Clock**

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Condition
XREFCK, SREFCK, and WREFCK frequency	f_{REFCLK}	148 MHz – 100 ppm		165 MHz + 100 ppm	MHz	Pins: REFSEL[1:0] = 00[1]
XREFCK, SREFCK, and WREFCK duty cycle	DC_{REFCK}	40		60	%	
Jitter tolerance[2]	JTL_{REFCLK}			2	ps (rms)	12 kHz to 20 MHz

1. The REFCLK rate multiplied by the internal multiplier cannot exceed a data line rate of 10.6 Gbps.
2. Lower jitter on the REFCLK results in better output data jitter.

Note: The clock rate for the SREFCK and WREFCK can be 4x as specified when the internal multiplier is 16x.

5.2.4 Two-Wire Serial (Slave) Interface

This section contains information about the AC specifications for the two-wire serial slave interface.

Table 573 • **Two-Wire Serial Interface**

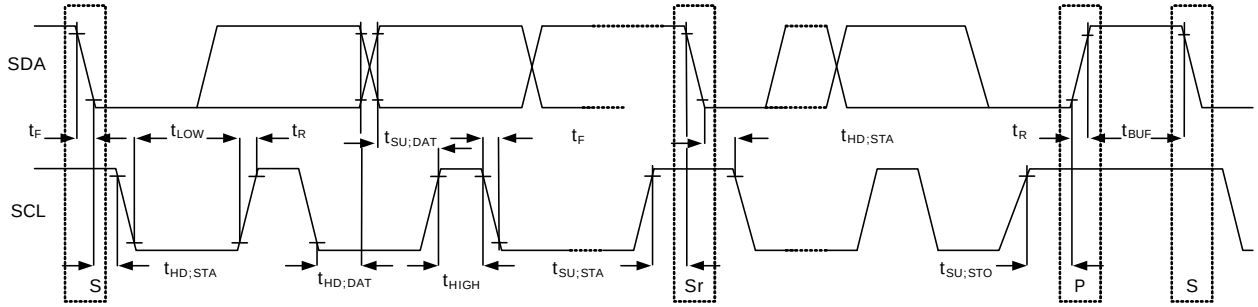
		Standard		Fast Mode		
Parameter	**Symbol**	**Minimum**	**Maximum**	**Minimum**	**Maximum**	**Unit**
Serial clock frequency	f_{SCL}		100		400	kHz
Hold time START condition after this period, the first clock pulse is generated	$t_{HD:STA}$	4.0		0.6		µs
Low period of SCL	t_{LOW}	4.7		1.3		µs
High period of SCL	t_{HIGH}	4.0		0.6		µs
Data hold time	$t_{HD:DAT}$	0	3.45	0	0.9	µs
Data setup time	$t_{SU:DAT}$	250		100		ns
Rise time for SDA and SCL	t_R		1000		300	ns
Fall time for SDA and SCL	t_F		300		300	ns
Setup time for STOP condition	$t_{SU:STO}$	4.0		0.6		µs
Bus free time between a STOP and START	t_{BUF}	4.7		1.3		µs

Table 573 • **Two-Wire Serial Interface *(continued)***

		Standard		Fast Mode		
Parameter	**Symbol**	**Minimum**	**Maximum**	**Minimum**	**Maximum**	**Unit**
Capacitive load for SCL and SDA bus line	C_B		400		330	pF
External pull-up resistor[1]	R_P	900	8×10^{-7}/CB	900	3×10^{-7}/CB	Ω

1. Minimum value is determined from I_{OL} and internal reliability requirements. Maximum value is determined by load capacitance. Microsemi recommends 10 kΩ for typical applications in which capacitance loads are below the specified minimums.

Figure 47 • **Two-Wire Serial Interface Timing**



S = START, P = STOP, and Sr = repeated START.

5.2.5 MDIO Interface

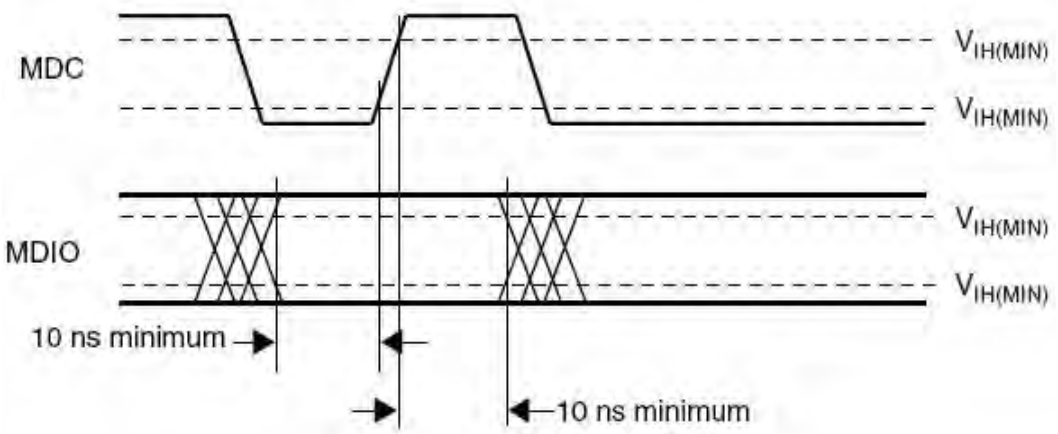
This section contains information about the AC specifications for the MDIO interface.

Table 574 • **MDIO Interface**

Parameter	Symbol	Minimum	Maximum	Unit	Condition
MDIO data hold time	t_{HOLD}	10		ns	
MDIO data setup time	t_{SU}	10		ns	
Delay from MDC rising edge to MDIO data change	t_{DELAY}		300	ns	
Delay from MDC rising edge to MDIO data change	t_{DELAY}		40	ns	12.0 MHz is supported with 200 Ω pull-up on MDIO pin and total capacitance < 80 µF
MDC clock rate	*f*		2.5	MHz	12.0 MHz is supported at 50% duty cycle and capacitance < 2 pF

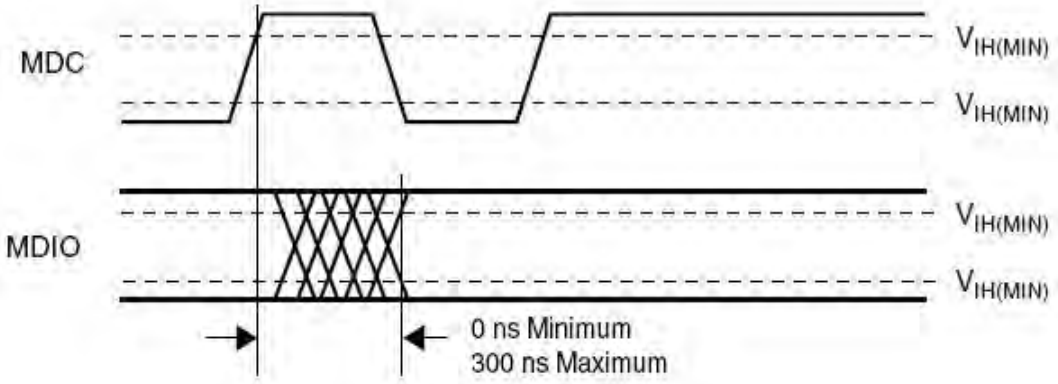
The following illustration shows the timing with the MDIO sourced by STA.

Figure 48 • **Timing with MDIO Sourced by STA**



The following illustration shows the timing with the MDIO sourced by MMD.

Figure 49 • **Timing with MDIO Sourced by MMD**



The following table lists the clock output specifications (RX0CKOUT, RX1CKOUT, TX0CKOUT, TX1CKOUT) for the VSC8484 device.

Table 575 • **Clock Output**

Parameter	Symbol	Minimum	Maximum	Unit
RX0CKOUT, RX1CKOUT, TX0CKOUT, and TX1CKOUT jitter generation	JG_{C64}		0.11	UI
RX0CKOUT, RX1CKOUT, TX0CKOUT, and TX1CKOUT output swing (half swing mode)[1]	ΔV	225	525	mV
RX0CKOUT, RX1CKOUT, TX0CKOUT, and TX1CKOUT output swing (full swing mode)[1]	ΔV	350	625	mV

1. Single-ended measurement. The amplitude will be double for differential measurement.

5.3 Operating Conditions

To ensure that the control pins remain set to the desired configured state when the VSC8484 device is powered up, perform a reset using the reset pin after power-up and after the control pins are steady for

1 ms. Then, to avoid PLL runaway problems caused by clock inputs, toggle 1x8003.0 from 0 to 1 and then back to 0. This forces the CRU to lock to reference and then to data.

Table 576 • **Recommended Operating Conditions**

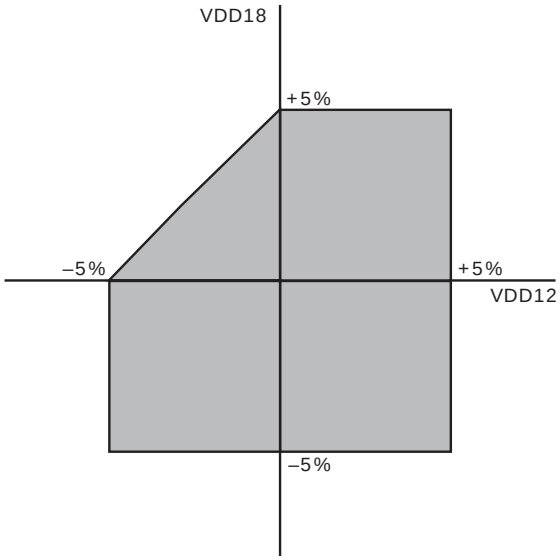
Parameter	Symbol	Minimum	Typical	Maximum	Unit	Condition
1.2 V power supply voltage	V_{DD12TX} V_{DD12X} V_{DDCLK} V_{DDB12}	1.14	1.2	1.26	V	
1.2 V power supply current	I_{DD12}		2.5	3.3	A	XAUI to 10 gigabit data in LAN mode
1.8 V power supply voltage	V_{DD18RX} V_{DD18TX}	1.71	1.8	1.89	V	
1.8 V power supply current	I_{DD18}		720	840	mA	XAUI to 10 gigabit data in LAN mode
Power consumption, LAN	P_{DD_LAN}		4.3	5.4	W	XAUI to XFI in LAN
Power consumption, WAN	P_{DD_WAN}		4.3	5.4	W	XAUI to XFI in WAN
3.3 V TTL I/O power supply voltage	V_{DDTTL} V_{DDMDIO}	3.14	3.3	3.47	V	
2.5 V TTL I/O power supply voltage	V_{DDTTL} V_{DDMDIO}	2.38	2.5	2.63	V	
1.8 V TTL I/O power supply voltage	V_{DDTTL} V_{DDMDIO}	1.71	1.8	1.89	V	
1.5 V TTL I/O power supply voltage	V_{DDTTL} V_{DDMDIO}	1.43	1.5	1.58	V	
1.2 V TTL I/O power supply voltage	V_{DDTTL} V_{DDMDIO}	1.14	1.2	1.26	V	
TTL I/O power supply current	I_{DDTTL}		10		mA	V_{DDTTL} = 3.3 V, 2.5 V, 1.8 V, 1.5 V, and 1.2 V
Operating temperature[1]	T	–40		105	°C	

1. Minimum specification is ambient temperature, and the maximum is junction temperature.

The relationship between the 1.2 V and 1.8 V power supplies need to be within 5% if the 1.8 V supply is high or if the 1.2 V supply is low. For example, with the 1.8 V supply at +4%, the 1.2 V supply needs to be no lower than –1%.

The following illustration shows the operating range of power requirements for 1.2 V and 1.8 V.

Figure 50 • **Power Supply Operating Range**



5.4 Stress Ratings

This section contains the stress ratings for the VSC8484 device.

Warning Stresses listed in the following table may be applied to devices one at a time without causing permanent damage. Functionality at or exceeding the values listed is not implied. Exposure to these values for extended periods may affect device reliability

Table 577 • **Stress Ratings**

Parameter	Symbol	Minimum	Maximum	Unit
3.3 V power supply voltage, potential to ground	V_{DDTTL}	–0.5	3.8	V
2.5 V power supply voltage, potential to ground	V_{DDTTL}	–0.5	2.9	V
1.8 V power supply voltage, potential to ground	V_{DDTTL}	–0.5	2.1	V
1.2 V power supply voltage, potential to ground	V_{DDB12}	–0.5	1.32	V
DC input voltage	V_I	–0.3	V_{DDTTL} or V_{DDB12} + 0.3	V
Output current (LVTTL)	I_{O_VDDTTL}	–16	16	mA
Absolute XAUI output voltage	V_{XAUI_ABS}	–0.4	2.3	V
Storage temperature	T_S	–65	150	°C
Electrostatic discharge voltage, charged device model	V_{ESD_CDM}	–100	100	V
Electrostatic discharge voltage, human body model	V_{ESD_HBM}	See note[1]		V

1. This device has completed all required testing as specified in the JEDEC standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*, and complies with a Class 2 rating. The definition of Class 2 is any part that passes an ESD pulse of 2000 V, but fails an ESD pulse of 4000 V.

Warning This device can be damaged by electrostatic discharge (ESD) voltage. Microsemi recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures may adversely affect reliability of the device.

6 Pin Descriptions

The VSC8484 device has 324 pins, which are described in this section.

The pin information is also provided as an attached Microsoft Excel file, so that you can copy it electronically. In Adobe Reader, double-click the attachment icon.

6.1 Pin Diagram

The following illustration shows the pin diagram for the VSC8484 device.

Figure 51 • **Pin Diagram**

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
A	GND	XTX1_3N	XTX1_2N	XTX1_1N	XTX1_0N	GND	XRX0_3N	XRX0_2N	XRX0_1N	XRX0_0N	GND	XTX0_3P	XTX0_2P	XTX0_1P	XTX0_0P	GND	GND	GND
B	GND	XTX1_3P	XTX1_2P	XTX1_1P	XTX1_0P	XAUIFILT0	XRX0_3P	XRX0_2P	XRX0_1P	XRX0_0P	GND	XTX0_3N	XTX0_2N	XTX0_1N	XTX0_0N	GND	RXIN0N	RXIN0P
C	GND	GND	GND	GND	GND	GND	VDDMDIO	RESETN	STWA1	STWA0	VDDTTLU	PADDR3	PADDR2	RESERVED2	RESERVED1	GND	GND	GND
D	XRX1_0N	XRX1_0P	GND	GPIO_0	GPIO_3	GPIO_6	GPIO_9	STWSDA	GND	RX0CKOUTP	GND	TX0CKOUTP	GND	RXCRUFILT0	RXINCM0	GND	TXOUT0N	TXOUT0P
E	XRX1_1N	XRX1_1P	GND	GPIO_1	GPIO_4	GPIO_7	GPIO_10	STWSCL	GND	RX0CKOUTN	GND	TX0CKOUTN	GND	CMUFILT0	RXCRUFILT1	GND	GND	GND
F	XRX1_2N	XRX1_2P	GND	GPIO_2	GPIO_5	GPIO_8	GPIO_11	LOPC1	RESERVED4	LOPC0	RESERVED3	STWA2	PADDR4	GND	CMUFILT1	GND	RXIN1N	RXIN1P
G	XRX1_3N	XRX1_3P	GND	MDIO	MDC	GND	VDD12TX0	VDD12TX0	GND	VDD18RX0	VDD18RX0	GND	TX1CKOUTP	VDD18TX0	CMUFILTR	GND	GND	GND
H	GND	XAUIFILT1	GND	VDD12X0	VDD12X0	GND	VDD12TX1	VDD12TX1	GND	RX1CKOUTP	RX1CKOUTN	GND	TX1CKOUTN	VDD18TX1	RXINCM1	GND	TXOUT1N	TXOUT1P
J	XTX2_0N	XTX2_0P	GND	VDD12X1	VDD12X1	GND	VDDB12	VDDB12	GND	VDD18RX1	VDD18RX1	GND	VDDCLK	GND	XREFCKP	GND	GND	GND
K	XTX2_1N	XTX2_1P	GND	VDD12X2	VDD12X2	GND	VDDB12	VDDB12	GND	VDD18RX2	VDD18RX2	GND	VDDB12	GND	XREFCKN	GND	RXIN2N	RXIN2P
L	XTX2_2N	XTX2_2P	GND	VDD12X3	VDD12X3	GND	VDD12TX2	VDD12TX2	GND	TX2CKOUTP	TX2CKOUTN	GND	RX2CKOUTN	VDD18TX2	RXINCM2	GND	GND	GND
M	XTX2_3N	XTX2_3P	GND	GPIO_23	GPIO_22	GND	VDD12TX3	VDD12TX3	GND	VDD18RX3	VDD18RX3	GND	RX2CKOUTP	VDD18TX3	RXCRUFILT2	GND	TXOUT2N	TXOUT2P
N	GND	XAUIFILT2	GND	GPIO_19	GPIO_18	GPIO_21	GPIO_14	GPIO_20	TMS	TDO	TCK	TRSTB	MODE0	GND	CMUFILT2	GND	GND	GND
P	XRX2_0P	XRX2_0N	GND	GPIO_16	GPIO_15	GPIO_17	GPIO_13	GPIO_12	LOPC3	GND	RX3CKOUTP	GND	TX3CKOUTP	GND	RXCRUFILT3	GND	RXIN3N	RXIN3P
R	XRX2_1P	XRX2_1N	GND	RESERVED8	RESERVED7	RESERVED6	RESERVED5	LOPC2	ANATEST	GND	RX3CKOUTN	GND	TX3CKOUTN	GND	CMUFILT3	GND	GND	GND
T	XRX2_2P	XRX2_2N	GND	GND	GND	GND	GND	VDDTTLL	TDI	SCAN_EN	MODE1	MODE2	TMON	GND	RXINCM3	GND	TXOUT3N	TXOUT3P
U	XRX2_3P	XRX2_3N	XAUIFILT3	XTX3_0P	XTX3_1P	XTX3_2P	XTX3_3P	GND	XRX3_0N	XRX3_1N	XRX3_2N	XRX3_3N	GND	SREFCKN	GND	GND	GND	GND
V	GND	GND	GND	XTX3_0N	XTX3_1N	XTX3_2N	XTX3_3N	GND	XRX3_0P	XRX3_1P	XRX3_2P	XRX3_3P	GND	SREFCKP	GND	WREFCKP	WREFCKN	GND

6.2 Pins by Function

This section contains the functional pin descriptions for the VSC8484 device.

6.2.1 General Purpose Inputs and Outputs

The following table lists the general purpose I/O pins for the VSC8484 device. For more information about setting the GPIO pins for different functions, see Multipurpose GPIO Pins, page 88. Leave unconnected when not used. When GPIO pins are configured as output, they are open-drained and a pull-up is required.

Table 578 • **Microcontroller Pins**

Name	Number	I/O	Type	Description
GPIO_0	D4	I/O	LVTTL_in/LVTTL_OD	General purpose I/O 0
GPIO_1	E4	I/O	LVTTL_in/LVTTL_OD	General purpose I/O 1
GPIO_2	F4	I/O	LVTTL_in/LVTTL_OD	General purpose I/O 2
GPIO_3	D5	I/O	LVTTL_in/LVTTL_OD	General purpose I/O 3
GPIO_4	E5	I/O	LVTTL_in/LVTTL_OD	General purpose I/O 4
GPIO_5	F5	I/O	LVTTL_in/LVTTL_OD	General purpose I/O 5
GPIO_6	D6	I/O	LVTTL_in/LVTTL_OD	General purpose I/O 6
GPIO_7	E6	I/O	LVTTL_in/LVTTL_OD	General purpose I/O 7
GPIO_8	F6	I/O	LVTTL_in/LVTTL_OD	General purpose I/O 8
GPIO_9	D7	I/O	LVTTL_in/LVTTL_OD	General purpose I/O 9
GPIO_10	E7	I/O	LVTTL_in/LVTTL_OD	General purpose I/O 10
GPIO_11	F7	I/O	LVTTL_in/LVTTL_OD	General purpose I/O 11
GPIO_12	P8	I/O	LVTTL_in/LVTTL_OD	General purpose I/O 0
GPIO_13	P7	I/O	LVTTL_in/LVTTL_OD	General purpose I/O 0
GPIO_14	N7	I/O	LVTTL_in/LVTTL_OD	General purpose I/O 0
GPIO_15	P5	I/O	LVTTL_in/LVTTL_OD	General purpose I/O 0
GPIO_16	P4	I/O	LVTTL_in/LVTTL_OD	General purpose I/O 0
GPIO_17	P6	I/O	LVTTL_in/LVTTL_OD	General purpose I/O 0
GPIO_18	N5	I/O	LVTTL_in/LVTTL_OD	General purpose I/O 0
GPIO_19	N4	I/O	LVTTL_in/LVTTL_OD	General purpose I/O 0
GPIO_20	N8	I/O	LVTTL_in/LVTTL_OD	General purpose I/O 0
GPIO_21	N6	I/O	LVTTL_in/LVTTL_OD	General purpose I/O 0
GPIO_22	M5	I/O	LVTTL_in/LVTTL_OD	General purpose I/O 0
GPIO_23	M4	I/O	LVTTL_in/LVTTL_OD	General purpose I/O 0

For more information about setting the GPIO pins for different functions, see PCS Activity Monitor LEDs, page 91.

6.2.2 JTAG Interface

The following table lists the JTAG testing pins for the VSC8484 device.

Table 579 • **JTAG Interface Pins**

Name	Number	I/O	Type	Description
TCK	N11	I	LVTTL	Boundary scan, test clock input. Internally pulled high. Leave unconnected when not used.

Table 579 • **JTAG Interface Pins *(continued)***

Name	Number	I/O	Type	Description
TDI	T9	I	LVTTL	Boundary scan, test data input. Internally pulled high. Leave unconnected when not used.
TDO	N10	O	LVTTL	Boundary scan, test data output. Leave unconnected when not used.
TMS	N9	I	LVTTL	Boundary scan, test mode select. Internally pulled high. Leave unconnected when not used.
TRSTB	N12	I	LVTTL	JTAG test access port test logic reset input. Internally pulled up. For TAP controller reset, this input must be pulled low. In normal operation, this pin should be connected to ground.

6.2.3 Management Interface

The following table lists the management interface pins for the VSC8484 device.

Table 580 • **Management Interface Pins**

Name	Number	I/O	Type	Description
MDC	G5	I	LVTTL	MDIO clock input.
MDIO	G4	I/O	LVTTL_in/LVTTL_OD	MDIO data I/O.
MODE0	N13	I	LVTTL	Mode select input bit 0. See Operating Modes, page 84.
MODE1	T11	I	LVTTL	Mode select input bit 1. See Operating Modes, page 84.
MODE2	T12	I	LVTTL	Mode select input bit 2. Connect to ground.
PADDR2	C13	I	LVTTL	MDIO port address bit 2. Internally pulled low.
PADDR3	C12	I	LVTTL	MDIO port address bit 3. Internally pulled low.
PADDR4	F13	I	LVTTL	MDIO port address bit 4. Internally pulled low.
STWA0	C10	I	LVTTL	Two-wire serial address 0. Leave unconnected when EEPROM is not used.
STWA1	C9	I	LVTTL	Two-wire serial address 1. Leave unconnected when EEPROM is not used.
STWA2	F12	I	LVTTL	Two-wire serial address 2. Leave unconnected.
STWSCL	E8	I/O	LVTTL_in/LVTTL_OD	Two-wire serial master clock. Leave unconnected when EEPROM is not used.
STWSDA	D8	I/O	LVTTL_in/LVTTL_OD	Two-wire serial slave data I/O. Leave unconnected when EEPROM is not used.

6.2.4 Ground

The following table lists the ground pins for the VSC8484 device.

Table 581 • **Ground Pins**

Name	Number	I/O	Description
GND	A1, A6, A11, A16, A17, A18, B1, B11, B16, C1, C2, C3, C4, C5, C6, C16, C17, C18, D3, D9, D11, D13, D16, E3, E9, E11, E13, E16, E17, E18, F3, F14, F16, G3, G6, G9, G12, G16, G17, G18, H1, H3, H6, H9, H12, H16, J3, J6, J9, J12, J14, J16, J17, J18, K3, K6, K9, K12, K14, K16, L3, L6, L9, L12, L16, L17, L18, M3, M6, M9, M12, M16, N1, N3, N14, N16, N17, N18, P3, P10, P12, P14, P16, R3, R10, R12, R14, R16, R17, R18, T3, T4, T5, T6, T7, T14, T16, U8, 13, U15, U16, U17, U18, V1, V2, V3, V8, V13, V15, V18	GND	Ground

6.2.5 Power Supply

The following table lists the power supply pins for the VSC8484 device.

Table 582 • **Power Supply Pins**

Name	Number	I/O	Description
VDD12TX0	G7, G8	Power supply	1.2 V power supply for PMA transmit channel 0
VDD12TX1	H7, H8	Power supply	1.2 V power supply for PMA transmit channel 1
VDD12TX2	L7, L8	Power supply	1.2 V power supply for PMA transmit channel 2
VDD12TX3	M7, M8	Power supply	1.2 V power supply for PMA transmit channel 3
VDD12X0	H4, H5	Power supply	1.2 V power supply for XAUI channel 0
VDD12X1	J4, J5	Power supply	1.2 V power supply for XAUI channel 1
VDD12X2	K4, K5	Power supply	1.2 V power supply for XAUI channel 2
VDD12X3	L4, L5	Power supply	1.2 V power supply for XAUI channel 3
VDD18RX0	G10, G11	Power supply	1.8 V power supply for PMA receive channel 0
VDD18RX1	J10, J11	Power supply	1.8 V power supply for PMA receive channel 1
VDD18RX2	K10, K11	Power supply	1.8 V power supply for PMA receive channel 2
VDD18RX3	M10, M11	Power supply	1.8 V power supply for PMA receive channel 3
VDD18TX0	G14	Power supply	1.8 V power supply for PMA transmit channel 0
VDD18TX1	H14	Power supply	1.8 V power supply for PMA transmit channel 1
VDD18TX2	L14	Power supply	1.8 V power supply for PMA transmit channel 2
VDD18TX3	M14	Power supply	1.8 V power supply for PMA transmit channel 3
VDDB12	J7, J8, K7, K8, K13	Power supply	1.2 V power supply for device core
VDDCLK	J13	Power supply	1.2 V power supply for internal reference clock generator
VDDMDIO	C7	Power supply	MDIO power supply
VDDTTLL	T8	Power supply	Lower TTL power supply(1)
VDDTTLU	C11	Power supply	Upper TTL power supply(1)

1. VDDTTLL and VDDTTLU should be tied to the same power supply.

6.2.6 Receive Path

The following table lists the receive path pins for the VSC8484 device.

Table 583 • **Receive Path Pins**

Name	Number	I/O	Type	Description
LOPC0	F10	I	LVTTL	Loss of optical carrier channel 0. Internally pulled high
LOPC1	F8	I	LVTTL	Loss of optical carrier channel 1. Internally pulled high
LOPC2	R8	I	LVTTL	Loss of optical carrier channel 2. Internally pulled high
LOPC3	P9	I	LVTTL	Loss of optical carrier channel 3. Internally pulled high
RXCRUFILT0	D14	Analog		Receive channel 0 CDR filter capacitor
RXCRUFILT1	E15	Analog		Receive channel 1 CDR filter capacitor
RXCRUFILT2	M15	Analog		Receive channel 2 CDR filter capacitor
RXCRUFILT3	P15	Analog		Receive channel 3 CDR filter capacitor
RXIN0N	B17	I	CML	Receive channel 0 input data complement
RXIN0P	B18	I	CML	Receive channel 0 input data true
RXIN1N	F17	I	CML	Receive channel 1 input data complement
RXIN1P	F18	I	CML	Receive channel 1 input data true
RXIN2N	K17	I	CML	Receive channel 2 input data complement
RXIN2P	K18	I	CML	Receive channel 2 input data true
RXIN3N	P17	I	CML	Receive channel 3 input data complement
RXIN3P	P18	I	CML	Receive channel 3 input data true
RXINCM0	D15	Analog		Receive channel 0 input data common-mode
RXINCM1	H15	Analog		Receive channel 1 input data common-mode
RXINCM2	L15	Analog		Receive channel 2 input data common-mode
RXINCM3	T15	Analog		Receive channel 3 input data common-mode

6.2.7 Reference Clock

The following table lists the LVPECL-tolerant reference clock pins for the VSC8484 device.

Table 584 • **Reference Clock Pins**

Name	Number	I/O	Type	Description
CMUFILTER	G15	Analog		Reference clock CMU filter capacitor
SREFCKN	U14	I	CML	Sync-E reference clock input complement
SREFCKP	V14	I	CML	Sync-E reference clock input true
WREFCKN	V17	I	CML	WAN reference clock input complement
WREFCKP	V16	I	CML	WAN reference clock input true
XREFCKN	K15	I	CML	Reference clock input complement
XREFCKP	J15	I	CML	Reference clock input true

6.2.8 Clock Outputs

The following table lists the clock pin outputs for the VSC8484 device.

Table 585 • **Clock Pins**

Name	Number	I/O	Type	Description
RX0CKOUTN	E10	O	CML	Selectable clock output channel 0 complement. See Register Device 1, Address A008.
RX0CKOUTP	D10	O	CML	Selectable clock output channel 0 true. See Register Device 1, Address A008.
RX1CKOUTN	H11	O	CML	Selectable clock output channel 1 complement. See Register Device 1, Address A008.
RX1CKOUTP	H10	O	CML	Selectable clock output channel 1 true. See Register Device 1, Address A008.
RX2CKOUTN	L13	O	CML	Selectable clock output channel 2 complement. See Register Device 1, Address A008.
RX2CKOUTP	M13	O	CML	Selectable clock output channel 2 true. See Register Device 1, Address A008.
RX3CKOUTN	R11	O	CML	Selectable clock output channel 3 complement. See Register Device 1, Address A008.
RX3CKOUTP	P11	O	CML	Selectable clock output channel 3 true. See Register Device 1, Address A008.
TX0CKOUTN	E12	O	CML	Selectable clock output channel 0 complement. See Register Device 1, Address A009.
TX0CKOUTP	D12	O	CML	Selectable clock output channel 0 true. See Register Device 1, Address A009.
TX1CKOUTN	H13	O	CML	Selectable clock output channel 1 complement. See Register Device 1, Address A009.
TX1CKOUTP	G13	O	CML	Selectable clock output channel 1 true. See Register Device 1, Address A009.
TX2CKOUTN	L11	O	CML	Selectable clock output channel 2 complement. See Register Device 1, Address A009.
TX2CKOUTP	L10	O	CML	Selectable clock output channel 2 true. See Register Device 1, Address A009.
TX3CKOUTN	R13	O	CML	Selectable clock output channel 3 complement. See Register Device 1, Address A009.
TX3CKOUTP	P13	O	CML	Selectable clock output channel 3 true. See Register Device 1, Address A009.

6.2.9 Test and Mode Control

The following table lists the test and mode control pins for the VSC8484 device.

Table 586 • **Test and Mode Control Pins**

Name	Number	I/O	Type	Description
ANATEST	R9	Analog	Analog	Analog test port. Factory test purpose only. Leave unconnected when not used.
RESETN	C8	I	LVTTL	Reset. Low = reset. Internally pulled high.

Table 586 • **Test and Mode Control Pins *(continued)***

Name	Number	I/O	Type	Description
SCAN_EN	T10	I	LVTTL	Scan enable input. Factory test purpose only. Connect to ground.
TMON	T13		Analog	Temperature monitor output. Leave unconnected when not used.

6.2.10 Transmit Path

The following table lists the transmit path pins for the VSC8484 device.

Table 587 • **Transmit Path Pins**

Name	Number	I/O	Type	Description
CMUFILT0	E14	Analog		Transmit channel 0 CMU filter capacitor
CMUFILT1	F15	Analog		Transmit channel 1 CMU filter capacitor
CMUFILT2	N15	Analog		Transmit channel 2 CMU filter capacitor
CMUFILT3	R15	Analog		Transmit channel 3 CMU filter capacitor
TXOUT0N	D17	O	CML	Transmit channel 0 output data complement
TXOUT0P	D18	O	CML	Transmit channel 0 output data true
TXOUT1N	H17	O	CML	Transmit channel 1 output data complement.
TXOUT1P	H18	O	CML	Transmit channel 1 output data true
TXOUT2N	M17	O	CML	Transmit channel 2 output data complement
TXOUT2P	M18	O	CML	Transmit channel 2 output data true
TXOUT3N	T17	O	CML	Transmit channel 3 output data complement
TXOUT3P	T18	O	CML	Transmit channel 3 output data true

6.2.11 XAUI Channel

The following table lists the XAUI channel pins for the VSC8484 device.

Table 588 • **XAUI Pins**

Name	Number	I/O	Type	Description
XAUIFILT0	B6		Analog	XAUI channel 0 CMU filter capacitor
XAUIFILT1	H2		Analog	XAUI channel 1 CMU filter capacitor
XAUIFILT2	N2		Analog	XAUI channel 2 CMU filter capacitor
XAUIFILT3	U3		Analog	XAUI channel 3 CMU filter capacitor
XRX0_0N	A10	I	CML	XAUI channel 0, Rx path lane 0, serial data input complement.
XRX0_0P	B10	I	CML	XAUI channel 0, Rx path lane 0, serial data input true.
XRX0_1N	A9	I	CML	XAUI channel 0, Rx path lane 1, serial data input complement.
XRX0_1P	B9	I	CML	XAUI channel 0, Rx path lane 1, serial data input true.
XRX0_2N	A8	I	CML	XAUI channel 0, Rx path lane 2, serial data input complement.
XRX0_2P	B8	I	CML	XAUI channel 0, Rx path lane 2, serial data input true.

Table 588 • **XAUI Pins** ***(continued)***

Name	Number	I/O	Type	Description
XRX0_3N	A7	I	CML	XAUI channel 0, Rx path lane 3, serial data input complement.
XRX0_3P	B7	I	CML	XAUI channel 0, Rx path lane 3, serial data input true.
XRX1_0N	D1	I	CML	XAUI channel 1, Rx path lane 0, serial data input, complement.
XRX1_0P	D2	I	CML	XAUI channel 1, Rx path lane 0, serial data input, true.
XRX1_1N	E1	I	CML	XAUI channel 1, Rx path lane 1, serial data input, complement.
XRX1_1P	E2	I	CML	XAUI channel 1, Rx path lane 1, serial data input, true.
XRX1_2N	F1	I	CML	XAUI channel 1, Rx path lane 2, serial data input, complement.
XRX1_2P	F2	I	CML	XAUI channel 1, Rx path lane 2, serial data input, true.
XRX1_3N	G1	I	CML	XAUI channel 1, Rx path lane 3, serial data input, complement.
XRX1_3P	G2	I	CML	XAUI channel 1, Rx path lane 3, serial data input, true.
XRX2_0N	P2	I	CML	XAUI channel 2, Rx path lane 0, serial data input, complement.
XRX2_0P	P1	I	CML	XAUI channel 2, Rx path lane 0, serial data input, true.
XRX2_1N	R2	I	CML	XAUI channel 2, Rx path lane 1, serial data input, complement.
XRX2_1P	R1	I	CML	XAUI channel 2, Rx path lane 1, serial data input, true.
XRX2_2N	T2	I	CML	XAUI channel 2, Rx path lane 2, serial data input, complement.
XRX2_2P	T1	I	CML	XAUI channel 2, Rx path lane 2, serial data input, true.
XRX2_3N	U2	I	CML	XAUI channel 2, Rx path lane 3, serial data input, complement.
XRX2_3P	U1	I	CML	XAUI channel 2, Rx path lane 3, serial data input, true.
XRX3_0N	U9	I	CML	XAUI channel 3, Rx path lane 0, serial data input, complement.
XRX3_0P	V9	I	CML	XAUI channel 3, Rx path lane 0, serial data input, true.
XRX3_1N	U10	I	CML	XAUI channel 3, Rx path lane 1, serial data input, complement.
XRX3_1P	V10	I	CML	XAUI channel 3, Rx path lane 1, serial data input, true.
XRX3_2N	U11	I	CML	XAUI channel 3, Rx path lane 2, serial data input, complement.
XRX3_2P	V11	I	CML	XAUI channel 3, Rx path lane 2, serial data input, true.
XRX3_3N	U12	I	CML	XAUI channel 3, Rx path lane 3, serial data input, complement.
XRX3_3P	V12	I	CML	XAUI channel 3, Rx path lane 3, serial data input, true.
XTX0_0N	B15	O	CML	XAUI channel 0, Tx path lane 0, serial data output complement.
XTX0_0P	A15	O	CML	XAUI channel 0, Tx path lane 0, serial data output true.

Table 588 • **XAUI Pins** ***(continued)***

Name	Number	I/O	Type	Description
XTX0_1N	B14	O	CML	XAUI channel 0, Tx path lane 1, serial data output complement.
XTX0_1P	A14	O	CML	XAUI channel 0, Tx path lane 1, serial data output true.
XTX0_2N	B13	O	CML	XAUI channel 0, Tx path lane 2, serial data output complement.
XTX0_2P	A13	O	CML	XAUI channel 0, Tx path lane 2, serial data output true.
XTX0_3N	B12	O	CML	XAUI channel 0, Tx path lane 3, serial data output complement.
XTX0_3P	A12	O	CML	XAUI channel 0, Tx path lane 3, serial data output true.
XTX1_0N	A5	O	CML	XAUI channel 1, Tx path lane 0, serial data output complement.
XTX1_0P	B5	O	CML	XAUI channel 1, Tx path lane 0, serial data output true.
XTX1_1N	A4	O	CML	XAUI channel 1, Tx path lane 1, serial data output complement.
XTX1_1P	B4	O	CML	XAUI channel 1, Tx path lane 1, serial data output true.
XTX1_2N	A3	O	CML	XAUI channel 1, Tx path lane 2, serial data output complement.
XTX1_2P	B3	O	CML	XAUI channel 1, Tx path lane 2, serial data output true.
XTX1_3N	A2	O	CML	XAUI channel 1, Tx path lane 3, serial data output complement.
XTX1_3P	B2	O	CML	XAUI channel 1, Tx path lane 3, serial data output true.
XTX2_0N	J1	O	CML	XAUI channel 2, Tx path lane 0, serial data output complement.
XTX2_0P	J2	O	CML	XAUI channel 2, Tx path lane 0, serial data output true.
XTX2_1N	K1	O	CML	XAUI channel 2, Tx path lane 1, serial data output complement.
XTX2_1P	K2	O	CML	XAUI channel 2, Tx path lane 1, serial data output true.
XTX2_2N	L1	O	CML	XAUI channel 2, Tx path lane 2, serial data output complement.
XTX2_2P	L2	O	CML	XAUI channel 2, Tx path lane 2, serial data output true.
XTX2_3N	M1	O	CML	XAUI channel 2, Tx path lane 3, serial data output complement.
XTX2_3P	M2	O	CML	XAUI channel 2, Tx path lane 3, serial data output true.
XTX3_0N	V4	O	CML	XAUI channel 3, Tx path lane 0, serial data output complement.
XTX3_0P	U4	O	CML	XAUI channel 3, Tx path lane 0, serial data output true.
XTX3_1N	V5	O	CML	XAUI channel 3, Tx path lane 1, serial data output complement.
XTX3_1P	U5	O	CML	XAUI channel 3, Tx path lane 1, serial data output true.
XTX3_2N	V6	O	CML	XAUI channel 3, Tx path lane 2, serial data output complement.
XTX3_2P	U6	O	CML	XAUI channel 3, Tx path lane 2, serial data output true.

Table 588 • **XAUI Pins *(continued)***

Name	Number	I/O	Type	Description
XTX3_3N	V7	O	CML	XAUI channel 3, Tx path lane 3, serial data output complement.
XTX3_3P	U7	O	CML	XAUI channel 3, Tx path lane 3, serial data output true.

6.2.12 Reserved

The following table lists the reserved pins for the VSC8484 device that should be left unconnected.

Table 589 • **Reserved Pins**

Name	Number	Description
RESERVED1	C15	Reserved
RESERVED2	C14	Reserved
RESERVED3	F11	Reserved
RESERVED4	F9	Reserved
RESERVED5	R7	Reserved
RESERVED6	R6	Reserved
RESERVED7	R5	Reserved
RESERVED8	R4	Reserved

7 Package Information

VSC8484XJP and VSC8484YJP are packaged in a lead-free (Pb-free), 324-pin FCBGA with a 19 mm × 19 mm body size, 1 mm pin pitch, and 2.74 mm maximum height. Note that for VSC8484XJP, only the second-level interconnect is lead-free.

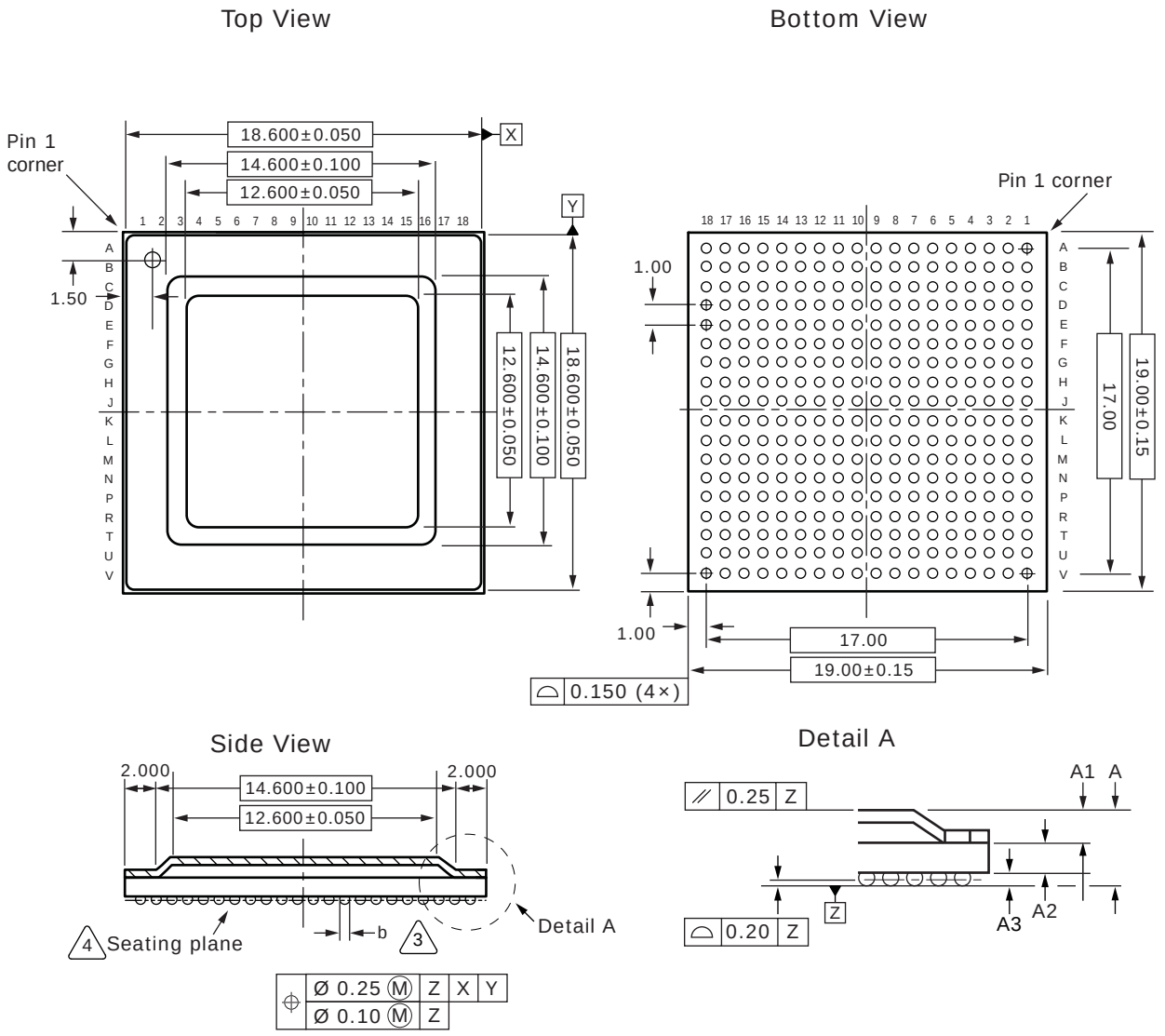
Lead-free products from Microsemi comply with the temperatures and profiles defined in the joint IPC and JEDEC standard IPC/JEDEC J-STD-020. For more information, see the IPC and JEDEC standard.

This section provides the package drawing, thermal specifications, and moisture sensitivity rating for the VSC8484 device.

7.1 Package Drawing

The following illustration shows the package drawing for the VSC8484 device. The drawing contains the top view, bottom view, side view, detail view, dimensions, tolerances, and notes.

Figure 52 • **Package Drawing**



Notes

1. All dimensions and tolerances are in millimeters (mm).
2. Maximum solder ball matrix size is 19 mm × 19 mm.
3. Dimension is measured at the maximum solder ball diameter, parallel to primary datum Z.
4. Primary datum Z and seating plane are defined by the spherical crowns of the solder balls.
5. Package corners are R1.00 mm.

Dimensions and Tolerances

Reference	Minimum	Nominal	Maximum
A	2.44	2.59	2.74
A1	1.25	1.30	1.35
A2	0.59	0.69	0.79
A3	0.4	0.5	0.6
b	0.5	0.60	0.7

7.2 Thermal Specifications

Thermal specifications for this device are based on the JEDEC JESD51 family of documents. These documents are available on the JEDEC Web site at www.jedec.org. The thermal specifications are modeled using a four-layer test board with two signal layers, a power plane, and a ground plane (2s2p

PCB). For more information about the thermal measurement method used for this device, see the JESD51-1 standard.

Table 590 • **Thermal Resistances**

Symbol	°C/W	Parameter
θ_{JCtop}	0.65	Die junction to package case top
θ_{JB}	5.9	Die junction to printed circuit board
θ_{JA}	14.2	Die junction to ambient
θ_{JMA} at 1 m/s	11.3	Die junction to moving air measured at an air speed of 1 m/s
θ_{JMA} at 2 m/s	9.4	Die junction to moving air measured at an air speed of 2 m/s

To achieve results similar to the modeled thermal measurements, the guidelines for board design described in the JESD51 family of publications must be applied. For information about applications using FCBGA packages, see the following:

- JESD51-2A, *Integrated Circuits Thermal Test Method Environmental Conditions, Natural Convection (Still Air)*
- JESD51-6, *Integrated Circuit Thermal Test Method Environmental Conditions, Forced Convection (Moving Air)*
- JESD51-8, *Integrated Circuit Thermal Test Method Environmental Conditions, Junction-to-Board*
- JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

7.3 Moisture Sensitivity

This device is rated moisture sensitivity level 4 as specified in the joint IPC and JEDEC standard IPC/JEDEC J-STD-020. For more information, see the IPC and JEDEC standard.

8 Design Guidelines

This section provides information about design guidelines for the VSC8484 device.

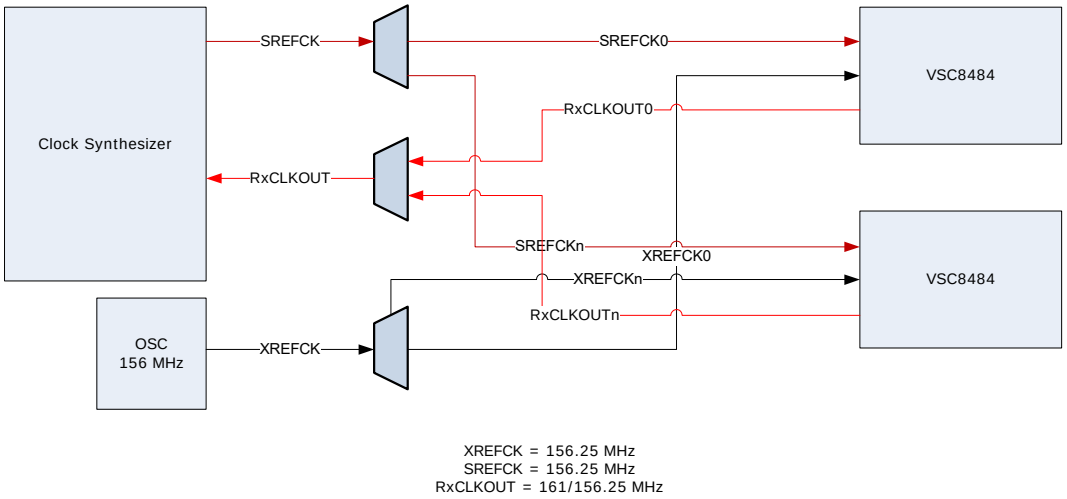
8.1 Sync-E in LAN Mode

In one implementation, a free-running clock for the XREFCK is used for the core logic, XAUI block, and CRU to recover the clock from the 10G input data. The recovered clock is fed back to an external PLL so that the PLL locks to this recovered clock and provides a Sync-E master clock for the Tx paths for all PHYs. This Sync-E clock is fed to the VSC8484 device CMU through SREFCK.

The advantage of this approach is that the clock for the Tx path (CMU) and Rx path (CRU) is separated. Moreover, the free-running clock to the XAUI and block eliminates having the local reference clock extract the recovered clock while requiring the recovered clock to be the local reference clock.

The following illustration shows the diagram using a free-running clock.

Figure 53 • **Sync-E LAN Mode with Free-Running Clock**

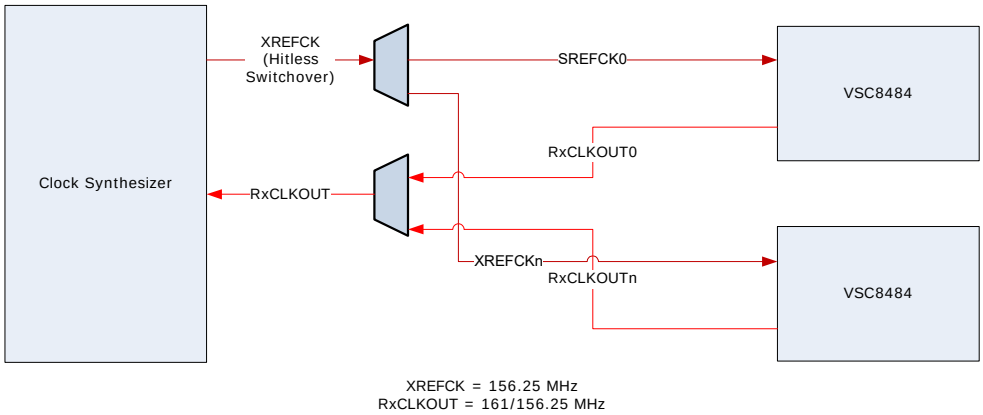


Another way to implement Sync-E is to use a hitless clock driver. An external PLL provides a clock to the XREFCK as a free running clock at the beginning. In this mode the XREFCK is used for core logic, XAUI block, CRU to recover the clock from the 10G input data, and the CMU to generate the 10G output data. When there is a recovered clock present, the PLL can switch its output from the original free running clock to a clock locked to the recovered clock. This switching is performed slowly within 100 ppm and the edge of the clock is moved gradually. As a result, the clock seen by the VSC8484 device is like a free-running clock with some jitter within specifications during the transition from one clock to another. This is called hitless switching.

Clock devices such as ZL30160 from Zarlink or SI5326 from Silab can provide this hitless feature. Because the switch of the clock is hitless, the VSC8484 device runs everything based on the XREFCK, and no SREFCK input is required.

The following illustration shows the diagram using a hitless clock.

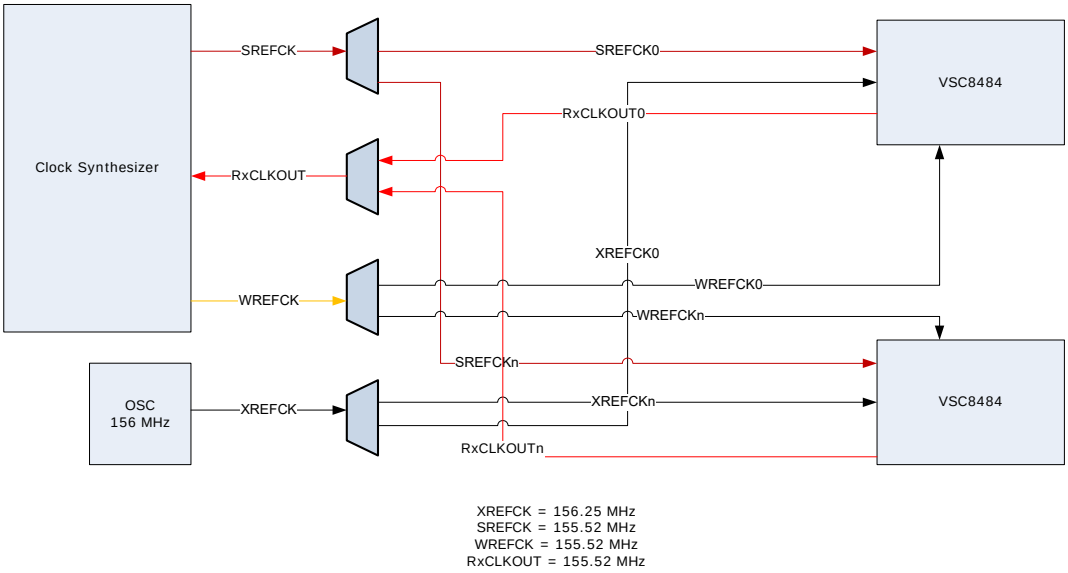
Figure 54 • **Sync-E LAN Mode with Hitless Clock**



8.2 Sync-E in WAN Mode

In Sync-E WAN mode, the concept is the same except that an extra WREFCK is required. The XREFCK is always needed for the core logic and XAUI block. The WREFCK is used for the CRU to recover the clock from the 10G input data. The recovered clock is fed back to an external PLL so that the PLL locks to this recovered clock and provides a Sync-E master clock for the Tx paths for all PHYs. This Sync-E clock is fed to the VSC8484 device CMU through SREFCK.

Figure 55 • **Sync-E WAN Mode**



In an alternative option, the role of XREFCK is the same for the core logic and XAUI block. The WREFCK is used for both the CRU and the CMU. Instead of using SREFCK for the CMU, the Sync-E master clock is fed back to WREFCK instead of XREFCK as in the Sync-E LAN mode. Again, the Sync-E master clock is supposed to be hitless as described in the previous section.

9 Ordering Information

VSC8484XJP and VSC8484YJP are packaged in a lead-free (Pb-free), 324-pin FCBGA with a 19 mm × 19 mm body size, 1 mm pin pitch, and 2.74 mm maximum height. Note that for VSC8484XJP, only the second-level interconnect is lead-free.

Lead-free products from Microsemi comply with the temperatures and profiles defined in the joint IPC and JEDEC standard IPC/JEDEC J-STD-020. For more information, see the IPC and JEDEC standard.

The following table lists the ordering information for the VSC8484 device.

Table 591 • **Ordering Information**

Part Order Number	Description
VSC8484XJP	Lead-free (second-level interconnect only), 324-pin FCBGA with a 19 mm × 19 mm body size, 1 mm pin pitch, and 2.74 mm maximum height
VSC8484YJP	Lead-free, 324-pin FCBGA with a 19 mm × 19 mm body size, 1 mm pin pitch, and 2.74 mm maximum height