TEXAS INSTRUMENTS

TAS5504-5142V4EVM User's Guide

Evaluation Module for TAS5504A 4-Channel Digital Audio PWM Processor and TAS5142 Digital Amplifier Power-Output Stage

User's Guide

June 2006 Digital Audio & Video Products

SLEU075

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About This Manual

This manual describes the operation of the TAS5504-5142V4EVM evaluation module from Texas Instruments (TI).

How to Use This Manual

This document contains the following chapters:

Chapter 1 - Overview

Chapter 2 - System Interfaces

Chapter 3 - Protection

Chapter 4 - Configuration for 2.1 System

Information About Cautions and Warnings

This manual may contain cautions and warnings.

CAUTION

This is an example of a caution statement.

A caution statement describes a situation that could potentially damage your software or equipment.

WARNING

This is an example of a warning statement.

A warning statement describes a situation that could potentially cause harm to you.

The information in a caution or a warning is provided for your protection. Please read each caution and warning carefully.

Related Documentation From TI

Table 1 contains a list of data manuals that have detailed descriptions of the integrated circuits used in the design of TAS5504-5142V4EVM. The data manuals can be obtained at http://www.ti.com.

Table 1. Related Documentation From TI

PART NUMBER	LITERATURE NUMBER
TAS5504A	SLES169
TAS5142	SLES126
LM358	SLOS068
UA78M12	SLVS059
TPS76733	SLVS208

Additional Documentation

- *TAS5504-5142V4EVM Application Report (SLEA060)*
- *PC Configuration Tool for TAS5504* (TAS5508 GUI Ver. 4.0 or later)
- General application notes

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Overview

The TAS5504-5142V4EVM PurePath Digital™ customer evaluation amplifier module demonstrates two audio integrated circuits, TAS5504A and TAS5142, from Texas Instruments (TI).

The TAS5504APAG is a high-performance 32-bit (24-bit input) multichannel PurePath Digital pulse width modulator (PWM) based on Equibit technology, with a fully symmetrical AD modulation scheme. It accepts input sample rates from 32 kHz to 192 kHz. The device also has digital audio processing (DAP) that provides 48-bit signal processing, advanced performance, and a high level of system integration. The device has interfaces for headphone output and power supply volume control (PSVC).

The TAS5142DDV is a compact, high-power, digital amplifier power stage designed to drive a 4-Ω loudspeaker up to 100 W/10% THD+N. It contains integrated gate drivers, eight matched and electrically isolated enhancement-mode N-channel power DMOS transistors, and protection/fault-reporting circuitry.

The DDV package has a PowerPAD™ on the top side for heat transfer through a heatsink. The heat sink in this design is for evaluation purpose only.

This EVM, together with a TI input-USB board, is a complete 4-channel (or 2.1-channel) digital audio amplifier system that includes digital input (S/PDIF), analog inputs, interface to PC, and DAP features, such as digital volume control, input and output mixers, auto mute, equalization, tone controls, loudness, and dynamic range compression.

This system is designed for home theater applications, such as flatscreen TVs, DVD minicomponent systems, home theater in a box (HTIB), or DVD receivers.

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1.1 TAS5504-5142V4EVM Features

- 4-channel (or 2.1-channel) PurePath Digital evaluation module
- Self-contained protection system (short circuit and thermal)
- Standard I^2S and I^2C/control connector for TI input board
- Double-sided plated-through PCB layout

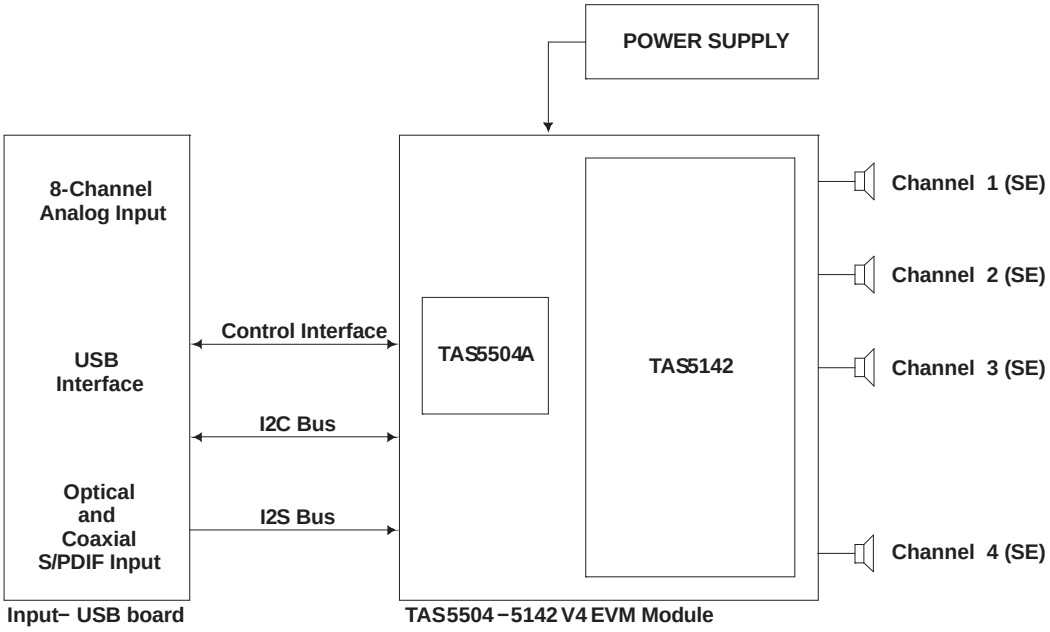

Figure 1-1. Integrated PurePath Digital™ Amplifier System

1.2 PCB Key Map

Physical structure for the TAS5504-5142V4EVM is illustrated in Figure 1-2.

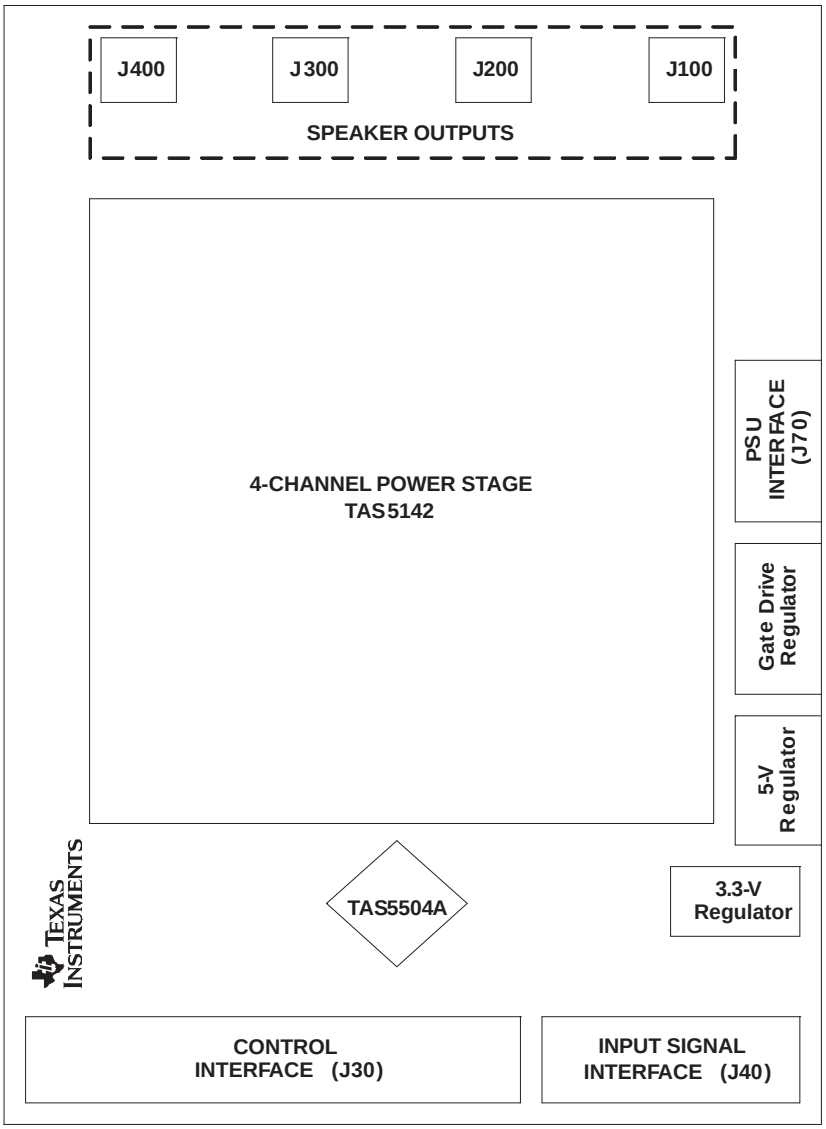

Figure 1-2. Physical Structure for TAS5504-5142V4EVM (Rough Outline)

System Interfaces

This chapter describes the TAS5504-5142V4EVM board, with regard to power supplies and system interfaces.

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2.1 Power Supply (PSU) Interface (J70)

The TAS5504-5142V4EVM module must be powered from external power supplies. High-end audio performance requires a stabilized power supply, with low ripple voltage and low output impedance.

Note: The length of power-supply cable must be minimized. Increasing the length of PSU cable is equal to increasing the distortion for the amplifier at high output levels and low frequencies.

Maximum output-stage supply voltage depends of the speaker load resistance. Check the recommended maximum supply voltage in the TAS5142 data sheet.

Table 2-1. Recommended Supply Voltages

DESCRIPTION	VOLTAGE LIMITATIONS (4-Ω LOAD)	CURRENT RECOMMENDATIONS
System power supply	15 V – 20 V	0.2 A
Output-stage power supply	0 V – 32 V	2 A (1)

(1) The rated current corresponds to two-channel full scale (30 W each), which most likely is adequate for a standard 2.1 channel amplifier design.

The recommended TAS5142 power-up sequence is shown in Figure 2-1. For proper TAS5142 operation, the $\overline{\text{RESET}}$ signal should be kept low during power up. $\overline{\text{RESET}}$ is pulled low during power up for 200 ms by the onboard reset generator (U73).

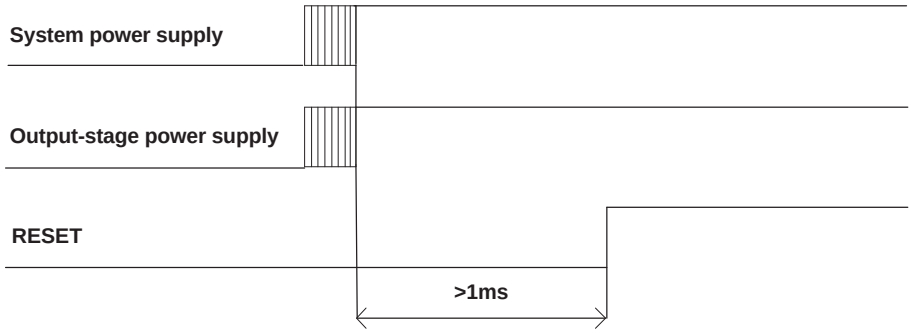
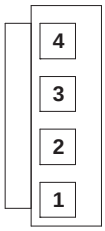


Figure 2-1. Recommended Power-Up Sequence



(PCB Connector Top View)

Figure 2-2. J70 Pin Numbers

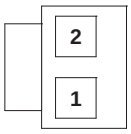
Table 2-2. J70 Pin Description

PIN NO.	NET NAME AT SCHEMATICS	DESCRIPTION
1	PVDD	Output-stage power supply
2		System power supply
3	GND	Ground
4	GND	Ground

2.2 Loudspeaker Connectors (J100 . . . J400)

CAUTION

Both positive and negative speaker outputs are floating and may not be connected to ground (e.g., through an oscilloscope).



(PCB Connector Top View)

Figure 2-3. J100 . . . J400 Pin Numbers

Table 2-3. J100 . . . J400 Pin Description

PIN NO.	NET NAME AT SCHEMATICS	DESCRIPTION
1	OUT-1	Speaker negative output
2	OUT-2	Speaker positive output

2.3 Control Interface (J40)

This interface connects the TAS5504-5142V4EVM board to a TI input-USB board.

Table 2-4. J40 Pin Description

PIN NO.	NET NAME AT SCHEMATICS	DESCRIPTION
1	GND	Ground
2	RESERVED	
3	GND	Ground
4	$\overline{\text{RESET}}$	System reset (bidirectional). Activate $\overline{\text{MUTE}}$ before $\overline{\text{RESET}}$ for quiet reset
5	$\overline{\text{BKND-ERR}}$	Backend error (or soft reset) provides reduced click and pop reset, without resetting I^2C volume register settings.
6	$\overline{\text{MUTE}}$	Ramp volume from any setting to noiseless soft mute. Mute also can be activated by I^2C.
7	$\overline{\text{PDN}}$	Power down. TAS5504A goes to the power-down state when activated.
8	RESERVED	
9	RESERVED	
10	SDA	I^2C bit clock
11	GND	Ground
12	SCL	I^2C bit clock
13	RESERVED	
14	RESERVED	
15	RESERVED	
16	RESERVED	
17	GND	Ground
18	RESERVED	
19	RESERVED	
20	$\overline{\text{SD}}$	Shutdown error reporting for all channels. Activated if TAS5142 has high current or high temperature. See Chapter 3: *Protection.*
21	RESERVED	
22	$\overline{\text{OTW}}$	Temperature warning. Activated if TAS5142 has reached temperature warning level.
23	RESERVED	
24	RESERVED	
25	GND	Ground
26	GND	Ground
27	RESERVED	
28	RESERVED	
29	RESERVED	
30	RESERVED	
31	GND	Ground
32	GND	Ground
33	+5 V	+5Vdc power supply (output)
34	+5 V	+5Vdc power supply (output)

2.4 Digital Audio Interface (J60)

The digital audio interface contains digital audio signal data (I^2S), clocks, etc. Please see the *TAS5504A Data Manual* for signal timing and details not explained in this document.

Table 2-5. J60 Pin Description

PIN NO.	NET NAME AT SCHEMATICS	DESCRIPTION
1	GND	Ground
2	MCLK	Master clock input. Low-jitter system clock for PWM generation and reclocking. Ground connection from source to TAS5504A must be a low impedance connection.
3	GND	Ground
4	SDIN1	I^2S data 1, channel 1 and 2
5	SDIN2	I^2S data 2, channel 3 and 4
6	SDIN3	I^2S data 3
7	SDIN4	I^2S data 4
8		Reserved
9		Reserved
10	GND	Ground
11	SCLK	I^2S bit clock
12	GND	Ground
13	LRCLK	I^2S left-right clock
14	GND	Ground
15		Reserved
16	GND	Ground

Protection

This section describes the short-circuit protection and fault-reporting circuitry of the TAS5142 device.

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3.1 Short-Circuit Protection and Fault-Reporting Circuitry

The TAS5142 is a self-protecting device that provides device fault reporting (including high-temperature protection and short-circuit protection). The TAS5142 is configured in back-end auto-recovery mode and therefore, resets automatically after all errors. This means that the device restarts itself after an error occasion and reports shortly through the $\overline{SD}$ signal.

3.2 Fault Reporting

The $\overline{OTW}$ and $\overline{SD}$ outputs from the TAS5142 indicate fault conditions. Please refer to the *TAS5142 Data Manual* for a description of these pins.

Table 3-1. TAS5152 Warning/Error Signal Decoding

$\overline{OTW}$	$\overline{SD}$	DEVICE CONDITION
0	0	High-temperature error and/or high-current error
0	1	High-temperature warning
1	0	Undervoltage lockout or high-current error
1	1	Normal operation, no errors/warnings

The shutdown signals, together with the temperature warning signal, gives chip state information as described in the Table 3-1. Device fault-reporting outputs are open-drain outputs.

Configuration for 2.1 System

The TAS5504-5142V4EVM can be configured for 2.1 operation. This gives two SE channels 30 W, and one BTL channel 60 W.

This section describes actions needed to change the EVM to 2.1 operation.

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4.1 TAS5504-5542V4EVM for 2.1 System

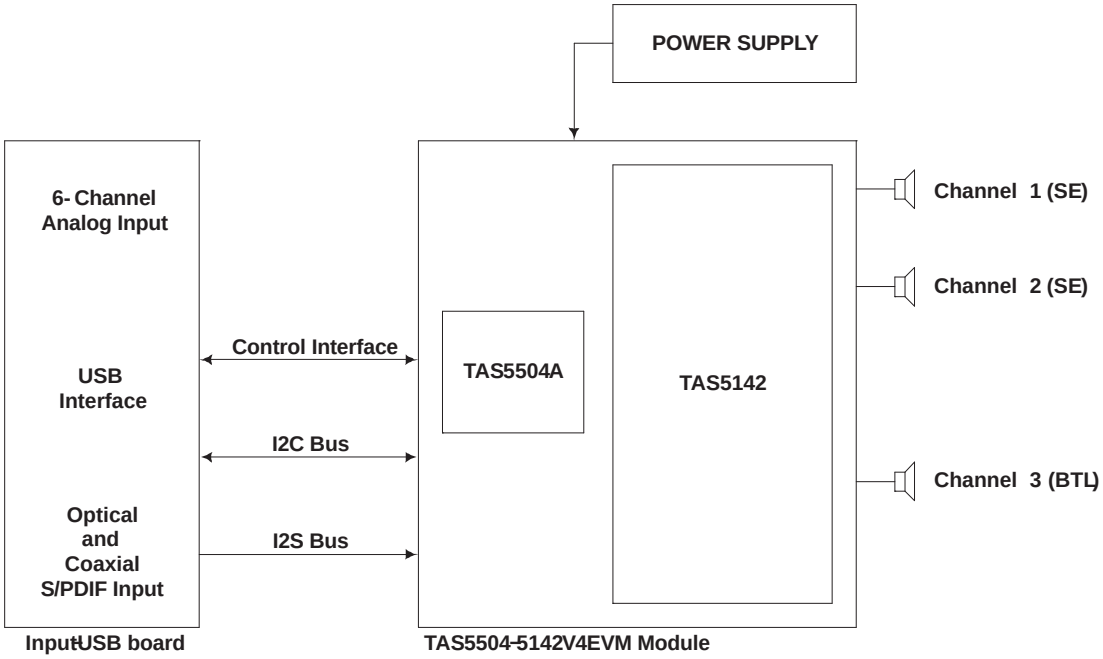

Figure 4-1. Integrated PurePath Digital™ Amplifier 2.1 System

For operation in 2.1 mode, channel 3 and channel 4 are used to create a BTL channel. This is done by using J350 (not mounted on standard EVM). Furthermore, the TAS5504A must be set up to use two outputs as one. This is done by mixing DAP channel 7 with a gain of –1 to PWM 8 output. Following commands will result in the settings in Table 4-1.

Table 4-1. TAS5504A Register Settings(1)

REGISTER	I²C ADDRESS	VALUE	NOTES
Output Mixer Register PWM channel 7	0×B0	40 80 00 00	Mix DAP channel 5 into PWM channel 7
		00 00 00 00	
Output Mixer Register PWM channel 8	0×B1	7F 80 00 00	Mix DAP channel 6 into PWM channel 8
		00 00 00 00	

(1) These register settings must be sent after each reset.

In a final application, this is implemented in hardware instead.

4.2 PCB Key Map for 2.1 Configuration

Physical structure for the TAS5504-5142V4EVM is illustrated in Figure 4-2.

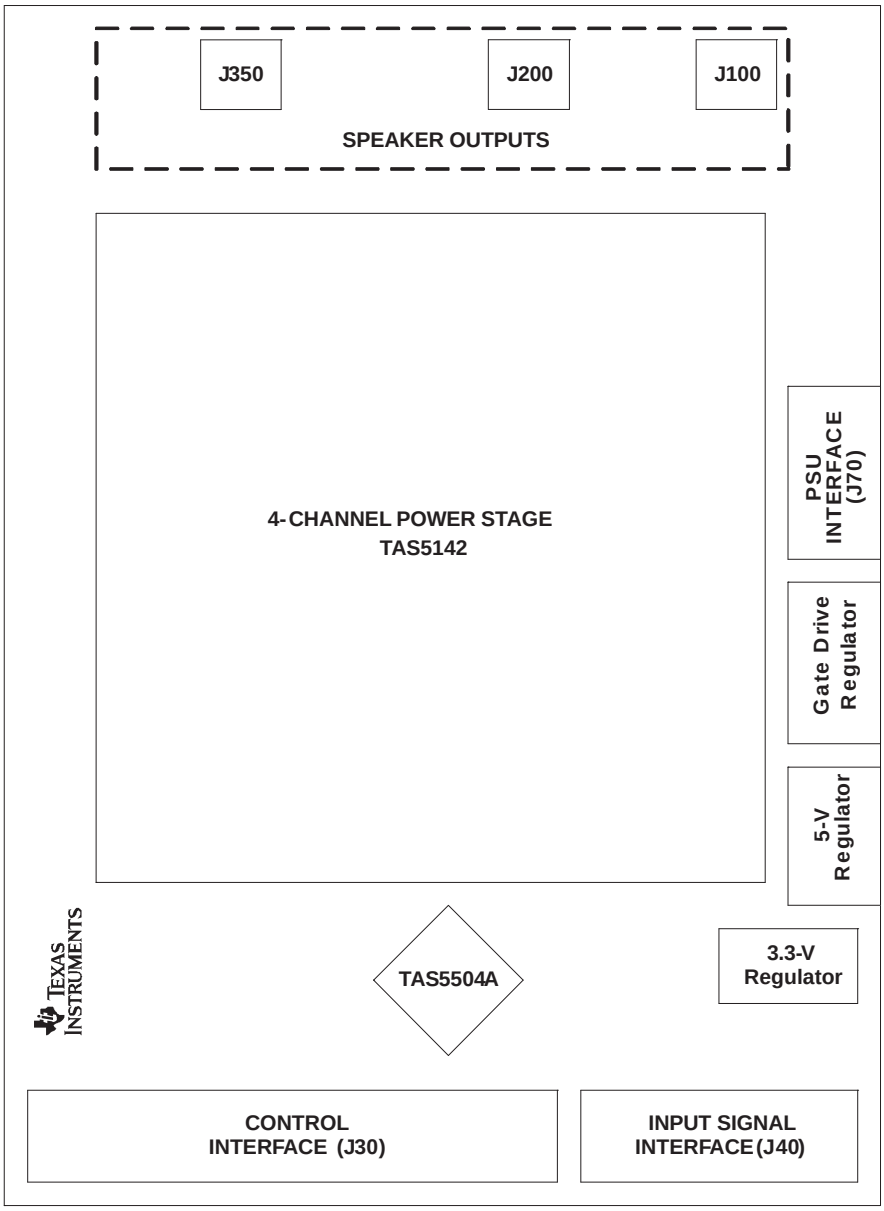

Figure 4-2. Physical Structure for TAS5504-5142V4EVM (Rough Outline)

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of 0 V to 35 V and the output voltage range of 15 V to 20 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 75° C. The EVM is designed to operate properly with certain components above 75° C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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