SBAS357A – SEPTEMBER 2006 – REVISED OCTOBER 2007

LOW-POWER, 12-Bit ANALOG-TO-DIGITAL CONVERTER with I²C™ INTERFACE

FEATURES

- **Complete 12-Bit Data Acquisition System in a Tiny SOT-23 Package**
- **Low Current Consumption: Only 90µA**
- **Integral Nonlinearity: 1LSB Max**
- **Single-Cycle Conversion**
- **Programmable Gain Amplifier Gain = 1, 2, 4, or 8**
- **128SPS Data Rate**
- **I²C Interface with Two Available Addresses**
- **Power Supply: 2.7V to 5.5V**
- **Pin- and Software-Compatible with 16-Bit ADS1100**

APPLICATIONS

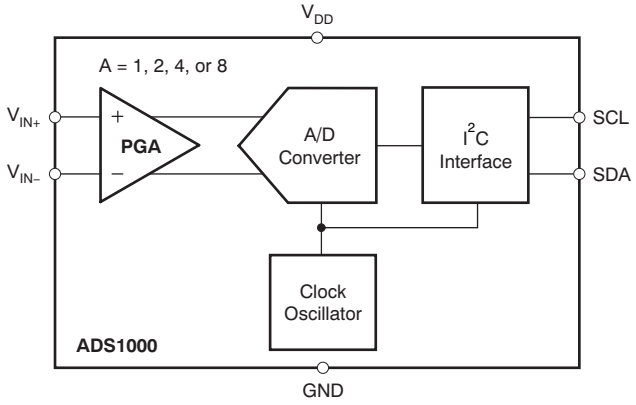
- **Voltage Monitors**
- **Battery Management**
- **Industrial Process Control**
- **Consumer Goods**
- **Temperature Measurement**

DESCRIPTION

The ADS1000 is an I²C-compatible serial interface Analog-to-Digital (A/D) converter with differential inputs and 12 bits of resolution in a tiny SOT23-6 package. Conversions are performed ratiometrically, using the power supply as the reference voltage. The ADS1000 operates from a single power supply ranging from 2.7V to 5.5V.

The ADS1000 performs conversions at a rate of 128 samples per second (SPS). The onboard programmable gain amplifier (PGA), which offers gains of up to 8, allows smaller signals to be measured with high resolution. In single-conversion mode, the ADS1000 automatically powers down after a conversion, greatly reducing current consumption during idle periods.

The ADS1000 is designed for applications where space and power consumption are major considerations. Typical applications include portable instrumentation, consumer goods, and voltage monitoring.



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

For the most current package and ordering information, see the Package Option Addendum located at the end of this datasheet or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range (unless otherwise noted).

	ADS1000	UNIT
V_{DD} to GND	–0.3 to +6	V
Input Current (Momentary)	100	mA
Input Current (Continuous)	10	mA
Voltage to GND, V_{IN+}, $V_{IN–}$	–0.3 to V_{DD} to +0.3	V
Voltage to GND, SDA, SCL	–0.5 to +6	V
Maximum Junction Temperature, T_J	+150	°C
Operating Temperature	–40 to +125	°C
Storage Temperature	–60 to +150	°C
Lead Temperature (soldering, 10s)	+300	°C

(1) Stresses above those listed under ***Absolute Maximum Ratings*** may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

PIN CONFIGURATIONS



NOTE: Marking text direction indicates pin 1. Marking text depends on I^2C address; see Package Option Addendum.

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ELECTRICAL CHARACTERISTICS

All specifications at –40°C to +85°C, V_{DD} = 5V, GND = 0V, and all PGAs, unless otherwise noted.

PARAMETER	CONDITIONS	ADS1000			UNIT
		MIN	TYP	MAX	
ANALOG INPUT					
Full-Scale Input Voltage	$(V_{IN+}) – (V_{IN–})$		$\pm V_{DD}/PGA$ (1)		V
Analog Input Voltage	V_{IN+}, $V_{IN–}$ to GND	GND – 0.2		V_{DD} + 0.2	V
Differential Input Impedance			2.4/PGA		MΩ
Common-Mode Input Impedance			8		MΩ
SYSTEM PERFORMANCE					
Resolution	No Missing Codes	12			Bits
Data Rate		104	128	184	SPS
Integral Nonlinearity (INL)			±0.1	1	LSB
Offset Error			1	±2	LSB
Gain Error			0.01	0.1	%
DIGITAL INPUT/OUTPUT					
Logic Level					
V_{IH}		0.7 VDD		6	V
V_{IL}		GND – 0.5		0.3 V_{DD}	V
V_{OL}	I_{OL} = 3mA	GND		0.4	V
Input Leakage					
I_{IH}	V_{IH} = 5.5V			10	µA
I_{IL}	V_{IL} = GND	– 10			µA
POWER-SUPPLY REQUIREMENTS					
Power-Supply Voltage	V_{DD}	2.7		5.5	V
Supply Current	Power-Down		0.05	2	µA
	Active		90	150	µA
Power Dissipation					µA
	V_{DD} = 5.0V		450	750	µW
	V_{DD} = 3.0V		210		µW

(1) Each input, V_{IN+} and $V_{IN–}$, must meet the absolute input voltage specifications.

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TYPICAL CHARACTERISTICS

At T_A = 25°C and V_{DD} = 5V, unless otherwise indicated.

SUPPLY CURRENT vs TEMPERATURE

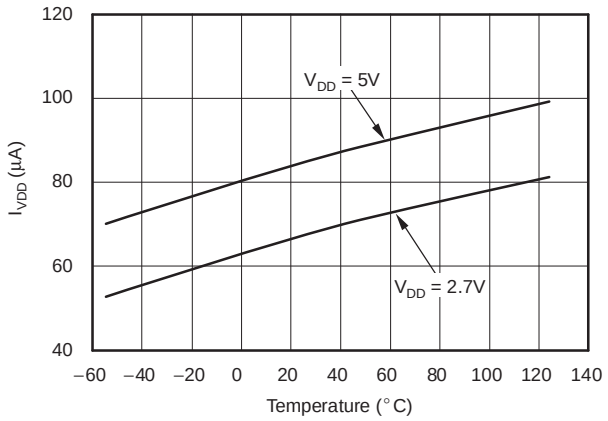


Figure 1.

SUPPLY CURRENT vs I²C BUS FREQUENCY

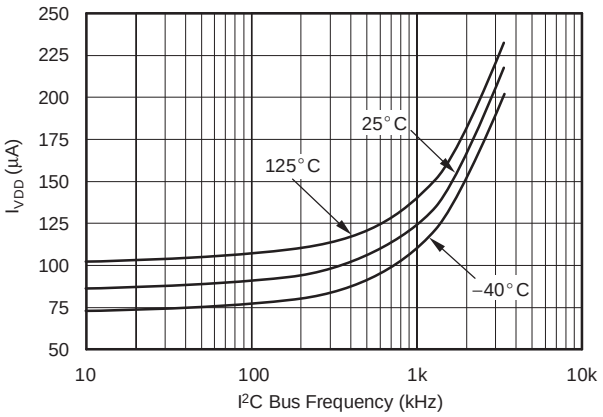


Figure 2.

OFFSET ERROR vs TEMPERATURE

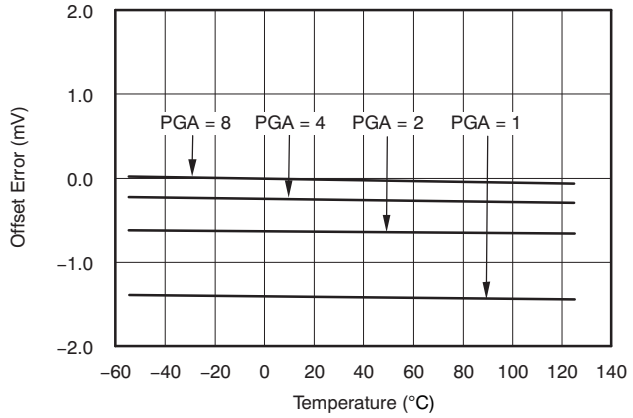


Figure 3.

GAIN ERROR vs TEMPERATURE

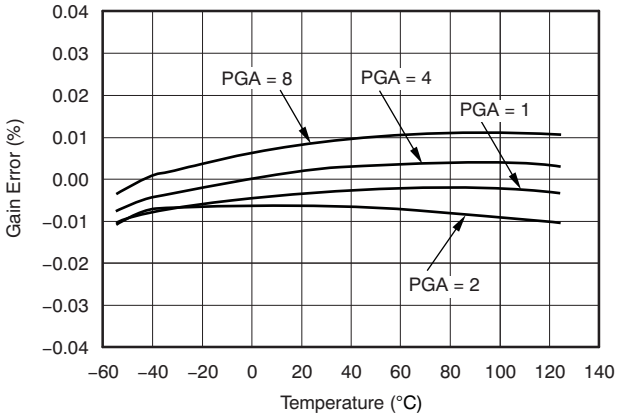


Figure 4.

DATA RATE vs TEMPERATURE

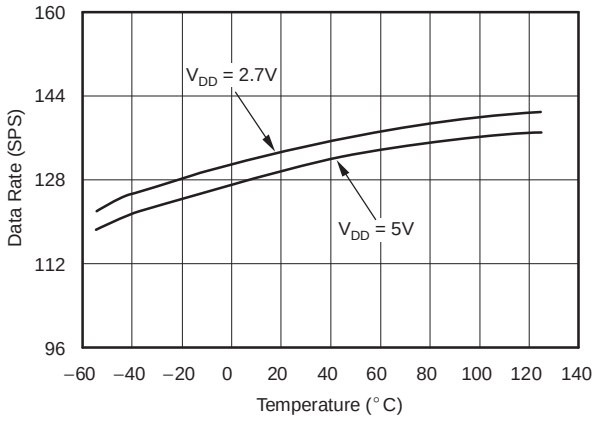


Figure 5.

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THEORY OF OPERATION

The ADS1000 is a fully differential, 12-bit A/D converter. The ADS1000 allows users to obtain precise measurements with a minimum of effort, and the device is extremely easy to design with and configure.

The ADS1000 consists of an A/D converter core with adjustable gain, a clock generator, and an I^2C interface. Each of these blocks are described in detail in the sections that follow.

ANALOG-TO-DIGITAL CONVERTER

The ADS1000 uses a switched-capacitor input stage. To external circuitry, it looks roughly like a resistance. The resistance value depends on the capacitor values and the rate at which they are switched. The switching clock is generated by the onboard clock generator, so its frequency, nominally 275kHz, is dependent on supply voltage and temperature. The capacitor values depend on the PGA setting.

The common-mode and differential input impedances are different. For a gain setting of PGA, the differential input impedance is typically 2.4MΩ/PGA.

The common-mode impedance is typically 8MΩ.

OUTPUT CODE CALCULATION

The ADS1000 outputs codes in binary two's complement format. The output code is confined to the range of numbers: –2048 to 2047, and is given by:

$$\text{Output Code} = 2048(\text{PGA})\left(\frac{V_{IN+} - V_{IN-}}{V_{DD}}\right)$$

CLOCK GENERATOR

The ADS1000 features an onboard clock generator. The Typical Characteristics show variations in data rate over supply voltage and temperature. It is not possible to operate the ADS1000 with an external clock.

USING THE ADS1000

OPERATING MODES

The ADS1000 operates in one of two modes: continuous conversion and single conversion.

In continuous conversion mode, the ADS1000 continuously performs conversions. Once a conversion has been completed, the ADS1000 places the result in the output register, and immediately begins another conversion. When the ADS1000 is in continuous conversion mode, the ST/BSY bit in the configuration register always reads '1'.

In single conversion mode, the ADS1000 waits until the ST/BSY bit in the conversion register is set to '1'. When this happens, the ADS1000 powers up and performs a single conversion. After the conversion completes, the ADS1000 places the result in the output register, resets the ST/BSY bit to '0' and powers down. Writing a '1' to ST/BSY while a conversion is in progress has no effect.

When switching from continuous conversion mode to single conversion mode, the ADS1000 will complete the current conversion, reset the ST/BSY bit to '0' and power-down the device.

RESET AND POWER-UP

When the ADS1000 powers up, it automatically performs a reset. As part of the reset, the ADS1000 sets all of the bits in the configuration register to their respective default settings.

The ADS1000 responds to the I^2C General Call Reset command. When the ADS1000 receives a General Call Reset, it performs an internal reset, exactly as though it had just been powered on.

I^2C INTERFACE

The ADS1000 communicates through an I^2C (Inter-Integrated Circuit) interface. The I^2C interface is a two-wire, open-drain interface supporting multiple devices and masters on a single bus. Devices on the I^2C bus only drive the bus lines low, by connecting them to ground; they never drive the bus lines high. Instead, the bus wires are pulled high by pull-up resistors, so the bus wires are high when no device is driving them low. This way, two devices cannot conflict; if two devices drive the bus simultaneously, there is no driver contention.

Communication on the I^2C bus always takes place between two devices, one acting as the master and the other acting as the slave. Both masters and slaves can read and write, but slaves can only do so under the direction of the master. Some I^2C devices can act as masters or slaves, but the ADS1000 can only act as a slave device.

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An I^2C bus consists of two lines, SDA and SCL. SDA carries data; SCL provides the clock. All data is transmitted across the I^2C bus in groups of eight bits. To send a bit on the I^2C bus, the SDA line is driven to the bit level while SCL is low (a Low on SDA indicates the bit is '0'; a High indicates the bit is '1'). Once the SDA line has settled, the SCL line is brought high, then low. This pulse on SCL clocks the SDA bit into the receiver shift register.

The I^2C bus is bidirectional: the SDA line is used both for transmitting and receiving data. When a master reads from a slave, the slave drives the data line; when a master sends to a slave, the master drives the data line. The master always drives the clock line. The ADS1000 never drives SCL, because it cannot act as a master. On the ADS1000, SCL is an input only.

Most of the time the bus is idle, no communication takes place, and both lines are high. When communication takes place, the bus is active. Only master devices can start a communication. They do this by causing a start condition on the bus. Normally, the data line is only allowed to change state while the clock line is low. If the data line changes state while the clock line is high, it is either a *start* condition or its counterpart, a *stop* condition. A start condition is when the clock line is high and the data line goes from high to low. A stop condition is when the clock line is high and the data line goes from low to high.

After the master issues a start condition, it sends a byte that indicates with which slave device it wants to communicate. This byte is called the *address byte*. Each device on an I^2C bus has a unique 7-bit address to which it responds. (Slaves can also have 10-bit addresses; see the I^2C specification for details.) The master sends an address in the address byte, together with a bit that indicates whether it wishes to read from or write to the slave device.

Every byte transmitted on the I^2C bus, whether it be address or data, is acknowledged with an *acknowledge* bit. When a master has finished sending a byte, eight data bits, to a slave, it stops driving SDA and waits for the slave to acknowledge the byte. The slave acknowledges the byte by pulling SDA low. The master then sends a clock pulse to clock the acknowledge bit. Similarly, when a master has finished reading a byte, it pulls SDA low to acknowledge to the slave that it has finished reading the byte. It then sends a clock pulse to clock the bit. (Remember that the master always drives the clock line.)

A *not-acknowledge* is performed by simply leaving SDA high during an acknowledge cycle. If a device is not present on the bus, and the master attempts to address it, it will receive a not-acknowledge because no device is present at that address to pull the line low.

When a master has finished communicating with a slave, it may issue a stop condition. When a stop condition is issued, the bus becomes idle again. A master may also issue another start condition. When a start condition is issued while the bus is active, it is called a *repeated start condition*.

A timing diagram for an ADS1000 I^2C transaction is shown in Figure 6. Table 1 gives the parameters for this diagram.

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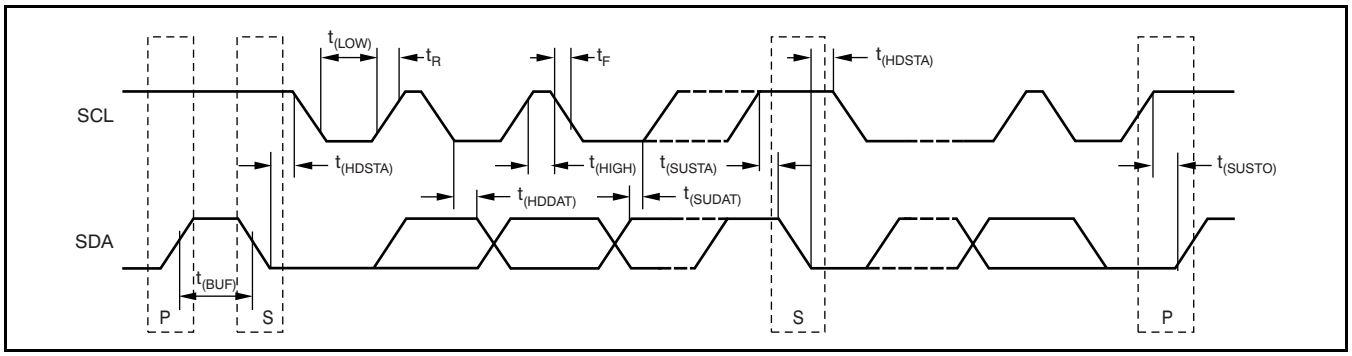


Figure 6. I²C Timing Diagram

Table 1. Timing Diagram Definitions

PARAMETER		FAST MODE		HIGH-SPEED MODE		UNITS
		MIN	MAX	MIN	MAX	
SCLK Operating Frequency	$f_{(SCLK)}$		0.4		3.4	MHz
Bus Free Time Between STOP and START Condition	$t_{(BUF)}$	600		160		ns
Hold Time After Repeated START Condition. After this period, the first clock is generated.	$t_{(HDSTA)}$	600		160		ns
Repeated START Condition Setup Time	$t_{(SUSTA)}$	600		160		ns
STOP Condition Setup Time	$t_{(SUSTO)}$	600		160		ns
Data Hold Time	$t_{(HDDAT)}$	0		0		ns
Data Setup Time	$t_{(SUDAT)}$	100		10		ns
SCLK Clock Low Period	$t_{(LOW)}$	1300		160		ns
SCLK Clock High Period	$t_{(HIGH)}$	600		60		ns
Clock/Data Fall Time	t_F		300		160	ns
Clock/Data Rise Time	t_R		300		160	ns

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ADS1000 I²C ADDRESSES

The ADS1000 I²C address is either 1001000 or 1001001, set at the factory. The address is identified with an A0 or an A1 within the orderable name.

The two different I²C variants are also marked differently. Devices with an I²C address of 1001000 have packages marked **BD0**, while devices with an I²C address of 1001001 are marked with **BD1**. See the Package/Ordering Information Table for a complete listing of the ADS1000 I²C addresses and tape and reel size.

I²C GENERAL CALL

The ADS1000 responds to General Call Reset, which is an address byte of 00h followed by a data byte of 06h. The ADS1000 acknowledges both bytes.

On receiving a General Call Reset, the ADS1000 performs a full internal reset, just as though it had been powered off and then on. If a conversion is in process, it is interrupted; the output register is set to zero, and the configuration register returns to its default setting.

The ADS1000 always acknowledges the General Call address byte of 00h, but it does not acknowledge any General Call data bytes other than 04h or 06h.

I²C DATA RATES

The I²C bus operates in one of three speed modes: *Standard*, which allows a clock frequency of up to 100kHz; *Fast*, which allows a clock frequency of up to 400kHz; and *High-speed* mode (also called Hs mode), which allows a clock frequency of up to 3.4MHz. The ADS1000 is fully compatible with all three modes.

No special action needs to be taken to use the ADS1000 in Standard or Fast modes, but High-speed mode must be activated. To activate High-speed mode, send a special address byte of 00001XXX following the start condition, where the ***XXX*** bits are unique to the Hs-capable master. This byte is called the *Hs master code*. (Note that this is different from normal address bytes; the low bit does not indicate read/write status.) The ADS1000 will not acknowledge this byte; the I²C specification prohibits acknowledgment of the Hs master code. On receiving a master code, the ADS1000 will switch on its High-speed mode filters, and will communicate at up to 3.4MHz. The ADS1000 switches out of Hs mode with the next stop condition.

For more information on High-speed mode, consult the I²C specification.

REGISTERS

The ADS1000 has two registers that are accessible via its I²C port. The output register contains the result of the last conversion; the configuration register allows users to change the ADS1000 operating mode and query the status of the device.

OUTPUT REGISTER

The 16-bit output register contains the result of the last conversion in binary two's complement format. Since the port yields 12 bits of data, the ADS1000 outputs right-justified and sign-extended codes. This output format makes it possible to perform averaging using a 16-bit accumulator.

Following reset or power-up, the output register is cleared to '0'; it remains zero until the first conversion is completed. Therefore, if a user reads the ADS1000 just after reset or power-up, the output register will read '0'.

The output register format is shown in Table 2.

Table 2. OUTPUT REGISTER

BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NAME	D15(1)	D14(1)	D13(1)	D12(1)	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

(1) D15–D12 are sign extensions of 12-bit data.

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CONFIGURATION REGISTER

A user controls the ADS1000 operating mode and PGA settings via the 8-bit configuration register. The configuration register format is shown in Table 3. The default setting is 80H.

Table 3. CONFIGURATION REGISTER

7	6	5	4	3	2	1	0
ST/BSY	0	0	SC	0	0	PGA1	PGA0

Bit 7: ST/BSY

The meaning of the ST/BSY bit depends on whether it is being written to or read from.

In single conversion mode, writing a '1' to the ST/BSY bit causes a conversion to start, and writing a '0' has no effect. In continuous conversion mode, the ADS1000 ignores the value written to ST/BSY.

When read in single conversion mode, ST/BSY indicates whether the A/D converter is busy taking a conversion. If ST/BSY is read as '1', the A/D converter is busy, and a conversion is taking place; if '0', no conversion is taking place, and the result of the last conversion is available in the output register.

In continuous mode, ST/BSY is always read as '1'.

Bits 6 - 5: Reserved

Bits 6 and 5 must be set to zero.

Bit 4: SC

SC controls whether the ADS1000 is in continuous conversion or single conversion mode. When SC is '1', the ADS1000 is in single conversion mode; when SC is '0', the ADS1000 is in continuous conversion mode. The default setting is '0'.

Bits 3 - 2: Reserved

Bits 3 and 2 must be set to zero.

Bits 1 - 0: PGA

Bits 1 and 0 control the ADS1000 gain setting; see Table 4.

Table 4. PGA Bits

PGA1	PGA0	GAIN
0(1)	0(1)	1(1)
0	1	2
1	0	4
1	1	8
(1) Default setting.		

READING FROM THE ADS1000

A user can read the output register and the contents of the configuration register from the ADS1000. To do this, address the ADS1000 for reading, and read three bytes from the device. The first two bytes are the output register contents; the third byte is the configuration register contents.

A user does not always have to read three bytes from the ADS1000. If only the contents of the output register are needed, read only two bytes.

Reading more than three bytes from the ADS1000 has no effect. All of the bytes beginning with the fourth byte will be FFh. See Figure 7 for a timing diagram of an ADS1000 read operation.

WRITING TO THE ADS1000

A user can write new contents into the configuration register (the contents of the output register cannot change). To do this, address the ADS1000 for writing, and write one byte to it. This byte is written into the configuration register.

Writing more than one byte to the ADS1000 has no effect. The ADS1000 ignores any bytes sent to it after the first one, and will only acknowledge the first byte. See Figure 8 for a timing diagram of an ADS1000 write operation.

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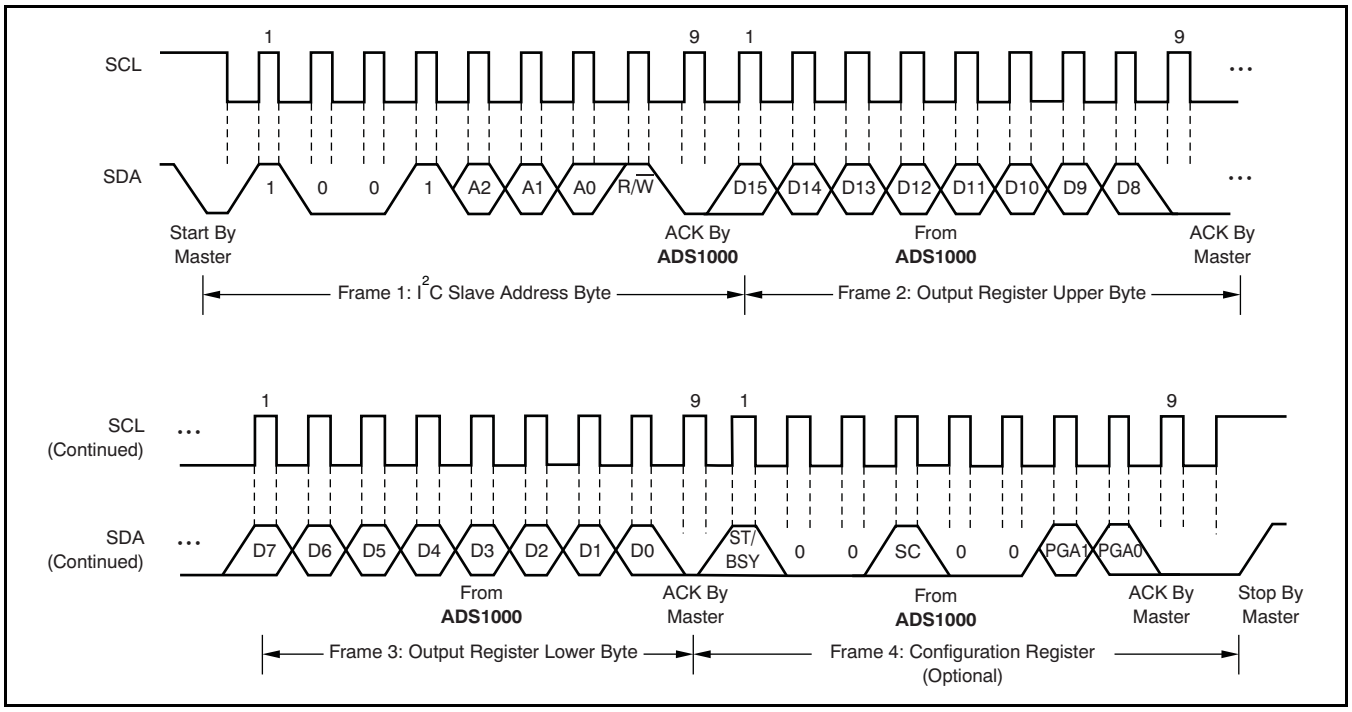


Figure 7. Timing Diagram for Reading from the ADS1000

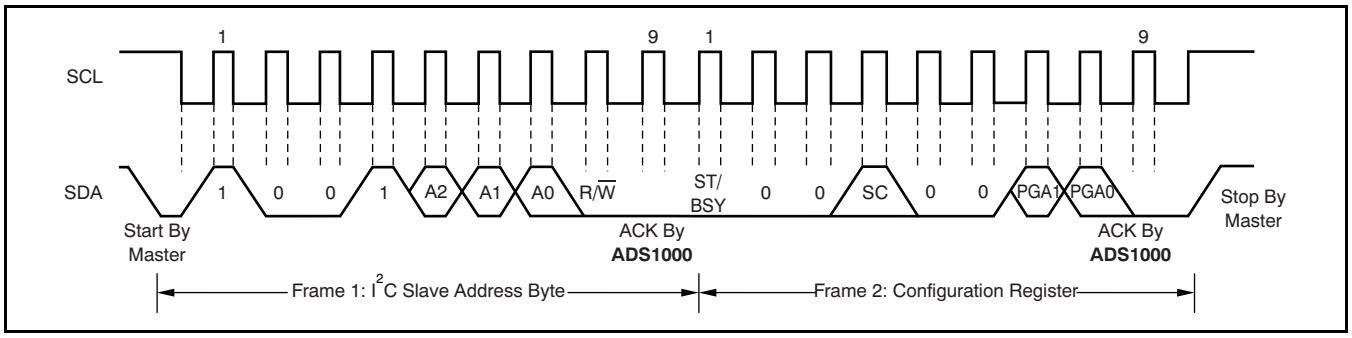


Figure 8. Timing Diagram for Writing to the ADS1000

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APPLICATION INFORMATION

BASIC CONNECTIONS

For many applications, connecting the ADS1000 is extremely simple. A basic connection diagram for the ADS1000 is shown in Figure 9.

The fully differential voltage input of the ADS1000 is ideal for connection to differential sources with moderately low source impedance, such as bridge sensors and thermistors. Although the ADS1000 can read bipolar differential signals, it cannot accept negative voltages on either input. It may be helpful to think of the ADS1000 positive voltage input as noninverting, and of the negative input as inverting.

When the ADS1000 is converting, it draws current in short spikes. The 0.1µF bypass capacitor supplies the momentary bursts of extra current needed from the supply.

The ADS1000 interfaces directly to standard mode, fast mode, and high-speed mode I^2C controllers. Any microcontroller I^2C peripheral, including master-only and non-multiple-master I^2C peripherals, will work with the ADS1000. The ADS1000 does not perform clock-stretching (that is, it never pulls the clock line low), so it is not necessary to provide for this unless other devices are on the same I^2C bus.

Pull-up resistors are necessary on both the SDA and SCL lines because I^2C bus drivers are open-drain. The size of these resistors depends on the bus operating speed and capacitance of the bus lines. Higher-value resistors consume less power, but increase the transition times on the bus, limiting the bus speed. Lower-value resistors allow higher speed at the expense of higher power consumption. Long bus lines have higher capacitance and require smaller pullup resistors to compensate. The resistors should not be too small; if they are, the bus drivers may not be able to pull the bus lines low.

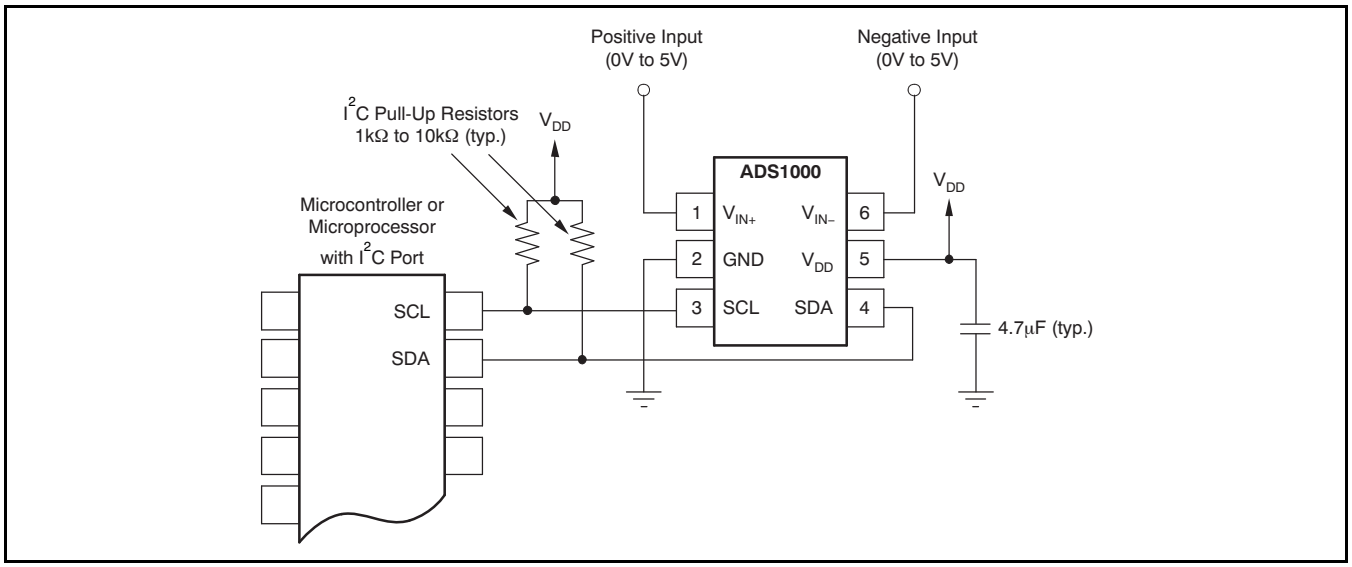


Figure 9. Typical Connections of the ADS1000

CONNECTING MULTIPLE DEVICES

Connecting two ADS1000s to a single bus is almost trivial. An example showing two ADS1000s and one ADS1100 connected on a single bus is shown in Figure 10. Multiple devices can be connected to a single bus (provided that their addresses are different).

Note that only one set of pull-up resistors is needed per bus. A user might find that he or she needs to lower the pull-up resistor values slightly to compensate for the additional bus capacitance presented by multiple devices and increased line length.

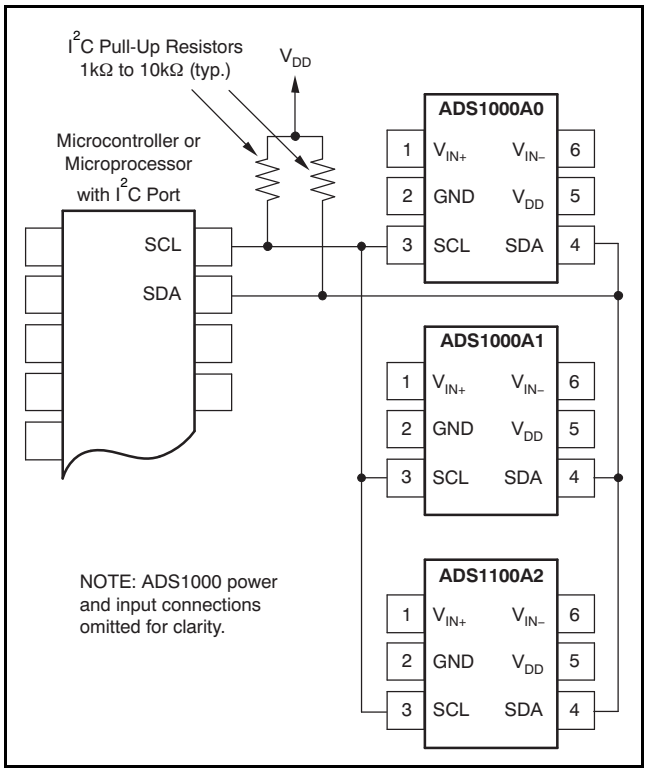


Figure 10. Connecting Multiple ADS1000s

USING GPIO PORTS FOR I²C

Most microcontrollers have programmable input/output pins that can be set in software to act as inputs or outputs. If an I²C controller is not available, the ADS1000 can be connected to GPIO pins, and the I²C bus protocol simulated, or bit-banged, in software. An example of this for a single ADS1000 is shown in Figure 11.

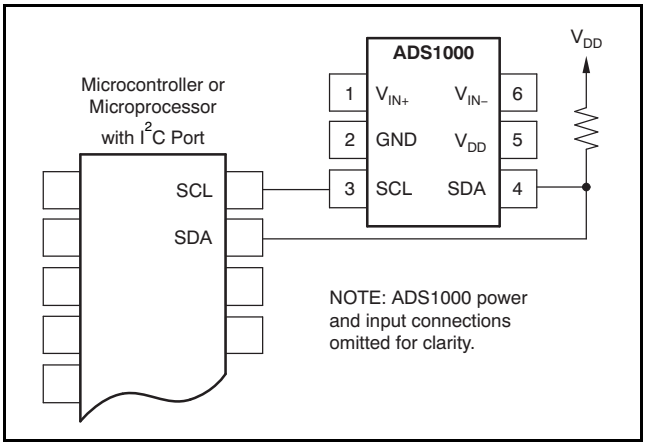


Figure 11. Using GPIO with a Single ADS1000

Bit-banging I²C with GPIO pins can be done by setting the GPIO line to zero and toggling it between input and output modes to apply the proper bus states. To drive the line low, the pin is set to output a '0'; to let the line go high, the pin is set to input. When the pin is set to input, the state of the pin can be read; if another device is pulling the line low, this device will read as a '0' in the port input register.

Note that no pull-up resistor is shown on the SCL line. In this simple case, the resistor is not needed; the microcontroller can simply leave the line on output, and set it to '1' or '0' as appropriate. It can do this because the ADS1000 never drives its clock line low. This technique can also be used with multiple devices, and has the advantage of lower current consumption resulting from the absence of a resistive pull-up.

If there are any devices on the bus that may drive their clock lines low, the above method should not be used; the SCL line should be high-Z or zero and a pull-up resistor provided as usual. Note also that this cannot be done on the SDA line in any case, because the ADS1000 does drive the SDA line low from time to time, as all I²C devices do.

Some microcontrollers have selectable strong pull-up circuits built into the GPIO ports. In some cases, these can be switched on and used in place of an external pull-up resistor. Weak pull-ups are also provided on some microcontrollers, but usually these are too weak for I²C communication. If there is any doubt about the matter, test the circuit before committing it to production.

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SINGLE-ENDED INPUTS

Although the ADS1000 has a fully differential input, it can easily measure single-ended signals. A simple single-ended connection scheme is shown in Figure 12. The ADS1000 is configured for single-ended measurement by grounding either of its input pins, usually V_{IN-}, and applying the input signal to V_{IN+}. The single-ended signal can range from –0.2V to V_{DD} + 0.3V. The ADS1000 loses no linearity anywhere in its input range. Negative voltages cannot be applied to this circuit because the ADS1000 inputs can only accept positive voltages.

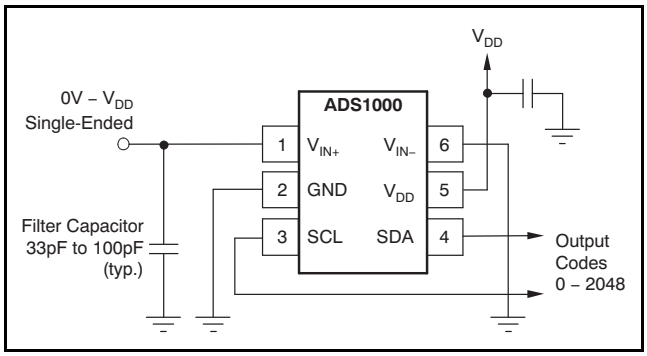


Figure 12. Measuring Single-Ended Inputs

The ADS1000 input range is bipolar differential with respect to the reference, that is, V_{DD}. The single-ended circuit shown in Figure 12 covers only half the ADS1000 input scale because it does not produce differentially negative inputs; therefore, one bit of resolution is lost. The DRV134 balanced line driver can be employed to regain this bit for single-ended signals.

Negative input voltages must be level-shifted. A good candidate for this function is the THS4130 differential amplifier, which can output fully differential signals. This device can also help recover the lost bit noted previously for single-ended positive signals. Level-shifting can also be performed using the DRV134.

LOW-SIDE CURRENT MONITOR

Figure 13 shows a circuit for a low-side shunt-type current monitor. The circuit reads the voltage across a shunt resistor, which is sized as small as possible while still giving a readable output voltage. This voltage is amplified by an OPA335 low-drift op-amp, and the result is read by the ADS1000.

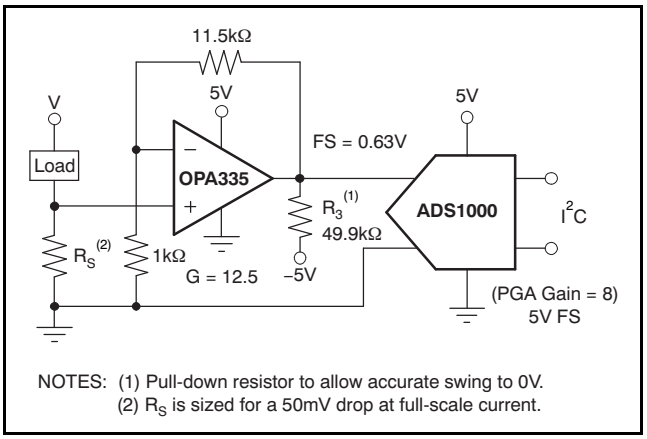


Figure 13. Low-Side Current Measurement

It is recommended that the ADS1000 be operated at a gain of 8. The gain of the OPA335 can then be set lower. For a gain of 8, the op amp should be configured to give a maximum output voltage of no greater than 0.75V. If the shunt resistor is sized to provide a maximum voltage drop of 50mV at full-scale current, the full-scale input to the ADS1000 is 0.63V.

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ADDITIONAL RECOMMENDATIONS

The ADS1000 is fabricated in a small-geometry low-voltage process. The analog inputs feature protection diodes to the supply rails. However, the current-handling ability of these diodes is limited, and the ADS1000 can be permanently damaged by analog input voltages that remain more than approximately 300mV beyond the rails for extended periods. One way to protect against overvoltage is to place current-limiting resistors on the input lines. The ADS1000 analog inputs can withstand momentary currents of as large as 10mA.

The previous paragraph does not apply to the I^2C ports, which can both be driven to 6V regardless of the supply.

If the ADS1000 is driven by an op amp with high voltage supplies, such as ±12V, protection should be provided, even if the op amp is configured so that it will not output out-of-range voltages. Many op amps seek to one of the supply rails immediately when power is applied, usually before the input has stabilized; this momentary spike can damage the ADS1000. Sometimes this damage is incremental and results in slow, long-term failure—which can be distastrous for permanently installed, low-maintenance systems.

If using an op amp or other front-end circuitry with the ADS1000, be sure to take the performance characteristics of this circuitry into account; a chain is only as strong as its weakest link.

Any data converter is only as good as its reference. For the ADS1000, the reference is the power supply, and the power supply must be clean enough to achieve the desired performance. If a power-supply filter capacitor is used, it should be placed close to the V_{DD} pin, with no vias placed between the capacitor and the pin. The trace leading to the pin should be as wide as possible, even if it must be necked down at the device.

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Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (September 2006) to Revision A	Page
• Changed logic level min value from (0.7GND) to (0.7VDD)	3

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS1000A0IDBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	BD0	Samples
ADS1000A0IDBVRG4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	BD0	Samples
ADS1000A0IDBVT	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	BD0	Samples
ADS1000A0IDBVTG4	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	BD0	Samples
ADS1000A1IDBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	BD1	Samples
ADS1000A1IDBVT	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	BD1	Samples
ADS1000A1IDBVTG4	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	BD1	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF ADS1000 :

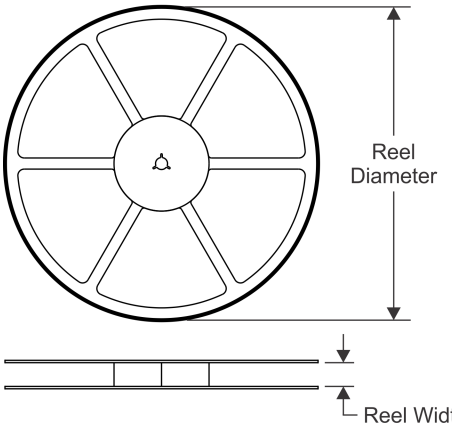
- Automotive: ADS1000-Q1

NOTE: Qualified Version Definitions:

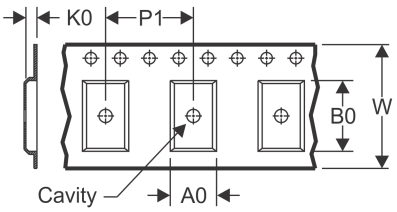
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

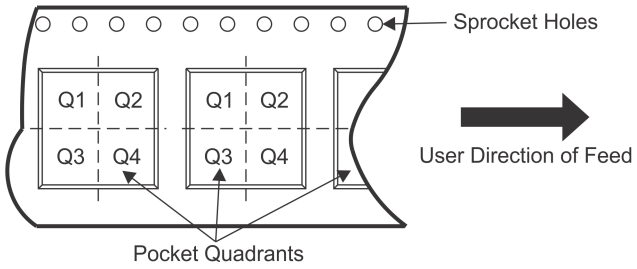


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

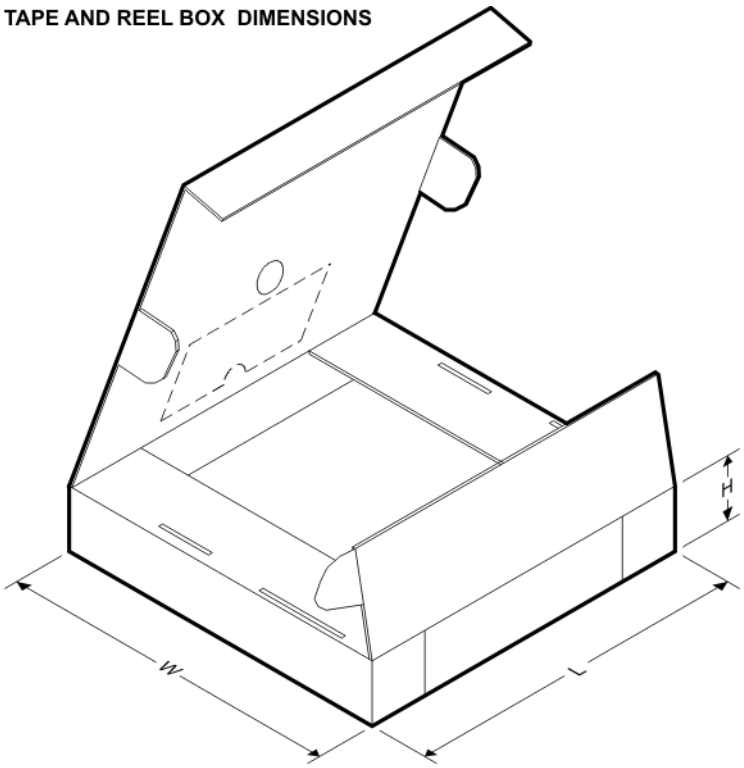
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS1000A0IDBVR	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
ADS1000A0IDBVT	SOT-23	DBV	6	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
ADS1000A1IDBVR	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
ADS1000A1IDBVT	SOT-23	DBV	6	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

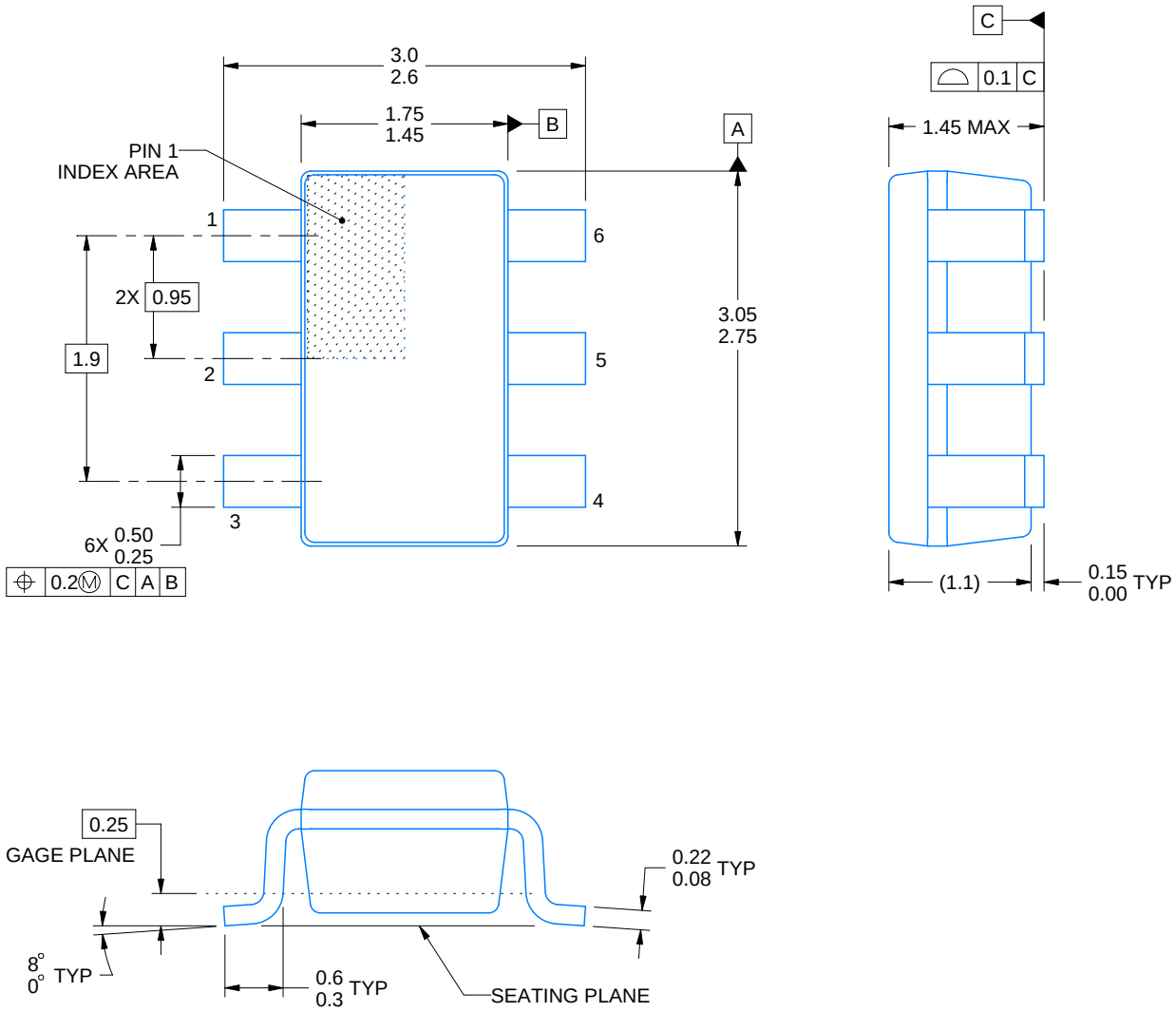
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS1000A0IDBVR	SOT-23	DBV	6	3000	180.0	180.0	18.0
ADS1000A0IDBVT	SOT-23	DBV	6	250	180.0	180.0	18.0
ADS1000A1IDBVR	SOT-23	DBV	6	3000	180.0	180.0	18.0
ADS1000A1IDBVT	SOT-23	DBV	6	250	180.0	180.0	18.0

PACKAGE OUTLINE

DBV0006A

SOT-23 - 1.45 mm max height

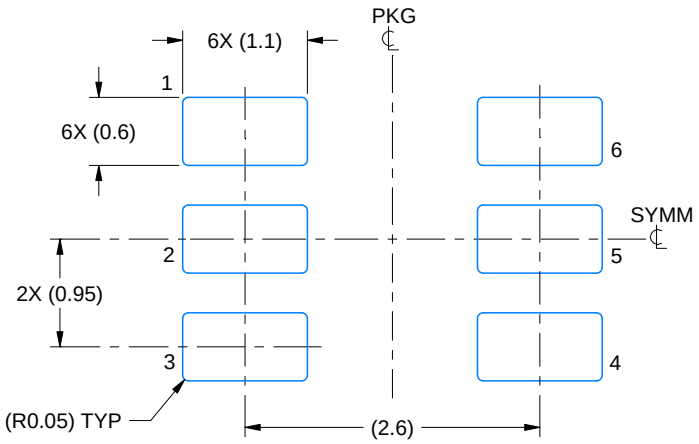
SMALL OUTLINE TRANSISTOR



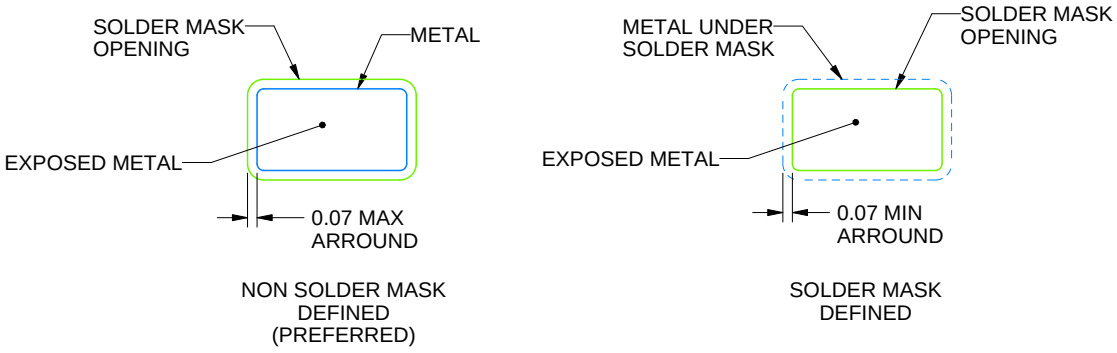
4214840/B 03/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

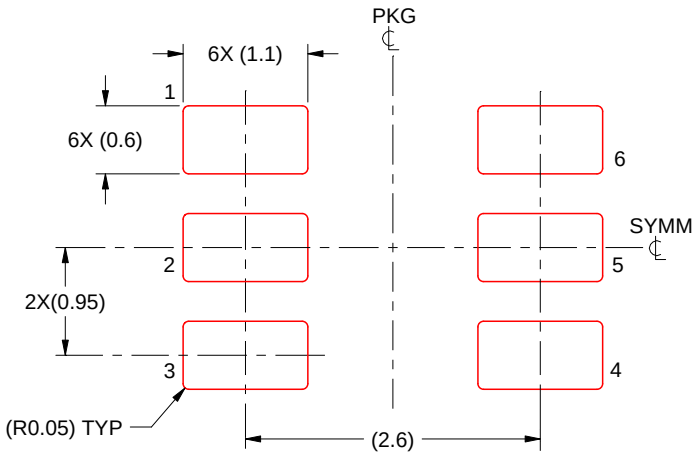


SOLDER MASK DETAILS

4214840/B 03/2018

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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