

TPS7B82-Q1 300-mA High-Voltage Ultralow- I_Q Low-Dropout Regulator

1 Features

- AEC-Q100 qualified for automotive applications:
 - Temperature grade 1: $-40^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$
- Extended junction temperature range: $-40^{\circ}\text{C} \leq T_J \leq 150^{\circ}\text{C}$
- Low quiescent current I_Q :
 - 300-nA shutdown I_Q
 - 2.7 μA typical at light loads
 - 5 μA maximum at light loads
- 3-V to 40-V wide V_{IN} input voltage range with up to 45-V transient
- Maximum output current: 300 mA
- 2% output-voltage accuracy
- Maximum dropout voltage: 700 mV at 200-mA load current for fixed 5-V output version
- Stable with low-ESR (0.001- Ω to 5- Ω) ceramic output-stability capacitor (1 μF to 200 μF)
- Fixed 2.5-V, 3.3-V, and 5-V output voltage
- Thermal resistance ($R_{\theta JA}$): 63.9 $^{\circ}\text{C/W}$
- Packages:
 - 8-pin HVSSOP, $R_{\theta JA} = 63.9^{\circ}\text{C/W}$
 - 6-pin WSON, $R_{\theta JA} = 72.8^{\circ}\text{C/W}$
 - 5-pin TO-252, $R_{\theta JA} = 38.8^{\circ}\text{C/W}$

2 Applications

- [Automotive head units](#)
- [Telematics control units](#)
- [Headlights](#)
- [Body control modules](#)
- [Inverter and motor controls](#)

3 Description

In automotive battery-connected applications, low quiescent current (I_Q) is important to save power and extend battery lifetime. It is especially necessary to have ultralow I_Q for always-on systems.

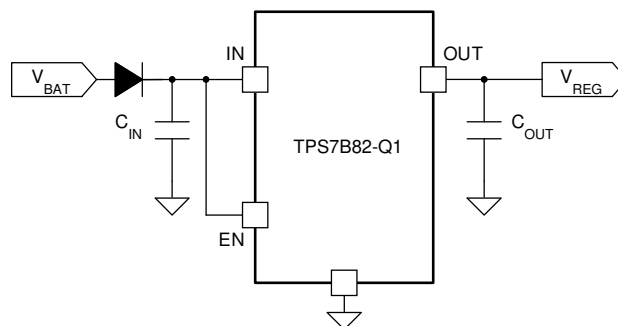
The TPS7B82-Q1 is a low-dropout linear regulator designed to operate with a wide input-voltage range from 3 V to 40 V (45-V load dump protection). Operation down to 3 V allows the TPS7B82-Q1 to continue operating during cold-crank and start and stop conditions. With only 2.7- μA typical quiescent current at light load, this device is an optimal solution for powering microcontrollers (MCUs) and CAN/LIN transceivers in standby systems.

The device features integrated short-circuit and overcurrent protection. This device operates in ambient temperatures from -40°C to 125°C and with junction temperatures from -40°C to 150°C . Additionally, this device uses a thermally conductive package to enable sustained operation despite significant dissipation across the device. Because of these features, the device is well suited as a power supply for various automotive applications.

Device Information

PART NUMBER (1)	PACKAGE	BODY SIZE (NOM)
TPS7B82-Q1	HVSSOP (8)	3.00 mm $\times$ 3.00 mm
	WSON (6)	2.00 mm $\times$ 2.00 mm
	TO-252 (5)	6.10 mm $\times$ 6.60 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Typical Application Schematic



Table of Contents

1 Features	1	7.4 Device Functional Modes.....	12
2 Applications	1	8 Application and Implementation	13
3 Description	1	8.1 Application Information.....	13
4 Revision History	2	8.2 Typical Application.....	13
5 Pin Configuration and Functions	4	9 Power Supply Recommendations	15
Pin Functions.....	4	10 Layout	15
6 Specifications	5	10.1 Layout Guidelines.....	15
6.1 Absolute Maximum Ratings.....	5	10.2 Layout Example.....	15
6.2 ESD Ratings.....	5	11 Device and Documentation Support	16
6.3 Recommended Operating Conditions.....	5	11.1 Receiving Notification of Documentation Updates..	16
6.4 Thermal Information.....	6	11.2 Support Resources.....	16
6.5 Electrical Characteristics.....	6	11.3 Trademarks.....	16
6.6 Typical Characteristics.....	8	11.4 Electrostatic Discharge Caution.....	16
7 Detailed Description	11	11.5 Glossary.....	16
7.1 Overview.....	11	12 Mechanical, Packaging, and Orderable Information	16
7.2 Functional Block Diagram.....	11		
7.3 Feature Description.....	11		

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from April 30, 2020 to June 30, 2020 (from Revision F (April 2020) to Revision G (July 2020))

	Page
• Changed numbering format for tables, figures, and cross-references throughout the document.....	1
• Added 2.5-V option to fixed output voltage <i>Features</i> bullet.....	1
• Added footnote to <i>Dropout voltage</i> parameter in <i>Electrical Characteristics</i> table.....	6

Changes from Revision E (June 2019) to Revision F (April 2020)

	Page
• Changed <i>Applications</i> section	1
• Changed automotive-specific <i>Features</i> bullets	1
• Changed KVV package from preview to production data.....	1
• Added ESD classification levels to <i>ESD Ratings</i> table	5

Changes from Revision D (October 2018) to Revision E (June 2019)

	Page
• Added KVV package to document as Preview device.....	1
• Changed DRV status from Preview to Production Data	1
• Added TO-252 sub-bullet and added $R_{\theta JA}$ values for HVSSOP and WSON sub-bullets in <i>Packages</i> bullet.....	1
• Added KVV to <i>Pin Configuration and Functions</i> section.....	4
• Changed <i>Electrical Characteristics</i> table.....	6
• Added second column in <i>Test Conditions</i> to call out device package differences	6

Changes from Revision C (February 2018) to Revision D (October 2018)

	Page
• Added DRV package to document	1
• Changed -40°C to 125°C to $-40^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$ in first <i>AEC-Q100 Qualified</i> sub-bullet in <i>Features</i> section .	1
• Changed <i>Extended Junction Temperature Range</i> bullet of <i>Features</i> section.....	1
• Changed first <i>Low Quiescent Current</i> I_Q sub-bullet in <i>Features</i> section.....	1
• Deleted <i>Integrated Fault Protection</i> bullet from <i>Features</i> section.....	1
• Added WSON to <i>Packages</i> bullet in <i>Features</i> section.....	1

• Changed MSOP to HVSSOP throughout document	1
• Changed first bullet in <i>Applications</i> section	1
• Added <i>Telematics Control Unit</i> bullet to <i>Applications</i> section	1
• Changed second paragraph of <i>Description</i> section.....	1
• Added DRV package to <i>Pin Configuration and Functions</i> section.....	4
• Changed maximum specification of second $I_{(Q)}$ parameter row from 5 μA to 6.5 μA	6
• Added first row and last three rows to $V_{(Dropout)}$ parameter	6
• Changed <i>Input Capacitor</i> section	13

Changes from Revision B (February 2018) to Revision C (February 2018)	Page
--	-------------

• Added <i>Feature</i> : Device Junction Temperature Range: $-40^{\circ}C$ to $150^{\circ}C$	1
• Changed <i>Feature</i> From: Fixed 5-V Output Voltage To: Fixed 5-V and 3.3-V Output Voltage.....	1
• Added <i>Feature</i> : "Thermal Resistance ($R_{\theta JA}$): $63.9^{\circ}C/W$ ".....	1
• Added "Powering MCUs and CAN/LIN Transceivers" to the <i>Applications</i> list.....	1
• Changed the <i>Description</i> section.....	1
• Changed the <i>Device Information</i> table.....	1
• Added PowerPAD to the DGN package description	4
• Changed pins 5 and 6 From: NC To: GND in the <i>Pin Configuration and Functions</i>	4
• Deleted Note 3 from V_{OUT} in the <i>Absolute Maximum Ratings</i>	5
• Changed the VALUE column for Output voltage From: 5 V To: 5 V or 3.3 V in Table 8-1	13

Changes from Revision A (November 2017) to Revision B (February 2018)	Page
--	-------------

• Deleted values from capacitors C_{IN} and C_{OUT} in the <i>Typical Application Schematic</i>	1
• Deleted values from capacitors C_{IN} and C_{OUT} in Figure 8-1	13

Changes from Revision * (September 2017) to Revision A (November 2017)	Page
---	-------------

• Deleted 2.5-V and 3.3-V device options from the <i>Features</i> list.....	1
• Changed V_{EN} to Enable input in the <i>Absolute Maximum Ratings</i>	5
• Deleted the blank NOM column from the <i>Recommended Operating Conditions</i> table.....	5
• Deleted requirements for 3.3-V and 2.5-V device versions from the <i>Electrical Characteristics</i> table.....	6
• Changed conditions for Figure 6-9	8
• Deleted 3.3-V and 2.5- output voltages from the <i>Design Requirements</i> table	13

5 Pin Configuration and Functions

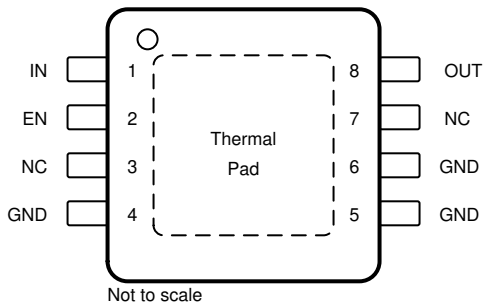


Figure 5-1. DGN Package, 8-Pin HVSSOP PowerPAD™, Top View

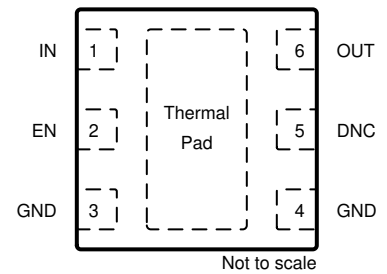


Figure 5-2. DRV Package, 6-Pin WSON PowerPAD™, Top View

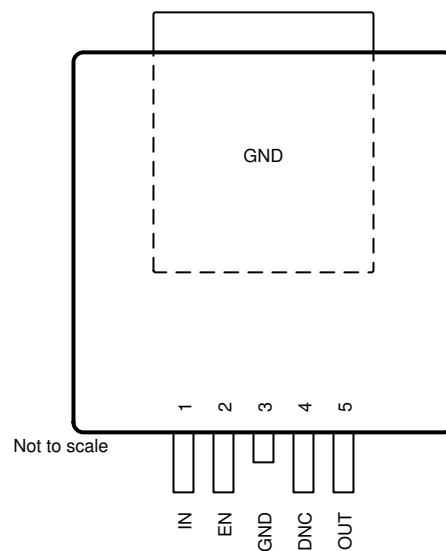


Figure 5-3. KVV Package, 5-Pin TO-252, Top View

NC – No internal connection

Pin Functions

PIN				I/O	DESCRIPTION
NAME	NO.				
	DGN	DRV	KVU		
DNC	—	5	4	—	Do not connect to a biased voltage. Tie this pin to ground or leave floating.
EN	2	2	2	I	Enable input pin
GND	4, 5, 6	3,4	3, TAB	—	Ground reference
IN	1	1	1	I	Input power-supply pin
NC	3, 7	—	—	—	Not internally connected
OUT	8	6	5	O	Regulated output voltage pin
Thermal pad				—	Connect the thermal pad to a large-area GND plane for improved thermal performance.

6 Specifications

6.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)^{(1) (2)}

		MIN	MAX	UNIT
V _{IN}	Unregulated input ⁽³⁾	−0.3	45	V
V _{EN}	Enable input ⁽³⁾	−0.3	V _{IN}	V
V _{OUT}	Regulated output	−0.3	7	V
T _J	Junction temperature range	−40	150	°C
T _{stg}	Storage temperature range	−40	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to GND.
- (3) Absolute maximum voltage, withstand 45 V for 200 ms.

6.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 ⁽¹⁾ HBM ESD classification level H2	±2000	V
		Charged-device model (CDM), per AEC Q100-011 CDM ESD classification level C3B	±750	
		Other pins	±500	

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V _{IN}	Unregulated input voltage	3	40	V
V _{EN}	Enable input voltage	0	V _{IN}	V
C _{OUT}	Output capacitor requirements ⁽¹⁾	1	200	μF
ESR	Output capacitor ESR requirements ⁽²⁾	0.001	5	Ω
T _A	Ambient temperature range	−40	125	°C
T _J	Junction temperature range	−40	150	°C

- (1) The output capacitance range specified in the table is the effective value.
- (2) Relevant ESR value at f = 10 kHz.

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TPS7B82-Q1			UNIT
		DGN (HVSSOP)	DRV (WSON)	KVU (TO-252)	
		8 PINS	6 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	63.9	72.8	31.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	50.2	85.8	39.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	22.6	37.4	9.9	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.8	2.7	4.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	22.3	37.3	9.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	12.1	13.8	2.8	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics application report](#).

6.5 Electrical Characteristics

$V_{IN} = 14\text{V}$, 10- μF ceramic output capacitor, $T_J = -40^\circ\text{C}$ to 150°C , over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE AND CURRENT (IN)							
V _{IN}	Input voltage			V _{OUT(NOM)} + V _(Dropout)	40		V
I _(SD)	Shutdown current	EN = 0 V		0.3	1		μA
I _(Q)	Quiescent current	V _{IN} = 6 V to 40 V, EN ≥ 2 V, I _{OUT} = 0 mA	DRV and KVU packages	1.9	3.5		μA
			DGN package	1.9	5		
		V _{IN} = 6 V to 40 V, EN ≥ 2 V, I _{OUT} = 0.2 mA	DRV and KVU packages	2.7	4.5		
			DGN package	2.7	6.5		
V _(IN, UVLO)	V _{IN} undervoltage detection	Ramp V _{IN} down until the output turns OFF			2.7		V
		Hysteresis			200		mV
ENABLE INPUT (EN)							
V _{IL}	Logic-input low level			0.7			V
V _{IH}	Logic-input high level			2			V
REGULATED OUTPUT (OUT)							
V _{OUT}	Regulated output	V _{IN} = V _{OUT} + V _(Dropout) to 40 V, I _{OUT} = 1 mA to 300 mA	DRV and KVU packages	−1.5%	1.5%		
			DGN package	−2%	2%		
V _(Line-Reg)	Line regulation	V _{IN} = 6 V to 40 V, I _{OUT} = 10 mA			10		mV
V _(Load-Reg)	Load regulation	V _{IN} = 14 V, I _{OUT} = 1 mA to 300 mA	DRV and KVU packages		10		mV
			DGN package		20		

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
V _(Dropout)	Dropout voltage ⁽¹⁾	V _{OUT(NOM)} = 5 V	I _{OUT} = 300 mA	DRV and KVVU packages		630	1170	mV
				DGN package			1000	
			I _{OUT} = 200 mA	DRV and KVVU packages		420	780	
				DGN package		400	700	
			I _{OUT} = 100 mA	DRV and KVVU packages		210	390	
				DGN package		200	350	
		V _{OUT} = 3.3 V	I _{OUT} = 300 mA	DRV and KVVU packages		730	1350	
				DGN package			1250	
			I _{OUT} = 200 mA	DRV and KVVU packages		475	900	
				DGN package			850	
			I _{OUT} = 100 mA					
I _{OUT}	Output current	V _{OUT} in regulation			0		300	mA
I _(CL)	Output current limit	V _{OUT} short to 90% × V _{OUT}			310	510	690	mA
PSRR	Power-supply ripple rejection	V _(Ripple) = 0.5 V _{PP} , I _{OUT} = 10 mA, frequency = 100 Hz, C _{OUT} = 2.2 μF				60		dB
OPERATING TEMPERATURE RANGE								
T _(SD)	Junction shutdown temperature					175		°C
T _(HYST)	Hysteresis of thermal shutdown					20		°C

(1) Dropout is not valid for the 2.5 V output because of the minimum input voltage limits.

6.6 Typical Characteristics

$V_{IN} = 14\text{ V}$, $V_{EN} \geq 2\text{ V}$, $T_J = -40^\circ\text{C}$ to 150°C (unless otherwise noted)

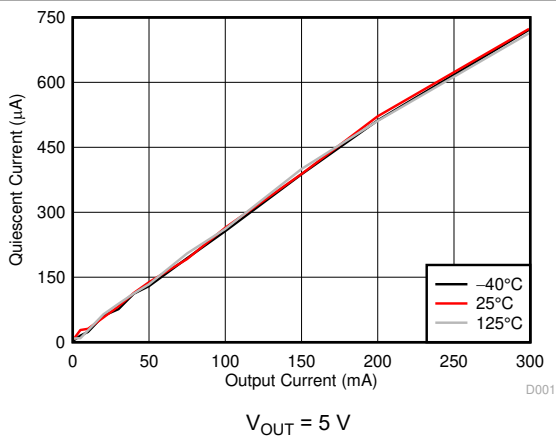


Figure 6-1. Quiescent Current vs Output Current

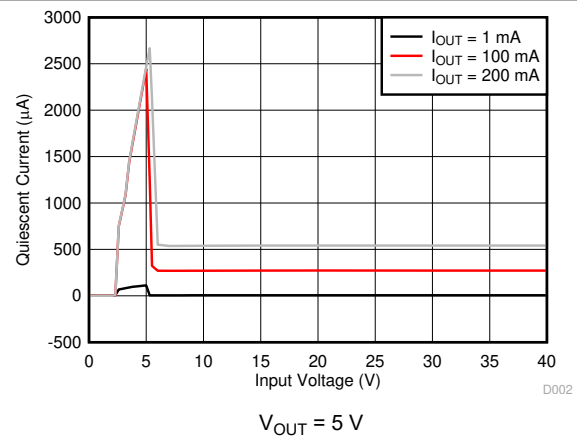


Figure 6-2. Quiescent Current vs Input Voltage

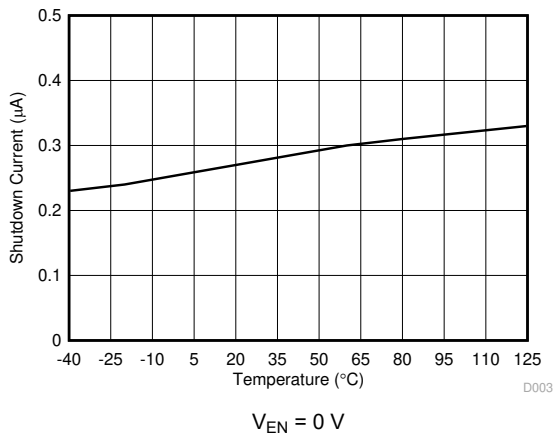


Figure 6-3. Shutdown Current vs Ambient Temperature

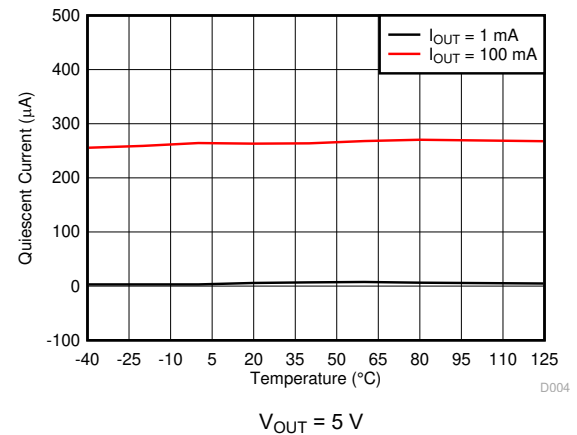


Figure 6-4. Quiescent Current vs Ambient Temperature

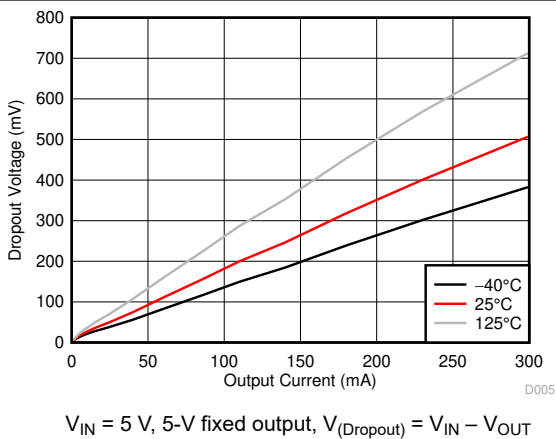


Figure 6-5. Dropout Voltage vs Output Current

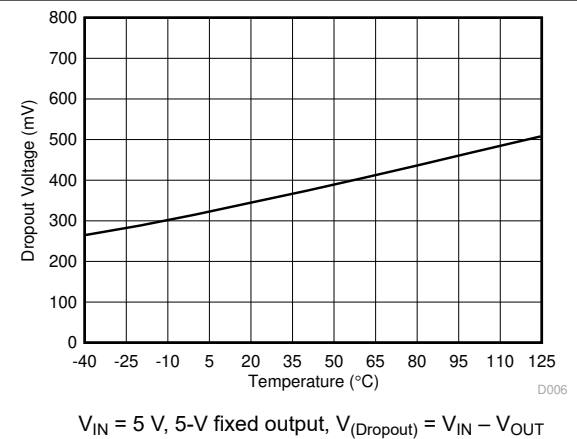


Figure 6-6. Dropout Voltage vs Ambient Temperature

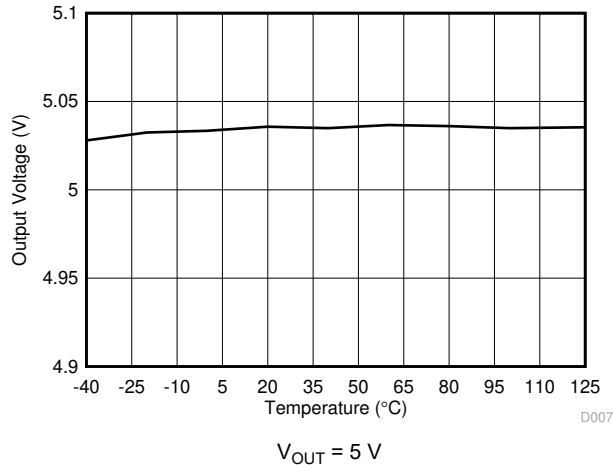


Figure 6-7. Output Voltage vs Ambient Temperature

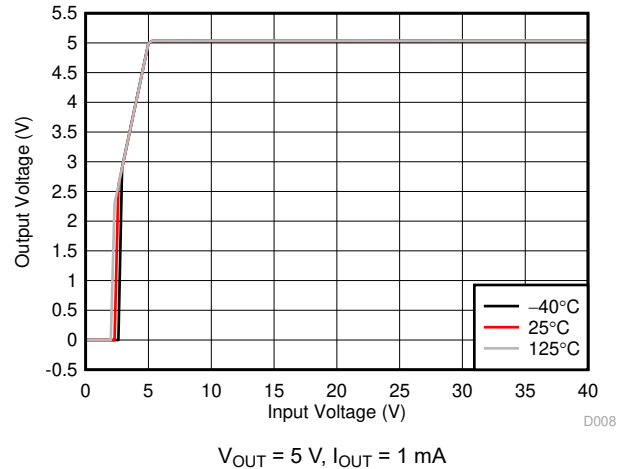


Figure 6-8. Output Voltage vs Input Voltage

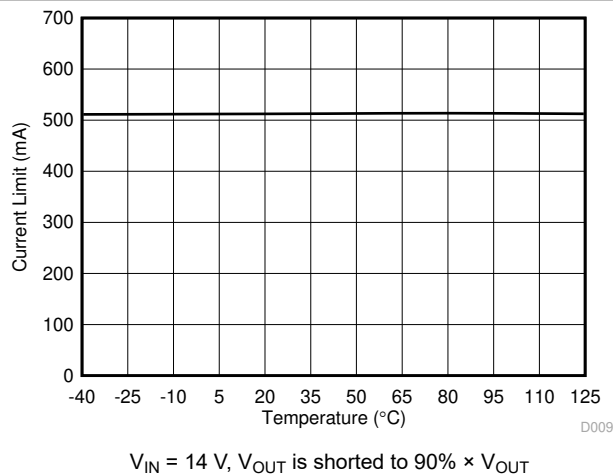


Figure 6-9. Output Current Limit vs Ambient Temperature

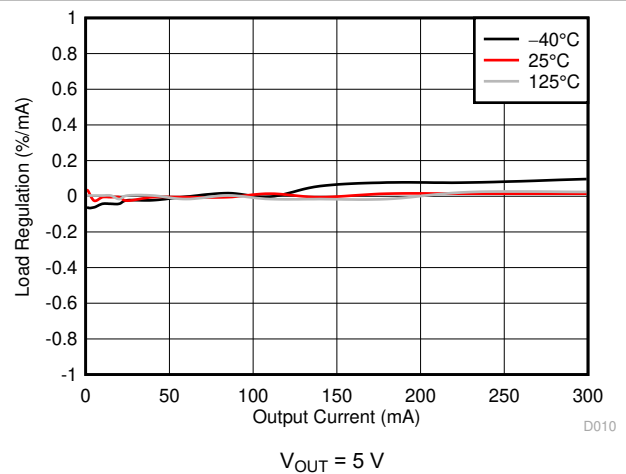


Figure 6-10. Load Regulation

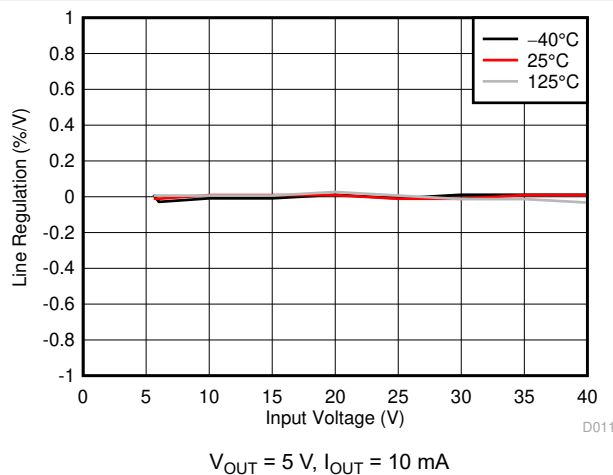


Figure 6-11. Line Regulation

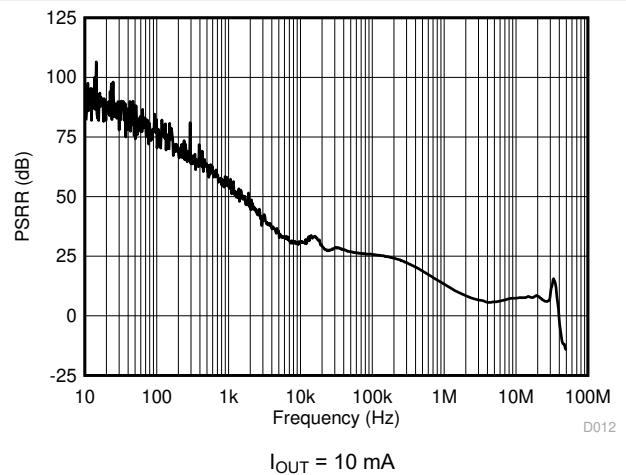


Figure 6-12. PSRR vs Frequency

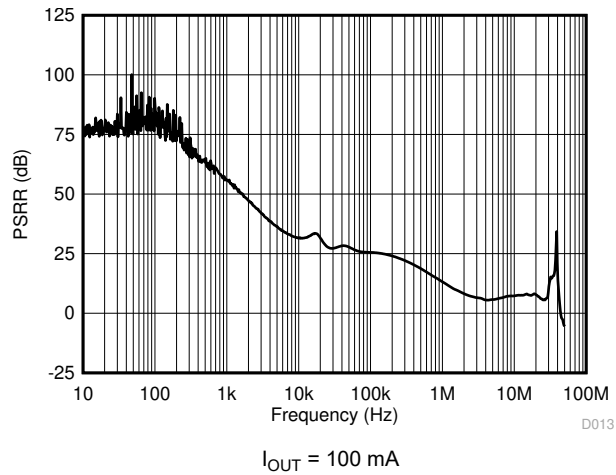


Figure 6-13. PSRR vs Frequency

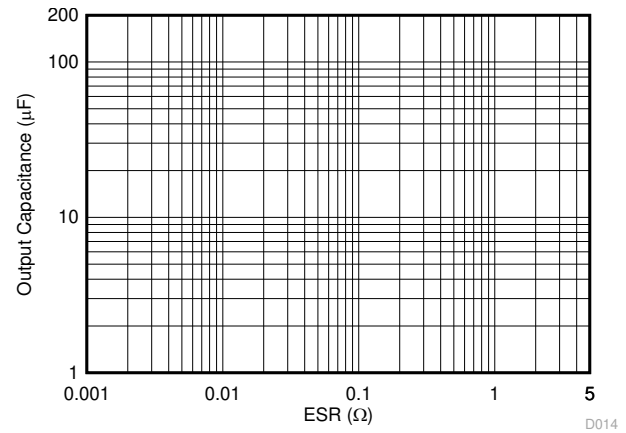


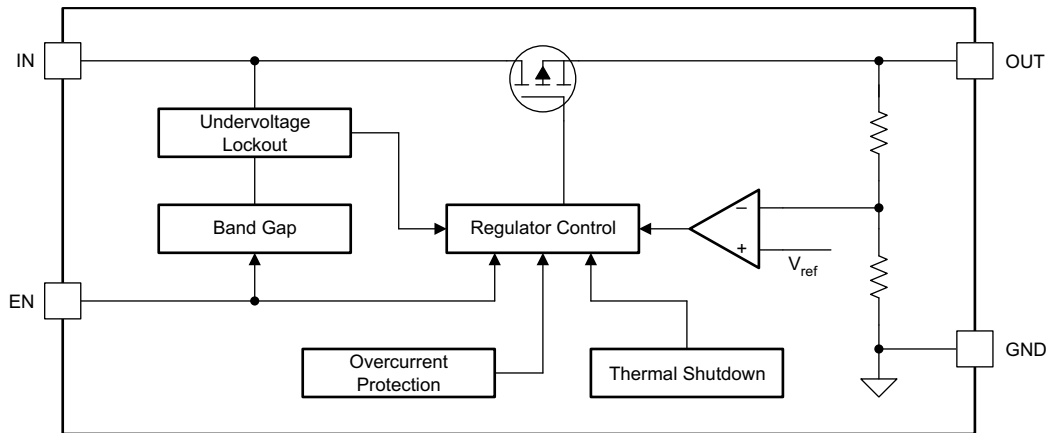
Figure 6-14. Output Capacitance vs ESR Stability

7 Detailed Description

7.1 Overview

The TPS7B82-Q1 is a 40-V 300-mA low-dropout linear regulator with ultralow quiescent current. This voltage regulator consumes only 3 μ A of quiescent current at light load, and is quite suitable for the automotive always-on application.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Device Enable (EN)

The EN pin is a high-voltage-tolerant pin. A high input activates the device and turns the regulation ON. Connect this pin to an external microcontroller or a digital circuit to enable and disable the device, or connect to the IN pin for self-bias applications.

7.3.2 Undervoltage Shutdown

This device has an integrated undervoltage lockout (UVLO) circuit to shut down the output if the input voltage (V_{IN}) falls below an internal UVLO threshold ($V_{(UVLO)}$). This ensures that the regulator does not latch into an unknown state during low-input-voltage conditions. If the input voltage has a negative transient which drops below the UVLO threshold and recovers, the regulator shuts down and powers up with a normal power-up sequence once the input voltage is above the required level.

7.3.3 Current Limit

This device features current-limit protection to keep the device in a safe operating area when an overload or output short-to-ground condition occurs. This protects the device from excessive power dissipation. For example, during a short-circuit condition on the output, fault protection limits the current through the pass element to $I_{(LIM)}$ to protect the device from excessive power dissipation.

7.3.4 Thermal Shutdown

This device incorporates a thermal shutdown (TSD) circuit as a protection from overheating. For continuous normal operation, the junction temperature should not exceed the TSD trip point. The junction temperature exceeding the TSD trip point causes the output to turn off. When the junction temperature falls below the TSD trip point minus thermal shutdown hysteresis, the output turns on again.

7.4 Device Functional Modes

7.4.1 Operation With V_{IN} Lower Than 3 V

The device normally operates with input voltages above 3 V. The device can also operate at lower input voltages; the maximum UVLO voltage is 2.7 V. At input voltages below the actual UVLO voltage, the device does not operate.

7.4.2 Operation With V_{IN} Larger Than 3 V

When V_{IN} is greater than 3 V, if V_{IN} is also higher than the output set value plus the device dropout voltage, V_{OUT} is equal to the set value. Otherwise, V_{OUT} is equal to V_{IN} minus the dropout voltage.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS7B82-Q1 is a 300-mA 40-V low-dropout linear regulator with ultralow quiescent current. The PSpice transient model is available for download on the product folder and can be used to evaluate the basic function of the device.

8.2 Typical Application

Figure 8-1 shows a typical application circuit for the TPS7B82-Q1. Different values of external components can be used, depending on the end application. An application may require a larger output capacitor during fast load steps to prevent a large drop on the output voltage. TI recommends using a low-ESR ceramic capacitor with a dielectric of type X5R or X7R.

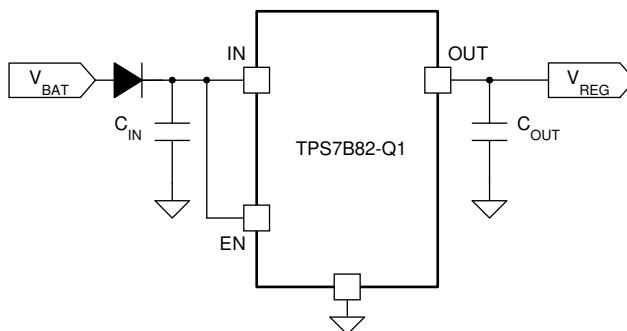


Figure 8-1. TPS7B82-Q1 Typical Application Schematic

8.2.1 Design Requirements

For this design example, use the parameters listed in Table 8-1.

Table 8-1. Design Requirements Parameters

PARAMETER	VALUE
Input voltage range	3 V to 40 V
Output voltage	5 V or 3.3 V
Output current	300 mA maximum

8.2.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
- Output voltage
- Output current

8.2.2.1 Input Capacitor

Although an input capacitor is not required for stability, good analog design practice is to connect a 10-μF to 22-μF capacitor from IN to GND. This capacitor counteracts reactive input sources and improves transient response, input ripple rejection, and PSRR. The voltage rating must be greater than the maximum input voltage.

8.2.2.2 Output Capacitor

To ensure the stability of the TPS7B82-Q1, the device requires an output capacitor with a value in the range from 1 μF to 200 μF and with an ESR range between 0.001 Ω and 5 Ω . TI recommends selecting a ceramic capacitor with low ESR to improve the load transient response.

8.2.3 Application Curve

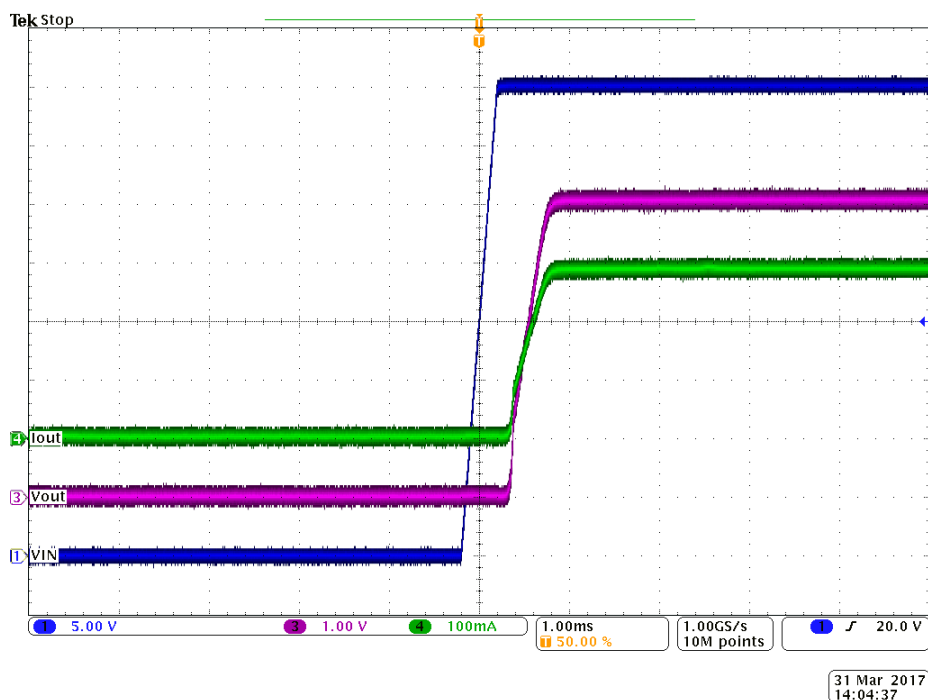


Figure 8-2. TPS7B82-Q1 Power-Up Waveform (5 V)

9 Power Supply Recommendations

The device is designed to operate from an input-voltage supply range from 3 V to 40 V. This input supply must be well regulated. If the input supply is located more than a few inches from the TPS7B82-Q1, TI recommends adding a capacitor with a value greater than or equal to 10 μ F with a 0.1- μ F bypass capacitor in parallel at the input.

10 Layout

10.1 Layout Guidelines

For LDO power supplies, especially these high-voltage and large-output-current ones, layout is an important step. If layout is not carefully designed, the regulator could fail to deliver enough output current because of thermal limitation. To improve the thermal performance of the device, and maximize the current output at high ambient temperature, TI recommends spreading the copper under the thermal pad as far as possible and placing enough thermal vias on the copper under the thermal pad. [Figure 10-1](#) shows an example layout.

10.2 Layout Example

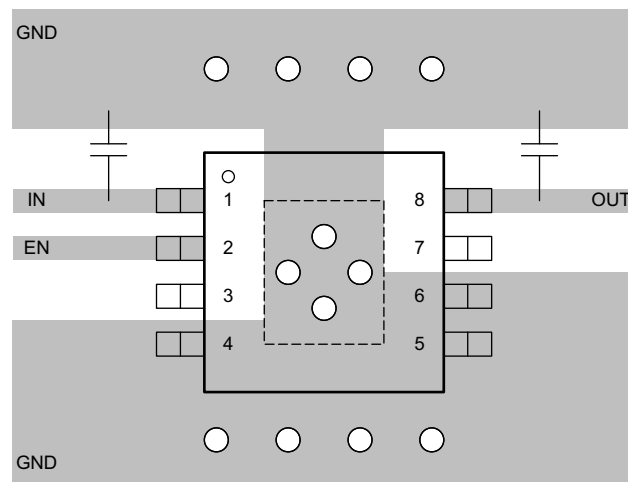


Figure 10-1. TPSB82-Q1 Example Layout Diagram

11 Device and Documentation Support

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

11.3 Trademarks

PowerPAD™ and TI E2E™ are trademarks of Texas Instruments Incorporated. All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most-current data available for the designated device. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, see the left-hand navigation pane.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS7B8225QDGNRQ1	ACTIVE	HVSSOP	DGN	8	2500	Green (RoHS & no Sb/Br)	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 150	1QFX	Samples
TPS7B8233QDGNRQ1	ACTIVE	HVSSOP	DGN	8	2500	Green (RoHS & no Sb/Br)	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 150	1GGX	Samples
TPS7B8233QDRVRQ1	ACTIVE	WSO	DRV	6	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	1ORH	Samples
TPS7B8233QKVURQ1	ACTIVE	TO-252	KVU	5	2500	Green (RoHS & no Sb/Br)	SN	Level-3-260C-168 HR	-40 to 150	7B8233Q1	Samples
TPS7B8250QDGNRQ1	ACTIVE	HVSSOP	DGN	8	2500	Green (RoHS & no Sb/Br)	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 150	19TX	Samples
TPS7B8250QDRVRQ1	ACTIVE	WSO	DRV	6	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	1UFH	Samples
TPS7B8250QKVURQ1	ACTIVE	TO-252	KVU	5	2500	Green (RoHS & no Sb/Br)	SN	Level-3-260C-168 HR	-40 to 150	7B8250Q1	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

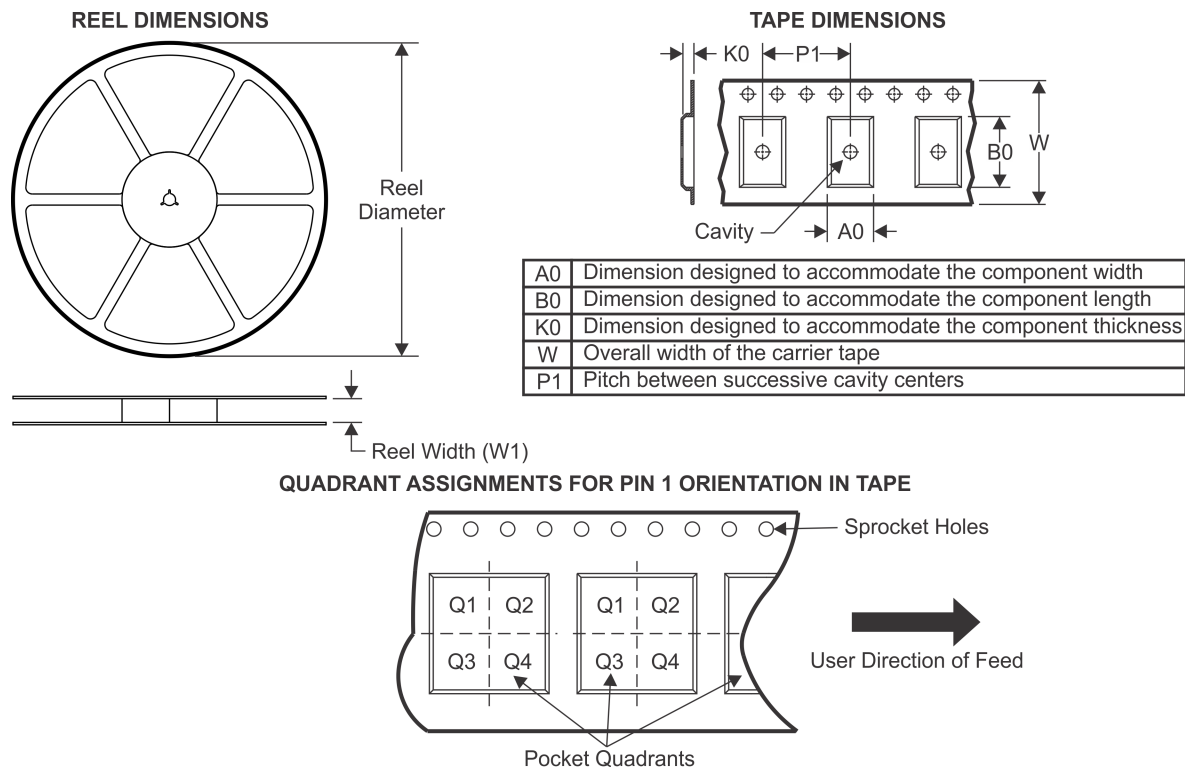
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

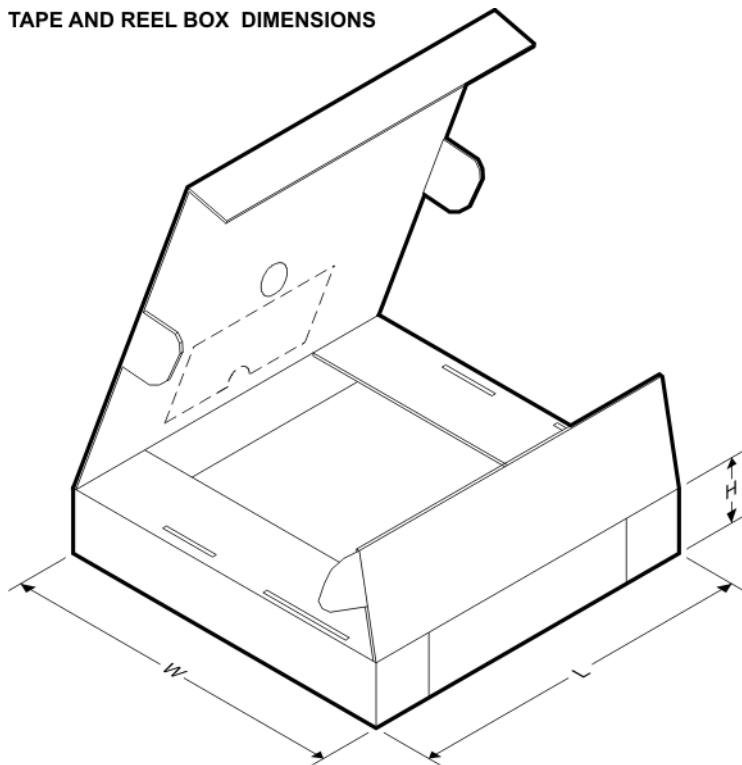
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7B8225QDGNRQ1	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS7B8233QDGNRQ1	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS7B8233QDRVRQ1	WSOP	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS7B8233QKVURQ1	TO-252	KVU	5	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2
TPS7B8250QDGNRQ1	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS7B8250QDRVRQ1	WSOP	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS7B8250QKVURQ1	TO-252	KVU	5	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS

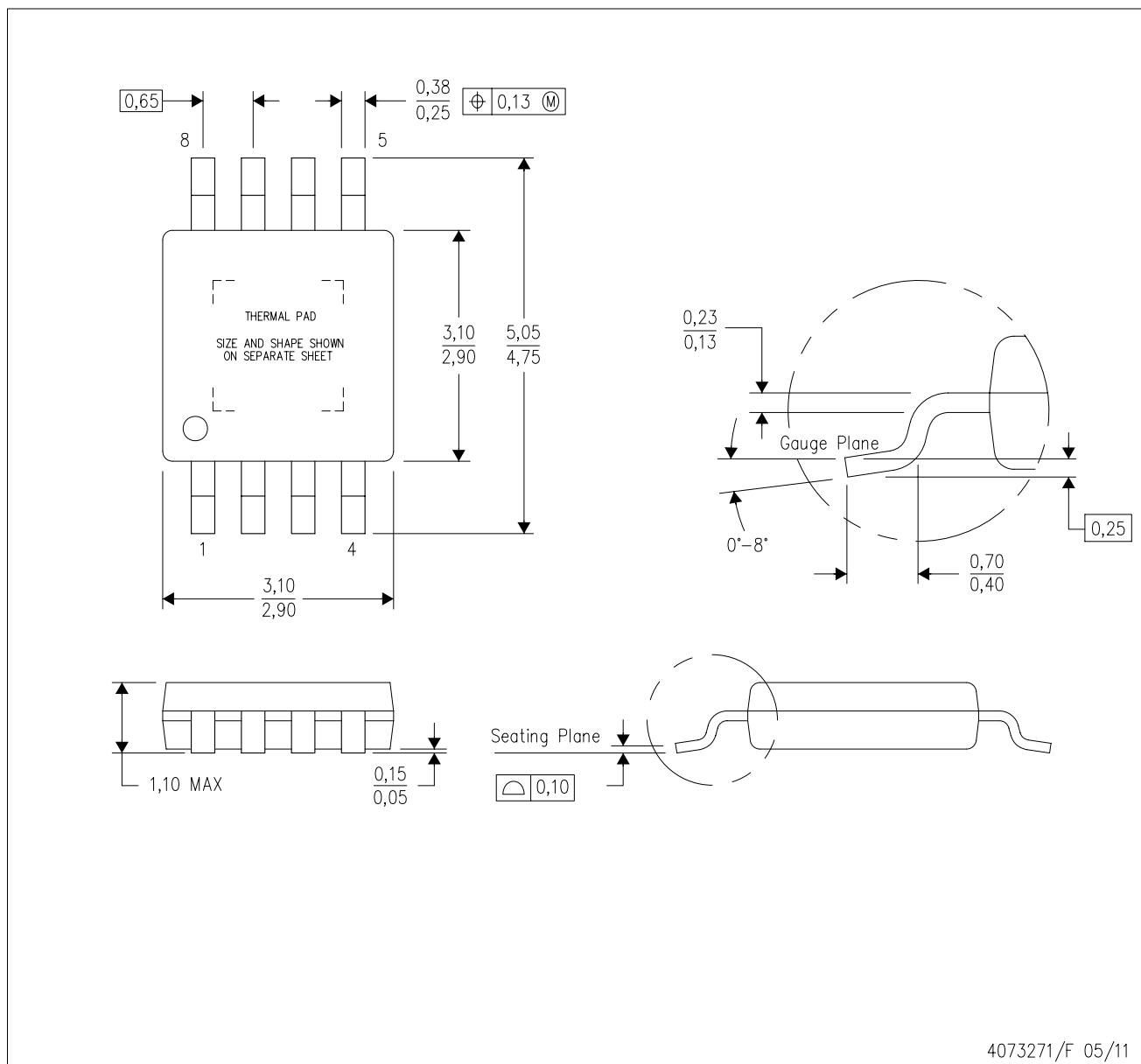


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7B8225QDGNRQ1	HVSSOP	DGN	8	2500	366.0	364.0	50.0
TPS7B8233QDGNRQ1	HVSSOP	DGN	8	2500	366.0	364.0	50.0
TPS7B8233QDRVRQ1	WSON	DRV	6	3000	210.0	185.0	35.0
TPS7B8233QKVURQ1	TO-252	KVU	5	2500	340.0	340.0	38.0
TPS7B8250QDGNRQ1	HVSSOP	DGN	8	2500	366.0	364.0	50.0
TPS7B8250QDRVRQ1	WSON	DRV	6	3000	210.0	185.0	35.0
TPS7B8250QKVURQ1	TO-252	KVU	5	2500	340.0	340.0	38.0

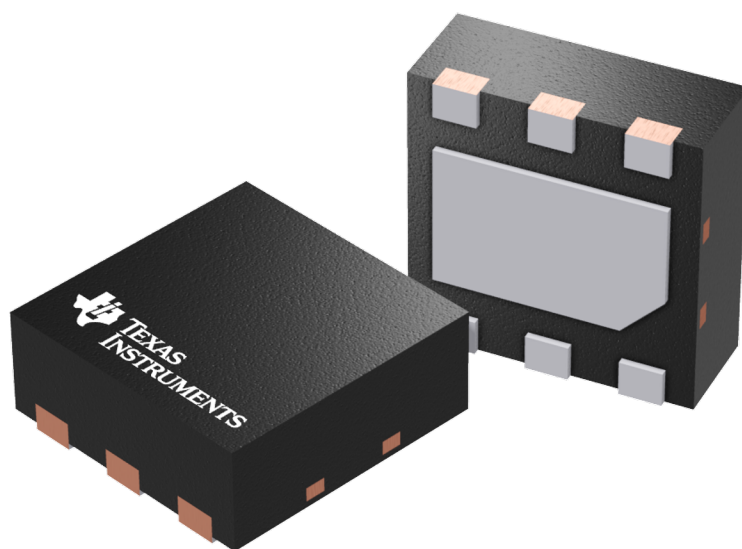
DGN (S-PDSO-G8)

PowerPAD™ PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <<http://www.ti.com>>.
 - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - Falls within JEDEC MO-187 variation AA-T

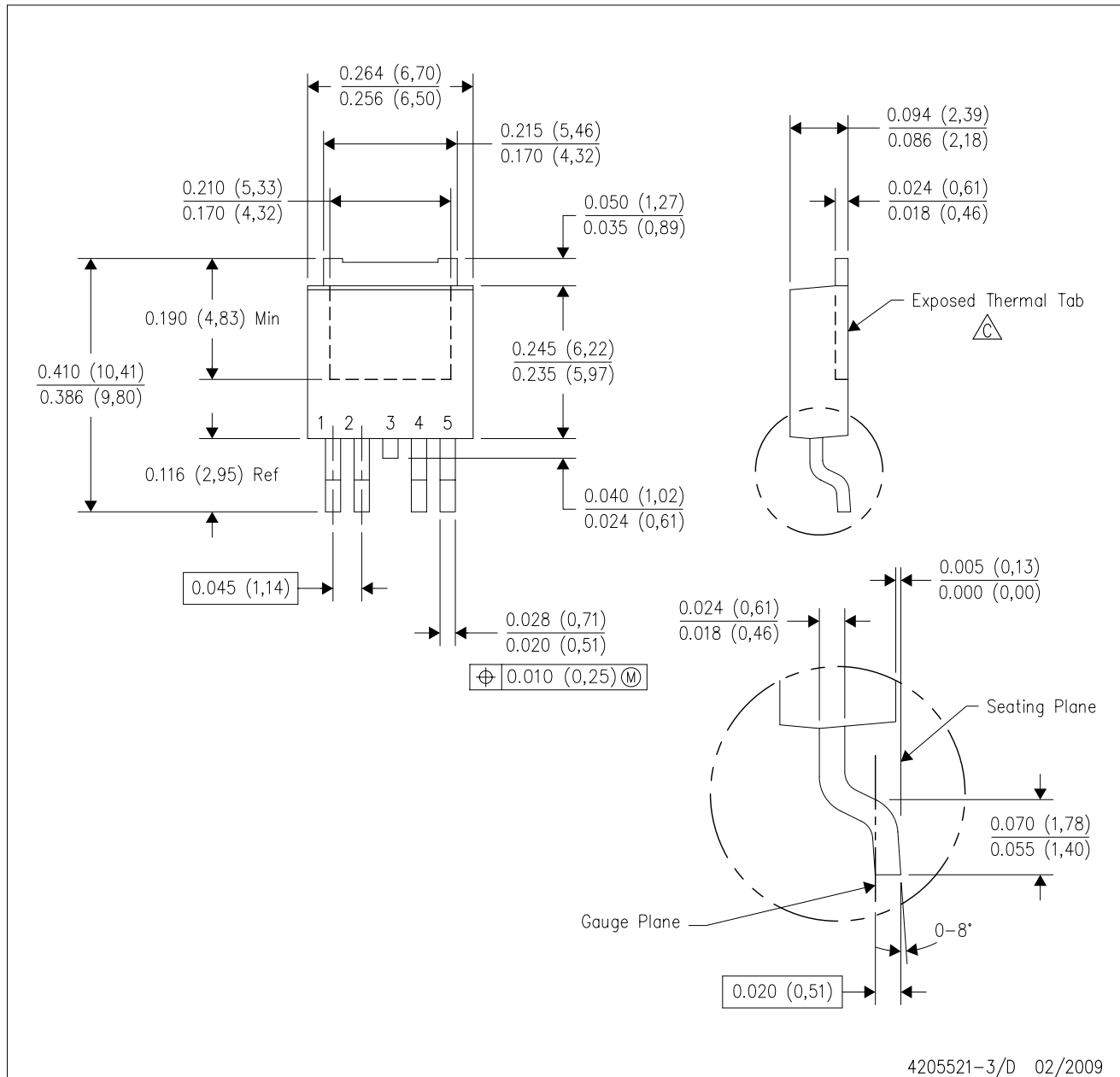
PowerPAD is a trademark of Texas Instruments.



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

KVU (R-PSFM-G5)

PLASTIC FLANGE-MOUNT PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. The center lead is in electrical contact with the exposed thermal tab.
 - D. Body Dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.006 (0,15) per side.
 - E. Falls within JEDEC TO-252 variation AD.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2020, Texas Instruments Incorporated