TLC59108 8-Bit Fm+ I²C-Bus Constant-Current LED Sink Driver

1 Features

- Eight LED Drivers (Each Output Programmable At Off, On, Programmable LED Brightness, Programmable Group Dimming/Blinking Mixed With Individual LED Brightness
- Eight Constant-Current Output Channels
- 256-Step (8-Bit) Linear Programmable Brightness Per LED Output Varying From Fully Off (Default) to Maximum Brightness Using a 97-kHz PWM Signal
- 256-Step Group Brightness Control Allows General Dimming (Using a 190-Hz PWM Signal From Fully Off to Maximum Brightness (Default)
- 256-Step Group Blinking With Frequency Programmable From 24 Hz to 10.73 s and Duty Cycle From 0% to 99.6%
- Four Hardware Address Pins Allow 14 TLC59108 Devices to be Connected to the Same I²C Bus
- Four Software-Programmable I²C Bus Addresses (One LED Group Call Address and Three LED Sub Call Addresses) Allow Groups of Devices to be Addressed at the Same Time in Any Combination. For Example, One Register Used for All Call, so That All the TLC59108 Devices on the I²C Bus Can be Addressed at the Same Time, and the Second Register Can be Used for Three Different Addresses so That One-Third of All Devices on the Bus Can be Addressed at the Same Time in a Group.
- Software Enable and Disable for I²C Bus Address
- Software Reset Feature (SWRST Call) Allows Device to be Reset Through I²C Bus
- Up to 14 Possible Hardware-Adjustable Individual I²C Bus Addresses Per Device, So That Each Device Can Be Programmed
- Open-Load/Overtemperature Detection Mode to Detect Individual LED Errors
- Output State Change Programmable on the Acknowledge or the Stop Command to Update Outputs Byte by Byte or All at the Same Time (Default to Change on Stop)
- Constant Output Current Adjusted Through an External Resistor (10mA to 120mA)
- Maximum Output Voltage: 17 V
- 25-MHz Internal Oscillator Requires No External Components
- 1-MHz Fast Mode Plus Compatible I²C Bus Interface With 30-mA High Drive Capability on SDA Output for Driving High-Capacitive Buses
- Internal Power-On Reset
- Noise Filter on SCL/SDA Inputs
- No Glitch on Power Up
- Active-Low Reset
- Supports Hot Insertion
- 3.3-V or 5-V Supply Voltage

2 Applications

- Gaming
- Small Signage
- Industrial Equipment

3 Description

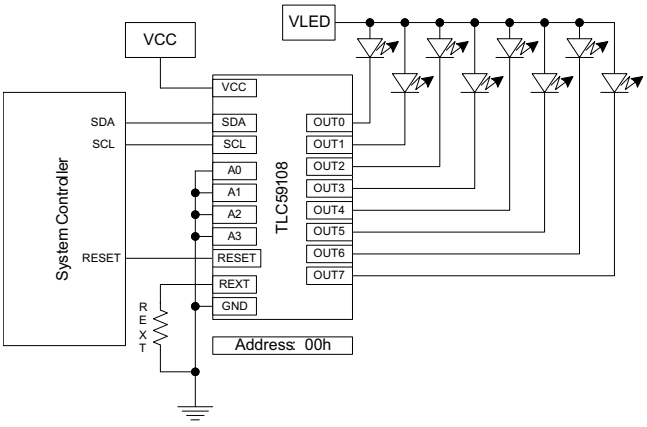
The TLC59108 is an I²C bus controlled 8-bit LED driver that is optimized for red/green/blue/amber (RGBA) color mixing and backlight applications.

Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TLC59108	TSSOP (20)	6.50 mm × 4.40 mm
	VQFN (20)	4.50 mm × 3.50 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Schematic



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Table of Contents

1 Features ... 1
2 Applications ... 1
3 Description ... 1
4 Revision History ... 2
5 Description (continued) ... 3
6 Pin Configuration and Functions ... 4
7 Specifications ... 5
7.1 Absolute Maximum Ratings ... 5
7.2 ESD Ratings ... 5
7.3 Recommended Operating Conditions ... 5
7.4 Thermal Information ... 6
7.5 Electrical Characteristics ... 6
7.6 Timing Requirements ... 8
7.7 Typical Characteristics ... 9
8 Parameter Measurement Information ... 9
9 Detailed Description ... 11
9.1 Overview ... 11
9.2 Functional Block Diagram ... 11
9.3 Feature Description ... 12
9.4 Device Functional Modes ... 14
9.5 Programming ... 14
9.6 Register Maps ... 22
10 Application and Implementation ... 29
10.1 Application Information ... 29
10.2 Typical Application ... 30
11 Power Supply Recommendations ... 33
12 Layout ... 33
12.1 Layout Guidelines ... 33
12.2 Layout Examples ... 33
13 Device and Documentation Support ... 35
13.1 Community Resources ... 35
13.2 Trademarks ... 35
13.3 Electrostatic Discharge Caution ... 35
13.4 Glossary ... 35
14 Mechanical, Packaging, and Orderable Information ... 35

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (December 2011) to Revision B **Page**

- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

Changes from Original (November 2011) to Revision A **Page**

- Changed SLEEP Symbol to OSC and removed the "Low power mode" description to clarify functionality. ... 23
- Changed ALLCALLADR register to IREF and changed register from 11h to 12h. ... 27
- Added I_{OUT} vs V_{OUT} graph. ... 29
- Added TLC59108 and TLC59108F Differences section. ... 30
- Added Typical Application Examples section. ... 30

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5 Description (continued)

Each LED output has its own 8-bit resolution (256 steps) fixed-frequency individual PWM controller that operates at 97 kHz, with a duty cycle that is adjustable from 0% to 99.6%. The individual PWM controller allows each LED to be set to a specific brightness value. An additional 8-bit resolution (256 steps) group PWM controller has both a fixed frequency of 190 Hz and an adjustable frequency between 24 Hz to once every 10.73 seconds, with a duty cycle that is adjustable from 0% to 99.6%. The group PWM controller dims or blinks all LEDs with the same value.

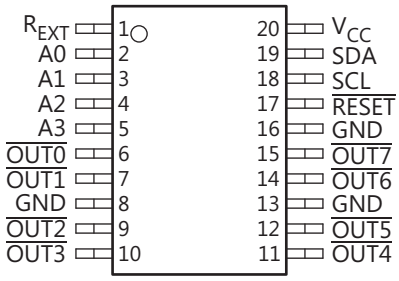
Each LED output can be off, on (no PWM control), or set at its individual PWM controller value at both individual and group PWM controller values.

Software programmable LED group and three Sub Call I^2C bus addresses allow all or defined groups of TLC59108 devices to respond to a common I^2C bus address, allowing for example, all red LEDs to be turned on or off at the same time or marquee chasing effect, thus minimizing I^2C bus commands. Four hardware address pins allow up to 14 devices on the same bus.

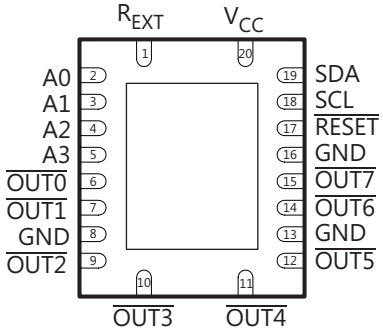
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6 Pin Configuration and Functions

PW Package
20-Pin TSSOP
(Top View)



RGY Package
20-Pin VQFN With Thermal Pad
(Top View)



Pin Functions

PIN		I/O (1)	DESCRIPTION
NAME	NO.		
A0	2	I	Address input 0
A1	3	I	Address input 1
A2	4	I	Address input 2
A3	5	I	Address input 3
GND	8, 13, 16	–	Ground
$\overline{OUT0}$	6	O	Constant current output 0, LED on at low
$\overline{OUT1}$	7	O	Constant current output 1, LED on at low
$\overline{OUT2}$	9	O	Constant current output 2, LED on at low
$\overline{OUT3}$	10	O	Constant current output 3, LED on at low
$\overline{OUT4}$	11	O	Constant current output 4, LED on at low
$\overline{OUT5}$	12	O	Constant current output 5, LED on at low
$\overline{OUT6}$	14	O	Constant current output 6, LED on at low
$\overline{OUT7}$	15	O	Constant current output 7, LED on at low
$\overline{RESET}$	17	I	Active-low reset input
R_{EXT}	1	–	Input terminal used to connect an external resistor for setting up all output currents
SCL	18	I	Serial clock input
SDA	19	I/O	Serial data input/output
V_{CC}	20	–	Power supply

(1) I = input, O = output

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	0	7	V
V_I	Input voltage	–0.4	7	V
V_O	Output voltage	–0.5	20	V
I_O	Output current		120	mA
T_J	Junction temperature	–40	150	°C
T_{stg}	Storage temperature	–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

				(1)MIN	MAX	UNIT
V_{CC}	Supply voltage			3	5.5	V
V_{IH}	High-level input voltage	SCL, SDA, $\overline{\text{RESET}}$, A0, A1, A2, A3		0.7 × V_{CC}	V_{CC}	V
V_{IL}	Low-level input voltage	SCL, SDA, $\overline{\text{RESET}}$, A0, A1, A2, A3		0	0.3 × V_{CC}	V
V_O	Supply voltage to output pins	$\overline{\text{OUT0}}$ to $\overline{\text{OUT7}}$			17	V
I_{OL}	Low-level output current sink	SDA	V_{CC} = 3 V		20	mA
			V_{CC} = 3 V		30	
I_O	Output current	$\overline{\text{OUT0}}$ to $\overline{\text{OUT7}}$		5	120	mA
T_A	Operating free-air temperature			–40	85	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

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7.4 Thermal Information

THERMAL METRIC (1)		TLC59108		UNIT
		PW (TSSOP)	RGY (VQFN)	
		20 PINS	20 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	98.9	39.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	32.9	44.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	49.9	14.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.7	1.0	°C/W
ψ_{JB}	Junction-to-board characterization parameter	49.3	14.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	–	7.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

V_{CC} = 3 V to 5.5 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP (1)	MAX	UNIT
I_I	Input/output leakage current	SCL, SDA, A0, A1, A2, A3, RESET	$V_I = V_{CC}$ or GND			±0.3	µA
	Output leakage current	$\overline{OUT0}$ to $\overline{OUT7}$	V_O = 17 V, T_J = 25°C			0.5	µA
V_{POR}	Power-on reset voltage				2.5		V
I_{OL}	Low-level output current	SDA	V_{CC} = 3 V, V_{OL} = 0.4 V	20			mA
			V_{CC} = 5 V, V_{OL} = 0.4 V	30			
$I_{O(1)}$	Output current 1	$\overline{OUT0}$ to $\overline{OUT7}$	V_O = 0.6 V, R_{ext} = 720 Ω, CG = 0.992		26		mA
	Output current error	$\overline{OUT0}$ to $\overline{OUT7}$	I_O = 26 mA, V_O = 0.6 V, R_{ext} = 720 Ω, T_J = 25°C			±8%	
	Output channel to channel current error	$\overline{OUT0}$ to $\overline{OUT7}$	I_O = 26 mA, V_O = 0.6 V, R_{ext} = 720 Ω, T_J = 25°C			±3%	
$I_{O(2)}$	Output current 2	$\overline{OUT0}$ to $\overline{OUT7}$	VO = 0.8 V, R_{ext} = 360 Ω, CG = 0.992		52		mA
	Output current error	$\overline{OUT0}$ to $\overline{OUT7}$	I_O = 52 mA, V_O = 0.8 V, R_{ext} = 360 Ω, T_J = 25°C			±8%	
	Output channel to channel current error	$\overline{OUT0}$ to $\overline{OUT7}$	I_O = 52 mA, V_O = 0.8 V, R_{ext} = 360 Ω, T_J = 25°C			±3%	
I_{OUT} vs V_{OUT}	Output current vs output voltage regulation	$\overline{OUT0}$ to $\overline{OUT7}$	V_O = 1 V to 3 V, I_O = 26 mA		±0.1		%/V
			V_O = 3 V to 5.5 V, I_O = 26 mA to 120 mA		±1		
$I_{OUT,Th1}$	Threshold current 1 for error detection	$\overline{OUT0}$ to $\overline{OUT7}$	$I_{OUT,target}$ = 26 mA		0.5% × I_{TARGET}		
$I_{OUT,Th2}$	Threshold current 2 for error detection	$\overline{OUT0}$ to $\overline{OUT7}$	$I_{OUT,target}$ = 52 mA		0.5% × I_{TARGET}		
$I_{OUT,Th3}$	Threshold current 3 for error detection	$\overline{OUT0}$ to $\overline{OUT7}$	$I_{OUT,target}$ = 104 mA		0.5% × I_{TARGET}		

(1) All typical values are at T_A = 25°C.

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Electrical Characteristics (continued)

V_{CC} = 3 V to 5.5 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP (1)	MAX	UNIT
T_{SD}	Overtemperature shutdown (2)				150	175	200	°C
T_{HYS}	Restart hysteresis					15		°C
C_i	Input capacitance	SCL, A0, A1, A2, A3, $\overline{RESET}$	$V_I = V_{CC}$ or GND				5	pF
C_{io}	Input/output capacitance	SDA	$V_I = V_{CC}$ or GND				5	pF
I_{CC}	Supply current		V_{CC} = 5.5 V	$\overline{OUT0}$ to $\overline{OUT7}$ = OFF, R_{ext} = Open			17	mA
				$\overline{OUT0}$ to $\overline{OUT7}$ = OFF, R_{ext} = 720 Ω			20	
				$\overline{OUT0}$ to $\overline{OUT7}$ = OFF, R_{ext} = 360 Ω			23	
				$\overline{OUT0}$ to $\overline{OUT7}$ = OFF, R_{ext} = 180 Ω			28	
				$\overline{OUT0}$ to $\overline{OUT7}$ = ON, R_{ext} = 720 Ω			21	
				$\overline{OUT0}$ to $\overline{OUT7}$ = ON, R_{ext} = 360 Ω			23	
				$\overline{OUT0}$ to $\overline{OUT7}$ = ON, R_{ext} = 180 Ω			28	

(2) Specified by design

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7.6 Timing Requirements

T_A = –40°C to 85°C

		STANDARD MODE I²C BUS		FAST MODE I²C BUS		FAST MODE PLUS I²C BUS		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
I²C Interface								
f_{SCL}	SCL clock frequency	0	100	0	400	0	1000	kHz
t_{BUF}	I²C bus free time between stop and start	4.7		1.3		0.5		µs
$t_{HD;STA}$	Hold time (repeated) Start condition	4		0.6		0.26		µs
$t_{SU;STA}$	Set-up time for a repeated Start condition	4.7		0.6		0.26		µs
$t_{SU;STO}$	Set-up time for Stop condition	4		0.6		0.26		µs
$t_{HD;DAT}$	Data hold time	0		0		0		ns
$t_{VD;ACK}$	Data valid acknowledge time (1)	0.3	3.45	0.1	0.9	0.05	0.45	µs
$t_{VD;DAT}$	Data valid time (2)	0.3	3.45	0.1	0.9	0.05	0.45	µs
$t_{SU;DAT}$	Data set-up time	250		100		50		ns
t_{LOW}	Low period of the SCL clock	4.7		1.3		0.5		µs
t_{HIGH}	High period of the SCL clock	4		0.6		0.26		µs
t_f	Fall time of both SDA and SCL signals (3) (4)		300	20+0.1C_b (5)	300		120	ns
t_r	Rise time of both SDA and SCL signals		1000	20+0.1C_b (5)	300		120	ns
t_{SP}	Pulse width of spikes that must be suppressed by the input filter (6)		50		50		50	ns
Reset								
t_W	Reset pulse width	10		10		10		ns
t_{REC}	Reset recovery time	0		0		0		ns
t_{RESET}	Time to reset (7) (8)	400		400		400		ns

(1) $t_{VD;ACK}$ = time for Acknowledgment signal from SCL low to SDA (out) low.
(2) $t_{VD;DAT}$ = minimum time for SDA data out to be valid following SCL low.
(3) A master device must internally provide a hold time of at least 300 ns for the SDA signal (refer to the V_{IL} of the SCL signal) in order to bridge the undefined region of the SCL falling edge.
(4) The maximum t_f for the SDA and SCL bus lines is specified at 300 ns. The maximum fall time (t_f) for the SDA output stage is specified at 250 ns. This allows series protection resistors to be connected between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified t_f.
(5) C_b = total capacitance of one bus line in pF.
(6) Input filters on the SDA and SCL inputs suppress noise spikes less than 50 ns
(7) Resetting the device while actively communicating on the bus may cause glitches or errant Stop conditions.
(8) Upon reset, the full delay is the sum of t_{RESET} and the RC time constant of the SDA bus.

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7.7 Typical Characteristics

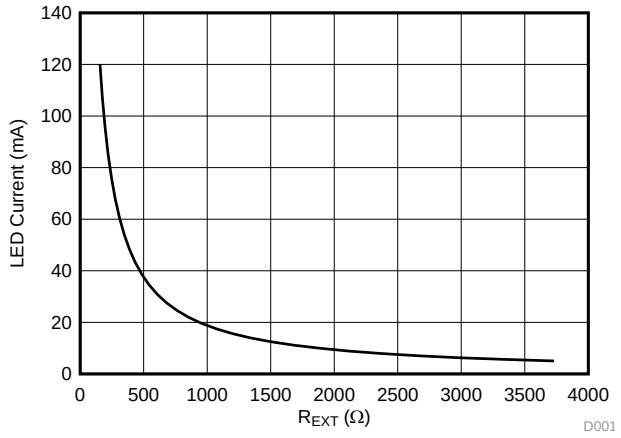


Figure 1. LED Current vs R_{EXT} Resistance

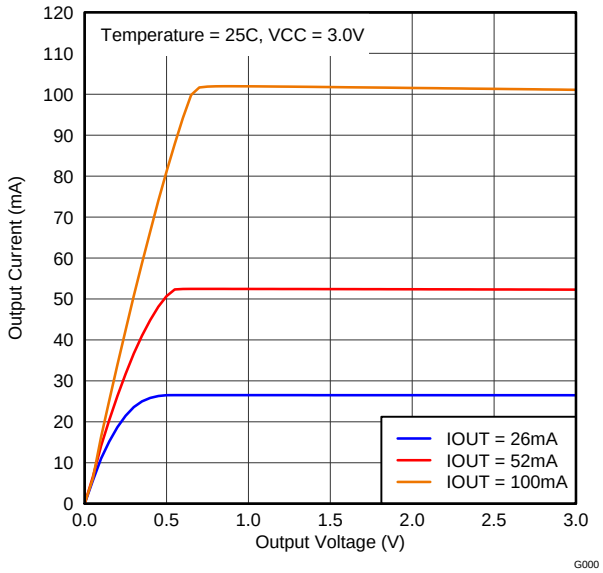


Figure 2. Output Current vs Output Voltage

8 Parameter Measurement Information

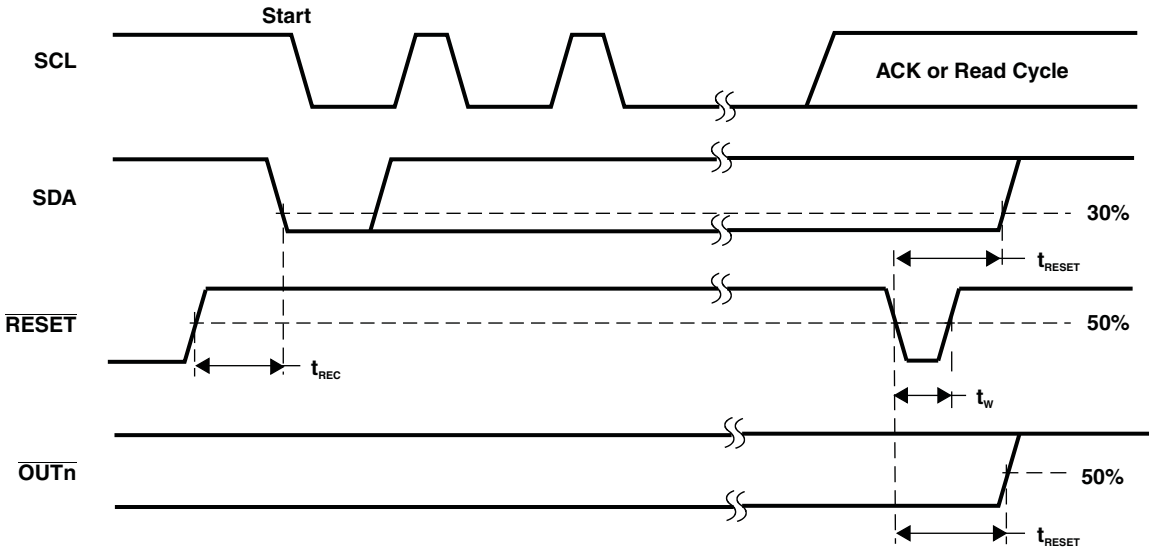


Figure 3. Reset Timing

Parameter Measurement Information (continued)

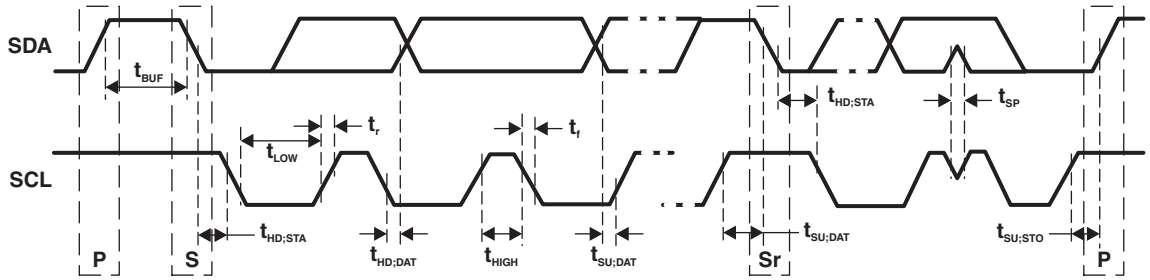
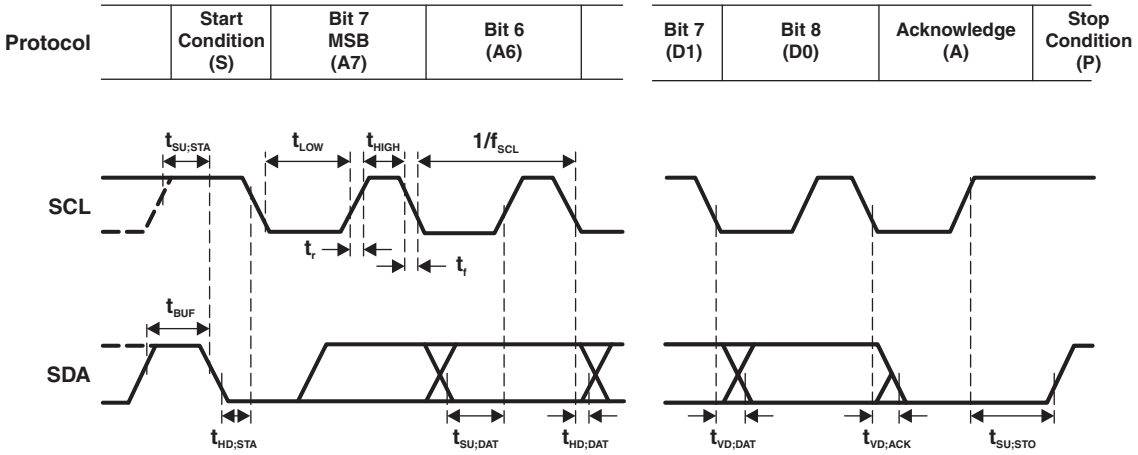
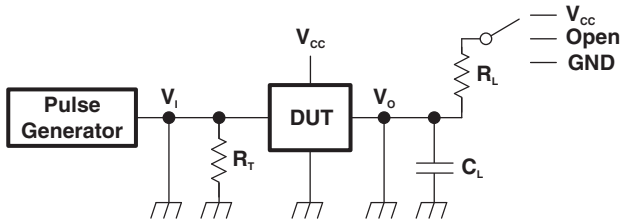


Figure 4. Definition of Timing



NOTE: Rise and fall times refer to V_{IL} and V_{IH}.

Figure 5. I^2C Bus Timing



NOTE: R_L = Load resistance for SDA and SCL; should be >1 kΩ at 3-mA or lower current.
C_L = Load capacitance; includes jig and probe capacitance.
R_T = Termination resistance; should be equal to the output impedance (Z_O) of the pulse generator.

Figure 6. Test Circuit for Switching Characteristics

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9 Detailed Description

9.1 Overview

The TLC59108 is an I2C bus controlled 8-bit LED driver that is optimized for red/green/blue/amber (RGBA) color mixing and backlight applications. Each LED output has its own 8-bit resolution (256 steps) fixed-frequency individual PWM controller that operates at 97 kHz, with a duty cycle that is adjustable from 0% to 99.6%. The individual PWM controller allows each LED to be set to a specific brightness value. An additional 8-bit resolution (256 steps) group PWM controller has both a fixed frequency of 190 Hz and an adjustable frequency between 24 Hz to once every 10.73 seconds, with a duty cycle that is adjustable from 0% to 99.6%. The group PWM controller dims or blinks all LEDs with the same value.

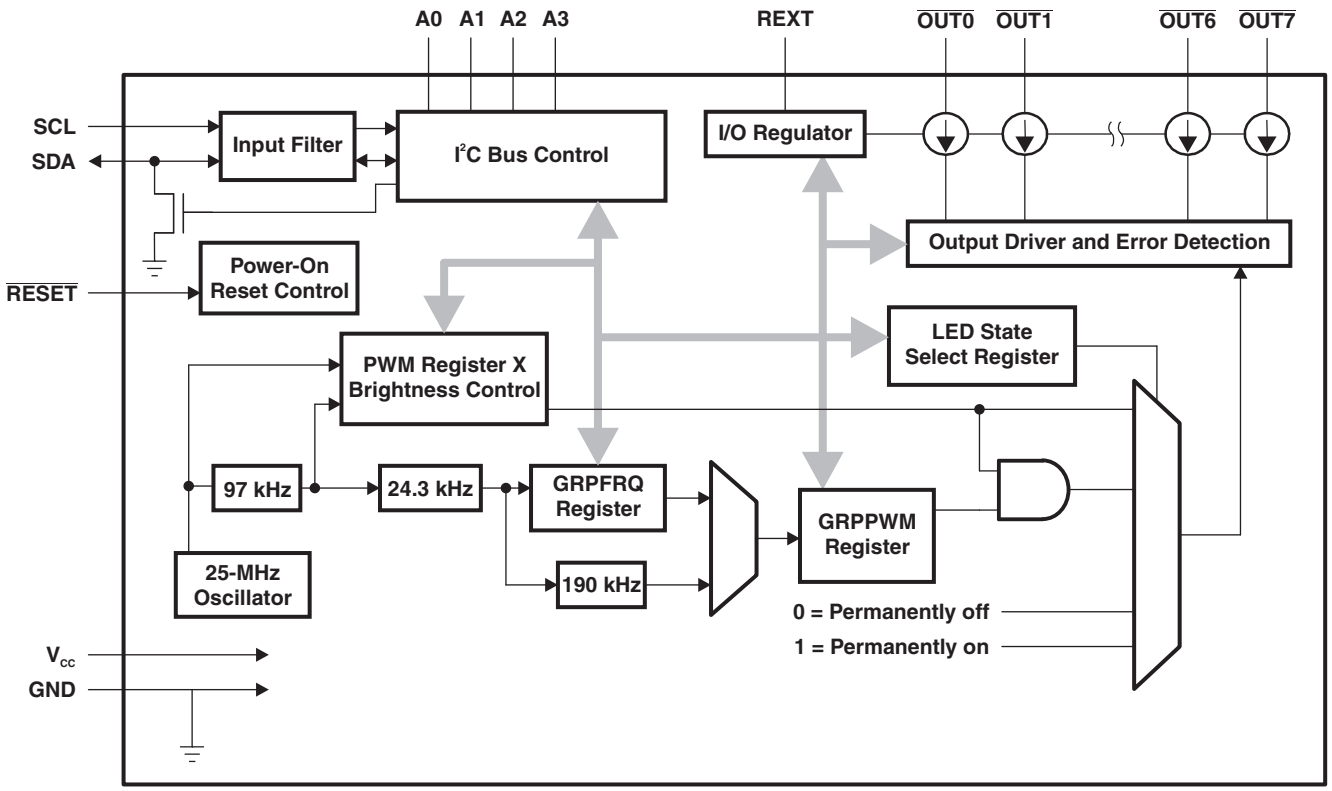
Each LED output can be off, on (no PWM control), or set at its individual PWM controller value at both individual and group PWM controller values.

The TLC59108 is one of the first LED controller devices in a new Fast-mode Plus (Fm+) family. Fm+ devices offer higher frequency (up to 1 MHz) and longer, more densely populated bus operation (up to 4000 pF).

Software programmable LED group and three Sub Call I2C bus addresses allow all or defined groups of TLC59108 devices to respond to a common I2C bus address, allowing for example, all red LEDs to be turned on or off at the same time or marquee chasing effect, thus minimizing I2C bus commands. Four hardware address pins allow up to 14 devices on the same bus.

The Software Reset (SWRST) call allows the master to perform a reset of the TLC59108 through the I2C bus, identical to the Power-On Reset (POR) that initializes the registers to their default state, causing the outputs to be set high (LED off). This allows an easy and quick way to reconfigure all device registers to the same condition.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Open-Circuit Detection

The TLC59108 LED open-circuit detection compares the effective current level I_{OUT} with the open load detection threshold current $I_{OUT,\ Th}$. If I_{OUT} is below the threshold $I_{OUT,\ Th}$ the TLC59108 detects an open load condition. This error status can be read out as an error flag through the EFLAG register.

For open-circuit error detection, a channel must be on.

Table 1. Open-Circuit Detection

STATE OF OUTPUT PORT	CONDITION OF OUTPUT CURRENT	ERROR STATUS CODE	MEANING
Off	I_{OUT} = 0 mA	0	Detection not possible
On	$I_{OUT} < I_{OUT,Th}$ (1)	0	Open circuit
	$I_{OUT} \geq I_{OUT,Th}$ (1)	Channel n error status bit 1	Normal

(1) $I_{OUT,Th} = 0.5 \times I_{OUT,target}$ (typical)

9.3.2 Overtemperature Detection and Shutdown

The TLC59108 LED is equipped with a global overtemperature sensor and eight individual channel-selective overtemperature sensors.

- When the global sensor reaches the trip temperature, all output channels are shutdown, and the error status is stored in the internal Error Status register of every channel. After shutdown, the channels automatically restart after cooling down, if the control signal (output latch) remains on. The stored error status is not reset after cooling down and can be read out as the error status code in the EFLAG register.
- When one of the channel-specific sensors reaches trip temperature, only the affected output channel is shut down, and the error status is stored only in the internal Error Status register of the affected channel. After shutdown, the channel automatically restarts after cooling down, if the control signal (output latch) remains on. The stored error status is not reset after cooling down and can be read out as error status code in the EFLAG register.

For channel-specific overtemperature error detection, a channel must be on.

The error flags of open-circuit and overtemperature are ORed to set the EFLAG register.

The error status code due to overtemperature is reset when the host writes 1 to bit 7 of the MODE2 register. The host must write 0 to bit 7 of the MODE2 register to enable the overtemperature error flag.

Table 2. Overtemperature Detection (1)

STATE OF OUTPUT PORT	CONDITION	ERROR STATUS CODE	MEANING
On On → all channels Off	$T_J < T_{J,trip}$ global	1	Normal
	$T_J > T_{J,trip}$ global	All error status bits = 0	Global overtemperature
On On → Off	$T_J < T_{J,trip}$ channel n	1	Normal
	$T_J > T_{J,trip}$ channel n	Channel n error status bit = 0	Channel n overtemperature

(1) The global shutdown threshold temperature is approximately 170°C.

9.3.3 Power-On Reset

When power is applied to V_{CC}, an internal power-on reset holds the TLC59108 in a reset condition until V_{CC} reaches V_{POR}. At this point, the reset condition is released and the TLC59108 registers, and I^2C bus state machine are initialized to their default states (all zeroes), causing all the channels to be deselected. Thereafter, V_{CC} must be lowered below 0.2 V to reset the device.

9.3.4 External Reset

A reset can be accomplished by holding the RESET pin low for a minimum of t_W. The TLC59108 registers and I^2C state machine are held in their default states until the RESET input is again high.

This input requires a pullup resistor to V_{CC} if no active connection is used.

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9.3.5 Software Reset

The Software Reset Call (SWRST Call) allows all the devices in the I^2C bus to be reset to the power-up state value through a specific I^2C bus command. To be performed correctly, the I^2C bus must be functional and there must be no device hanging the bus.

The SWRST Call function is defined as the following:

1. A Start command is sent by the I^2C bus master.
2. The reserved SWRST I^2C bus address 1001 011 with the R/$\overline{W}$ bit set to 0 (write) is sent by the I^2C bus master.
3. The TLC59108 device(s) acknowledge(s) after seeing the SWRST Call address 1001 0110 (96h) only. If the R/$\overline{W}$ bit is set to 1 (read), no acknowledge is returned to the I^2C bus master.
4. Once the SWRST Call address has been sent and acknowledged, the master sends two bytes with two specific values (SWRST data byte 1 and byte 2):
   (a) Byte1 = A5h: the TLC59108 acknowledges this value only. If byte 1 is not equal to A5h, the TLC59108 does not acknowledge it.
   (b) Byte 2 = 5Ah: the TLC59108 acknowledges this value only. If byte 2 is not equal to 5Ah, the TLC59108 does not acknowledge it.

   If more than two bytes of data are sent, the TLC59108 does not acknowledge any more.
5. Once the correct two bytes (SWRST data byte 1 and byte 2 only) have been sent and correctly acknowledged, the master sends a Stop command to end the SWRST Call. The TLC59108 then resets to the default value (power-up value) and is ready to be addressed again within the specified bus free time (t_{BUF}).

The I^2C bus master may interpret a non-acknowledge from the TLC59108 (at any time) as a SWRST Call Abort. The TLC59108 does not initiate a reset of its registers. This happens only when the format of the Start Call sequence is not correct.

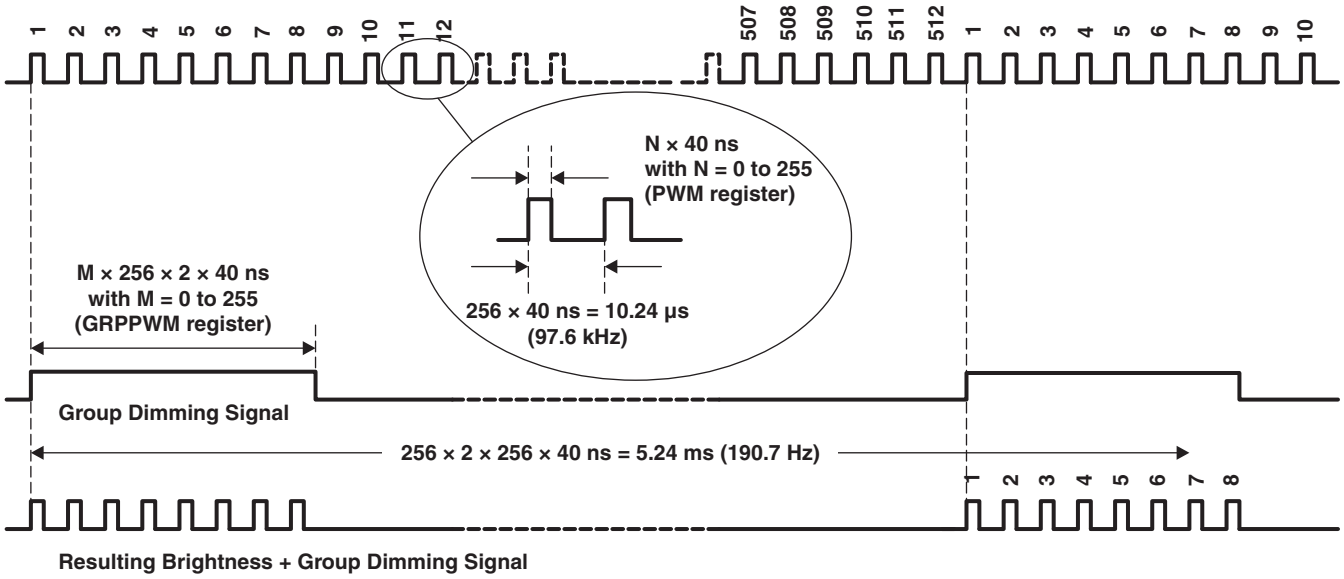
9.3.6 Individual Brightness Control With Group Dimming/Blinking

A 97-kHz fixed-frequency signal with programmable duty cycle (8 bits, 256 steps) is used to control the individual brightness for each LED.

On top of this signal, one of the following signals can be superimposed (this signal can be applied to the four LED outputs):

- A lower 190-Hz fixed-frequency signal with programmable duty cycle (8 bits, 256 steps) provides a global brightness control.
- A programmable frequency signal from 24 Hz to 1/10.73 s (8 bits, 256 steps) provides a global blinking control.

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NOTE: Minimum pulse width for LEDn brightness control is 40 ns.
Minimum pulse width for group dimming is 20.48 µs.
When M = 1 (GRPPWM register value), the resulting LEDn Brightness Control + Group Dimming signal has two pulses of the LED Brightness Control signal (pulse width = n × 40 ns, with n defined in the PWMx register).
This resulting Brightness + Group Dimming signal shows a resulting control signal with n = 4 (8 pulses).

Figure 7. Brightness and Group Dimming Signals

9.4 Device Functional Modes

Active Active mode occurs when one or more of the output channels is enabled.

Standby Standby mode occurs when all output channels are disabled. Standby mode may be entered via I^2C command or by pulling the $\overline{\text{RESET}}$ pin low.

9.5 Programming

9.5.1 Characteristics of the I^2C Bus

The I^2C bus is for two-way two-line communication between different devices or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pullup resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

9.5.1.1 Bit Transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the high period of the clock pulse as changes in the data line at this time are interpreted as control signals (see Figure 8).

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Programming (continued)

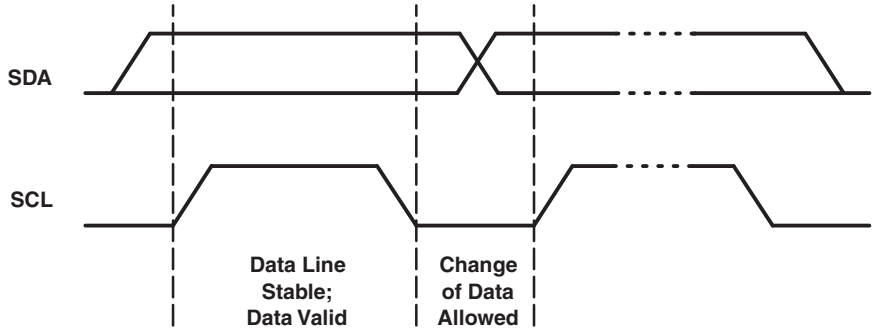


Figure 8. Bit Transfer

9.5.1.2 Start and Stop Conditions

Both data and clock lines remain high when the bus is not busy. A high-to-low transition of the data line while the clock is high is defined as the Start condition (S). A low-to-high transition of the data line while the clock is high is defined as the Stop condition (P) (see Figure 9).

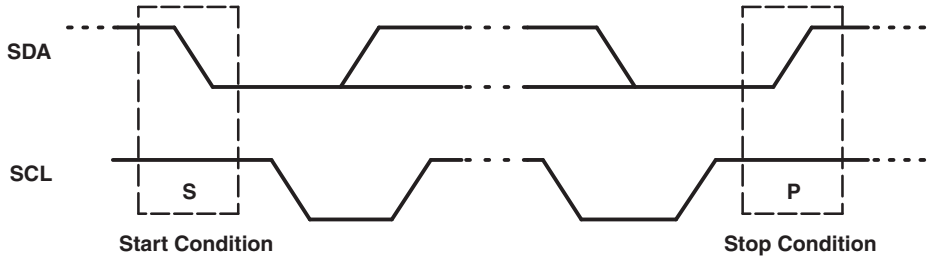


Figure 9. Start and Stop Conditions

9.5.2 System Configuration

A device generating a message is a transmitter; a device receiving is the receiver. The device that controls the message is the master and the devices which are controlled by the master are the slaves (see Figure 10).

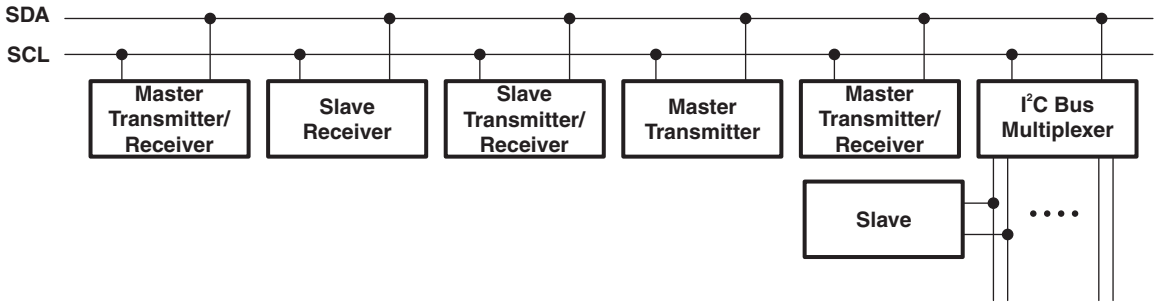


Figure 10. System Configuration

9.5.3 Acknowledge

The number of data bytes transferred between the Start and the Stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a high level put on the bus by the transmitter, whereas the master generates an extra acknowledge related clock pulse.

Programming (continued)

A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable low during the high period of the acknowledge related clock pulse; set-up time and hold time must be taken into account.

A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line high to enable the master to generate a Stop condition.

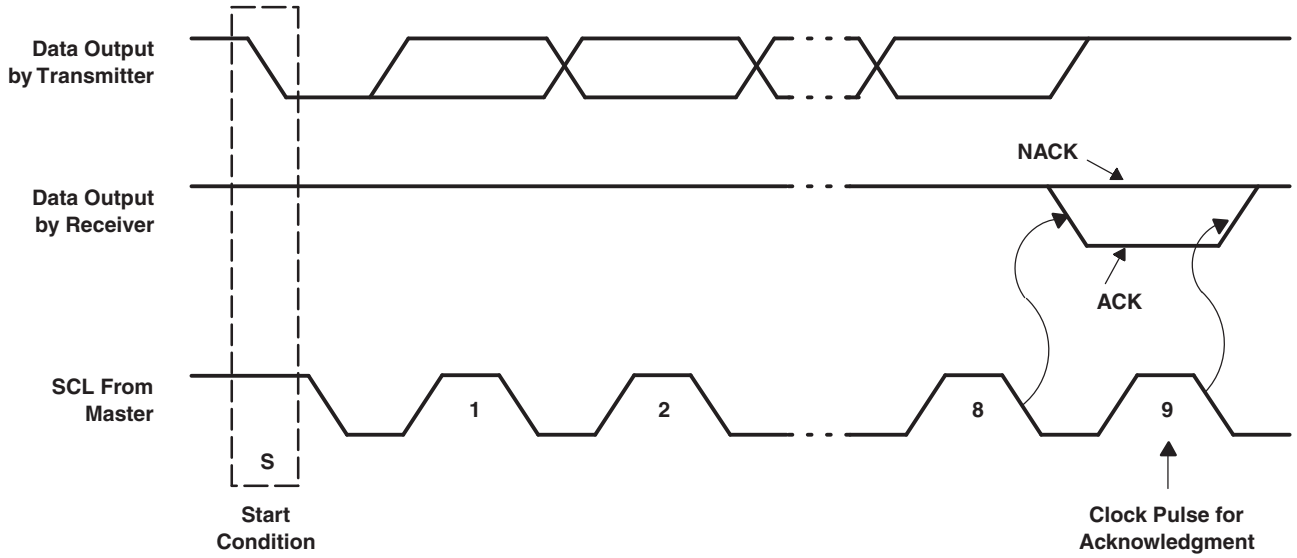


Figure 11. Acknowledge/Not Acknowledge on I²C Bus

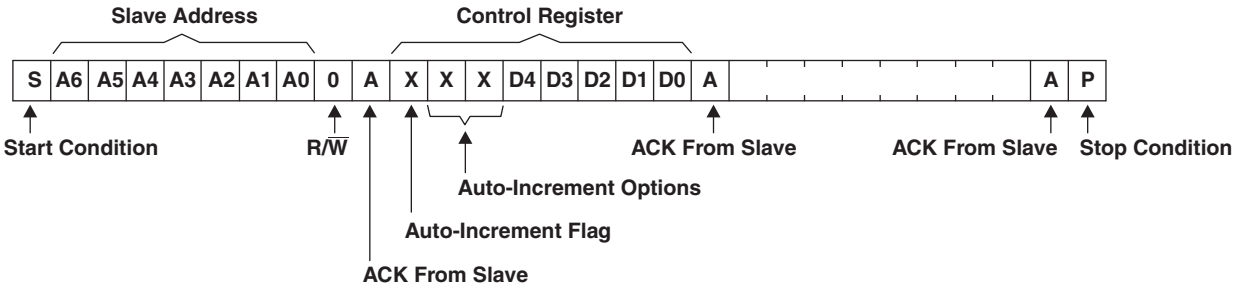
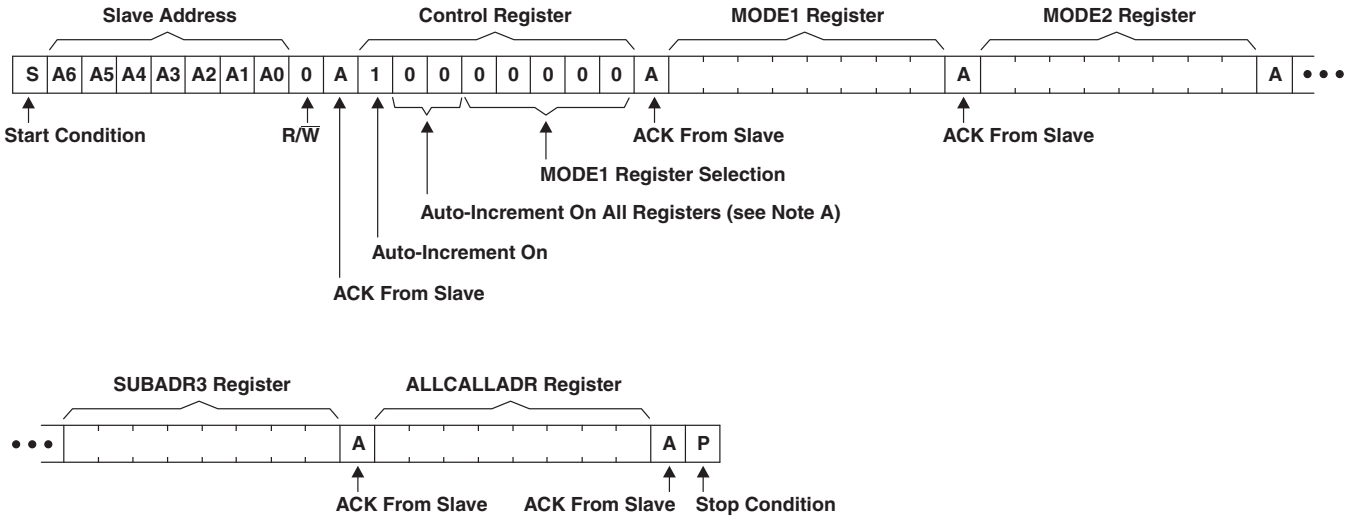


Figure 12. Write to a Specific Register

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Programming (continued)



A. See Table 4 for register definitions.

Figure 13. Write to All Registers Using Auto-Increment

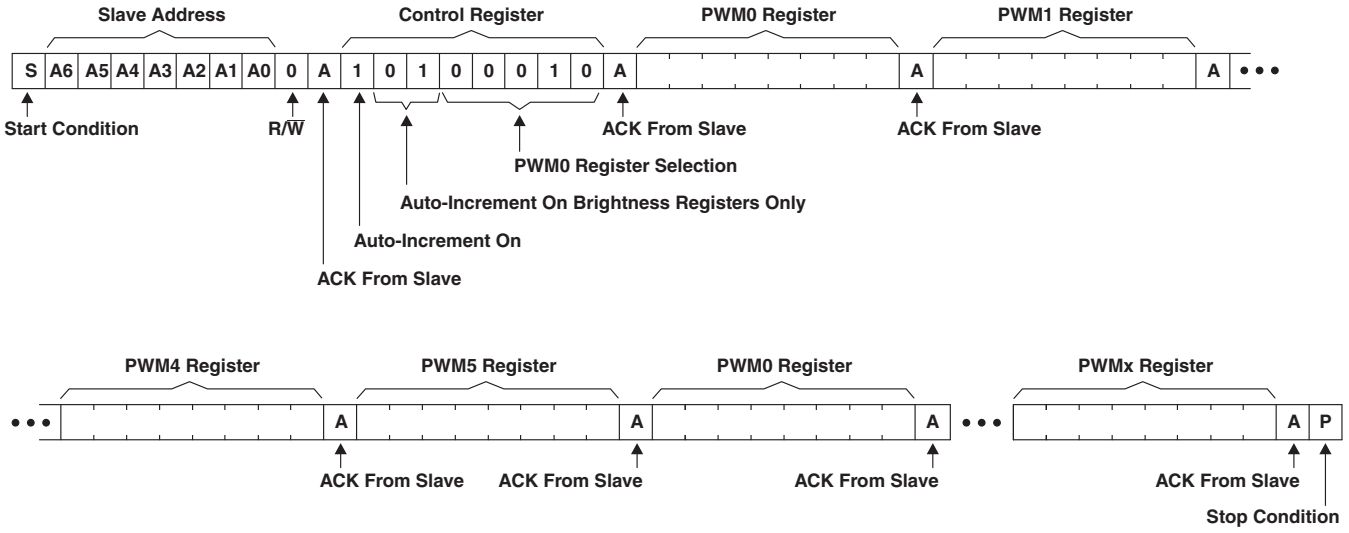


Figure 14. Multiple Writes to Individual Brightness Registers Using Auto-Increment

Programming (continued)

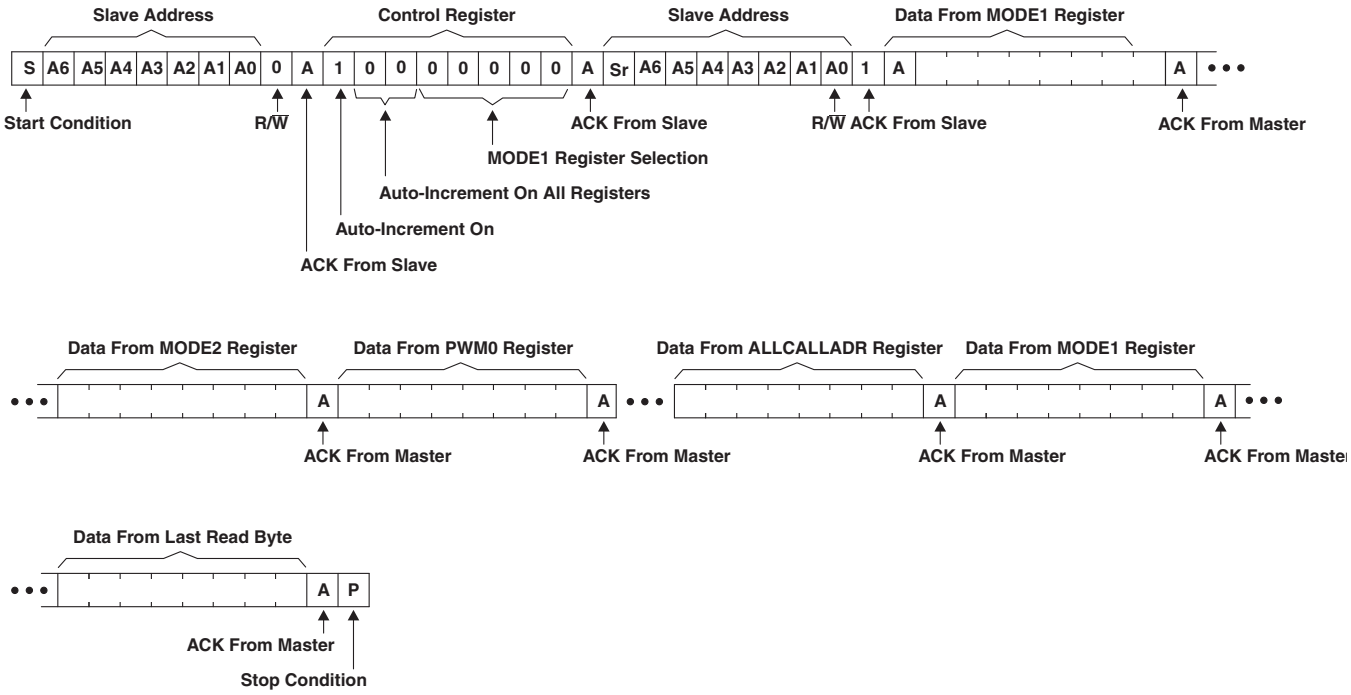
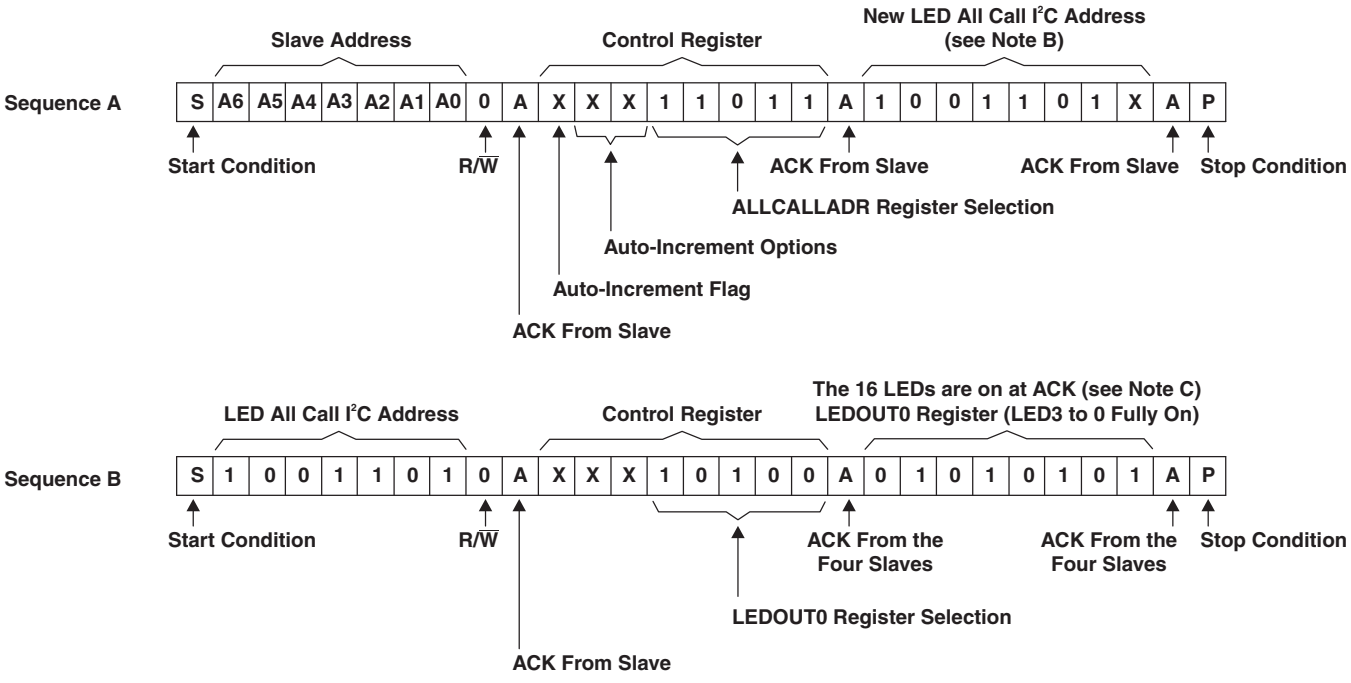


Figure 15. Read All Registers Auto-Increment



A. In this example, several TLC59108 devices are used, and the same Sequence A is sent to each of them.

B. The ALLCALL bit in the MODE1 register is equal to 1 for this example.

C. The OCH bit in the MODE2 register is equal to 1 for this example.

Figure 16. LED All Call I²C Bus Address Programming and LED All Call Sequence

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Programming (continued)

9.5.4 Device Address

Following a Start condition, the bus master must output the address of the slave it is accessing.

9.5.5 Regular I²C Bus Slave Address

The I²C bus slave address of the TLC59108 is shown in Figure 17. To conserve power, no internal pullup resistors are incorporated on the hardware-selectable address pins, and they must be pulled high or low. For buffer management purpose, a set of sector information data should be stored.

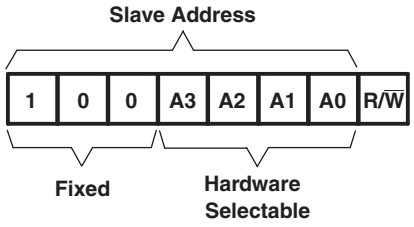


Figure 17. Slave Address

The last bit of the address byte defines the operation to be performed. When set to logic 1, a read operation is selected. When set to logic 0, a write operation is selected.

9.5.6 LED All Call I²C Bus Address

- Default power-up value (ALLCALLADR register): 90h or 1001 000
- Programmable through I²C bus (volatile programming)
- At power-up, LED All Call I²C bus address is enabled. TLC59108 sends an ACK when 90h (R/$\overline{W}$ = 0) or 91h (R/$\overline{W}$ = 1) is sent by the master.

See *LED All Call I²C Bus Address Register (ALLCALLADR)* for more detail.

NOTE

The default LED All Call I²C bus address (90h or 1001 000) must not be used as a regular I²C bus slave address since this address is enabled at power-up. All the TLC59108 devices on the I²C bus acknowledge the address if sent by the I²C bus master.

9.5.7 LED Sub Call I²C Bus Address

- Three different I²C bus address can be used
- Default power-up values:
  - SUBADR1 register: 92h or 1001 001
  - SUBADR2 register: 94h or 1001 010
  - SUBADR3 register: 98h or 1001 100
- Programmable through I²C bus (volatile programming)
- At power-up, Sub Call I²C bus address is disabled. TLC59108 does not send an ACK when 92h (R/$\overline{W}$ = 0) or 93h (R/$\overline{W}$ = 1) or 94h (R/$\overline{W}$ = 0) or 95h (R/$\overline{W}$ = 1) or 98h (R/$\overline{W}$ = 0) or 99h (R/$\overline{W}$ = 1) is sent by the master.

See *I²C Bus Subaddress Registers 1 to 3 (SUBADR1 to SUBADR3)* for more detail.

NOTE

The default LED Sub Call I²C bus address may be used as a regular I²C bus slave address as long as they are disabled.

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Programming (continued)

9.5.8 Software Reset I²C Bus Address

The address shown in Figure 18 is used when a reset of the TLC59108 needs to be performed by the master. The software reset address (SWRST Call) must be used with R/$\overline{W}$ = 0. If R/$\overline{W}$ = 1, the TLC59108 does not acknowledge the SWRST. See *Software Reset* for more detail.

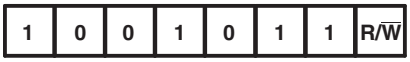


Figure 18. Software Reset Address

NOTE

The Software Reset I²C bus address is reserved address and cannot be use as regular I²C bus slave address or as an LED All Call or LED Sub Call address.

9.5.9 Control Register

Following the successful acknowledgment of the slave address, LED All Call address or LED Sub Call address, the bus master sends a byte to the TLC59108, which is stored in the Control register. The lowest 5 bits are used as a pointer to determine which register is accessed (D[4:0]). The highest 3 bits are used as Auto-Increment flag and Auto-Increment options (AI[2:0]).

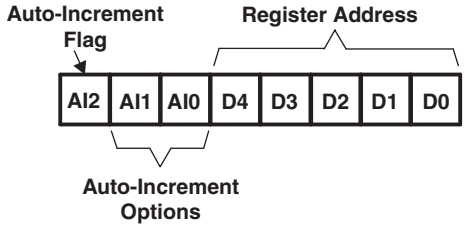


Figure 19. Control Register

When the Auto-Increment flag is set (AI2 = logic 1), the five low order bits of the Control register are automatically incremented after a read or write. This allows the user to program the registers sequentially. Four different types of Auto-Increment are possible, depending on AI1 and AI0 values.

Table 3. Auto-Increment Options

AI2	AI1	AI0	DESCRIPTION
0	0	0	No auto-increment
1	0	0	Auto-increment for all registers. D[4:0] roll over to 0 0000 after the last register (1 0001) is accessed.
1	0	1	Auto-increment for individual brightness registers only. D[4:0] roll over to 0 0010 after the last register (0 1001) is accessed.
1	1	0	Auto-increment for global control registers only. D[4:0] roll over to 0 1010 after the last register (0 1011) is accessed.
1	1	1	Auto-increment for individual and global control registers only. D[4:0] roll over to 0 0010 after the last register (0 1011) is accessed.

NOTE

Other combinations not shown in Table 3. (AI[2:0] = 001, 010 and 011) are reserved and must not be used for proper device operation.

IREF and EFLAG not included in Auto-Increment

AI[2:0] = 000 is used when the same register must be accessed several times during a single I²C bus communication, for example, changes the brightness of a single LED. Data is overwritten each time the register is accessed during a write operation.

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AI[2:0] = 100 is used when all the registers must be sequentially accessed, for example, power-up programming.

AI[2:0] = 101 is used when the four LED drivers must be individually programmed with different values during the same I^2C bus communication, for example, changing color setting to another color setting.

AI[2:0] = 110 is used when the LED drivers must be globally programmed with different settings during the same I^2C bus communication, for example, global brightness or blinking change.

AI[2:0] = 111 is used when individually and global changes must be performed during the same I^2C bus communication, for example, changing color and global brightness at the same time.

Only the 5 least significant bits D[4:0] are affected by the AI[2:0] bits.

When the Control register is written, the register entry point determined by D[4:0] is the first register that is addressed (read or write operation), and can be anywhere between 0 0000 and 1 0001 (as defined in Table 4). When AI[2] = 1, the Auto-Increment flag is set and the rollover value at which the point where the register increment stops and goes to the next one is determined by AI[2:0]. See Table 3 for rollover values. For example, if the Control register = 1110 1100 (ECh), then the register addressing sequence is (in hex):

0C → ... → 11 → 00 → ... → 0B → 02 → ... → 0B → 02 → ... as long as the master keeps sending or reading data.

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9.6 Register Maps

9.6.1 Register Descriptions

Table 4 describes the registers in the TLC59108.

Table 4. Register Descriptions

REGISTER NUMBER (HEX)	NAME	ACCESS (1)	DESCRIPTION
00	MODE1	R/W	Mode 1
01	MODE2	R/W	Mode 2
02	PWM0	R/W	Brightness control LED0
03	PWM1	R/W	Brightness control LED1
04	PWM2	R/W	Brightness control LED2
05	PWM3	R/W	Brightness control LED3
06	PWM4	R/W	Brightness control LED4
07	PWM5	R/W	Brightness control LED5
08	PWM6	R/W	Brightness control LED6
09	PWM7	R/W	Brightness control LED7
0A	GRPPWM	R/W	Group duty cycle control
0B	GRPFREQ	R/W	Group frequency
0C	LEDOUT0	R/W	LED output state 0
0D	LEDOUT1	R/W	LED output state 1
0E	SUBADR1	R/W	I^2C bus subaddress 1
0F	SUBADR2	R/W	I^2C bus subaddress 2
10	SUBADR3	R/W	I^2C bus subaddress 3
11	ALLCALLADR	R/W	LED All Call I^2C bus address
12	IREF	R/W	IREF configuration
13	EFLAG	R	Error flag

(1) R = read, W = write

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9.6.1.1 Mode Register 1 (MODE1)

Table 5 describes Mode Register 1.

Table 5. MODE1 – Mode Register 1 (Address 00h) Bit Description

BIT	SYMBOL	ACCESS (1)	VALUE	DESCRIPTION
7	AI2	R	0 (2)	Register Auto-Increment disabled
			1	Register Auto-Increment enabled
6	AI1	R	0 (2)	Auto-Increment bit 1 = 0
			1	Auto-Increment bit 1 = 1
5	AI0	R	0 (2)	Auto-Increment bit 0 = 0
			1	Auto-Increment bit 0 = 1
4	OSC	R/W	0	Normal mode (3)
			1 (2)	Oscillator off (4).
3	SUB1	R/W	0 (2)	Device does not respond to I^2C bus subaddress 1.
			1	Device responds to I^2C bus subaddress 1.
2	SUB2	R/W	0 (2)	Device does not respond to I^2C bus subaddress 2.
			1	Device responds to I^2C bus subaddress 2.
1	SUB3	R/W	0 (2)	Device does not respond to I^2C bus subaddress 3.
			1	Device responds to I^2C bus subaddress 3.
0	ALLCALL	R/W	0	Device does not respond to LED All Call I^2C bus address.
			1 (2)	Device responds to LED All Call I^2C bus address.

(1) R = read, W = write
(2) Default value
(3) Requires 500 µs maximum for the oscillator to be up and running once SLEEP bit has been set to logic 1. Timings on LED outputs are not guaranteed if PWMx, GRPPWM, or GRPFREQ registers are accessed within the 100 µs window.
(4) No blinking or dimming is possible when the oscillator is off.

9.6.1.2 Mode Register 2 (MODE2)

Table 6 describes Mode Register 2.

Table 6. MODE2 – Mode Register 2 (Address 01h) Bit Description

BIT	SYMBOL	ACCESS (1)	VALUE	DESCRIPTION
7	EFCLR	R/W	0 (2)	Enable error status flag
			1	Clear error status flag
6		R	0 (2)	Reserved
5	DMBLNK	R/W	0 (2)	Group control = dimming
			1	Group control = blinking
4		R	0 (2)	Reserved
3	OCH	R/W	0 (2)	Outputs change on Stop command (3)
			1	Outputs change on ACK
2:0		R	000 (2)	Reserved

(1) R = read, W = write
(2) Default value
(3) Change of the outputs at the Stop command allows synchronizing outputs of more than one TLC59108. Applicable to registers from 02h (PWM0) to 0Dh (LEDOUT) only.

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9.6.1.3 Brightness Control Registers 0 to 7 (PWM0 to PWM7)

Table 7 describes Brightness Control Registers 0 to 7.

Table 7. PWM0 to PWM7 – PWM Registers 0 to 7 (Address 02h to 09h) Bit Description

ADDRESS	REGISTER	BIT	SYMBOL	ACCESS (1)	VALUE	DESCRIPTION
02h	PWM0	7:0	IDC0[7:0]	R/W	0000 0000 (2)	PWM0 individual duty cycle
03h	PWM1	7:0	IDC1[7:0]	R/W	0000 0000 (2)	PWM1 individual duty cycle
04h	PWM2	7:0	IDC2[7:0]	R/W	0000 0000 (2)	PWM2 individual duty cycle
05h	PWM3	7:0	IDC3[7:0]	R/W	0000 0000 (2)	PWM3 individual duty cycle
06h	PWM4	7:0	IDC4[7:0]	R/W	0000 0000 (2)	PWM4 individual duty cycle
07h	PWM5	7:0	IDC5[7:0]	R/W	0000 0000 (2)	PWM5 individual duty cycle
08h	PWM6	7:0	IDC6[7:0]	R/W	0000 0000 (2)	PWM6 individual duty cycle
09h	PWM7	7:0	IDC7[7:0]	R/W	0000 0000 (2)	PWM7 individual duty cycle

(1) R = read, W = write
(2) Default value

A 97-kHz fixed frequency signal is used for each output. Duty cycle is controlled through 256 linear steps from 00h (0% duty cycle = LED output off) to FFh (99.6% duty cycle = LED output at maximum brightness). Applicable to LED outputs programmed with LDRx = 10 or 11 (LEDOUT0 and LEDOUT1 registers).

Duty cycle = IDCn[7:0] / 256

9.6.1.4 Group Duty Cycle Control Register (GRPPWM)

Table 8 describes the Group Duty Cycle Control Register.

Table 8. GRPPWM – Group Brightness Control Register (Address 0Ah) Bit Description

ADDRESS	REGISTER	BIT	SYMBOL	ACCESS (1)	VALUE	DESCRIPTION
0Ah	GRPPWM	7:0	GDC0[7:0]	R/W	1111 1111 (2)	GRPPWM register

(1) R = read, W = write
(2) Default value

When the DMBLNK bit (MODE2 register) is programmed with logic 0, a 190-Hz fixed-frequency signal is superimposed with the 97-kHz individual brightness control signal. GRPPWM is then used as a global brightness control, allowing the LED outputs to be dimmed with the same value. The value in GRPFREQ is then a Don't care.

General brightness for the eight outputs is controlled through 256 linear steps from 00h (0% duty cycle = LED output off) to FFh (99.6% duty cycle = maximum brightness). Applicable to LED outputs programmed with LDRx = 11 (LEDOUT0 and LEDOUT1 registers).

When DMBLNK bit is programmed with logic 1, the GRPPWM and GRPFREQ registers define a global blinking pattern, where GRPFREQ defines the blinking period (from 24 Hz to 10.73 s) and GRPPWM defines the duty cycle (ON/OFF ratio in %).

Duty cycle = GDC0[7:0] / 256

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9.6.1.5 Group Frequency Register (GRPFREQ)

Table 9 describes the Group Frequency Register.

Table 9. GRPFREQ – Group Frequency Register (Address 0Bh) Bit Description

ADDRESS	REGISTER	BIT	SYMBOL	ACCESS (1)	VALUE	DESCRIPTION
0Bh	GRPFREQ	7:0	GFRQ[7:0]	R/W	0000 0000 (2)	GRPFREQ register

(1) R = read, W = write
(2) Default value

GRPFREQ is used to program the global blinking period when the DMBLNK bit (MODE2 register) is equal to 1. Value in this register is a Don't care when DMBLNK = 0. Applicable to LED output programmed with LDRx = 11 (LEDOUT0 and LEDOUT1 registers).

Blinking period is controlled through 256 linear steps from 00h (41 ms, frequency 24 Hz) to FFh (10.73 s).

Global blinking period (seconds) = (GFRQ[7:0] + 1) / 24

9.6.1.6 LED Driver Output State Registers (LEDOUT0, LEDOUT1)

Table 10 describes LED Driver Output State Registers 0 and 1.

Table 10. LEDOUT0 and LEDOUT1 – LED Driver Output State Registers (Address 0Ch and 0Dh) Bit Description

ADDRESS	REGISTER	BIT	SYMBOL	ACCESS (1)	VALUE	DESCRIPTION
0Ch	LEDOUT0	7:6	LDR3[1:0]	R/W	00 (2)	LED3 output state control
		5:4	LDR2[1:0]	R/W	00 (2)	LED2 output state control
		3:2	LDR1[1:0]	R/W	00 (2)	LED1 output state control
		1:0	LDR0[1:0]	R/W	00 (2)	LED0 output state control
0Dh	LEDOUT1	7:6	LDR7[1:0]	R/W	00 (2)	LED7 output state control
		5:4	LDR6[1:0]	R/W	00 (2)	LED6 output state control
		3:2	LDR5[1:0]	R/W	00 (2)	LED5 output state control
		1:0	LDR4[1:0]	R/W	00 (2)	LED4 output state control

(1) R = read, W = write
(2) Default value

LDRx = 00: LED driver x is off (default power-up state).

LDRx = 01: LED driver x is fully on (individual brightness and group dimming/blinking not controlled).

LDRx = 10: LED driver x is individual brightness can be controlled through its PWMx register.

LDRx = 11: LED driver x is individual brightness and group dimming/blinking can be controlled through its PWMx register and the GRPPWM registers.

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9.6.1.7 I²C Bus Subaddress Registers 1 to 3 (SUBADR1 to SUBADR3)

Table 11 describes I²C Bus Subaddress Registers 1 to 3.

Table 11. SUBADR1 to SUBADR3 – I²C Bus Subaddress Registers 1 to 3 (Address 0Eh to 10h) Bit Description

ADDRESS	REGISTER	BIT	SYMBOL	ACCESS (1)	VALUE	DESCRIPTION
0Eh	SUBADR1	7:5	A1[7:5]	R	100 (2)	Reserved
		4:1	A1[4:1]	R/W	1001 (2)	I²C bus subaddress 1
		0	A1[0]	R	0 (2)	Reserved
0Fh	SUBADR2	7:5	A2[7:1]	R	100 (2)	Reserved
		4:1	A2[4:1]	R/W	1010 (2)	I²C bus subaddress 2
		0	A2[0]	R	0 (2)	Reserved
10h	SUBADR3	7:5	A3[7:1]	R	100 (2)	Reserved
		4:1	A3[4:1]	R/W	1100 (2)	I²C bus subaddress 3
		0	A3[0]	R	0 (2)	Reserved

(1) R = read, W = write
(2) Default value

Subaddresses are programmable through the I²C bus. Default power-up values are 92h, 94h, 98h. The TLC59108 does not acknowledge these addresses immediately after power-up (the corresponding SUBx bit in MODE1 register is equal to 0).

Once subaddresses have been programmed to valid values, the SUBx bits (MODE1 register) must be set to 1 to allows the device to acknowledge these addresses.

Only the 7 MSBs representing the I²C bus subaddress are valid. The LSB in SUBADRx register is a read-only bit (0).

When SUBx is set to 1, the corresponding I²C bus subaddress can be used during either an I²C bus read or write sequence.

9.6.1.8 LED All Call I²C Bus Address Register (ALLCALLADR)

Table 12 describes the LED All Call I²C Bus Address Register.

Table 12. ALLCALLADR – LED All Call I²C Bus Address Register (Address 11h) Bit Description

ADDRESS	REGISTER	BIT	SYMBOL	ACCESS (1)	VALUE	DESCRIPTION
11h	ALLCALLADR	7:5	AC[7:5]	R	100 (2)	Reserved
		4:1	AC[4:1]	R/W	1000 (2)	All Call I²C bus address register
		0	AC[0]	R	0 (2)	Reserved

(1) R = read, W = write
(2) Default value

The LED All Call I²C bus address allows all the TLC59108 devices in the bus to be programmed at the same time (ALLCALL bit in register MODE1 must be equal to 1, which is the power-up default state). This address is programmable through the I²C bus and can be used during either an I²C bus read or write sequence. The register address can also be programmed as a Sub Call.

Only the 7 MSBs representing the All Call I²C bus address are valid. The LSB in ALLCALLADR register is a read-only bit (0).

If ALLCALL bit = 0, the device does not acknowledge the address programmed in register ALLCALLADR.

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9.6.1.9 Output Gain Control Register (IREF)

Table 13 describes the Output Gain Control Register.

Table 13. IREF – Output Gain Control Register (Address 12h) Bit Description

ADDRESS	REGISTER	BIT	SYMBOL	ACCESS (1)	VALUE	DESCRIPTION
12h	IREF	7	CM	R/W	1 (2)	High/low current multiplier
		6	HC	R/W	1 (2)	Subcurrent
		5:0	CC[5:0]	R/W	11 1111 (2)	Current multiplier

(1) R = read, W = write
(2) Default value

I_{REF} determines the voltage gain (VG), which affects the voltage at the R_{EXT} terminal and indirectly the reference current (I_{REF}) flowing through the external resistor at terminal R_{EXT}. Bit 0 is the Current Multiplier (CM) bit, which determines the ratio $I_{OUT,target}/I_{ref}$. Each combination of VG and CM sets a Current Gain (CG).

- VG: the relationship between {HC,CC[0:5]} and the voltage gain is calculated as shown below:
  $VG = (1 + HC) \times (1 + D/64) / 4$
  $D = CC0 \times 2^5 + CC1 \times 2^4 + CC2 \times 2^3 + CC3 \times 2^2 + CC4 \times 2^1 + CC5 \times 2^0$
  Where HC is 1 or 0, and D is the binary value of CC[0:5]. So, the VG could be regarded as a floating-point number with 1-bit exponent HC and 6-bit mantissa CC[0:5]. {HC,CC[0:5]} divides the programmable voltage gain VG into 128 steps and two sub-bands:
  Low voltage sub-band (HC = 0): VG = 1/4 to 127/256, linearly divided into 64 steps
  High voltage sub-band (HC = 1): VG = 1/2 to 127/128, linearly divided into 64 steps
- CM: In addition to determining the ratio $I_{OUT,target}/I_{ref}$, CM limits the output current range.
  High Current Multiplier (CM = 1): $I_{OUT,target}/I_{ref} = 15$, suitable for output current range I_{OUT} = 10 mA to 120 mA.
  Low Current Multiplier (CM = 0): $I_{OUT,target}/I_{ref} = 5$, suitable for output current range I_{OUT} = 5 mA to 40 mA
- CG: The total Current Gain is defined as the following.
  $V_{REXT} = 1.26\ V \times VG$
  $I_{ref} = V_{REXT}/R_{ext}$, if the external resistor, R_{ext}, is connected to ground.
  $I_{OUT,target} = I_{ref} \times 15 \times 3^{CM-1} = 1.26\ V/R_{ext} \times VG \times 15 \times 3^{CM-1} = (1.26\ V/R_{ext} \times 15) \times CG$
  $CG = VG \times 3^{CM-1}$
  Therefore, CG = (1/12) to (127/128), and it is divided into 256 steps. If CG = 127/128 = 0.992, the $I_{OUT,target}$-R_{ext}.

Examples

- I_{REF} Code {CM, HC, CC[0:5]} = {1,1,111111}
  VG = 127/128 = 0.992 and $CG = VG \times 3^0 = VG = 0.992$
- I_{REF} Code {CM, HC, CC[0:5]} = {1,1,000000}
  VG = (1 + 1) × (1 + 0/64)/4 = 1/2 = 0.5, and CG = 0.5
- I_{REF} Code {CM, HC, CC[0:5]} = {0,0,000000}
  VG = (1 + 0) × (1 + 0/64)/4 = 1/4, and $CG = (1/4) \times 3^{-1} = 1/12$

After power on, the default value of the Configuration Code {CM, HC, CC[0:5]} is {1,1,111111}. Therefore, VG = CG = 0.992. The relationship between the Configuration Code and the Current Gain is shown in Figure 20.

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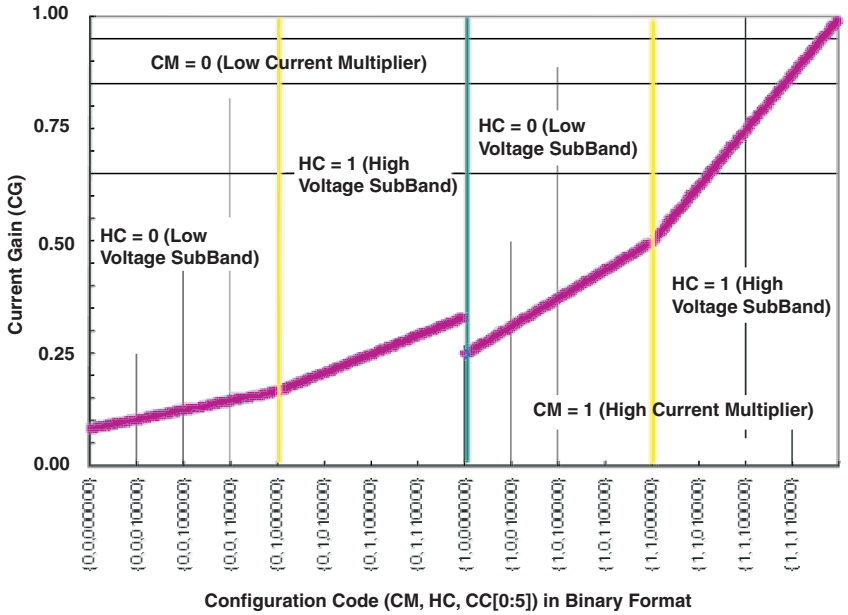


Figure 20. Current Gain vs Configuration Code

9.6.1.10 Error Flags Registers (EFLAG)

Table 14 describes the Error Flags Register.

Table 14. EFLAG – Error Flags Register (Address 13h) Bit Description

ADDRESS	REGISTER	BIT	SYMBOL	ACCESS (1)	VALUE	DESCRIPTION
13h	EFLAG	7:0	EFLAG[7:0]	R	1111 1111 (2)	Error flag status by channel

(1) R = read, W = write
(2) Default value

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10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

10.1.1 Driver Output

10.1.1.1 Constant Current Output

In LED display applications, TLC59108 provides nearly no current variations from channel to channel and from device to device. While $I_{OUT} \leq 100$ mA, the maximum current skew between channels is less than ±3% and less than ±6% between devices.

10.1.1.2 Adjusting Output Current

TLC59108 scales up the reference current (I_{ref}) set by the external resistor (R_{ext}) to sink the output current (I_{out}) at each output port. The following formulas can be used to calculate the target output current $I_{OUT,target}$ in the saturation region:

$$V_{REXT} = 1.26\ V \times VG \quad (1)$$

$$I_{ref} = V_{REXT}/R_{ext}, \text{ if another end of the external resistor } R_{ext} \text{ is connected to ground} \quad (2)$$

$$I_{OUT,target} = I_{ref} \times 15 \times 3^{CM-1} \quad (3)$$

Where R_{ext} is the resistance of the external resistor connected to the R_{EXT} terminal, and V_{REXT} is the voltage of R_{EXT}, which is controlled by the programmable voltage gain (VG), which is defined by the Configuration Code. The Current Multiplier (CM) determines that the ratio $I_{OUT,target}/I_{ref}$ is 15 or 5. After power on, the default value of VG is 127/128 = 0.992, and the default value of CM is 1, so that the ratio $I_{OUT,target}/I_{ref} = 15$. Based on the default VG and CM.

$$V_{REXT} = 1.26\ V \times 127/128 = 1.25\ V \quad (4)$$

$$I_{OUT,target} = (1.25\ V/R_{ext}) \times 15 \quad (5)$$

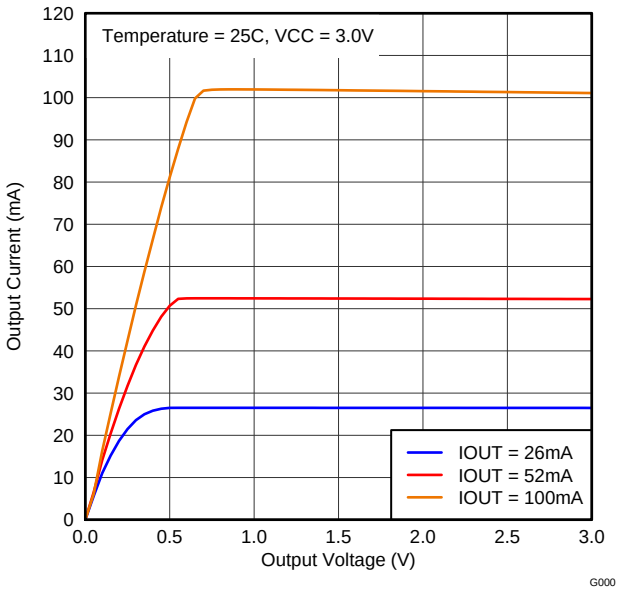


Figure 21. I_{OUT} vs V_{OUT}

Application Information (continued)

10.1.2 TLC59108 and TLC59108F Differences

The TLC59108 and TLC59108F are similar devices with the difference being the output structure. The TLC59108 has 8 constant-current outputs while the TLC59108F has 8 open drain outputs. The REXT is used to program the current on the TLC59108 for all channels. The in-line resistors on the OUT pins are used in conjunction with the VLED to set the currents on each TLC59108F channel. Since the resistors are unique for each output, the currents can be set by output by changing the resistor value.

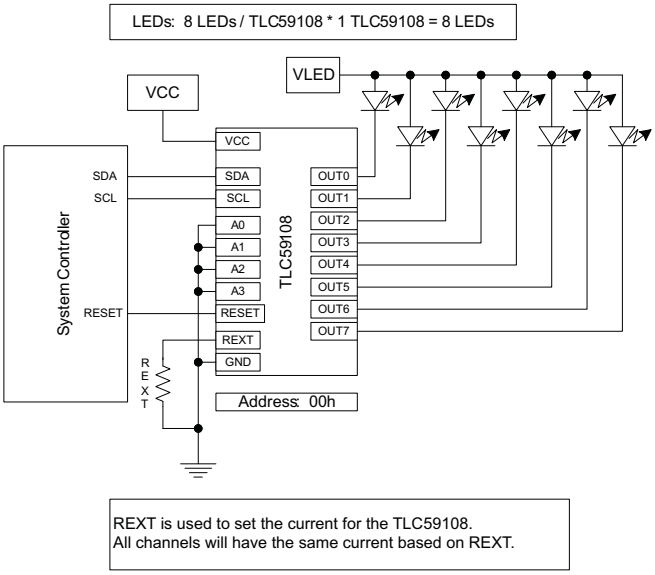


Figure 22. TLC59108 One Driver

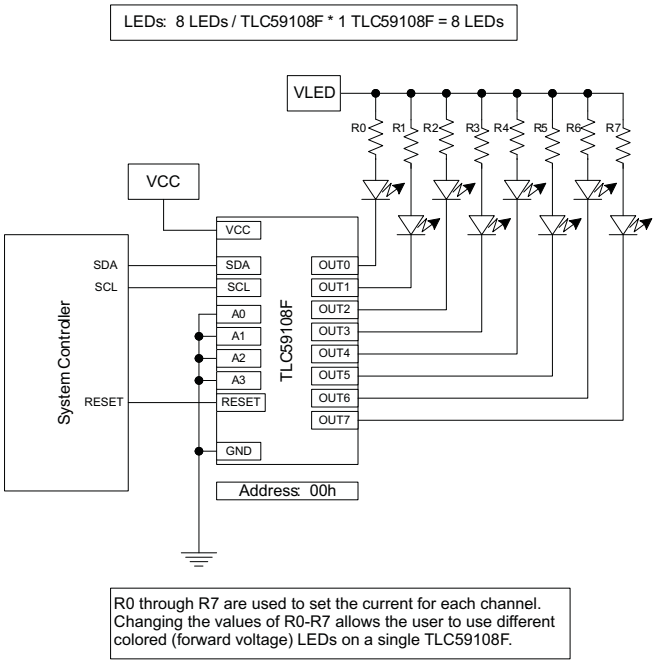


Figure 23. TLC59108F One Driver

10.2 Typical Application

10.2.1 Parallel Outputs

The TLC59108 outputs can be wired in parallel to increase the current per LED string.

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Typical Application (continued)

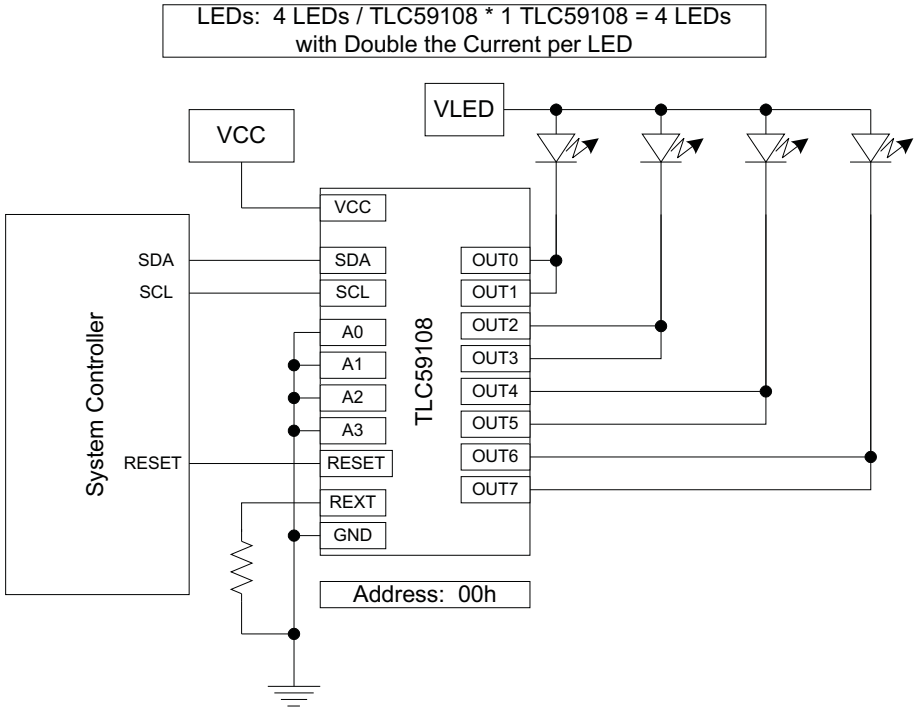


Figure 24. Parallel Channels

10.2.1.1 Design Requirements

Set the LED current to 50 mA while the IREF register is at the default value (CG = 0.992).

10.2.1.2 Detailed Design Procedure

The goal of this design is to set the LED current to 50 mA. Because there are two outputs in parallel, the LED current should actually be set to 25 mA. With the IREF register at the default value:

$$I_{OUT,target} = (1.25\ V / R_{EXT}) \times 15 \quad (6)$$

Using this equation, the appropriate R_{EXT} is calculated to be 750 Ω.

10.2.1.3 Application Curve

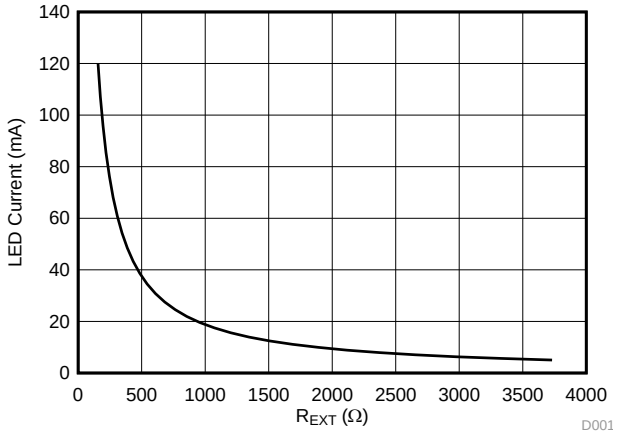


Figure 25. LED Current vs R_{EXT}Resistor

Typical Application (continued)

10.2.2 Multiple Devices

This drawing is an example of using the TLC59108 in a system requiring up to 48 LED strings. The TLC59108 drivers share a single I^2C bus. The address pins are set high or low to enable the drivers to be independently accessed (all can be written in parallel through the ALLCALLADR function). The REXT pins are each tied to ground through a programming resistor. Since the devices are independent the resistors on the REXT pins can be of different values allowing multi-color displays.

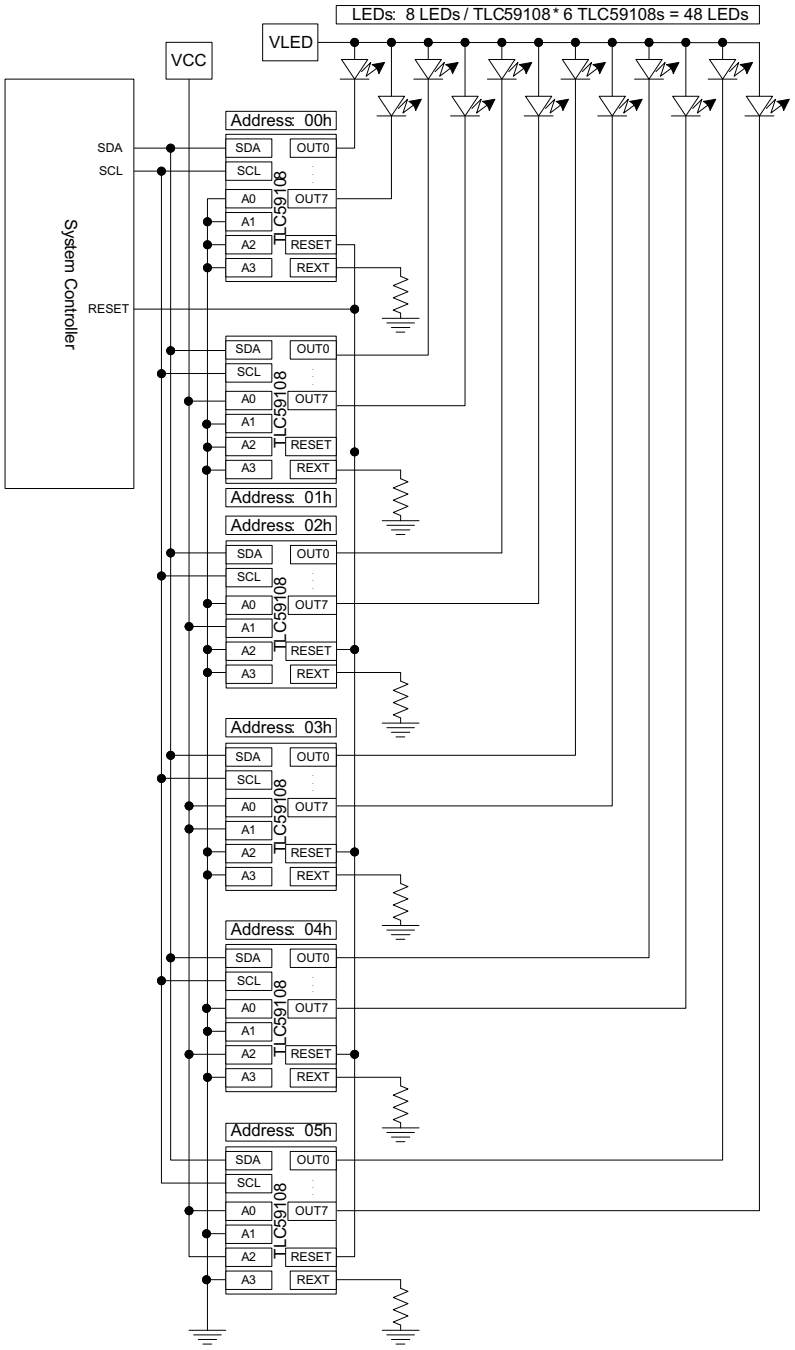


Figure 26. Six Drivers

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11 Power Supply Recommendations

TLC59108 is designed to operate from a V_{CC} range of 3 V to 5.5 V. The system must also include the VLED power supply. VLED must be greater than the forward voltage of the LED. However, VLED must be set such that V_O does not exceed 17 V.

12 Layout

12.1 Layout Guidelines

The I^2C signals (SDA / SCL) should be kept away from potential noise sources.

The traces carrying power through the LEDs should be wide enough to handle the necessary current.

All LED current passes through the device and into the ground node. There must be a strong connection between the device ground and the circuit board ground. For the RGY package, the thermal pad should be connected to the ground to help dissipate heat.

12.2 Layout Examples

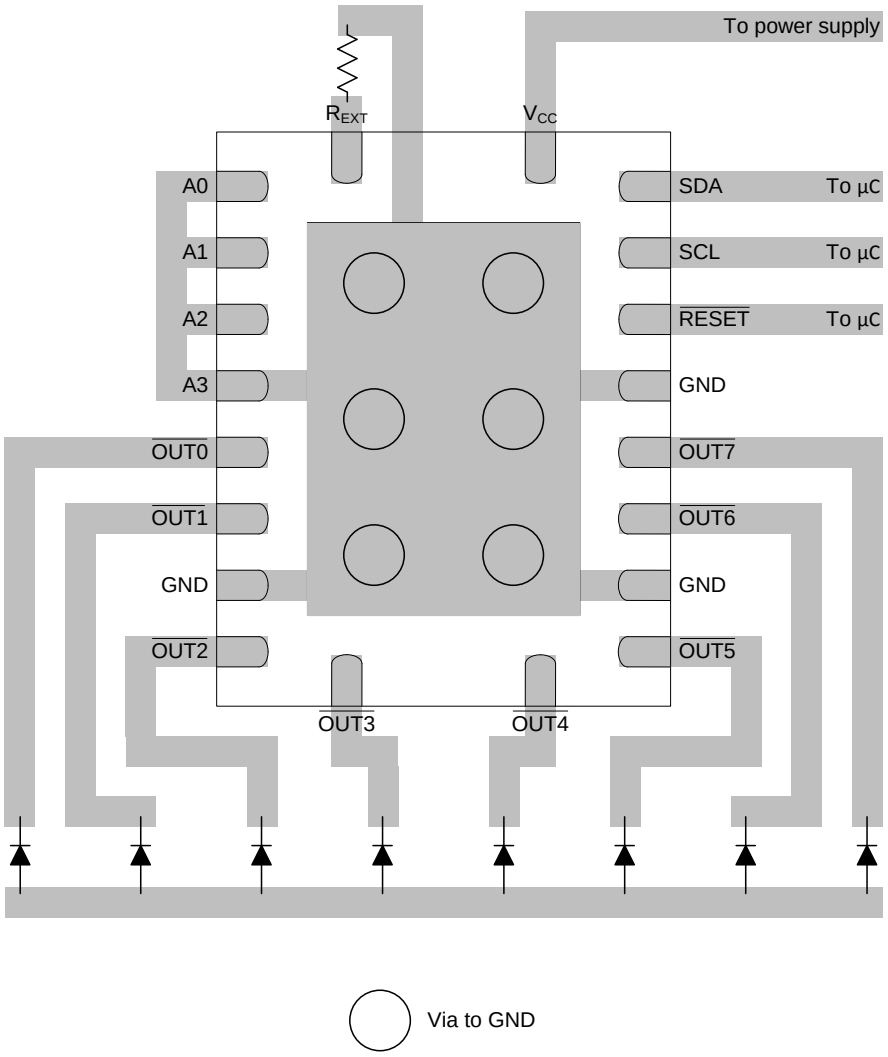


Figure 27. Layout Example for RGY Package

Layout Examples (continued)

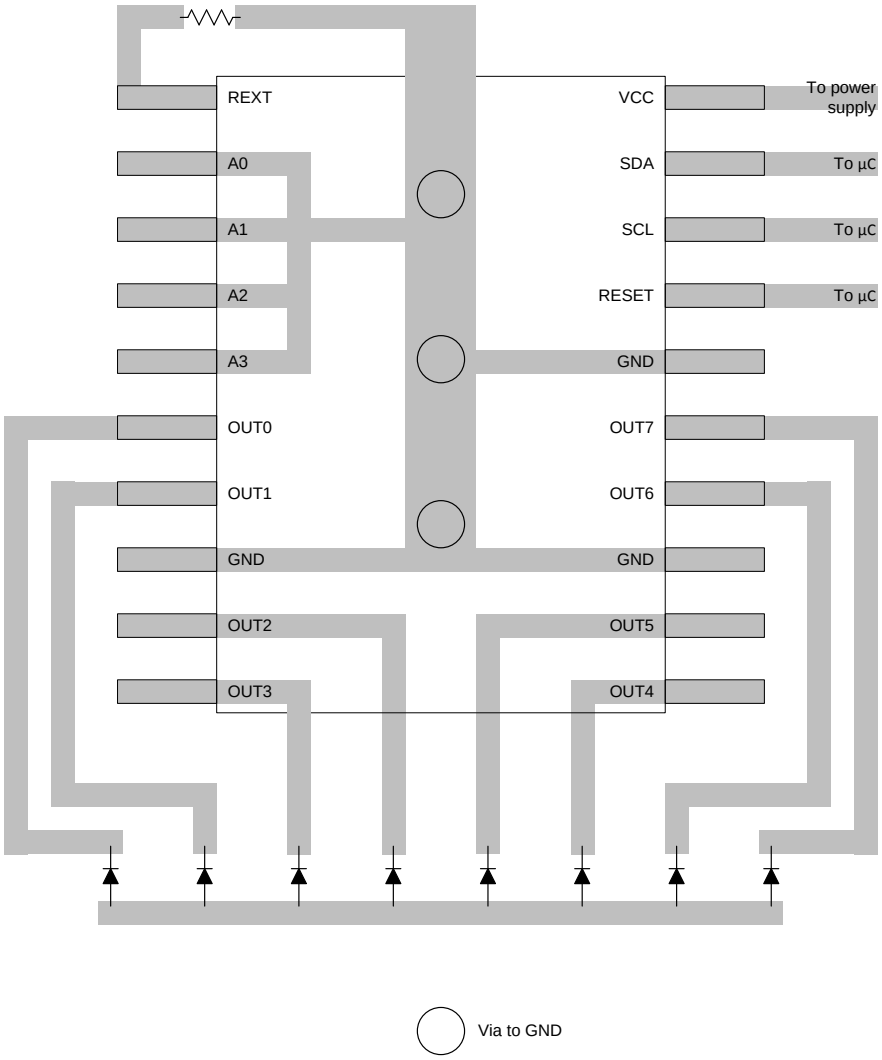


Figure 28. Layout Example for PW Package

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13 Device and Documentation Support

13.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.2 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

13.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLC59108IPWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	Y59108	Samples
TLC59108IRGYR	ACTIVE	VQFN	RGY	20	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	Y59108	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

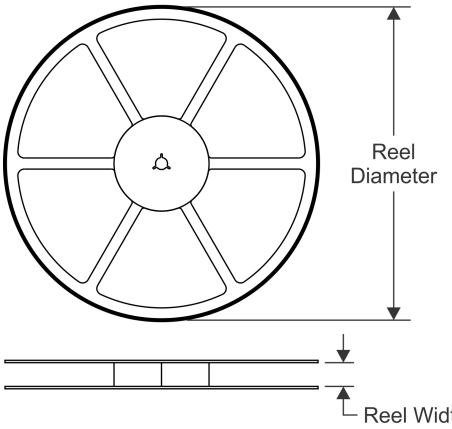
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

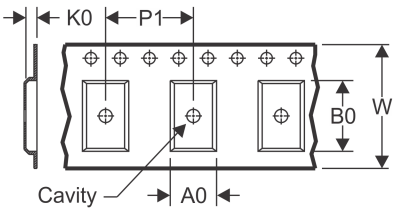
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

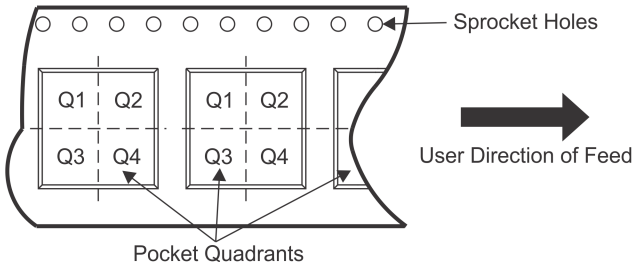


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

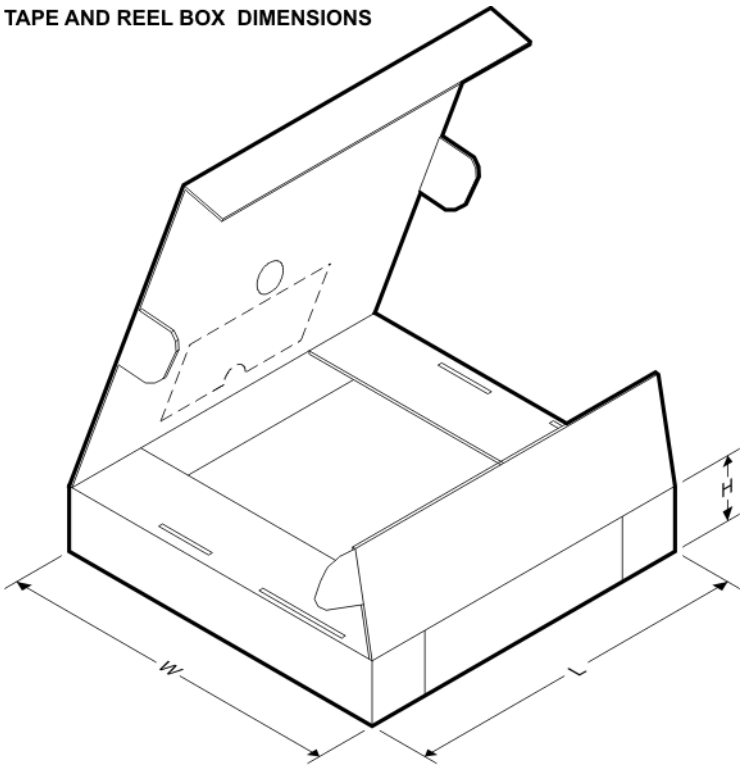
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC59108IPWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
TLC59108IRGYR	VQFN	RGY	20	3000	330.0	12.4	3.8	4.8	1.6	8.0	12.0	Q1

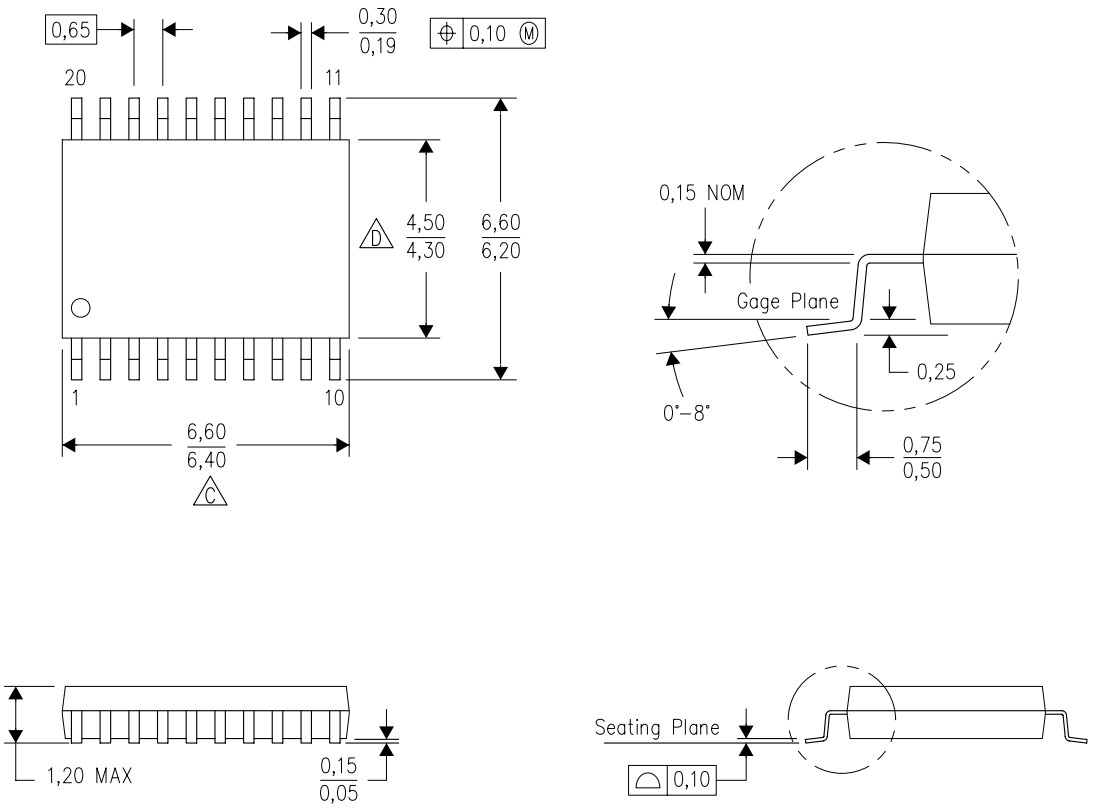
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC59108IPWR	TSSOP	PW	20	2000	367.0	367.0	38.0
TLC59108IRGYR	VQFN	RGY	20	3000	367.0	367.0	35.0

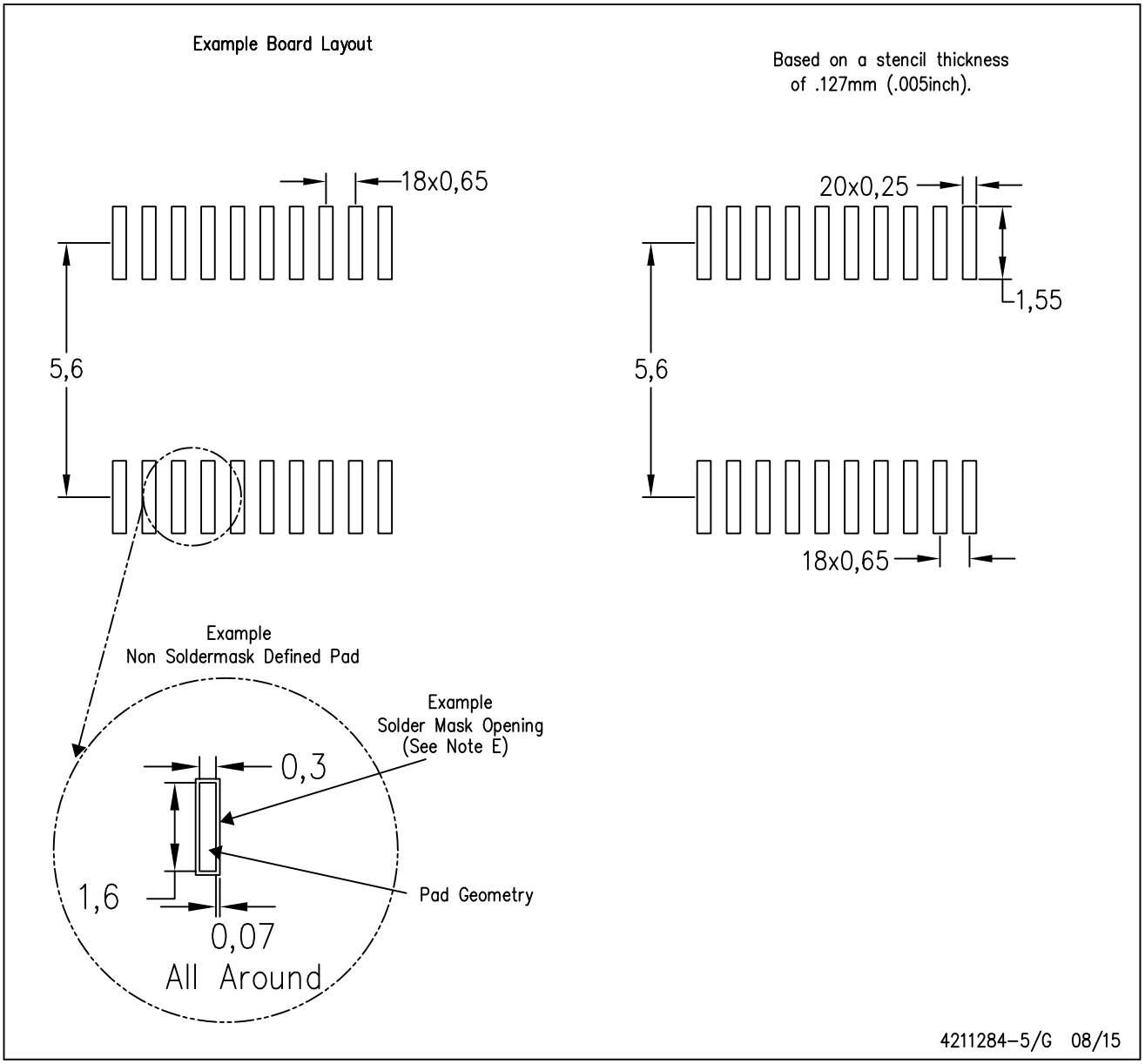
PW (R–PDSO–G20) PLASTIC SMALL OUTLINE



4040064–5/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G20) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

GENERIC PACKAGE VIEW

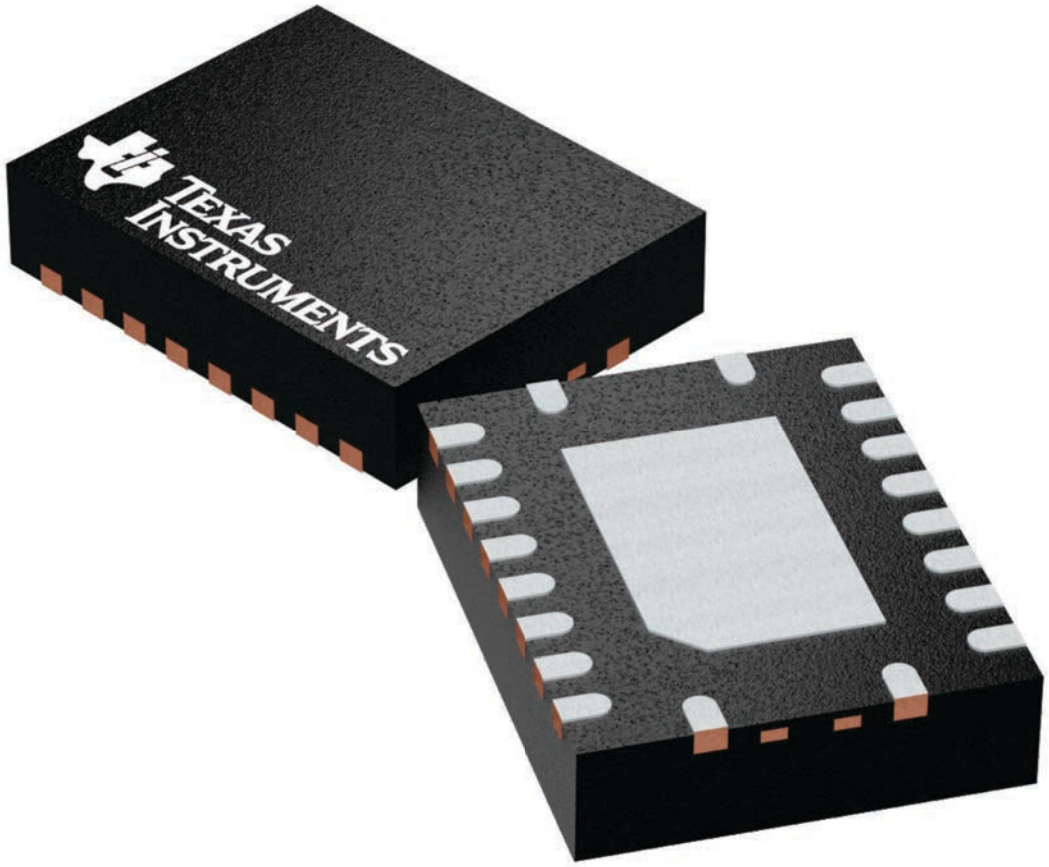
RGY 20

VQFN - 1 mm max height

3.5 x 4.5, 0.5 mm pitch

PLASTIC QUAD FGLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



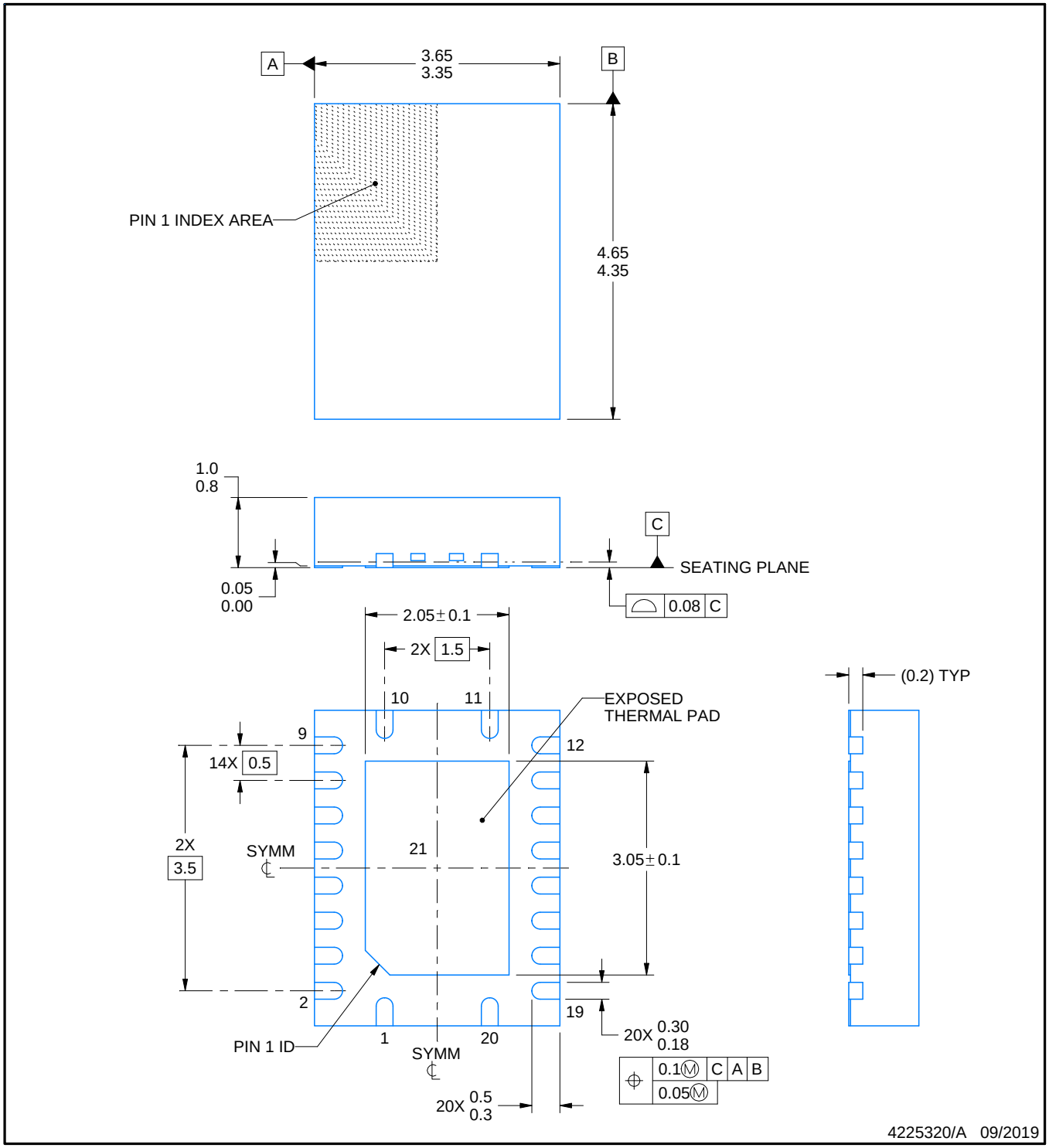
4225264/A

PACKAGE OUTLINE

RGY0020A

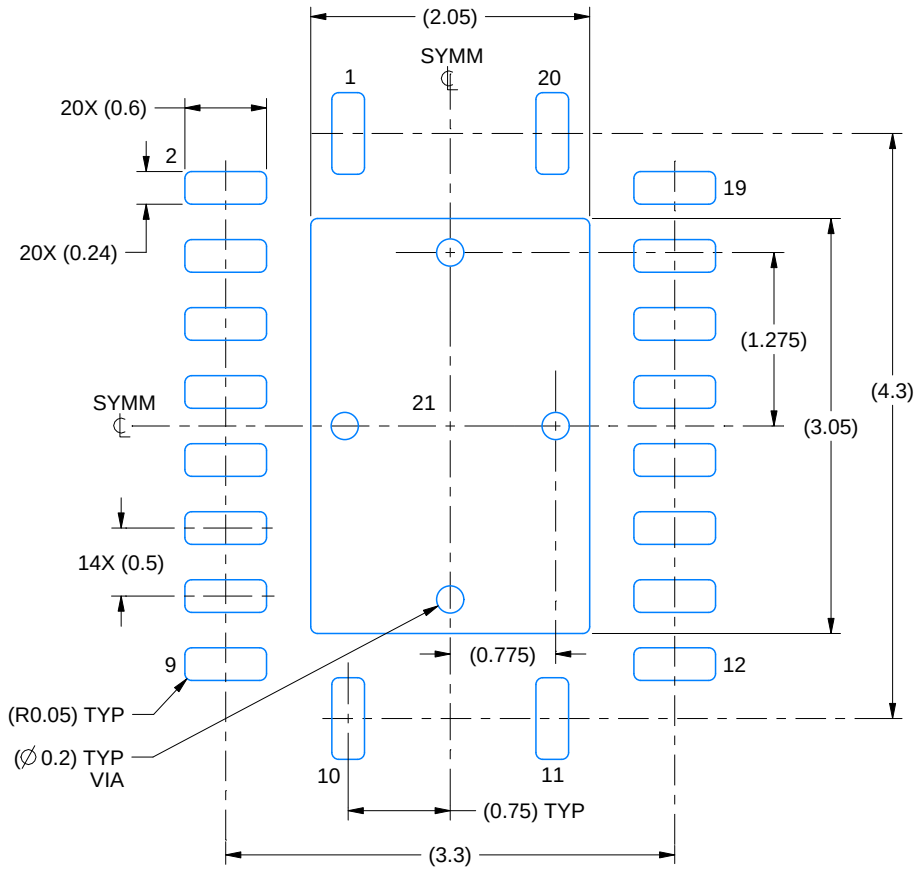
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

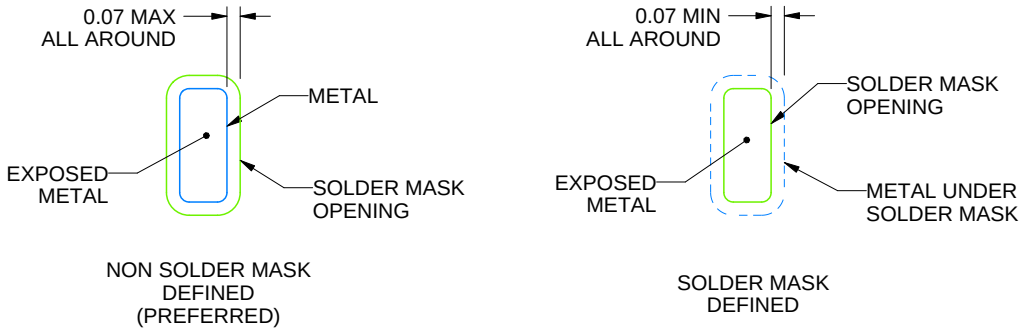


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

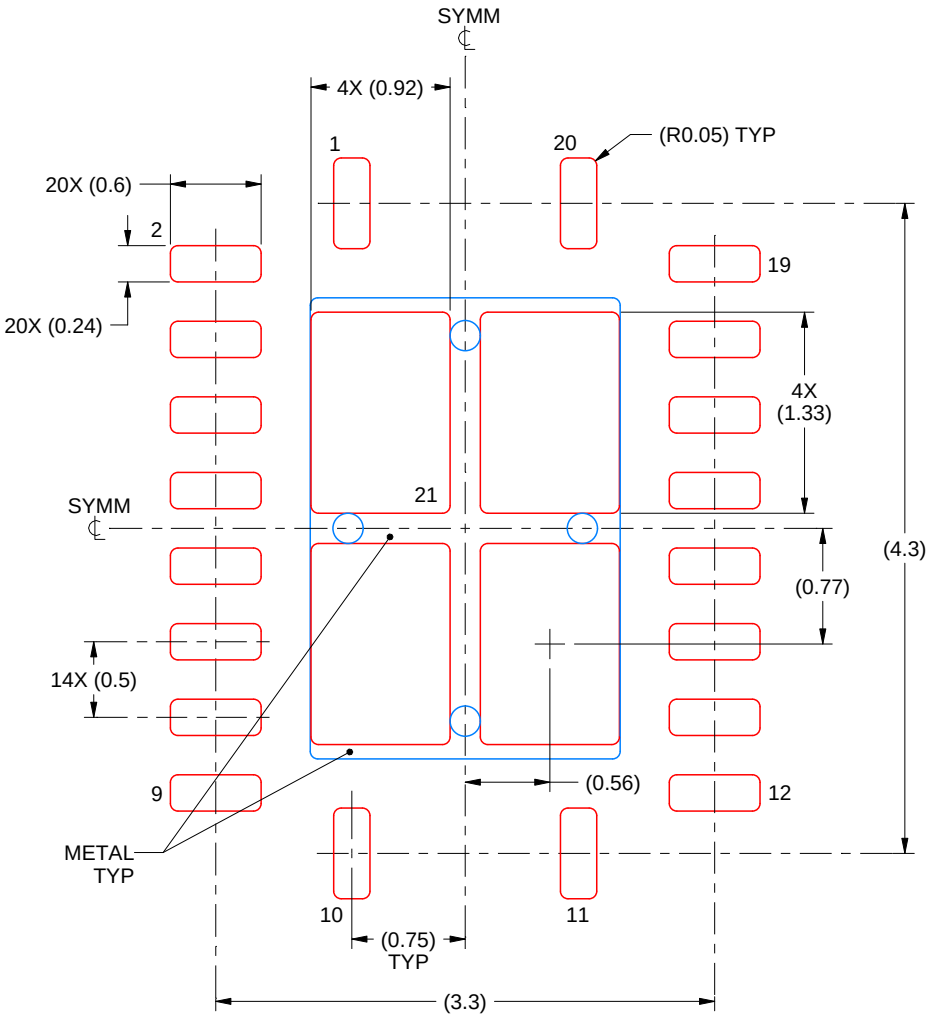


SOLDER MASK DETAILS

4225320/A 09/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 21
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4225320/A 09/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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