1.4GHz Low Phase Noise, Low Jitter PLL with Clock Distribution

FEATURES

- **Low Phase Noise and Jitter**
- **Additive Jitter: 18fs$_{RMS}$ (12kHz to 20MHz)**
- **Additive Jitter: 85fs$_{RMS}$ (10Hz to Nyquist)**
- **EZSync™ Multichip Clock Edge Synchronization**
- Full PLL Core with Lock Indicator
- –226dBc/Hz Normalized In-Band Phase Noise Floor
- –274dBc/Hz Normalized 1/f Phase Noise
- 1.4GHz Maximum VCO Input Frequency
- Four Independent, Low Noise 1.4GHz LVPECL Outputs
- One LVDS/CMOS Configurable Output
- Five Independently Programmable Dividers Covering All Integers from 1 to 63
- Five Independently Programmable VCO Clock Cycle Delays Covering All Integers from 0 to 63
- –40°C to 105°C Junction Temperature Range

APPLICATIONS

- Clocking High Speed, High Resolution ADCs, DACs and Data Acquisition Systems
- Low Jitter Clock Generation and Distribution

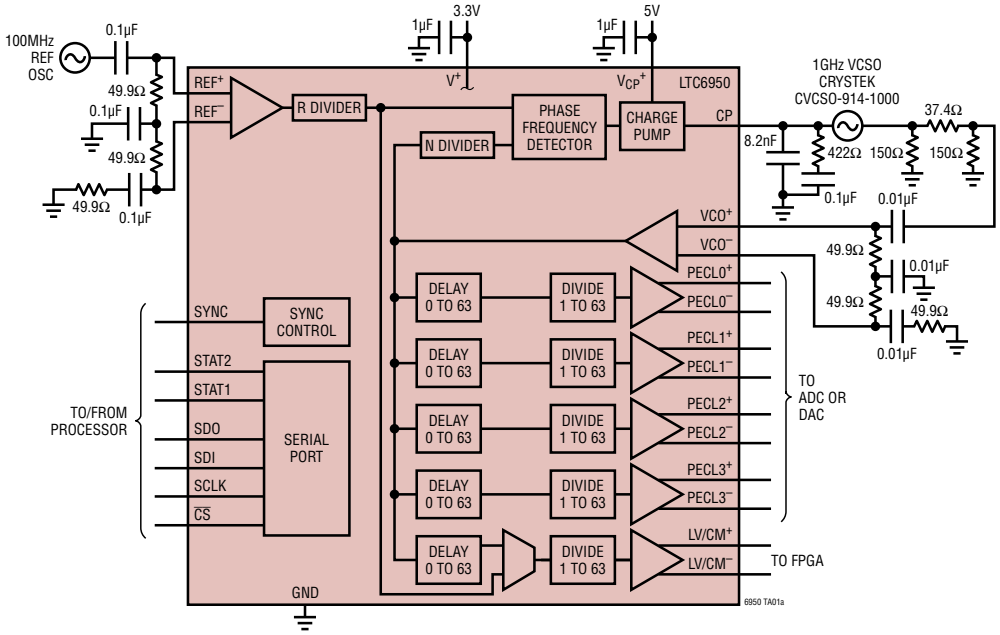
DESCRIPTION

The LTC®6950 is a low phase noise integer-N frequency synthesizer core with clock distribution. The LTC6950 delivers the low phase noise clock signals demanded in high frequency, high resolution data acquisition systems.

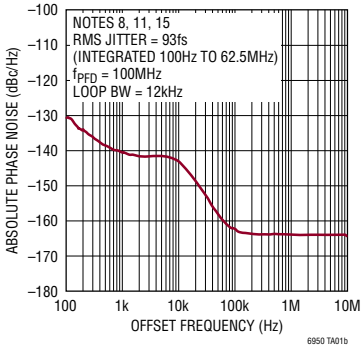
The frequency synthesizer contains a full low noise PLL core with a programmable reference divider (R), a programmable feedback divider (N), a phase/frequency detector (PFD) and a low noise charge pump (CP). The clock distribution section of the LTC6950 delivers up to five outputs based on the VCO input. Each output is individually programmed to divide the VCO input frequency by any integer from 1 to 63 and to delay the output by 0 to 63 VCO clock cycles. Four of the outputs feature very low noise, low skew LVPECL logic signals capable of operation up to 1.4GHz. The fifth output is selectable as either an LVDS (800MHz) or CMOS (250MHz) logic type. This output is also programmed to produce an output signal based on either the VCO input or the reference divider output.

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TYPICAL APPLICATION



PECLx Closed-Loop Phase Noise, f_{VCSO} = 1GHz, Mx[5:0] = 8, f_{PECLx} = 125MHz

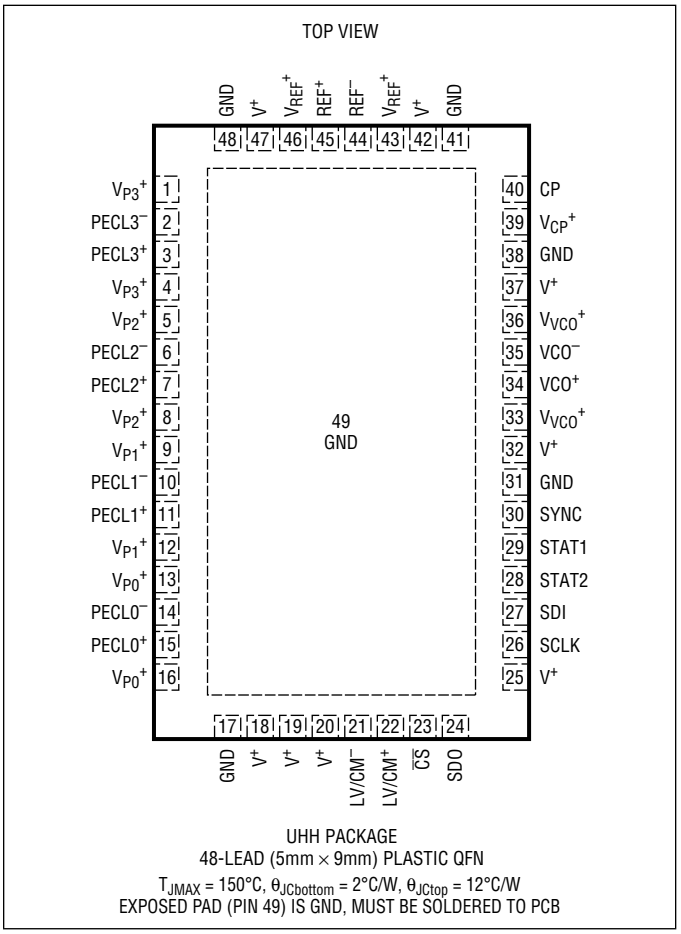


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltages
V^+, V_{P0}^+, V_{P1}^+, V_{P2}^+, V_{P3}^+,
V_{VCO}^+, and V_{REF}^+ to GND 3.6V
V_{CP}^+ to GND 5.5V
CP Voltage ..... –0.3V to (V_{CP}^+ + 0.3V)
$\overline{CS}$, SCLK, SDI, SDO, SYNC, VCO^+, VCO^-,
REF^+, REF^-, Voltage ..... –0.3V to (V^+ + 0.3V)
$PECL3^-$, $PECL3^+$, $PECL2^-$, $PECL2^+$, $PECL1^-$,
$PECL1^+$, $PECL0^-$, $PECL0^+$, LV/CM^-, LV/CM^+,
STAT2, STAT1 ..... (Note 28)
Operating Junction Temperature Range, T_J (Note 2)
LTC6950I ..... –40°C to 105°C
Junction Temperature, T_{JMAX} ..... 150°C
Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION



UHH PACKAGE
48-LEAD (5mm × 9mm) PLASTIC QFN
T_{JMAX} = 150°C, $\theta_{JCbottom}$ = 2°C/W, θ_{JCtop} = 12°C/W
EXPOSED PAD (PIN 49) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	JUNCTION TEMPERATURE RANGE
LTC6950IUHH#PBF	LTC6950IUHH#TRPBF	6950	48-Lead (5mm × 9mm) Plastic QFN	–40°C to 105°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC Marketing for information on nonstandard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). $V^+ = V_{REF}^+ = V_{VCO}^+ = V_{P0}^+ = V_{P1}^+ = V_{P2}^+ = V_{P3}^+ = 3.3V$, $V_{CP}^+ = 5V$ unless otherwise specified. All voltages are with respect to ground.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Reference Inputs (REF⁺, REF⁻)							
f_{REF}	Input Frequency		●	2		250	MHz
V_{REF}	Input Signal Level	Single-Ended	●		0.8	1.5	V_{P-P}
	Minimum Input Slew Rate				10		V/µs
DC_{REF}	Input Duty Cycle				50		%
	Self-Bias Voltage		●	1.9	2.05	2.2	V
	Minimum Common Mode Level	400mV_{P-P} Differential Input			1.5		V
	Maximum Common Mode Level	400mV_{P-P} Differential Input			2.3		V
	Minimum Input Signal Detected	NO_REF = 0, 2MHz ≤ f_{REF} ≤ 250MHz, Sine Wave			350		mV_{P-P}
	Maximum Input Signal Not Detected	NO_REF = 1, 2MHz ≤ f_{REF} ≤ 250MHz, Sine Wave			100		mV_{P-P}
	Input Resistance	Differential	●	1.45	2.2	3.0	kΩ
	Input Capacitance	Differential			1		pF
VCO Inputs (VCO⁺, VCO⁻)							
f_{VCO}	Input Frequency		●			1400	MHz
V_{VCO}	Input Signal Level	Single-Ended	●	0.2	0.8	1.5	V_{P-P}
	Input Slew Rate		●	100			V/µs
DC_{VCO}	Input Duty Cycle				50		%
	Self-Bias Voltage		●	1.9	2.05	2.2	V
	Minimum Common Mode Level	400mV_{P-P} Differential Input			1.5		V
	Maximum Common Mode Level	400mV_{P-P} Differential Input			2.3		V
	Minimum Input Signal Detected	NO_VCO = 0, 30MHz ≤ f_{VCO} ≤ 1400MHz, Sine Wave			350		mV_{P-P}
	Maximum Input Signal Not Detected	NO_VCO = 1, 30MHz ≤ f_{VCO} ≤ 1400MHz, Sine Wave			100		mV_{P-P}
	Input Resistance	Differential	●	1.45	2.2	3.0	kΩ
	Input Capacitance	Differential			1		pF
Phase/Frequency Detector (PFD)							
f_{PFD}	Input Frequency		●			100	MHz
	Up/Down Pulse Width, Standard	CPWIDE = 0			1		ns
	Up/Down Pulse Width, Wide	CPWIDE = 1			2		ns
Lock Indicator (LOCK)							
t_{LWW}	Lock Window Width	LKWIN[1:0] = 0 LKWIN[1:0] = 1 LKWIN[1:0] = 2 LKWIN[1:0] = 3			3 10 30 90		ns ns ns ns
t_{LWHYS}	Lock Window Hysteresis	Increase in t_{LWW} Moving from Locked State to Unlocked State			22		%
	Lock Entry PFD Counts	LKCT[1:0] = 0 LKCT[1:0] = 1 LKCT[1:0] = 2 LKCT[1:0] = 3			32 128 512 2048		Counts Counts Counts Counts

ELECTRICAL CHARACTERISTICS

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SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Charge Pump (CP)							
I_{CP}	Output Source/Sink Current Range	12 Settings (See Table 3)		0.25		11.2	mA
	Output Source/Sink Current Accuracy	I_{CP} = 250µA to 1.4mA, $V_{CP} = V_{CP}^+/2$ I_{CP} = 2mA to 11.2mA, $V_{CP} = V_{CP}^+/2$		–7.5 –6		7.5 6	% %
	Output Source/Sink Current Matching	I_{CP} = 250µA to 1.4mA, $V_{CP} = V_{CP}^+/2$ I_{CP} = 2mA to 11.2mA, $V_{CP} = V_{CP}^+/2$		–7 –3.5		7 3.5	% %
	Output Source/Sink Current vs Output Voltage Sensitivity	$0.85V \le V_{CP} \le (V_{CP}^+ - 0.85V)$ $0.95V \le V_{CP} \le (V_{CP}^+ - 0.95V)$		–7 –2	0.1 0.1	1.5 1	% %
	Output Current vs Temperature	$V_{CP} = V_{CP}^+/2$	●		170		ppm/°C
	Output Hi-Z Leakage Current	I_{CP} = 350µA, CPCLO = CPCHI = 0 (Note 3) I_{CP} = 700µA, CPCLO = CPCHI = 0 (Note 3) I_{CP} = 11.2mA, CPCLO = CPCHI = 0 (Note 3)	● ● ●		0.5 0.5 1	10 10 10	nA nA nA
$V_{CLMP(LO)}$	Low Clamp Voltage	CPCLO = 1			0.9		V
$V_{CLMP(HI)}$	High Clamp Voltage	CPCHI = 1			$V_{CP}^+ - 0.9$		V
V_{MID}	Mid Supply Output Bias Ratio	Referenced to (V_{CP}^+ – GND)	●	0.47	0.49	0.53	V/V
R_{MID}	Mid Supply Mode Impedance				8.8		kΩ
Reference Divider (R)							
R	Divide Range	All Integers Included	●	1		1023	Cycles
VCO Divider (N)							
N	Divide Range	All Integers Included	●	1		2047	Cycles
Digital Inputs ($\overline{CS}$, SDI, SCLK, SYNC)							
V_{IH}	Input High Voltage	$\overline{CS}$, SDI, SCLK, SYNC	●	1.55			V
V_{IL}	Input Low Voltage	$\overline{CS}$, SDI, SCLK, SYNC	●			0.8	V
V_{IHYS}	Input Voltage Hysteresis	$\overline{CS}$, SDI, SCLK, SYNC			250		mV
	Input Current	$\overline{CS}$, SDI, SCLK, SYNC	●	–1		1	µA
Digital Outputs (SDO, STAT1, STAT2)							
I_{OH}	High Level Output Current	SDO, STAT1, STAT2, $V_{OH} = V^+ - 400mV$	●		–2.4	–1.4	mA
I_{OL}	Low Level Output Current	SDO, STAT1, STAT2, V_{OH} = 400mV	●	2.0	3.4		mA
	SDO Hi-Z Current		●	–1		1	µA
Digital Timing Specifications (See Figures 21 and 22)							
t_{CKH}	SCLK High Pulse Width		●	25			ns
t_{CKL}	SCLK Low Pulse Width		●	25			ns
t_{CSST}	$\overline{CS}$ Setup Time		●	10			ns
t_{CSHT}	$\overline{CS}$ Hold Time		●	10			ns
t_{CSH}	$\overline{CS}$ High Pulse Width		●	10			ns
t_{CS}	SDI to SCLK Setup Time		●	6			ns
t_{CH}	SDI to SCLK Hold Time		●	6			ns
t_{DO}	SDO Propagation Delay	C_{LOAD} = 30pF			16		ns
t_{SYNCH}	SYNC High Pulse Width		●	1			ms
t_{SYNCL}	Minimum SYNC Low Pulse Width	Before Next SYNC High Pulse			1		ms

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SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Output Divider (M)							
Mx[5:0]	Divider Range M0[5:0], M1[5:0], M2[5:0], M3[5:0], M4[5:0]	All Integers Included	●	1		63	Cycles
DELx[5:0]	Divider Delay in VCO Clock Cycles DEL0[5:0], DEL1[5:0], DEL2[5:0], DEL3[5:0], DEL4[5:0]	All Integers Included	●	0		63	Cycles
PECLx Clock Outputs ($PECL0^+$, $PECL0^-$, $PECL1^+$, $PECL1^-$, $PECL2^+$, $PECL2^-$, $PECL3^+$, $PECL3^-$)							
f_{PECLx}	Frequency	Single-Ended Termination = 50Ω to (V_{Px}^+ – 2V)	●			1400	MHz
V_{CM}	Common Mode Voltage (Outputs Static)	Single-Ended Termination = 50Ω to (V_{Px}^+ – 2V)	●	V_{Px}^+ – 1.68	V_{Px}^+ – 1.48	V_{Px}^+ – 1.25	V
$\|V_{OD}\|$	Differential Voltage (Outputs Static)	Single-Ended Termination = 50Ω to (V_{Px}^+ – 2V) Differential Termination = 100Ω, Internal Bias On	●	610	800 800	1050	mV_{PK} mV_{PK}
t_{RISE}	Rise Time, 20% to 80%	Single-Ended Termination = 50Ω to (V_{Px}^+ – 2V) Differential Termination = 100Ω, Internal Bias On			135 135		ps ps
t_{FALL}	Fall Time, 80% to 20%	Single-Ended Termination = 50Ω to (V_{Px}^+ – 2V) Differential Termination = 100Ω, Internal Bias On			135 135		ps ps
DC_{PECL}	Duty Cycle	Mx[5:0] = 1 Mx[5:0] > 1 (Even or Odd)	 ●	 45	DC_{VCO} 50	 55	% %
t_{PDP3}	Propagation Delay from VCO to PECL3	M3[5:0] = 1, FILTV = 0 M3[5:0] = 1, FILTV = 1 M3[5:0] > 1, FILTV = 0	● ●	285 335	495 700 560	660 745	ps ps ps
	Propagation Delay from VCO to PECL3, Temperature Variation	M3[5:0] = 1, FILTV = 0 M3[5:0] = 1, FILTV = 1 M3[5:0] > 1, FILTV = 0	● ● ●		0.35 0.50 0.45		ps/°C ps/°C ps/°C
t_{SKEWPx}	Skew, from PECL3 to PECL0	M0[5:0] = M3[5:0] = 1 M0[5:0] = M3[5:0] > 1	● ●	–50 –50	–1.0 –1.5	50 50	ps ps
	Skew, from PECL3 to PECL1	M1[5:0] = M3[5:0] = 1 M1[5:0] = 1, M3[5:0] > 1 M1[5:0] > 1, M3[5:0] = 1 M1[5:0] = M3[5:0] > 1	● ● ● ●	–50 –125 5 –50	4.5 –60 69 5	50 0 135 50	ps ps ps ps
	Skew, from PECL3 to PECL2	M2[5:0] = M3[5:0] = 1 M2[5:0] = M3[5:0] > 1	● ●	–50 –50	5 5.5	50 50	ps ps
	Skew, All PECLx Outputs	FILTV = 0, Same Part	●			55	ps
	Skew, Same PECLx Output	FILTV = 0, Across Multiple Parts (Note 4)	●			320	ps
	Skew, All PECLx Outputs	FILTV = 0, Across Multiple Parts (Note 5)	●			330	ps

ELECTRICAL CHARACTERISTICS

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SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
LVDS Clock Outputs (LV/CM⁺ and LV/CM⁻)							
f_{LVDS}	Frequency	Differential Termination = 100Ω	●			800	MHz
$\|V_{OD}\|$	Differential Voltage (Outputs Static)	Differential Termination = 100Ω	●	280	400	525	mV_{PK}
$\|\Delta V_{OD}\|$	Delta V_{OD}	Differential Termination = 100Ω	●		5	60	mV
V_{OS}	Offset Voltage (Outputs Static)	Differential Termination = 100Ω	●	1.125	1.23	1.375	V
$\|\Delta V_{OS}\|$	Delta V_{OS}	Differential Termination = 100Ω	●		5	50	mV
t_{RISE}	Rise Time, 20% to 80%	Differential Termination = 100Ω	●		140		ps
t_{FALL}	Fall Time, 80% to 20%	Differential Termination = 100Ω	●		130		ps
$\|I_{SA}\|$, $\|I_{SB}\|$	Short Circuit Current to Common	Shorted to GND			4.2		mA
$\|I_{SAB}\|$	Short Circuit Current to Complementary				4.2		mA
DC_{LVDS}	Duty Cycle	RDIVOUT = 0, M4[5:0] = 1 RDIVOUT = 1, R[9:0] = 1, M4[5:0] = 1 RDIVOUT = 0, M4[5:0] > 1 (Even or Odd) RDIVOUT = 1, M4[5:0] > 1 (Even) RDIVOUT = 1, R[9:0] = 3, M4[5:0] = 3 RDIVOUT = 1, R[9:0] = 1023, M4[5:0] = 3	 ● 	 45 	DC_{VCO} DC_{REF} 50 50 56 33	 55 	% % % % % %
t_{PD}	Propagation Delay from VCO to LVDS with RDIVOUT Disabled	M4[5:0] = 1, FILTV = 0 M4[5:0] = 1, FILTV = 1 M4[5:0] > 1, FILTV = 0			1.85 2.05 1.91		ns ns ns
	Propagation Delay from REF to LVDS with RDIVOUT Enabled	M4[5:0] = 1, R = 1, FILTR = 0 M4[5:0] = 1, R = 1, FILTR = 1 M4[5:0] > 1, R = 1, FILTR = 0 M4[5:0] = 1, R > 1, FILTR = 0 M4[5:0] > 1, R > 1, FILTR = 0			2.26 3.12 2.32 2.40 2.47		ns ns ns ns ns
	Propagation Delay from VCO to LVDS with RDIVOUT Disabled, Temperature Variation	M4[5:0] = 1, FILTV = 0 M4[5:0] = 1, FILTV = 1 M4[5:0] > 1, FILTV = 0	● ● ●		4.05 4.20 4.00		ps/°C ps/°C ps/°C
	Propagation Delay from REF to LVDS with RDIVOUT Enabled, Temperature Variation	M4[5:0] = 1, R = 1, FILTR = 0 M4[5:0] = 1, R = 1, FILTR = 1 M4[5:0] > 1, R = 1, FILTR = 0 M4[5:0] = 1, R > 1, FILTR = 0 M4[5:0] > 1, R > 1, FILTR = 0	● ● ● ● ●		4.55 4.50 4.53 4.55 4.70		ps/°C ps/°C ps/°C ps/°C ps/°C
t_{SKEWL}	Skew, from PECL3 to LVDS with RDIVOUT Disabled	M3[5:0] = M4[5:0] = 1 M3[5:0] = M4[5:0] > 1			1.32 1.32		ns ns
	Skew, from PECL3 to LVDS with RDIVOUT Disabled, Temperature Variation	M3[5:0] = M4[5:0] = 1 M3[5:0] = M4[5:0] > 1	● ●		3.70 3.55		ps/°C ps/°C

ELECTRICAL CHARACTERISTICS

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SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
CMOS Clock Outputs (LV/CM⁺ and LV/CM⁻)							
f_{CMOS}	Frequency		●			250	MHz
V_{OH}	High Voltage (Outputs Static)	2.5mA Load	●	$V^+ – 0.4$			V
V_{OL}	Low Voltage (Outputs Static)	2.5mA Load	●			0.4	V
t_{RISE}	Rise Time, 20% to 80%	C_{LOAD} = 2pF, CMSINV = 1			1010		ps
t_{FALL}	Fall Time, 80% to 20%	C_{LOAD} = 2pF, CMSINV = 1			840		ps
DC_{CMOS}	Duty Cycle	RDIVOUT = 0, M4[5:0] = 1 RDIVOUT = 1, R[9:0] = 1, M4[5:0] = 1 RDIVOUT = 0, M4[5:0] > 1 (Even or Odd) RDIVOUT = 1, M4[5:0] > 1 (Even) RDIVOUT = 1, R[9:0] = 3, M4[5:0] = 3 RDIVOUT = 1, R[9:0] = 1023, M4[5:0] = 3			DC_{VCO} DC_{REF} 50 50 56 33		% % % % % %
t_{PD}	Propagation Delay from VCO to CMOS with RDIVOUT Disabled	M4[5:0] = 1, FILTV = 0, CMSINV = 1 M4[5:0] = 1, FILTV = 1, CMSINV = 1 M4[5:0] > 1, FILTV = 0, CMSINV = 1			2.12 2.32 2.20		ns ns ns
	Propagation Delay from REF to CMOS with RDIVOUT Enabled	M4[5:0] = 1, R = 1, FILTR = 0, CMSINV = 1 M4[5:0] = 1, R = 1, FILTR = 1, CMSINV = 1 M4[5:0] > 1, R = 1, FILTR = 0, CMSINV = 1 M4[5:0] = 1, R > 1, FILTR = 0, CMSINV = 1 M4[5:0] > 1, R > 1, FILTR = 0, CMSINV = 1			2.55 3.40 2.60 2.69 2.76		ns ns ns ns ns
	Propagation Delay from VCO to CMOS with RDIVOUT Disabled, Temperature Variation	M4[5:0] = 1, FILTV = 0, CMSINV = 1 M4[5:0] = 1, FILTV = 1, CMSINV = 1 M4[5:0] > 1, FILTV = 0, CMSINV = 1	● ● ●		4.90 5.10 5.05		ps/°C ps/°C ps/°C
	Propagation Delay from REF to CMOS with RDIVOUT Enabled, Temperature Variation	M4[5:0] = 1, R = 1, FILTR = 0, CMSINV = 1 M4[5:0] = 1, R = 1, FILTR = 1, CMSINV = 1 M4[5:0] > 1, R = 1, FILTR = 0, CMSINV = 1 M4[5:0] = 1, R > 1, FILTR = 0, CMSINV = 1 M4[5:0] > 1, R > 1, FILTR = 0, CMSINV = 1	● ● ● ● ●		5.90 5.80 5.85 5.90 6.00		ps/°C ps/°C ps/°C ps/°C ps/°C
t_{SKEWC}	Skew, from PECL3 to CMOS with RDIVOUT Disabled	M3[5:0] = M4[5:0] = 1, CMSINV = 1 M3[5:0] = M4[5:0] > 1, CMSINV = 1 M3[5:0] = M4[5:0] = 1, CMSINV = 0			1.60 1.60 1.83		ns ns ns
	Skew, from PECL3 to CMOS with RDIVOUT Disabled, Temperature Variation	M3[5:0] = M4[5:0] = 1, CMSINV = 1 M3[5:0] = M4[5:0] > 1, CMSINV = 1 M3[5:0] = M4[5:0] = 1, CMSINV = 0	● ● ●		4.55 4.60 4.15		ps/°C ps/°C ps/°C

ELECTRICAL CHARACTERISTICS

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SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Supplies							
	V^+, V_{REF}^+, V_{VCO}^+, V_{P0}^+, V_{P1}^+, V_{P2}^+, V_{P3}^+ Supply Voltage Range		●	3.15	3.3	3.45	V
	V_{CP}^+ Supply Voltage Range		●	V^+		5.25	V
Supply Current							
	V_{CP}^+ Supply Current	I_{CP} = 11.2mA	●		35	43	mA
		I_{CP} = 4mA	●		21	25	mA
		I_{CP} = 1mA	●		13	16	mA
		I_{CP} = 0.5mA	●		11.5	15	mA
		I_{CP} = 250µA	●		11	14	mA
		PDALL = 1	●		0.235	0.6	mA
	Sum of V^+, V_{REF}^+, V_{VCO}^+, V_{P0}^+, V_{P1}^+, V_{P2}^+, V_{P3}^+ Supply Currents (Changes to Default Power-Up Configuration Noted)	f_{VCO} = 800MHz, f_{REF} = 106.25MHz + Internal Bias Enabled, All PECLx	●		485	550	mA
		f_{VCO} = 800MHz, f_{REF} = 106.25MHz + Termination = 50Ω to (V_{Px}^+ – 2V), All PECLx	●		495	565	mA
		f_{VCO} = 800MHz, f_{REF} = 106.25MHz + External 150Ω Bias, All PECLx			510		mA
		f_{VCO} = 800MHz, f_{REF} = 106.25MHz + No Internal/External Bias, All PECLx	●		405	460	mA
		f_{VCO} = 800MHz, f_{REF} = 106.25MHz + IBIAS0 = 1, IBIAS3 = 1 + PD_DIV1 = 1, PD_DIV2 = 1, PD_DIV4 = 1			260		mA
		f_{VCO} = 800MHz, f_{REF} = 106.25MHz + IBIAS0 = 1, IBIAS3 = 1 + PD_DIV1 = 1, PD_DIV2 = 1, PD_DIV4 = 1 + M0[5:0] = M3[5:0] = 1			220		mA
		PDALL = 1	●		1.6	2.2	mA
Supply Current Delta (Note 6)							
	REF Input Signal Present Circuit On	PDREFAC = 0	●		2.3	3.5	mA
	VCO Input Signal Present Circuit On	PDVCOAC = 0	●		0.6	1.0	mA
	VCO Input On	PDALL = 0, PDREFAC = 1, PDVCOAC = 1, PDPLL = 1, All PD_DIVx = 1, All PD_OUTx = 1,	●		32	40	mA
	REF Input, RDIV, NDIV, PFD, CP On	I_{CP}^+ Current, PDPLL = 0, I_{CP} = 11.2mA setting	●		35	43	mA
		All Other Current, PDPLL = 0	●		73	90	mA
	PECLx Output Divider On PECLx = PECL0, PECL1, PECL2, PECL3	PD_DIVx = 0, Mx[5:0] = 1	●		28	35	mA
		PD_DIVx = 0, Mx[5:0] > 1	●		46	56	mA
	LV/CM Output Divider On	PD_DIV4 = 0, M4[5:0] = 1	●		34	41	mA
		PD_DIV4 = 0, M4[5:0] > 1	●		52	63	mA
	PECLx Output Driver On PECLx = PECL0, PECL1, PECL2, PECL3	PD_OUTx = 0, Termination = 50Ω to (V_{Px}^+ – 2V)	●		32	45	mA
		PD_OUTx = 0, IBIASx = 1 (Internal Bias On)	●		30	38	mA
		PD_OUTx = 0, No Internal/External Bias	●		10	15	mA
	LV/CM Output Driver On	PD_OUT4 = 0, LVDS at 800MHz	●		22	28	mA
		PD_OUT4 = 0, CMOS at 50MHz	●		12	16	mA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). $V^+ = V_{REF}^+ = V_{VCO}^+ = V_{P0}^+ = V_{P1}^+ = V_{P2}^+ = V_{P3}^+ = 3.3V$, $V_{CP}^+ = 5V$ unless otherwise specified. All voltages are with respect to ground.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
VCO to PECLx (PECL0$^+$, PECL0$^-$, PECL1$^+$, PECL1$^-$, PECL2$^+$, PECL2$^-$, PECL3$^+$, PECL3$^-$) Additive Phase Noise/Time Jitter (Note 7)							
	Phase Noise: Distribution Only f_{VCO} = 245.76MHz, Mx[5:0] = 1, f_{PECLx} = 245.76MHz	10Hz Offset 100Hz Offset 1kHz Offset 10kHz Offset 100kHz Offset >1MHz Offset			–135 –144 –153 –158 –159.5 –159.5		dBc/Hz dBc/Hz dBc/Hz dBc/Hz dBc/Hz dBc/Hz
	Jitter: Distribution Only f_{VCO} = 245.76MHz, Mx[5:0] = 1, f_{PECLx} = 245.76MHz	12kHz to 20MHz Integration Bandwidth 10Hz to 122.88MHz Integration Bandwidth			44 108		fs_{RMS} fs_{RMS}
	Phase Noise: Distribution Only f_{VCO} = 245.76MHz, Mx[5:0] = 4, f_{PECLx} = 61.44MHz	10Hz Offset 100Hz Offset 1kHz Offset 10kHz Offset 100kHz Offset >1MHz Offset			–146 –156 –164 –168 –168 –168		dBc/Hz dBc/Hz dBc/Hz dBc/Hz dBc/Hz dBc/Hz
	Jitter: Distribution Only f_{VCO} = 245.76MHz, Mx[5:0] = 4, f_{PECLx} = 61.44MHz	12kHz to 20MHz Integration Bandwidth 10kHz to 30.72MHz Integration Bandwidth			69 85		fs_{RMS} fs_{RMS}
	Phase Noise: Distribution Only f_{VCO} = 622.08MHz, Mx[5:0] = 1, f_{PECLx} = 622.08MHz	10Hz Offset 100Hz Offset 1kHz Offset 10kHz Offset 100kHz Offset >1MHz Offset			–128 –136 –146 –153.5 –155.5 –155.5		dBc/Hz dBc/Hz dBc/Hz dBc/Hz dBc/Hz dBc/Hz
	Jitter: Distribution Only f_{VCO} = 622.08MHz, Mx[5:0] = 1, f_{PECLx} = 622.08MHz	12kHz to 20MHz Integration Bandwidth 10Hz to 311.04MHz Integration Bandwidth			28 108		fs_{RMS} fs_{RMS}
	Phase Noise: Distribution Only f_{VCO} = 622.08MHz, Mx[5:0] = 4, f_{PECLx} = 155.52MHz	10Hz Offset 100Hz Offset 1kHz Offset 10kHz Offset 100kHz Offset >1MHz Offset			–139 –148 –157 –163 –163.5 –163.5		dBc/Hz dBc/Hz dBc/Hz dBc/Hz dBc/Hz dBc/Hz
	Jitter: Distribution Only f_{VCO} = 622.08MHz, Mx[5:0] = 4, f_{PECLx} = 155.52MHz	12kHz to 20MHz Integration Bandwidth 10Hz to 77.76MHz Integration Bandwidth			45 85		fs_{RMS} fs_{RMS}
	Phase Noise: Distribution Only f_{VCO} = 622.08MHz, Mx[5:0] = 16, f_{PECLx} = 38.88MHz	10Hz Offset 100Hz Offset 1kHz Offset 10kHz Offset 100kHz Offset >1MHz Offset			–150 –160 –166 –169 –169.5 –169.5		dBc/Hz dBc/Hz dBc/Hz dBc/Hz dBc/Hz dBc/Hz
	Phase Noise: Distribution Only f_{VCO} = 1400MHz, Mx[5:0] = 1, f_{PECLx} = 1400MHz	10Hz Offset 100Hz Offset 1kHz Offset 10kHz Offset 100kHz Offset >1MHz Offset			–123 –131 –140 –147 –151 –152.5		dBc/Hz dBc/Hz dBc/Hz dBc/Hz dBc/Hz dBc/Hz
	Jitter: Distribution Only f_{VCO} = 1400MHz, Mx[5:0] = 1, f_{PECLx} = 1400MHz	12kHz to 20MHz Integration Bandwidth 10Hz to 700MHz Integration Bandwidth			18 98		fs_{RMS} fs_{RMS}

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). $V^+ = V_{REF}^+ = V_{VCO}^+ = V_{P0}^+ = V_{P1}^+ = V_{P2}^+ = V_{P3}^+ = 3.3V$, $V_{CP}^+ = 5V$ unless otherwise specified. All voltages are with respect to ground.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	Phase Noise: Distribution Only f_{VCO} = 1400MHz, Mx[5:0] = 4, f_{PECLx} = 350MHz	10Hz Offset 100Hz Offset 1kHz Offset 10kHz Offset 100kHz Offset >1MHz Offset			–132 –143 –151 –157 –160 –160		dBc/Hz dBc/Hz dBc/Hz dBc/Hz dBc/Hz dBc/Hz
	Jitter: Distribution Only f_{VCO} = 1400MHz, Mx[5:0] = 4, f_{PECLx} = 350MHz	12kHz to 20MHz Integration Bandwidth 10Hz to 175MHz Integration Bandwidth			29 85		fs_{RMS} fs_{RMS}
	Phase Noise: Distribution Only f_{VCO} = 1400MHz, Mx[5:0] = 16, f_{PECLx} = 87.5MHz	10Hz Offset 100Hz Offset 1kHz Offset 10kHz Offset 100kHz Offset >1MHz Offset			–144 –155 –163 –166.5 –166.5 –166.5		dBc/Hz dBc/Hz dBc/Hz dBc/Hz dBc/Hz dBc/Hz
	Jitter: Distribution Only f_{VCO} = 1400MHz, Mx[5:0] = 16, f_{PECLx} = 87.5MHz	12kHz to 20MHz Integration Bandwidth 10Hz to 43.75MHz Integration Bandwidth			56 85		fs_{RMS} fs_{RMS}
VCO to LVDS Additive Phase Noise/Time Jitter (Note 7)							
	Phase Noise: Distribution Only f_{VCO} = 245.76MHz, M4[5:0] = 1, f_{LVDS} = 245.76MHz	10Hz Offset 100Hz Offset 1kHz Offset 10kHz Offset 100kHz Offset >1MHz Offset			–122 –132 –144 –151.5 –155 –156		dBc/Hz dBc/Hz dBc/Hz dBc/Hz dBc/Hz dBc/Hz
	Jitter: Distribution Only f_{VCO} = 245.76MHz, M4[5:0] = 1, f_{LVDS} = 245.76MHz	12kHz to 20MHz Integration Bandwidth 10Hz to 122.88MHz Integration Bandwidth			65 155		fs_{RMS} fs_{RMS}
	Phase Noise: Distribution Only f_{VCO} = 245.76MHz, M4[5:0] = 4, f_{LVDS} = 61.44MHz	10Hz Offset 100Hz Offset 1kHz Offset 10kHz Offset 100kHz Offset >1MHz Offset			–133 –140 –153 –161 –163 –163.5		dBc/Hz dBc/Hz dBc/Hz dBc/Hz dBc/Hz dBc/Hz
	Jitter: Distribution Only f_{VCO} = 245.76MHz, M4[5:0] = 4, f_{LVDS} = 61.44MHz	12kHz to 20MHz Integration Bandwidth 10Hz to 30.72MHz Integration Bandwidth			110 138		fs_{RMS} fs_{RMS}
	Phase Noise: Distribution Only f_{VCO} = 622.08MHz, M4[5:0] = 1, f_{LVDS} = 622.08MHz	10Hz Offset 100Hz Offset 1kHz Offset 10kHz Offset 100kHz Offset >1MHz Offset			–113 –124 –135 –143 –147 –151		dBc/Hz dBc/Hz dBc/Hz dBc/Hz dBc/Hz dBc/Hz
	Jitter: Distribution Only f_{VCO} = 622.08MHz, M4[5:0] = 1, f_{LVDS} = 622.08MHz	12kHz to 20MHz Integration Bandwidth 10Hz to 311.04MHz Integration Bandwidth			47 170		fs_{RMS} fs_{RMS}

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). $V^+ = V_{REF}^+ = V_{VCO}^+ = V_{P0}^+ = V_{P1}^+ = V_{P2}^+ = V_{P3}^+ = 3.3V$, $V_{CP}^+ = 5V$ unless otherwise specified. All voltages are with respect to ground.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	Phase Noise: Distribution Only f_{VCO} = 622.08MHz, M4[5:0] = 4, f_{LVDS} = 155.52MHz	10Hz Offset 100Hz Offset 1kHz Offset 10kHz Offset 100kHz Offset >1MHz Offset			–125 –134 –147 –154 –158 –159		dBc/Hz dBc/Hz dBc/Hz dBc/Hz dBc/Hz dBc/Hz
	Jitter: Distribution Only f_{VCO} = 622.08MHz, M4[5:0] = 4, f_{LVDS} = 155.52MHz	12kHz to 20MHz Integration Bandwidth 10Hz to 77.76MHz Integration Bandwidth			73 138		fs_{RMS} fs_{RMS}
	Phase Noise: Distribution Only f_{VCO} = 622.08MHz, M4[5:0] = 16, f_{LVDS} = 38.88MHz	10Hz Offset 100Hz Offset 1kHz Offset 10kHz Offset 100kHz Offset >1MHz Offset			–137 –145 –156 –164 –165 –165		dBc/Hz dBc/Hz dBc/Hz dBc/Hz dBc/Hz dBc/Hz
VCO to CMOS Additive Phase Noise/Time Jitter (Note 7)							
	Phase Noise: Distribution Only f_{VCO} = 245.76MHz, M4[5:0] = 1, f_{CMOS} = 245.76MHz	10Hz Offset 100Hz Offset 1kHz Offset 10kHz Offset 100kHz Offset >1MHz Offset			–120 –130 –143 –150.5 –155 –157		dBc/Hz dBc/Hz dBc/Hz dBc/Hz dBc/Hz dBc/Hz
	Jitter: Distribution Only f_{VCO} = 245.76MHz, M4[5:0] = 1, f_{CMOS} = 245.76MHz	12kHz to 20MHz integration bandwidth 10Hz to 122.88MHz integration bandwidth			57 135		fs_{RMS} fs_{RMS}
	Phase Noise: Distribution Only f_{VCO} = 245.76MHz, M4[5:0] = 4, f_{CMOS} = 61.44MHz	10Hz Offset 100Hz Offset 1kHz Offset 10kHz Offset 100kHz Offset >1MHz Offset			–132 –140 –153 –161 –164 –164		dBc/Hz dBc/Hz dBc/Hz dBc/Hz dBc/Hz dBc/Hz
	Jitter: Distribution Only f_{VCO} = 245.76MHz, M4[5:0] = 4, f_{CMOS} = 61.44MHz	12kHz to 20MHz Integration Bandwidth 10Hz to 30.72MHz integration bandwidth			104 125		fs_{RMS} fs_{RMS}
	Phase Noise: Distribution Only f_{VCO} = 622.08MHz, M4[5:0] = 4, f_{CMOS} = 155.52MHz	10Hz Offset 100Hz Offset 1kHz Offset 10kHz Offset 100kHz Offset >1MHz Offset			–125 –135 –146 –155 –159 –160		dBc/Hz dBc/Hz dBc/Hz dBc/Hz dBc/Hz dBc/Hz
	Jitter: Distribution Only f_{VCO} = 622.08MHz, M4[5:0] = 4, f_{CMOS} = 155.52MHz	12kHz to 20MHz Integration Bandwidth 10Hz to 77.76MHz Integration Bandwidth			65 125		fs_{RMS} fs_{RMS}
	Phase Noise: Distribution Only f_{VCO} = 622.08MHz, M4[5:0] = 16, f_{CMOS} = 38.88MHz	10Hz Offset 100Hz Offset 1kHz Offset 10kHz Offset 100kHz Offset >1MHz Offset			–136 –146 –157 –163 –165 –165		dBc/Hz dBc/Hz dBc/Hz dBc/Hz dBc/Hz dBc/Hz

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). $V^+ = V_{REF}^+ = V_{VCO}^+ = V_{P0}^+ = V_{P1}^+ = V_{P2}^+ = V_{P3}^+ = 3.3V$, $V_{CP}^+ = 5V$ unless otherwise specified. All voltages are with respect to ground.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Absolute Phase Noise and Spurious Energy							
$L_{M(MIN)}$	Output Phase Noise Floor (Notes 8, 9)	Mx[5:0] = 1, f_{PECLx} = 1GHz Mx[5:0] = 4, f_{PECLx} = 250MHz Mx[5:0] = 16, f_{PECLx} = 62.5MHz Mx[5:0] = 40, f_{PECLx} = 25MHz			–155 –161 –167 –171		dBc/Hz dBc/Hz dBc/Hz dBc/Hz
$L_{M(NORM)}$	Normalized In-Band Phase Noise Floor	I_{CP} = 11.2mA (Notes 10, 11, 12)			–226		dBc/Hz
$L_{M(NORM-1/f)}$	Normalized In-Band 1/f Phase Noise	I_{CP} = 11.2mA (Notes 10, 13)			–274		dBc/Hz
$L_{M(IB)}$	In-Band Phase Noise Floor	f_{OUT} = 1GHz (Notes 10, 11, 12, 14)			–112.5		dBc/Hz
	Integrated Phase Noise from 100Hz to 62.5MHz	Mx[5:0] = 8, f_{PECLx} = 125MHz (Notes 8, 11, 15)			93		fs_{RMS}
	Spurious Signals, PLL Locked	f_{PFD} = 5MHz (Notes 16, 17, 18) f_{PFD} = 10MHz (Notes 8, 11, 16, 19)			–105 –88		dBc dBc

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC6950IUHH is guaranteed to meet specified performance limits over the full operating junction temperature range of –40°C to 105°C. Under maximum operating conditions, air flow or heat sinking may be required to maintain a junction temperature of 105°C or lower. It is strongly recommended that the Exposed Pad (pin 49) be soldered directly to the ground plane with an array of thermal vias as described in the Applications information section.

Note 3: For $0.9V \le V_{CP} \le (V_{CP}^+ – 0.9V)$.

Note 4: This parameter is the difference in the propagation delay over multiple parts for the same PECLx output at the same supply voltages, at the same temperature and in the same configuration.

Note 5: This parameter is the difference in the propagation delay over multiple parts for any two PECLx outputs at the same supply voltages, at the same temperature and in the same configuration.

Note 6: An LTC6950 configured with an individual block powered down will add the specified supply current delta when powered up. Similarly, the specified supply current delta will subtract from the total chip supply current when the block is powered down. Except when noted, the supply current comes from the 3.3V supplies (V^+, V_{REF}^+, V_{VCO}^+, V_{P0}^+, V_{P1}^+, V_{P2}^+, V_{P3}^+)

Note 7: Additive phase noise and jitter are the phase noise added by the LTC6950. It does not include noise from the external signal source.

Note 8: VCO is a Crystek CVCSO-914-1000 voltage controlled SAW oscillator

Note 9: f_{VCO} = 1GHz, f_{OFFSET} = 5MHz

Note 10: Measured inside the loop bandwidth with the loop locked.

Note 11: Reference frequency supplied by a Wenzel 501-04517D, f_{REF} = 100MHz.

Note 12: Output phase noise floor is calculated from normalized phase noise floor by $L_{M(OUT)} = –226 + 10\log_{10}(f_{PFD}) + 20\log_{10}(f_{OUT}/f_{PFD})$.

Note 13: Output 1/f phase noise is calculated from normalized 1/f phase noise by $L_{M(OUT-1/f)} = –274 + 20\log_{10}(f_{OUT}) – 10\log_{10}(f_{OFFSET})$.

Note 14: I_{CP} = 11.2mA, f_{PFD} = 5MHz, Loop BW = 13.6kHz, IBIASx = 1.

Note 15: I_{CP} = 11.2mA, f_{PFD} = 100MHz, Loop BW = 12kHz, IBIASx = 1.

Note 16: Measured using DC1795.

Note 17: Reference frequency is supplied by a Wenzel 501-04609A, f_{REF} = 10MHz.

Note 18: VCO is a Crystek CVSS-945-125.000 voltage controlled crystal oscillator. I_{CP} = 11.2mA, f_{PFD} = 5MHz, Loop BW = 250Hz, IBIASx = 1.

Note 19: I_{CP} = 11.2mA, f_{PFD} = 10MHz, Loop BW = 4kHz, IBIASx = 1.

Note 20: VCO is a Crystek CVCO55CC-1220-1340 voltage controlled oscillator. Reference frequency is supplied by a Crystek CCHD-957-25-49.152, f_{REF} = 49.152MHz. I_{CP} = 11.2mA, f_{PFD} = 49.152MHz, Loop BW = 26kHz, IBIASx = 1.

Note 21: Reference frequency is supplied by a Wenzel 501-04605D, f_{REF} = 5MHz.

Note 22: The outputs are differentially terminated with a 100Ω resistor across PECLx$^+$ and PECLx$^–$ at the far-end. The internal DC bias is enabled by programming IBIASx = 1.

Note 23: PECLx$^+$ and PECLx$^–$ are each AC-coupled to a 50Ω termination resistor at the far end. DC bias for PECLx$^+$ and PECLx$^–$ is provided by a 150Ω resistor to ground on each output. Internal bias is disabled by programming IBIASx = 0.

Note 24: Default LTC6950 configuration, with the following changes: PDPLL = 1, PDREFAC = 1, PDVCOAC = 1, PD_DIV1 = 1, PD_DIV2 = 1, PD_OUT1 = 1, PD_OUT2 = 1, IBIAS0 = 1, IBIAS3 = 1

Note 25: PD_DIV4 = 1, PD_OUT4 = 1

Note 26: RDIVOUT = 0, LVCMS = 1

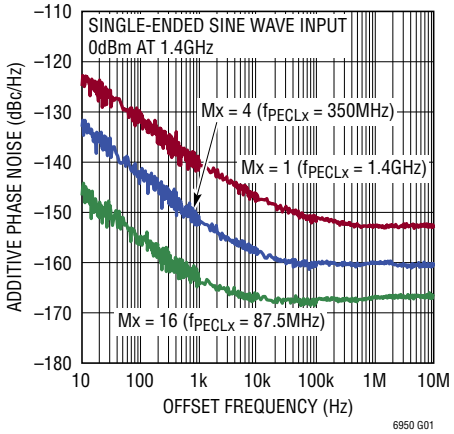
Note 27: RDIVOUT = 0, CMSINV = 1

Note 28: Do not apply a voltage or current source to these output pins. They must only be connected to input buffers and any associated level-shift or termination circuitry as described in the Applications Information section.

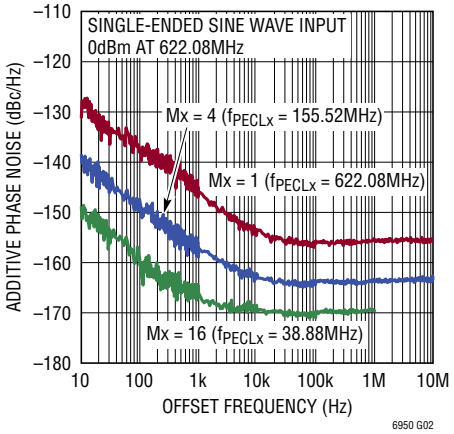
TYPICAL PERFORMANCE CHARACTERISTICS

$V^+ = V_{REF}^+ = V_{VCO}^+ = V_{P0}^+ = V_{P1}^+ = V_{P2}^+ = V_{P3}^+ = 3.3V$, $V_{CP}^+ = 5V$ and $T_A = 25°C$ unless otherwise specified. All voltages are with respect to ground.

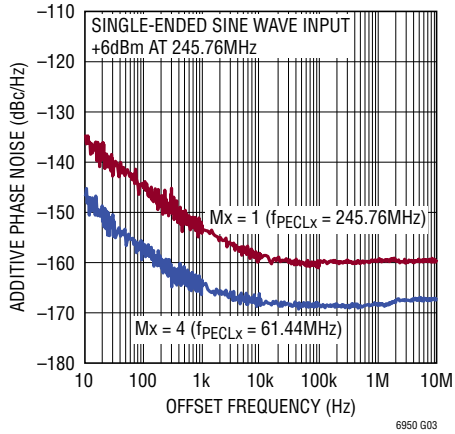
PECLx Additive Phase Noise with 1.4GHz Input (IBIASx = 1)



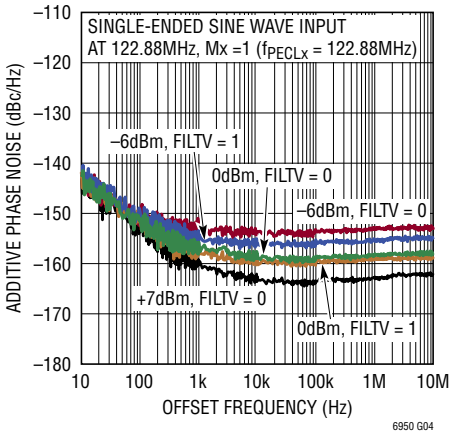
PECLx Additive Phase Noise with 622.08MHz Input (IBIASx = 1)



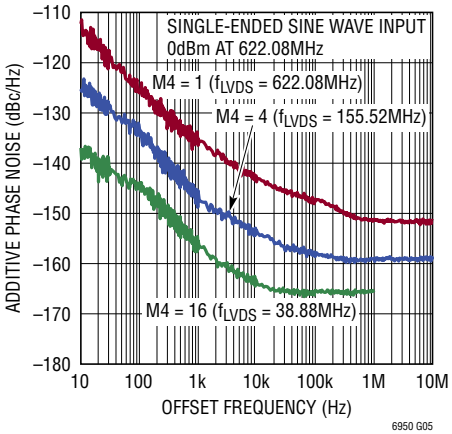
PECLx Additive Phase Noise with 245.76MHz Input (IBIASx = 1)



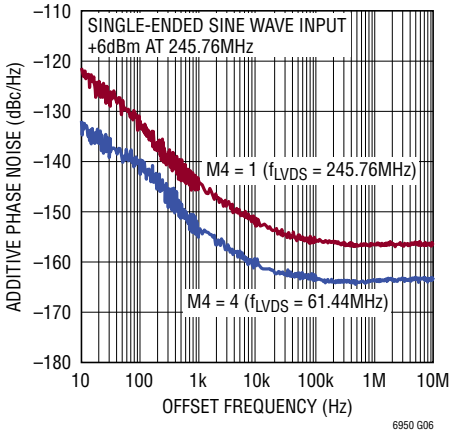
PECLx Additive Phase Noise vs Amplitude (IBIASx = 1)



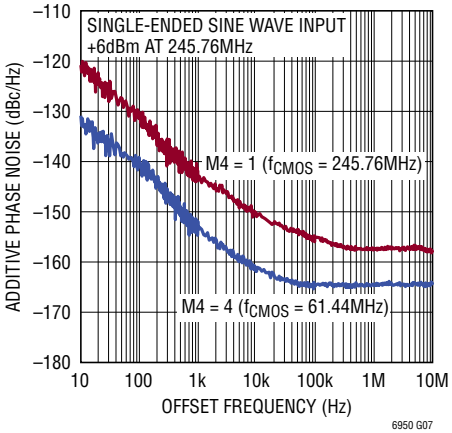
LVDS Additive Phase Noise with 622.08MHz Input



LVDS Additive Phase Noise with 245.76MHz Input



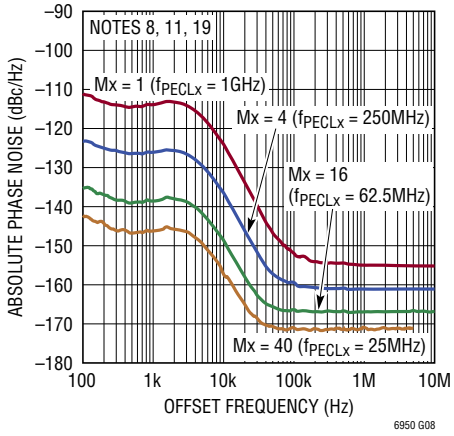
CMOS Additive Phase Noise with 245.76MHz Input (CMSINV = 1)



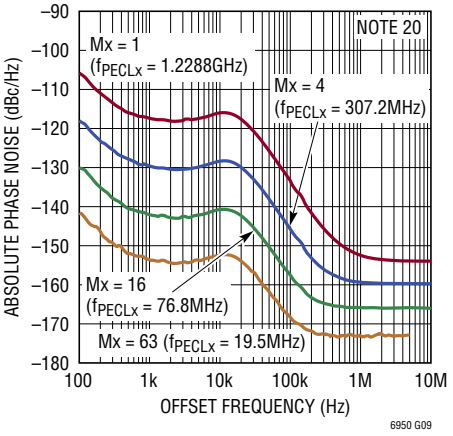
TYPICAL PERFORMANCE CHARACTERISTICS

$V^+ = V_{REF}^+ = V_{VCO}^+ = V_{P0}^+ = V_{P1}^+ = V_{P2}^+ = V_{P3}^+ = 3.3V$, $V_{CP}^+ = 5V$ and $T_A = 25°C$ unless otherwise specified. All voltages are with respect to ground.

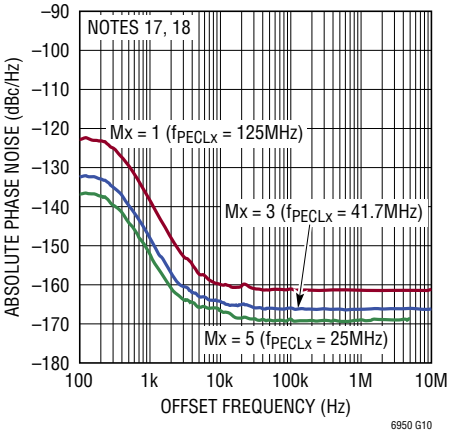
PECLx Closed-Loop Phase Noise VCSO Input at 1GHz



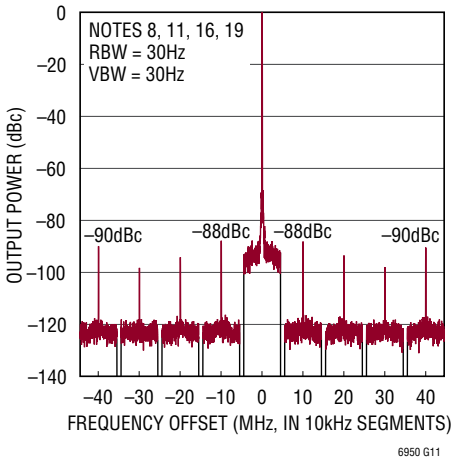
PECLx Closed-Loop Phase Noise VCO Input at 1.2288GHz



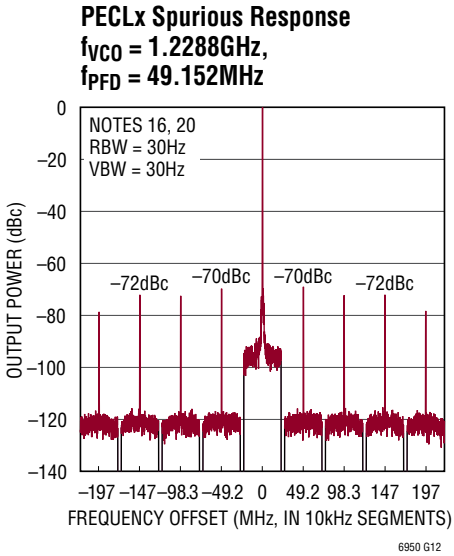
PECLx Closed-Loop Phase Noise VCXO Input at 125MHz



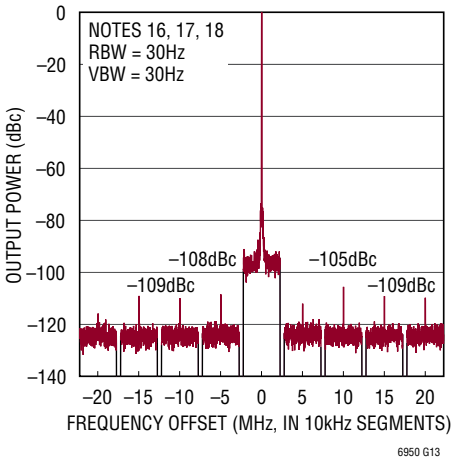
PECLx Spurious Response f_{VCSO} = 1GHz, f_{PFD} = 10MHz



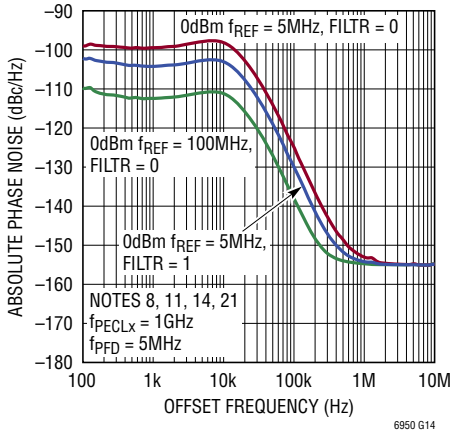
PECLx Spurious Response f_{VCO} = 1.2288GHz, f_{PFD} = 49.152MHz



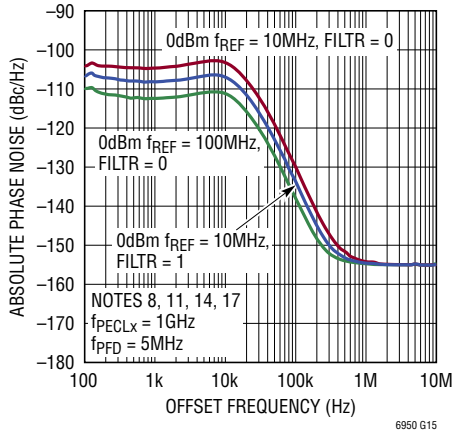
PECLx Spurious Response f_{VCXO} = 125MHz, f_{PFD} = 5MHz



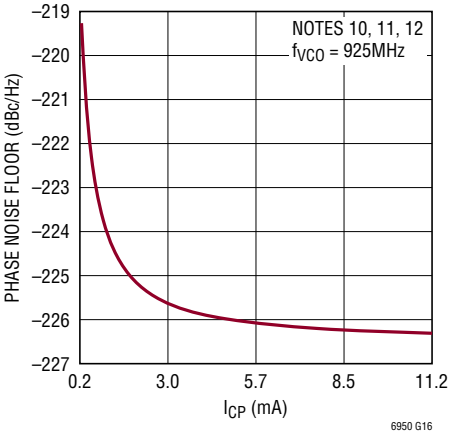
PECLx Closed-Loop Phase Noise 5MHz vs 100MHz Sine Wave Reference Input



PECLx Closed-Loop Phase Noise 10MHz vs 100MHz Sine Wave Reference Input



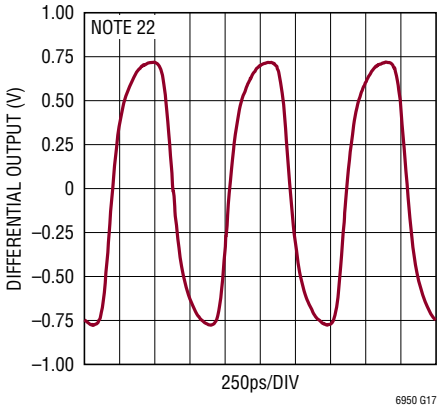
Normalized In-Band Phase Noise Floor vs Charge Pump Current



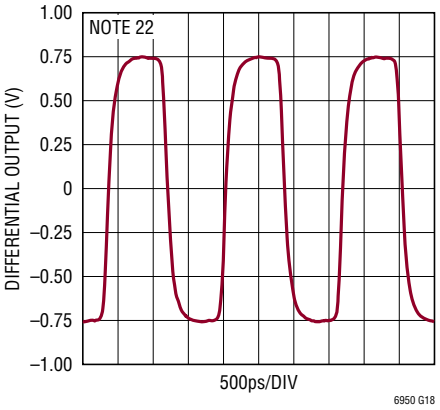
TYPICAL PERFORMANCE CHARACTERISTICS

$V^+ = V_{REF}^+ = V_{VCO}^+ = V_{P0}^+ = V_{P1}^+ = V_{P2}^+ = V_{P3}^+ = 3.3V$, $V_{CP}^+ = 5V$ and $T_A = 25°C$ unless otherwise specified. All voltages are with respect to ground.

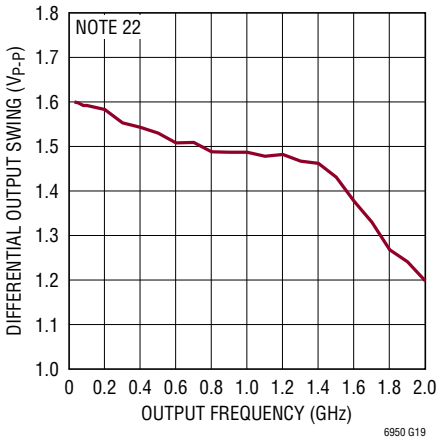
PECLx Differential Output at 1.2GHz (IBIASx = 1)



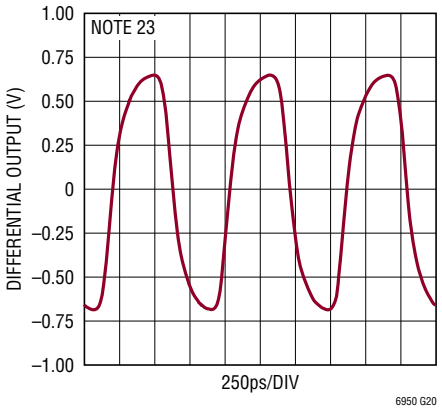
PECLx Differential Output at 600MHz (IBIASx = 1)



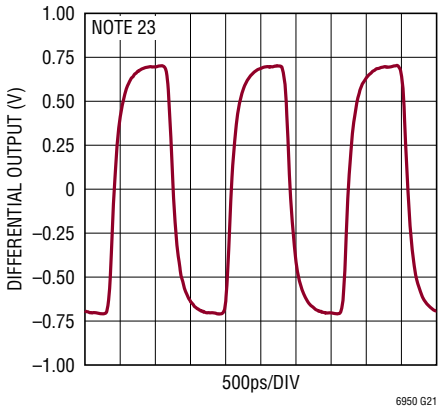
PECLx Differential Output Swing vs Frequency (IBIASx = 1)



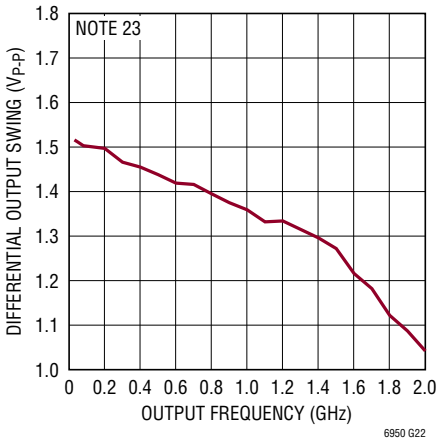
PECLx Differential Output at 1.2GHz (IBIASx = 0)



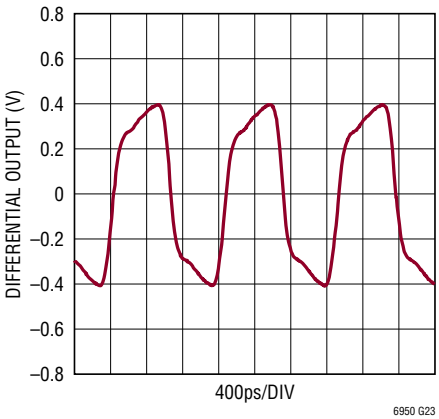
PECLx Differential Output at 600MHz (IBIASx = 0)



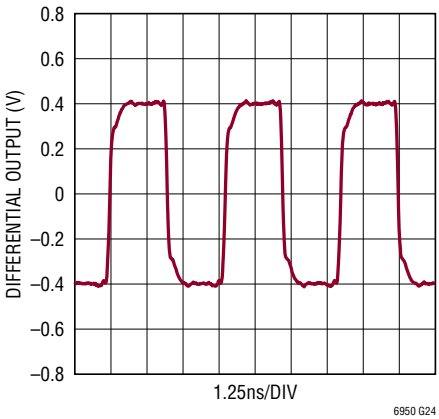
PECLx Differential Output Swing vs Frequency (IBIASx = 0)



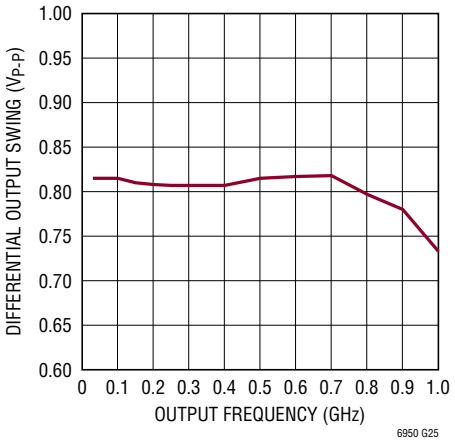
LVDS Output at 800MHz



LVDS Output at 250MHz



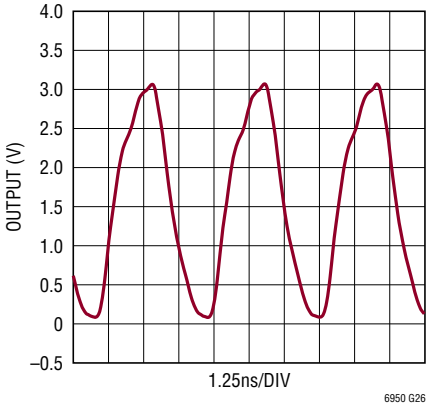
LVDS Output Swing vs Frequency



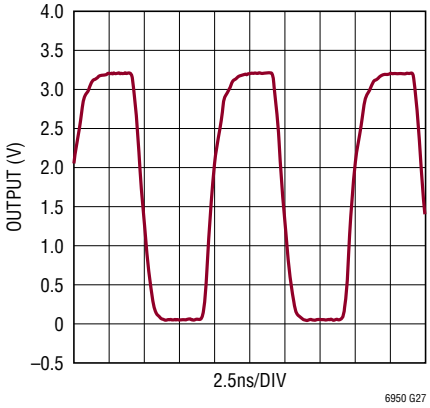
TYPICAL PERFORMANCE CHARACTERISTICS

$V^+ = V_{REF}^+ = V_{VCO}^+ = V_{P0}^+ = V_{P1}^+ = V_{P2}^+ = V_{P3}^+ = 3.3V$, $V_{CP}^+ = 5V$ and $T_A = 25°C$ unless otherwise specified. All voltages are with respect to ground.

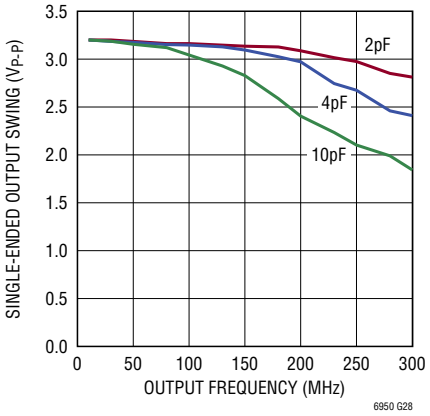
CMOS Single-Ended Output at 250MHz (2pF Load, CMSINV = 1)



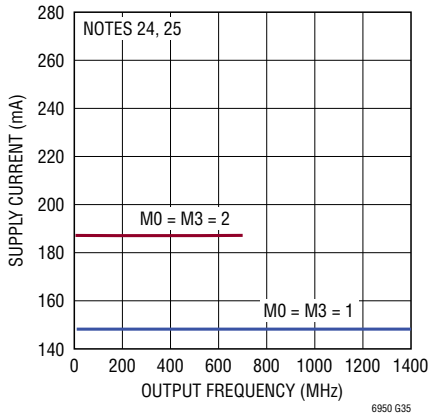
CMOS Single-Ended Output at 100MHz (2pF Load, CMSINV = 1)



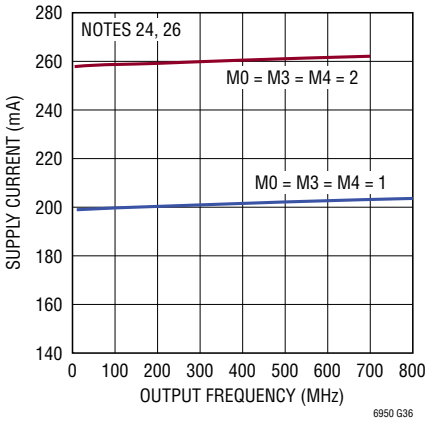
CMOS Single-Ended Output Swing vs Frequency (CMSINV = 1)



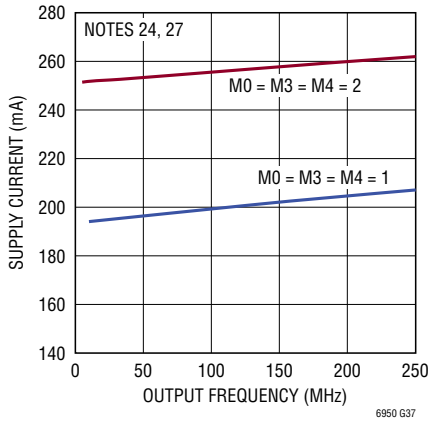
Supply Current vs Frequency PECL0 and PECL3 On



Supply Current vs Frequency PECL0, PECL3 and LVDS On



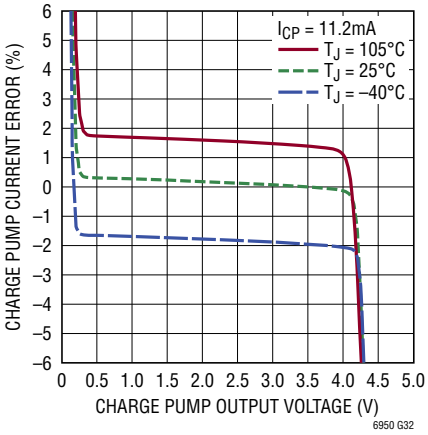
Supply Current vs Frequency PECL0, PECL3 and CMOS On



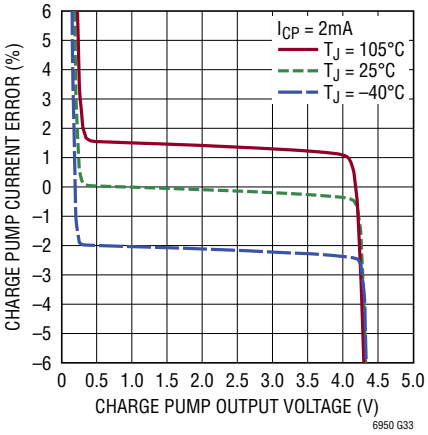
TYPICAL PERFORMANCE CHARACTERISTICS

$V^+ = V_{REF}^+ = V_{VCO}^+ = V_{P0}^+ = V_{P1}^+ = V_{P2}^+ = V_{P3}^+ = 3.3V$, $V_{CP}^+ = 5V$ and $T_A = 25°C$ unless otherwise specified. All voltages are with respect to ground.

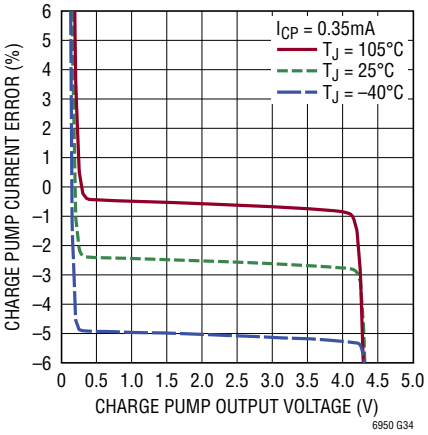
Charge Pump Source Current Error vs Voltage, Temperature (I_{CP} = 11.2mA)



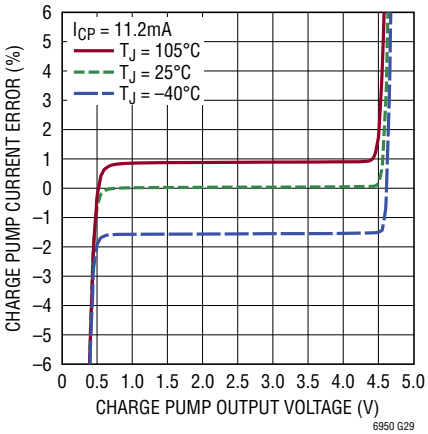
Charge Pump Source Current Error vs Voltage, Temperature (I_{CP} = 2mA)



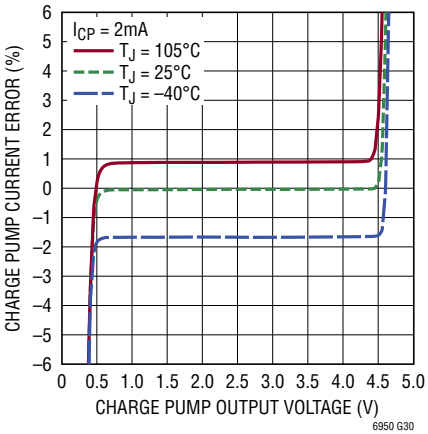
Charge Pump Source Current Error vs Voltage, Temperature (I_{CP} = 0.35mA)



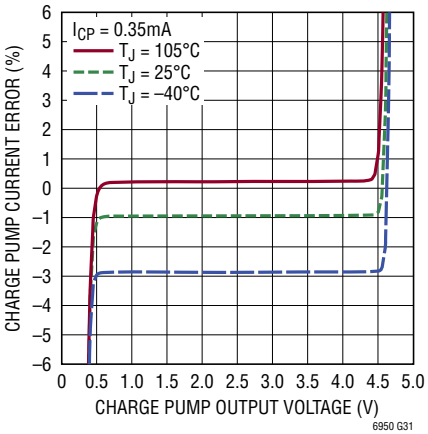
Charge Pump Sink Current Error vs Voltage, Temperature (I_{CP} = 11.2mA)



Charge Pump Sink Current Error vs Voltage, Temperature (I_{CP} = 2mA)



Charge Pump Sink Current Error vs Voltage, Temperature (I_{CP} = 0.35mA)



PIN FUNCTIONS

V_{P3}^+, V_{P2}^+, V_{P1}^+, V_{P0}^+ (Pins 1, 4, 5, 8, 9, 12, 13, 16): PECLx Output Supply Voltages. The supply range is from 3.15V to 3.45V. This supply should be kept free of noise and ripple. The use of a low impedance power plane is recommended. All V_{PX}^+ pins must be connected to the same supply voltage as the V^+ pins. Each pin, or in some cases pin pairs, must be separately bypassed directly to GND with a 0.01µF ceramic capacitor as close to the pin as possible. Refer to the Applications Information section for more details on supply connections and bypassing.

PECL3⁻, PECL3⁺ (Pins 2, 3): LVPECL Logic Compatible Output Pins. Differential logic outputs typically terminated by 50Ω connected to a supply 2V below the V_{P3}^+ supply. Refer to the Operation and the Applications Information sections for more details.

PECL2⁻, PECL2⁺ (Pins 6, 7): LVPECL Logic Compatible Output Pins. Differential logic outputs typically terminated by 50Ω connected to a supply 2V below the V_{P2}^+ supply. Refer to the Operation and the Applications Information sections for more details.

PECL1⁻, PECL1⁺ (Pins 10, 11): LVPECL Logic Compatible Output Pins. Differential logic outputs typically terminated by 50Ω connected to a supply 2V below the V_{P1}^+ supply. Refer to the Operation and the Applications Information sections for more details.

PECL0⁻, PECL0⁺ (Pins 14, 15): LVPECL Logic Compatible Output Pins. Differential logic outputs typically terminated by 50Ω connected to a supply 2V below the V_{P0}^+ supply. Refer to the Operation and the Applications Information sections for more details.

GND (Pins 17, 31, 38, 41, 48): Ground Connections. Should be tied directly to the die attach paddle (DAP) and to a low impedance ground plane for best performance. Refer to the Applications Information section for more details on grounding for signal integrity and thermal considerations.

V^+ (Pins 18, 19, 20, 25, 32, 37, 42, 47): Positive Supply Voltage. The supply range is from 3.15V to 3.45V. This supply should be kept free of noise and ripple. The use of a low impedance power plane is recommended. All V^+ pins must be connected to the same supply voltage. Each pin, or in some cases pin pairs, must be separately bypassed directly to GND with a 0.01µF ceramic capacitor as close to the pin as possible. Refer to the Applications Information section for more details on supply connections and bypassing.

LV/CM⁻, LV/CM⁺ (Pins 21, 22): LVDS/CMOS Logic Output Pins. These outputs may be programmed as either LVDS or CMOS logic outputs using the serial port. Refer to the Operation and the Applications Information sections for more details.

$\overline{CS}$ (Pin 23): Serial Port Chip Select Input. This active low CMOS logic input initiates a serial port transaction when brought to a logic low. It finalizes the serial port transaction when brought to a logic high after 16 serial port clock cycles. Refer to the Operation section for more details.

SDO (Pin 24): Serial Port Data Output. Data read from the serial port is presented on this CMOS three-state logic pin. Optionally attach a resistor of >200k to GND to prevent a floating output. Refer to the Operation section for more details.

SCLK (Pin 26): Serial Port Clock Input. This positive edge triggered CMOS logic input signal clocks serial port data in on rising edges. Refer to the Operation section for more details.

SDI (Pin 27): Serial Port Data Input. Data written into the serial port is presented on this CMOS logic pin. Refer to the Operation section for more details.

STAT2, STAT1 (Pins 28, 29): Status Output Pins. These CMOS outputs are configured through the serial port to provide direct status of critical signals that are monitored on-chip. Examples include the lock indicator and REF signal present. Refer to the Operation section for more details.

PIN FUNCTIONS

SYNC (Pin 30): Synchronization Input Pin. A rising edge on this CMOS logic input initiates an output clock synchronization sequence. Precision output synchronization of one or more parts is handled on chip, so the timing of this signal is not critical. Refer to the Operation and the Applications Information sections for more details.

V_{VCO}^+ (Pins 33, 36): VCO Input Supply Voltage. The supply range is from 3.15V to 3.45V. This supply should be kept free of noise and ripple. The use of a low impedance power plane is recommended. Both V_{VCO}^+ pins must be connected to the same supply voltage as the V^+ pins. Each pin must be separately bypassed directly to GND with a 0.01µF ceramic capacitor as close to the pin as possible. Refer to the Applications Information section for more details on supply connections and bypassing.

VCO^+, VCO^- (Pins 34, 35): VCO Input Pins. The VCO signal can be either differential or single-ended. It can be a sine wave, LVPECL logic or LVDS logic. Refer to the Operation and the Applications Information sections for more details on the correct use of the VCO inputs.

V_{CP}^+ (Pin 39): Charge Pump Supply Voltage. This supply should be kept free of noise and ripple. This pin can go above the V^+ supply up to 5.25V maximum supply. It must be bypassed directly to GND with a 0.1µF ceramic capacitor as close to the pin as possible. Refer to the Applications Information section for more details on the charge pump supply bypassing.

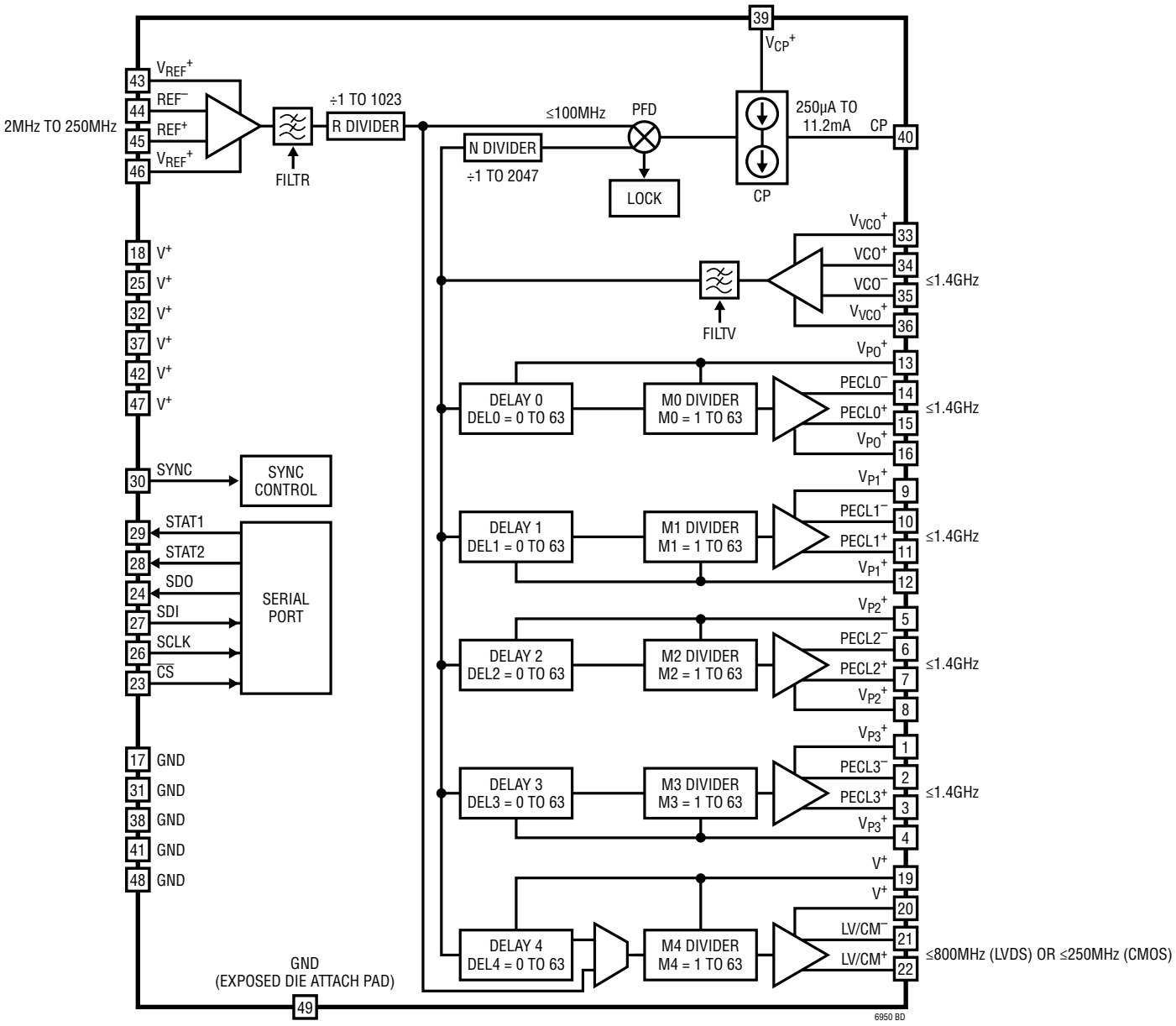
CP (Pin 40): Charge Pump Output Pin. This pin typically connects directly to the VCO tune input to close the PLL loop. Shunt capacitive and resistive elements are necessary to set the loop bandwidth and compensation. Refer to the Operation and the Applications Information sections for more details.

V_{REF}^+ (Pins 43, 46): REF Input Supply Voltage. The supply range is from 3.15V to 3.45V. This supply should be kept free of noise and ripple. The use of a low impedance power plane is recommended. Both V_{REF}^+ pins must be connected to the same supply voltage as the V^+ pins. Each pin must be separately bypassed directly to GND with a 0.01µF ceramic capacitor as close to the pin as possible. Refer to the Applications Information section for more details on supply connections and bypassing.

REF^-, REF^+ (Pins 44, 45): Reference Input Pins. The reference input signal can be either differential or single-ended. It can be a sine wave, LVPECL logic, LVDS logic or CMOS logic. Refer to the Operation and the Applications Information sections for more details on the correct use of the reference inputs.

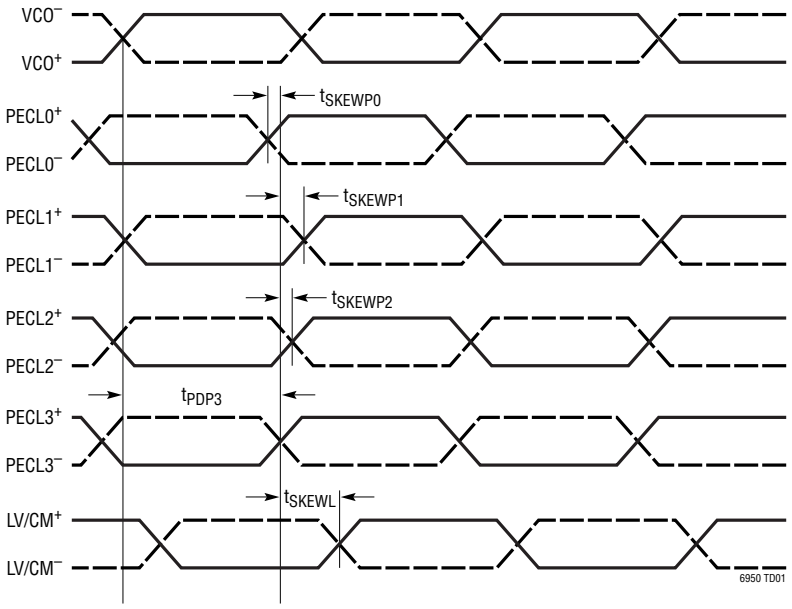
GND (Exposed Pad Pin 49): Ground Connection. The package exposed pad must be soldered directly to the PCB land. The PCB land pattern should have multiple thermal vias to the ground plane for both low ground inductance and also low thermal resistance. Refer to the Applications Information section for more details on grounding for signal integrity and thermal considerations.

BLOCK DIAGRAM

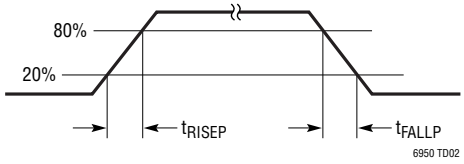


TIMING DIAGRAMS

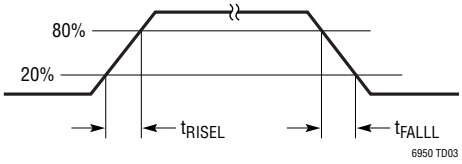
Output Propagation Delays and Skews, Mx[5:0] = 1



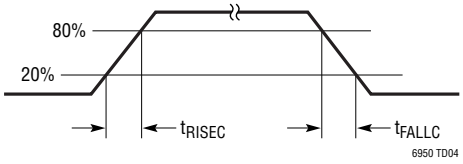
Single-Ended PECLx Rise/Fall Times



Differential LVDS Rise/Fall Times



Single-Ended CMOS Rise/Fall Times



OPERATION

LTC6950 INTRODUCTION

The LTC6950 is a low phase noise integer-N frequency synthesizer core with clock distribution. The LTC6950 delivers the low phase noise and low jitter clock signals demanded in high frequency, high resolution data acquisition systems. As shown in Figure 1, the LTC6950 consists of three distinct circuit sections: phase-locked loop (PLL) core, clock distribution and digital control.

The PLL section of the LTC6950 contains a low noise integer-N PLL core with a programmable reference divider (R), a programmable feedback divider (N), a phase/frequency detector (PFD) and a low noise charge pump (CP). The charge pump's low noise and well balanced design delivers the LTC6950's –226dBc/Hz normalized PLL in-band phase noise floor. To form a complete frequency synthesizer, both an external reference oscillator and a voltage controlled oscillator (VCO) are required.

OPERATION

The clock distribution section of the LTC6950 receives a VCO input signal with a maximum frequency of 1.4GHz and delivers five output signals based on the VCO input. Each output is individually programmed to divide the VCO input frequency by any integer from 1 to 63 and to delay the output by 0 to 63 VCO clock cycles. For a VCO input with a 50% duty cycle, the output duty cycle will always be 50% regardless of the divide number. Four outputs feature very low noise, low skew LVPECL logic signals capable of operation up to 1.4GHz. The fifth output is selectable as either an LVDS (800MHz) or a CMOS (250MHz) logic type. This fifth output is also programmed to produce an output signal based on either the VCO input or the reference divider output.

The digital control section contains a full SPI-compatible serial control bus along with two device status bits and the clock synchronization (SYNC) function. All device settings and operating modes are controlled through the SPI bus. The status output pins (STAT1 and STAT2) indicate the status of the part's input signals, the PLL lock state, the charge pump clamp condition or a logical combination of any of these signals. This is useful as an alert flag or to drive an LED for a visible PLL lock indicator.

To minimize power consumption, most sections of the LTC6950 can be powered down when not in use. As shown in Figure 2, the LTC6950 can be used as a full PLL synthesizer with clock distribution. Any unused outputs from the clock distribution section may be powered down. Alternatively, Figure 3 shows that the LTC6950 can also be used in a clock distribution application with the PLL section powered down.

Figure 4 highlights two LTC6950 parts cascaded as CONTROLLER and FOLLOWER devices. This example shows a single FOLLOWER device, but each output from the CONTROLLER device can control separate FOLLOWER devices for support of up to five FOLLOWER devices. The LTC6950's EZSync multichip synchronization feature assures consistent edge alignment of all outputs from all devices. See the EZSync Clock Output Synchronization section for more details on EZSync operation.

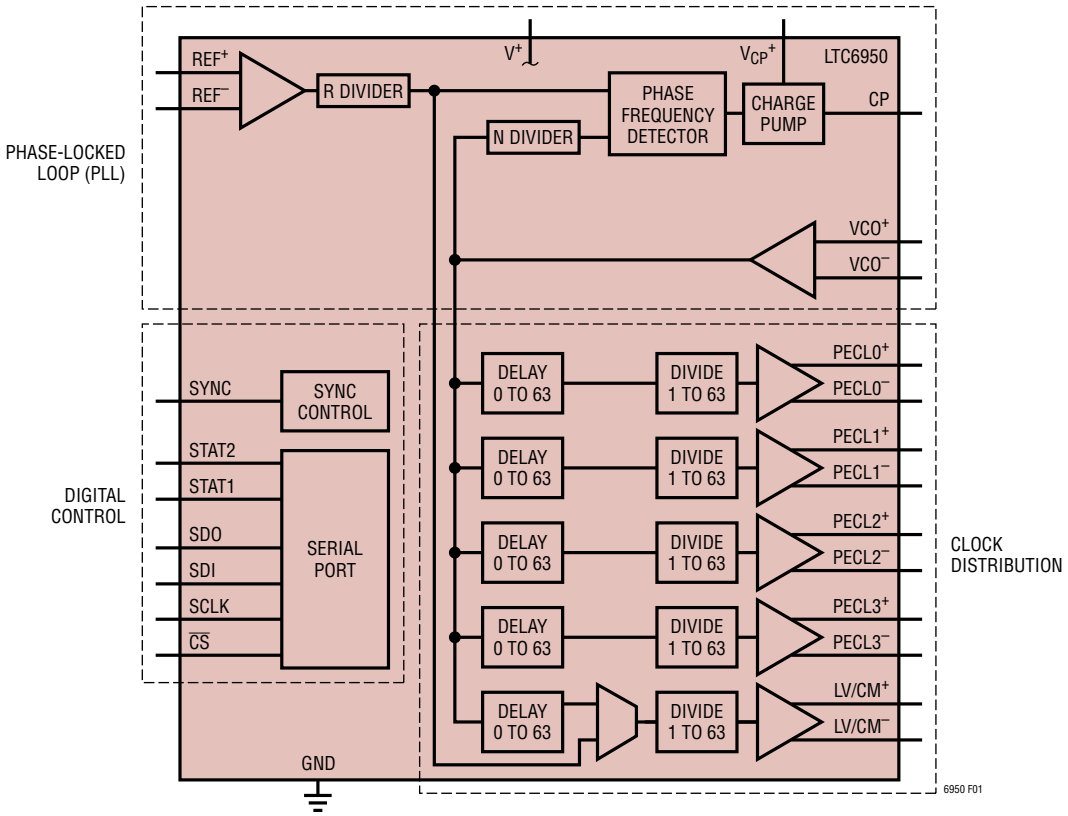


Figure 1. The LTC6950 Highlighting the Three Main Circuit Blocks

OPERATION

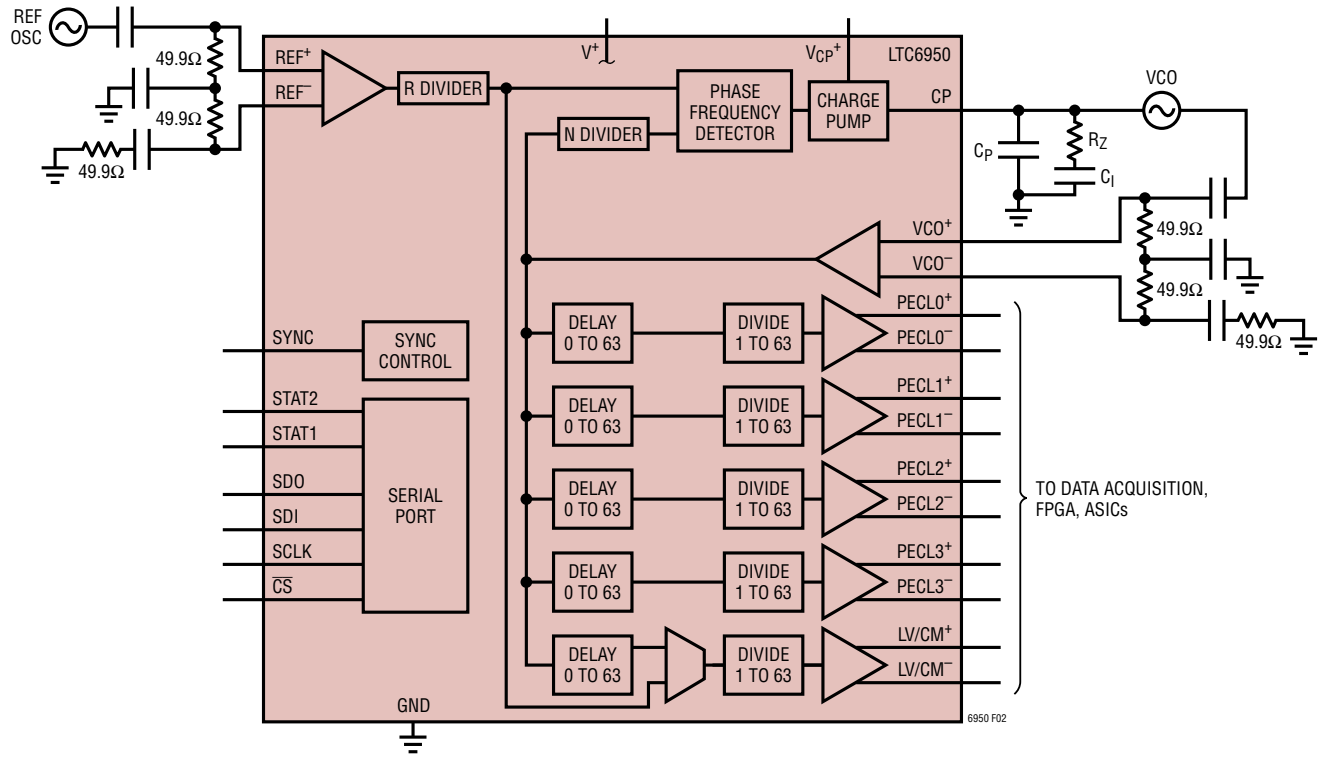


Figure 2. The LTC6950 Connected in PLL plus Clock Distribution Mode (Single-Ended, 50Ω Output Reference Oscillator and VCO Shown as an Example)

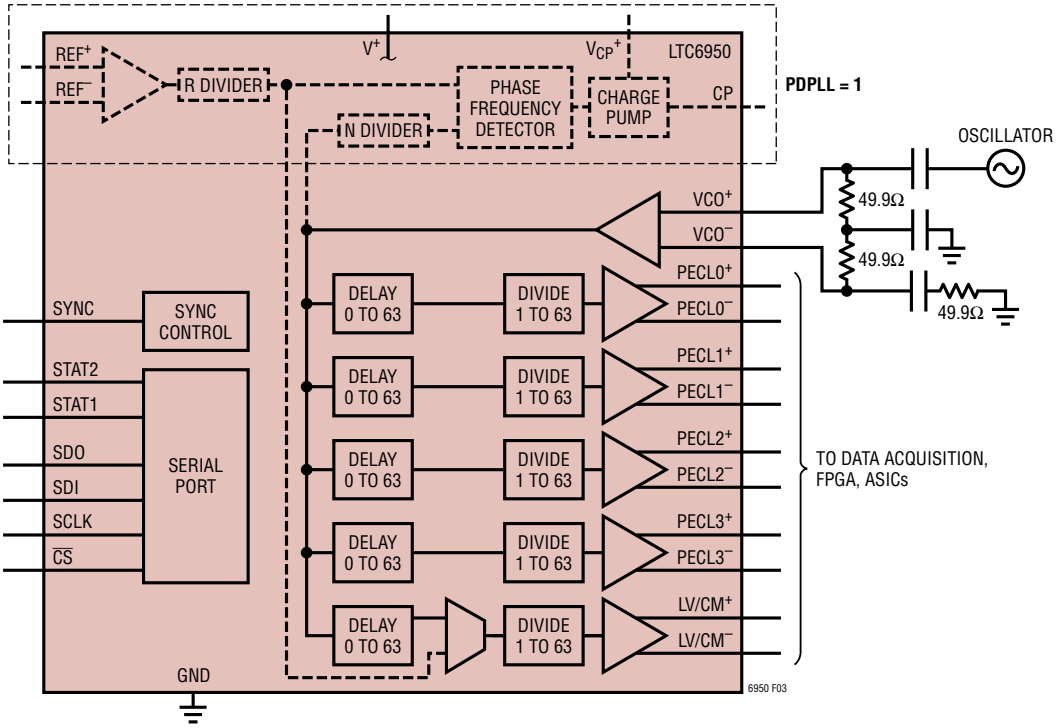


Figure 3. The LTC6950 Connected in Clock Distribution Only Mode with the PLL Section Powered Down (Single-Ended, 50Ω Output Oscillator Shown as an Example)

OPERATION

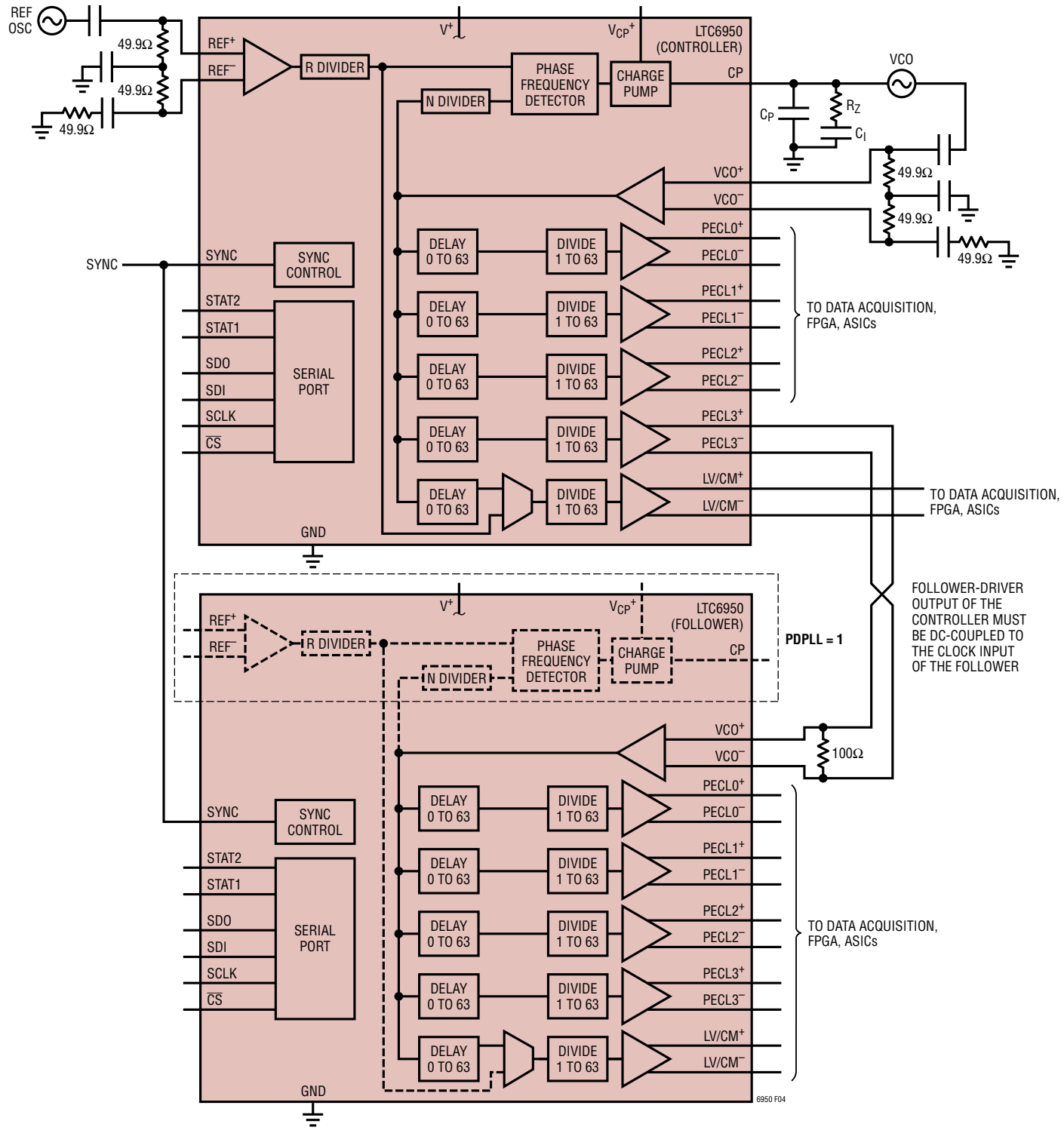


Figure 4. The LTC6950 in PLL plus Clock Distribution Mode (CONTROLLER) Clocking Another LTC6950 in Clock Distribution Only Mode (FOLLOWER). For Best Performance Use One of the PECLx Outputs from the CONTROLLER LTC6950 (with its IBIASx Enabled) to Clock the FOLLOWER LTC6950 with its PLL Section Powered Down. (Single-Ended, 50Ω Output Reference Oscillator and VCO Shown as an Example)

OPERATION

PHASE-LOCKED LOOP

The LTC6950 contains a high performance phase-locked loop (PLL), including low noise reference and VCO input buffers and dividers, phase/frequency detector (PFD), charge pump and lock indicator. The following section describes the function of these different blocks.

REFERENCE INPUT BUFFER

The LTC6950's reference input buffer provides a flexible interface to either differential or single-ended frequency sources. The frequency range for the reference input is from 2MHz to 250MHz. A differential LVPECL reference source may be applied directly to the REF± pins with a 100Ω differential far-end termination. A single-ended reference frequency source may also be used, as long as its peak-to-peak output swing is less than 1.5V to avoid turning on the input protection diodes (see Figure 5).

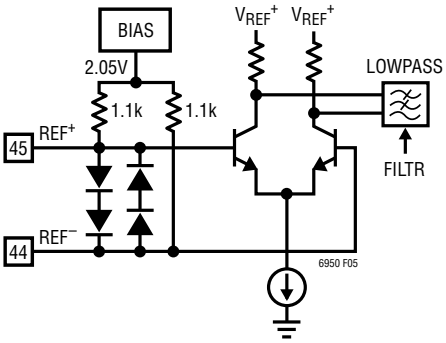


Figure 5. Simplified Reference Input Schematic

Because the signal applied to the REF± inputs provides the frequency reference for the PLL, it is important that this frequency source have low phase noise and a slew rate of at least 100V/µs. For applications where using a reference source with an output slew rate at least 100V/µs is not possible, better phase noise performance will be achieved by enabling the internal broadband noise filtering circuit within the reference input buffer. This is accomplished by asserting the configuration bit FILTR in serial port register h0B. Note that setting FILTR = 1 when the slew rate of the reference frequency source is greater than 100V/µs will degrade the overall PLL phase noise performance. See the Applications Information section for more information on REF input signal requirements and interfacing.

REFERENCE INPUT SIGNAL PRESENT

A reference input signal present circuit is also connected to the REF± pins of the LTC6950. The signal present circuit detects when either a single-ended or differential AC-frequency is applied to the REF± pins, and asserts the status flag NO_REF, found in register h00, when no signal is found. For a reference frequency between 2MHz and 250MHz, NO_REF will go high when the differential input applied at REF± is less than $100mV_{P-P}$. For an applied differential signal greater than $350mV_{P-P}$, the NO_REF flag will remain low.

REFERENCE (R) DIVIDER

A 10-bit reference divider (R) is used to reduce the frequency seen at the PFD. Its divide ratio may be set to any integer from 1 to 1023, inclusive, by directly programming the R[9:0] bits found in registers h07 and h08. The programmed value of R[9:0] will automatically be read when the R divider reaches its terminal count, but this could theoretically take 1023 cycles of the reference input.

For applications where this delay is too long, it may be useful to force a load of the programmed divide ratio by asserting the configuration bit RESET_R in serial port register h07. Because the R divider does not transition while RESET_R = 1, it must then be programmed back to 0 before the R divider will resume dividing. See the Applications Information section for the relationship between R and the f_{REF}, f_{PFD} and f_{VCO} frequencies.

VCO INPUT BUFFER

The LTC6950's VCO input buffer provides a flexible interface to either differential or single-ended frequency sources. The maximum VCO input frequency is 1.4GHz. A differential VCO/VCXO/VCSO may be applied directly to the VCO± pins with a 100Ω differential far-end termination. Alternatively, a single-ended input may also be used, as long as its signal swing is less than $1.5V_{P-P}$ to avoid turning on the input protection diodes (see Figure 6).

It is also important that the VCO± inputs be low noise and have a slew rate of at least 100V/µs, although better performance will be achieved with a higher slew rate. For applications where using a VCO/VCXO/VCSO with an

OPERATION

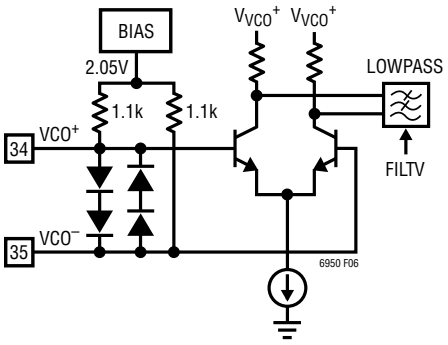


Figure 6. Simplified VCO Input Schematic

output slew rate at least 300V/µs is not possible, better phase noise performance will be achieved by enabling the internal broadband noise filtering circuit within the VCO input buffer. This is accomplished by asserting the configuration bit FILTV in serial port register h0B. Note that setting FILTV = 1 when the slew rate of the reference frequency source is greater than 300V/µs will degrade the overall PLL phase noise performance. See the Applications Information section for more information on VCO input signal requirements and interfacing.

VCO INPUT SIGNAL PRESENT

A VCO input signal present circuit is also connected to the VCO± pins of the LTC6950. The signal present circuit detects when either a single-ended or differential AC-frequency is applied to the VCO± pins, and asserts the status flag NO_VCO found in register h00 when no signal is found. For a VCO frequency between 30MHz and 1.4GHz, NO_VCO will go high when the differential input applied at VCO± is less than $100mV_{P-P}$. For an applied differential signal greater than $350mV_{P-P}$, the NO_VCO flag will remain low.

VCO (N) DIVIDER

An 11-bit VCO feedback divider (N) is used to reduce the VCO frequency that is seen at the PFD. Its divide ratio may be set to any integer from 1 to 2047, inclusive, by directly programming the N[10:0] bits found in registers h09 and h0A. The programmed value of N[10:0] will automatically be read when the N divider reaches its terminal count, but this can theoretically take 2047 cycles of the VCO input.

For applications where this delay is too long, it may be useful to force a load of the programmed divide ratio by asserting the configuration bit RESET_N in serial port register h09. Because the N divider does not transition while RESET_N = 1, it must then be programmed back to 0 before the N divider will resume dividing. See the Applications Information section for the relationship between N and the f_{REF}, f_{PFD} and f_{VCO} frequencies.

PHASE-FREQUENCY DETECTOR

The phase-frequency detector (PFD), in conjunction with the charge pump, produces source and sink current pulses proportional to the phase difference between the outputs of the R and N dividers. This action provides the necessary feedback to phase lock the loop, forcing a phase alignment at the PFD's inputs. The PFD may be disabled with the CPRST bit, which prevents UP and DOWN pulses from being produced. See Figure 7 for a simplified schematic of the PFD.

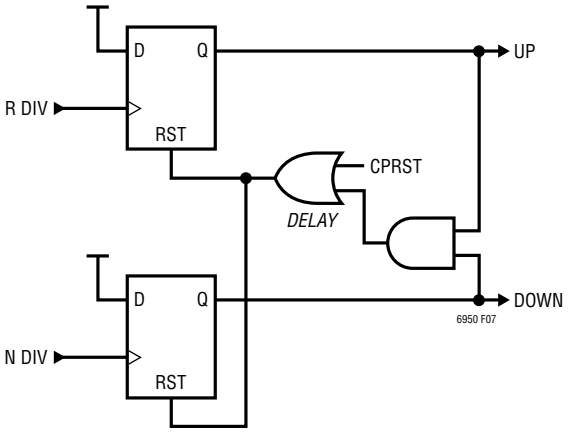


Figure 7. Simplified PFD Schematic

LOCK INDICATOR

The lock indicator uses internal signals from the PFD to measure phase coincidence between the R and N divider output signals. It is enabled by setting the lock enable (LKEN) bit in the serial port register h03 and produces both the loop locked (LOCK) status flag and the loop unlocked (UNLOCK) status flag. Note that the reference input frequency must be present for the LOCK and UNLOCK flags to properly assert and clear. The LOCK and UNLOCK

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flags may be accessed via serial port register h00 or by configuring the status registers, STAT1 or STAT2, to output these indicators.

The user sets the phase difference, or lock window width (t_{LWW}), for a valid loop locked condition with the LKWIN[1:0] bits found in serial port register h05. The loop is considered locked as long as the phase difference at the PFD is within t_{LWW}. Refer to Table 1 for recommended settings of t_{LWW} based on different PFD frequencies.

Table 1. Lock Window Programming (Register h05)

LKWIN[1:0]	t_{LWW}	f_{PFD}
0	3ns	>5MHz
1	10ns	≤5MHz
2	30ns	≤1.7MHz
3	90ns	≤550kHz

The PFD phase difference must be less than t_{LWW} for the LOCK_COUNT number of successive PFD cycle counts before the lock indicator asserts the LOCK flag. The LKCT[1:0] bits found in register h05 are used to set LOCK_COUNT depending upon the application. Choosing the correct LOCK_COUNT value depends upon the ratio of the bandwidth of the loop to the PFD frequency (BW/f_{PFD}). Smaller ratios dictate larger LOCK_COUNT values. See Table 2 for LKCT[1:0] programming and the Applications Information section for examples.

Table 2. Lock Count Programming (Register h05)

LKCT[1:0]	LOCK_COUNT
0	32
1	128
2	512
3	2048

When the PFD phase difference is greater than t_{LWW}, the lock indicator immediately asserts the UNLOCK status flag and clears the LOCK flag, indicating an out-of-lock condition. The UNLOCK flag is immediately de-asserted when the phase difference is less than t_{LWW}. The LOCK flag asserts only when the phase difference is within the t_{LWW} for LOCK_COUNT continuous PFD clock cycles. See Figure 8 for more details.

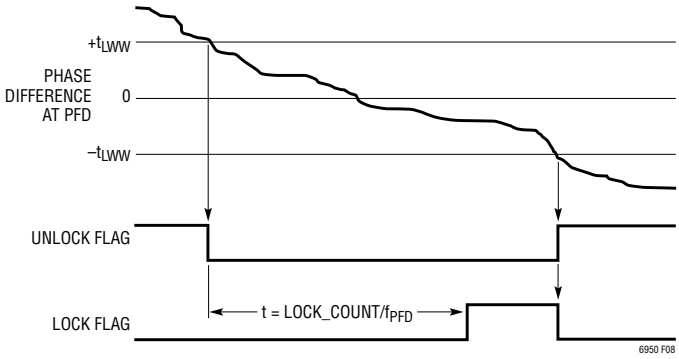


Figure 8. UNLOCK and LOCK Timing

CHARGE PUMP

The charge pump, controlled by the PFD, forces sink (DOWN) or source (UP) current pulses onto the CP pin, which should be connected to an appropriate loop filter. See Figure 9 for a simplified schematic of the charge pump.

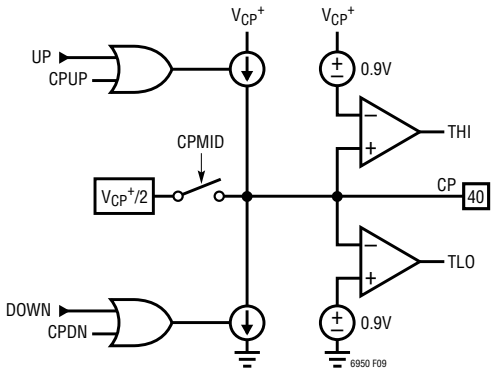


Figure 9. Simplified Charge Pump Schematic

The output current magnitude I_{CP} may be set from 250µA to 11.2mA using the CP[3:0] bits found in serial port register h05. A larger I_{CP} can result in lower in-band noise due to the lower impedance of the loop filter components. See Table 3 for programming specifics and the Applications Information section for loop filter examples.

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Table 3. Charge Pump Current Programming (Register h05)

CP[3:0]	I_{CP}
0	250µA
1	350µA
2	500µA
3	700µA
4	1.0mA
5	1.4mA
6	2.0mA
7	2.8mA
8	4.0mA
9	5.6mA
10	8.0mA
11	11.2mA
12	4.0mA
13	5.6mA
14	4.0mA
15	5.6mA

The CPINV bit found in register h06 should be set for applications requiring signal inversion from the PFD, such as for loops using negative-slope tuning oscillators or for complex external loops using an inverting op amp in conjunction with a positive-slope tuning oscillator. A passive loop filter used in conjunction with a positive-slope VCO requires no inversion, so CPINV = 0.

CHARGE PUMP FUNCTIONS

The charge pump contains several features to aid in system startup and monitoring. See Table 4 for a summary.

Table 4. Charge Pump Function Descriptions

BIT	DESCRIPTION
CPCHI	Enable High Voltage Output Clamp
CPCLO	Enable Low Voltage Output Clamp
CPDN	Force Sink Current
CPINV	Invert PFD Phase
CPMID	Enable Mid-Voltage Bias
CPRST	Reset PFD
CPUP	Force Source Current
CPWIDE	Extend Current Pulse Width
THI	High Voltage Clamp Flag
TLO	Low Voltage Clamp Flag

The CPCHI and CPCLO bits found in register h06 enable the high and low voltage clamps, respectively. When CPCHI is enabled and the CP pin voltage exceeds approximately $V_{CP}^+ - 0.9V$, the THI status flag is set, and the charge pump sourcing current is disabled. Alternatively, when CPCLO is enabled and the CP pin voltage is less than 0.9V, the TLO status flag is set, and the charge pump sinking current is disabled (see Figure 9).

The CPMID bit also found in register h06 enables a resistive $V_{CP}^+/2$ output bias, which may be used to pre-bias the charge pump into a valid voltage range. When using CPMID, it is recommended to assert the CPRST bit at the same time, forcing a PFD reset. Both CPMID and CPRST must be set to 0 for the loop to lock.

The CPUP and CPDN bits force a constant I_{CP} source or sink current, respectively, on the CP pin. The CPRST bit may also be used in conjunction with CPUP and CPDN to allow a pre-charge of the loop to a known state. CPUP, CPDN and CPRST must all be set to 0 for the loop to lock.

The CPWIDE bit extends the charge pump output current pulse width by increasing the PFD reset path's delay value. CPWIDE is normally set to 0.

CLOCK DISTRIBUTION

The LTC6950 also provides low noise clock distribution capability via five low skew distribution paths. Each distribution path includes an output divider, a VCO-cycle delay block and an output driver. In addition, the LTC6950 assures repeatable edge alignment of all outputs from all devices with the EZSync multichip synchronization feature. The output driver for four paths is LVPECL compatible. The remaining path provides a configurable LVDS or CMOS output driver. The following sections describe the different clock distribution blocks and the EZSync multichip synchronization feature.

OUTPUT (M) DIVIDER

Each clock distribution path includes a 6-bit output divider that reduces the input frequency by the programmed divide modulus, M. By programming the Mx[5:0] bits for each output divider, the divide modulus is set to any integer from 1 to 63, inclusive. When Mx[5:0] is programmed to

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a value of either 1 or 0, the output divider is bypassed and powered down. See Table 5 for a summary of the registers containing the output divider control bits for each clock output distribution path. See Table 11, Serial Port Register Mapping, for complete register mapping information.

Table 5. Output (M) Divider Control Registers

CLOCK OUTPUT	DIVIDE MODULUS	BITS	REG ADDR (HEX)
PECL0	M0	[5:0]	0D
PECL1	M1	[5:0]	0F
PECL2	M2	[5:0]	11
PECL3	M3	[5:0]	13
LV/CM	M4	[5:0]	15

For the four clock distribution paths employing LVPECL compatible output drivers (PECL0, PECL1, PECL2 and PECL3), the input to their respective output divider blocks is always the VCO. For these outputs, circuitry within the output divider ensures the output duty cycle will always be 50% for a programmed divide modulus greater than 1, as long as the VCO input duty cycle is approximately 50%. When the output divider has been programmed for a divide modulus of 1 or 0 (i.e. bypassed), the PECLx output duty cycle will be the same as that of the VCO input.

For the clock distribution path utilizing the LV/CM output driver, either the VCO or the R divider output may be selected as the input to the output divider block. Setting the RDIVOUT bit in register h15 to 0 selects the VCO as the input. In this case, the duty cycle behavior of the LV/CM output will be the same as the PECLx outputs. That is, for a programmed divide modulus greater than 1, the LV/CM output will always be 50%. Similarly, when the output divider has been bypassed, the LV/CM output duty cycle will match the VCO input duty cycle.

Setting the RDIVOUT bit to 1 selects the R divider output as the input to the LV/CM output divider. This configuration allows access to the reference divider output, which can be useful in applications that require operations consistently synchronized with the R divider. Note that in this configuration, the cycle delay capability is disabled for the LV/CM output. As a result, the LV/CM output will be unaffected by the programmed settings of SYNC_EN4, FLDRV4 or DEL4[5:0], since these configuration bits are ignored when RDIVOUT is set to 1. See the VCO-Cycle Delay section for more information.

When RDIVOUT is 1, the LV/CM output duty cycle may not be 50%, since the R divider output duty cycle is not necessarily 50%. For example, if the R divider is programmed to divide by 8, and the LV/CM output divider is bypassed (see Figure 10), the LV/CM output duty cycle will be identical to the R divider output duty cycle.

In another example using a similar configuration for the R divider, but where the LV/CM output divider is programmed to divide by two (see Figure 11), the output will in fact have a 50% duty cycle.

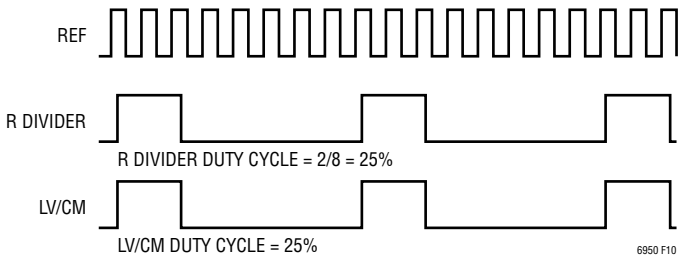


Figure 10. LV/CM Duty Cycle (R = 8, M4 = 1)

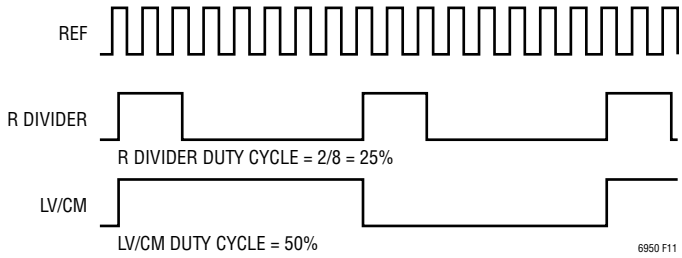


Figure 11. LV/CM Duty Cycle (R = 8, M4 = 2)

However, when the LV/CM output divider is programmed to divide by three, the output duty cycle will likely not be 50% because the R divider output duty cycle is not 50% in most configurations. (see Figures 12a, 12b and 12c).

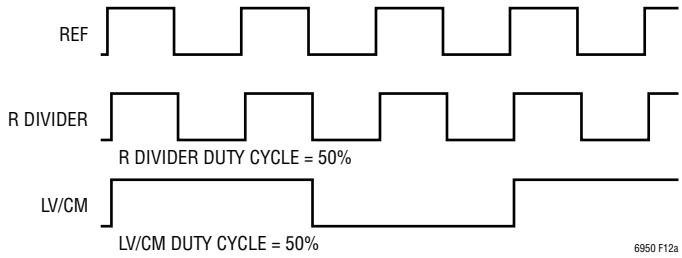


Figure 12a. LV/CM Duty Cycle (R = 1, M4 = 3)

OPERATION

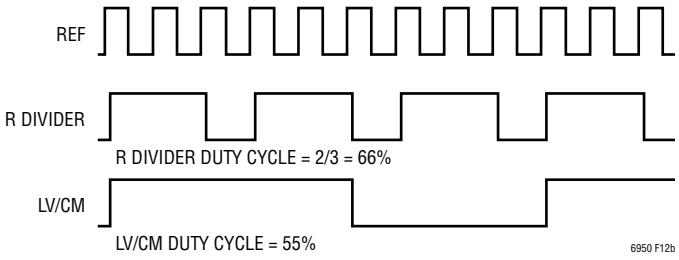


Figure 12b. LV/CM Duty Cycle (R = 3, M4 = 3)

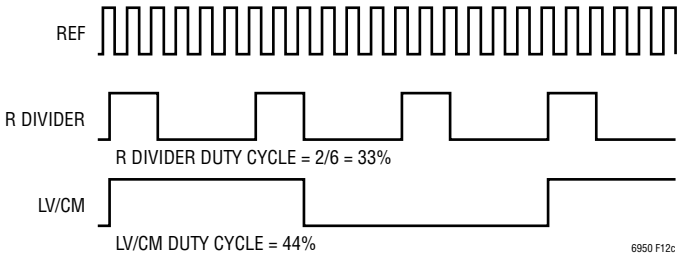


Figure 12c. LV/CM Duty Cycle (R = 6, M4 = 3)

In general, the LV/CM output duty cycle will be 50% for every even divide modulus. For most configurations using an odd divide modulus, the LV/CM output duty cycle can be computed with the following Equation 1:

$$DC_{LV/CM} = 50\% + \frac{1}{M4} \bullet \left(\frac{2}{R} - \frac{1}{2}\right) \bullet 100\% \quad R > 2, M4 \text{ odd} \qquad (1)$$

See Table 6 for a summary of LV/CM output duty cycle depending on configuration.

Table 6. LV/CM Duty Cycle (RDIVOUT = 1)

R[9:0]	M4[5:0]	$DC_{LV/CM}$
1	1	DC_{REF}
2	Don't Care	50%
Don't Care	Even	50%
1	>1, Odd	$50\% + \frac{1}{M4} \bullet \left(DC_{REF} - \frac{1}{2}\right) \bullet 100\%$
>2	Odd	$50\% + \frac{1}{M4} \bullet \left(\frac{2}{R} - \frac{1}{2}\right) \bullet 100\%$

VCO-CYCLE DELAY (DEL)

Each clock distribution path includes a 6-bit VCO-cycle delay block, which is used in conjunction with the synchronization input pin, SYNC, to force phase alignments of the various clock outputs. When the SYNC input de-asserts, the delay block begins counting VCO cycles. When the count reaches the programmed configuration for each path, the output driver begins transitioning. To save power, the VCO-cycle delay block powers down when all output phase alignments complete.

The number of cycles of delay adjustment allowed for each output may be any integer from 0 to 63, inclusive, and is configured by enabling the specific delay block and then directly programming the number of delay cycles into the appropriate DELx[5:0] bits. Setting the SYNC_ENx bit to 1 enables each delay block. Alternatively, setting SYNC_ENx to 0 results in the selected VCO-cycle delay block being bypassed and powered down.

Programming the RDIVOUT bit in register h15 to 1 bypasses and powers down the VCO-cycle delay block in the LV/CM clock distribution path. In this configuration there is no delay capability for the LV/CM distribution path.

Because the VCO-cycle delay block operates independently of the output divider block, the programmed VCO-cycle delay adjustment occurs regardless of the modulus setting of the output divider (see the example in Figure 13).

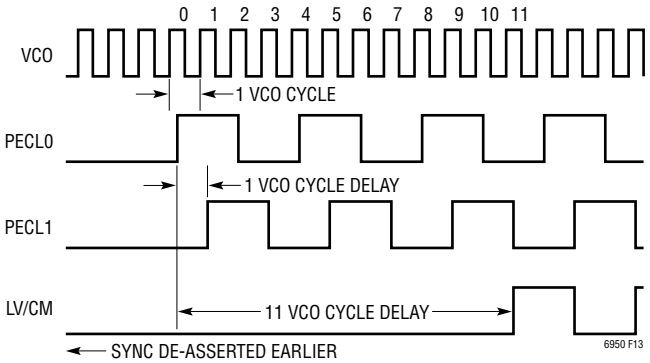


Figure 13. VCO DELAY Operation (M0 = M1 = M4 = 4, DEL0 = 0, DEL1 = 1, DEL4 = 11)

Refer to the EZSync Clock Output Synchronization section for more information about using the SYNC input pin to achieve specific output phase alignments.

See Table 7 for a summary of the registers containing the output delay control bits for each clock output distribution path. For complete register mapping information, see Table 11, Serial Port Register Mapping.

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Table 7. Output Delay (DEL) Control Registers

CLOCK OUTPUT	VCO DELAY	BITS	SYNC ENABLE	BIT	REG ADDR (HEX)
PECL0	DEL0	[5:0]	SYNC_EN0	[7]	0C
PECL1	DEL1	[5:0]	SYNC_EN1	[7]	0E
PECL2	DEL2	[5:0]	SYNC_EN2	[7]	10
PECL3	DEL3	[5:0]	SYNC_EN3	[7]	12
LV/CM	DEL4	[5:0]	SYNC_EN4	[7]	14

LV/CM OUTPUT DRIVER

The LTC6950 contains one output driver capable of being configured as an LVDS or CMOS output driver. Programming the LVCMS bit in register h0B to 1 allows LVDS compatible operation at frequencies up to 800MHz. Setting it to 0 configures two CMOS compatible output drivers with a maximum operating frequency of 250MHz. When the output driver is configured for CMOS operation, programming the bit CMSINV in register h0B to 1 inverts the LV/CM$^-$ (pin 21) relative to LV/CM$^+$ (pin 22). Setting CMSINV to 0 results in both LV/CM$^+$ and LV/CM$^-$ being in phase. See the Application Information section for LVDS and CMOS output driver interface circuits.

PECLx OUTPUT DRIVER

The LTC6950 contains four low noise, low skew LVPECL compatible output drivers designed for operation at frequencies up to 1.4GHz. The output driver provides considerable flexibility for biasing and termination. Internal biasing for the output emitter followers may be selected by programming the IBIASx to 1 for the appropriate output driver block. See Figure 14 for a simplified schematic.

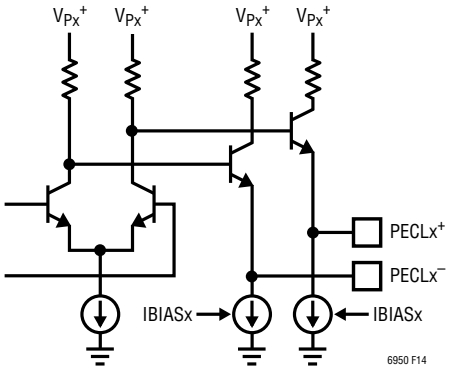


Figure 14. Simplified PECLx Output Schematic

Enabling the internal bias will usually reduce the number of passive components required off-chip. In many cases, a single 100Ω differential termination at the far end is all that is required. In addition, more symmetrical rise/fall times may result from using the constant current internal bias.

Setting IBIASx to 0 disables the internal bias and allows the PECLx output driver to be configured using standard LVPECL bias and termination networks. See the Applications Information section for more information about recommended bias and termination networks.

EZSync CLOCK OUTPUT SYNCHRONIZATION

The LTC6950 allows easy synchronization of the rising edges of clock outputs of a single chip or of multiple chips by asserting the CMOS logic compatible SYNC input pin. For applications where some clock outputs need to be synchronized, but others must not be disturbed, the LTC6950 allows the user to disable the synchronization on a per output basis.

An additional feature of EZSync allows some configurations to generate clock outputs with a known, repeatable phase relationship with respect to the N divider output once synchronization completes. In these configurations, when the PLL is locked, the clock outputs will have the same phase relationship with the R divider output as they do with the N divider. Because the R divider is clocked by the rising edges of the REF input, the clock outputs will also have a known, repeatable phase relationship with the REF input's rising edges. Therefore, when the PLL is locked in these configurations, it is possible for the user to optimally place the clock output rising edges with respect to the N divider, R divider and REF input's rising edges.

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SINGLE CHIP SYNCHRONIZATION

For single chip output synchronization, the Sync Mode bits, SYNCMD[1:0], should be programmed for STANDALONE operation (see Table 8 for SYNCMD[1:0] Function). Each synchronized clock output should be Sync Enabled, by programming its SYNC_ENx bit to 1. Programming an output to be Sync Enabled results in that clock output being gated, or noncontinuous, during the synchronization process. Therefore, clock outputs that must not be disturbed (gated) during a synchronization operation should have their SYNC_ENx bits programmed to 0. When a chip is in STANDALONE mode, the programmed settings of the FLDRVx bits are ignored.

Table 8. Chip Level Synchronization Modes (Register h0B)

SYNCMD[1:0]	SYNC MODE FUNCTION
0	CONTROL
1	STANDALONE
2	FOLLOW
3	FOLLOW

A synchronization operation is performed by forcing the SYNC input (pin 30) to a logic high for at least 1ms. An LTC6950 in STANDALONE mode then retimes the SYNC input with respect to the VCO input signal, and this signal is then retimed with respect to its N divider output to create an internal SYNC_RET signal, as shown in Figure 15. When SYNC_RET transitions high, all sync enabled clock outputs remain low once they transition to that state. Note that the LTC6950 has circuitry to prevent runt-pulses even during a synchronization operation, so the clock outputs only transition low when they would do so normally. Once the internal SYNC_RET signal transitions low, all Sync Enabled outputs transition high simultaneously, and the synchronization operation is complete.

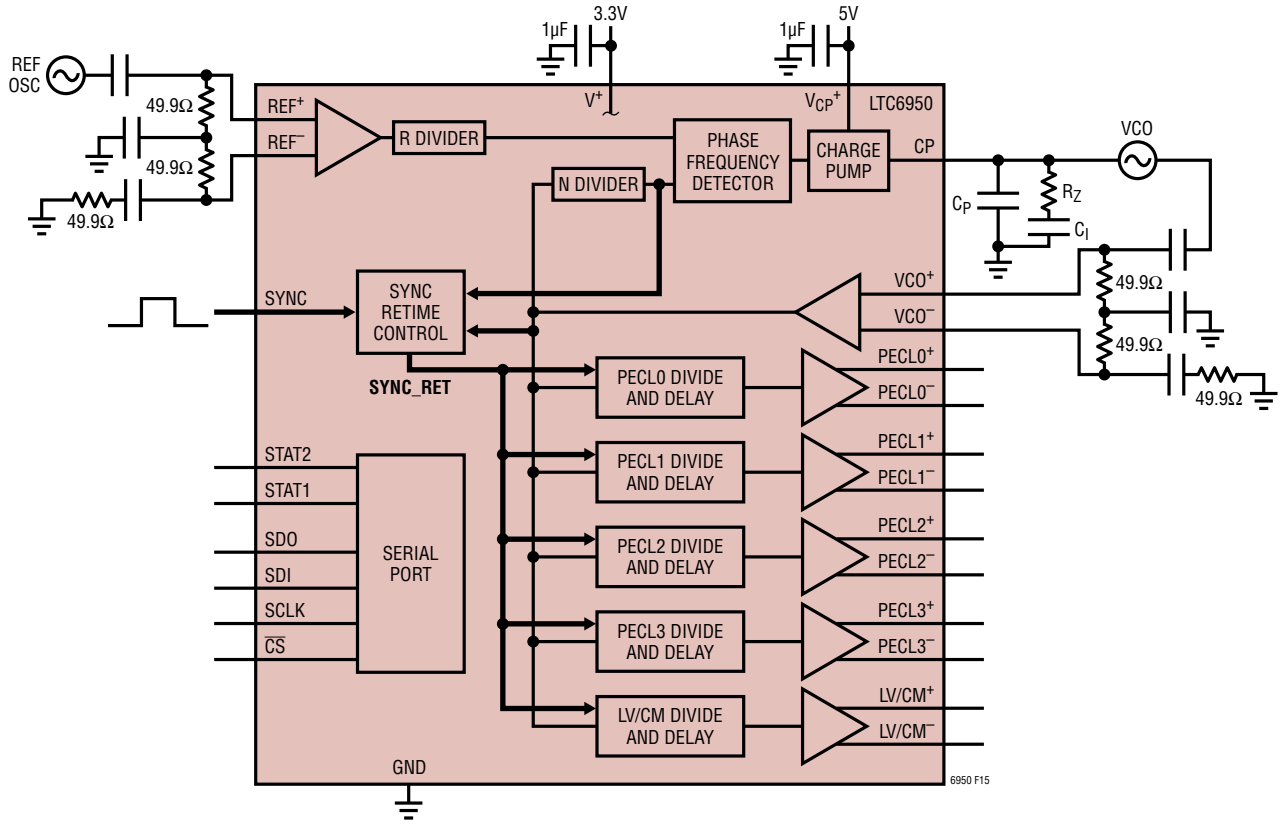


Figure 15. SYNC_RET Propagation

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By programming the delay bits, DELx[5:0], the user may configure the LTC6950 to provide clock outputs with phase relationships other than synchronized first rising edges. When DELx[5:0] are programmed, each sync enabled output may be independently configured to wait up to 63 additional VCO cycles before rising, relative to the 0 delay case. For example, assuming the PECL0 and PECL1 outputs are both configured to divide by 4, programming DEL0[5:0] to 0 and DEL1[5:0] to 1 allows the outputs to have a quadrature relationship once a synchronization operation completes (see Figure 16). To conserve power, the VCO cycle delay circuitry is turned off after a synchronization completes.

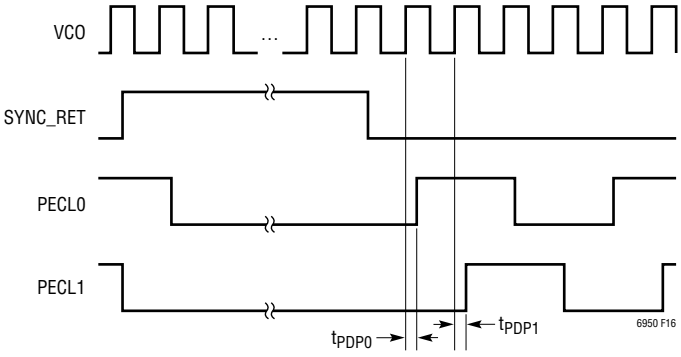


Figure 16. Synchronization to Obtain I/Q Clocks SYNCMD[1:0] = 1, SYNC_EN0 = SYNC_EN1 = 1, M0[5:0] = M1[5:0] = 4, DEL0[5:0] = 0, DEL1[5:0] = 1

As mentioned previously, the synchronized outputs of the LTC6950 in STANDALONE mode will have a repeatable, but normally noncoincident, phase relationship with respect to the rising edge of the N divider output. Figure 17 illustrates that the N divider output rising edge will lead a synchronized clock output rising edge by 6 VCO cycles in STANDALONE mode, assuming the delay is programmed to a 0 value. However, if the LTC6950 has been programmed to power down the PLL, the N divider will no longer transition. For this reason, when the PLL has been powered down, the LTC6950 will automatically disable the circuitry which retimes the SYNC input with respect to the N divider. In this case, all sync enabled clock outputs will transition high simultaneously, but with no relationship to the N divider output. Lastly, ensure the PFD frequency, f_{PFD}, is greater than or equal to 50kHz when synchronizing to the N divider in STANDALONE mode.

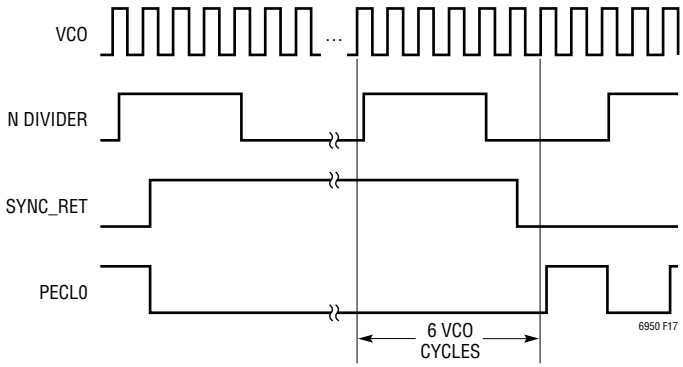


Figure 17: N Divider to PECL0 Relationship SYNCMD[1:0] = 1, N = 8, M0[5:0] = 4, DEL0[5:0] = 0

MULTIPLE CHIP SYNCHRONIZATION

Multiple LTC6950 chips may be easily configured to provide more synchronized outputs than are available on a single chip. All LTC6950 chips being synchronized should share a common SYNC input, but there is no requirement for precise timing of this signal between the different chips. The only requirements are that the skew of the SYNC pulse between the different chips is no greater than 10µs, and the SYNC pulse is at least 1ms in duration.

The general concept behind synchronizing multiple LTC6950 chips is to designate one chip the CONTROLLER, while all other chips are FOLLOWERS. The CONTROLLER LTC6950 controls the timing of all chips because it provides gated clock inputs to all FOLLOWER LTC6950 chips. By providing an appropriate gated clock signal to each FOLLOWER chip, the CONTROLLER ensures the outputs of all FOLLOWER chips will have their first rising edge synchronized. Furthermore, any output of the CONTROLLER LTC6950 not being used as a follower-driver may be configured to be follower-synchronous, which forces its output to have a first rising edge synchronized with all FOLLOWER parts' outputs.

The LTC6950's EZSync feature allows easy multichip synchronization of rising clock edges, so outputs of multiple chips will have a repeatable phase alignment. EZSync does not guarantee absolute time synchronization. That is, EZSync makes VCO cycle delay adjustments only, so any PCB trace delay from the CONTROLLER to the FOLLOWER plus the propagation delay of the FOLLOWER device will be reflected as a delta absolute time between

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the FOLLOWER and CONTROLLER when measured at their respective output pins.

The simplest configuration for synchronizing multiple LTC6950 devices is shown in Figure 18. The first LTC6950 has its SYNCMD[1:0] bits programmed to CONTROL mode, and the second LTC6950 has its SYNCMD[1:0] bits programmed to FOLLOW mode (see Table 8). Because the PECL0 output of the CONTROLLER LTC6950 is used as an input to a FOLLOWER chip, the CONTROLLER chip should be configured to make that output a follower-driver, which is accomplished by programming FLDRV0 to 1. To configure PECL1, PECL2 and PECL3 of the CONTROLLER LTC6950 as follower-synchronous, an internal VCO cycle delay cell must be enabled, which is accomplished by programming the FLDRV1, FLDRV2 and FLDRV3 bits to 0. All four outputs should have their SYNC_ENx bits programmed to 1 to allow synchronization. If there is an output which should not be disturbed (gated), program its SYNC_ENx bit to 0. See Table 9 for a summary of the effect of various configuration bits on the clock outputs of a chip in different synchronization modes.

The example in Figure 18 makes an arbitrary choice of using the PECL0 differential outputs to drive the LVPECL compatible VCO inputs of the FOLLOWER LTC6950. Any of the outputs from the CONTROLLER LTC6950 may be used as long as the appropriate FLDRVx bit is programmed to 1. Note that since the follower-driver clock output is gated (or briefly stopped), it is important to DC-couple this signal to the clock input of the FOLLOWER device.

As mentioned earlier, the second LTC6950 in the example shown in Figure 18 should be configured to FOLLOW mode operation. In addition, the SYNC_ENx bits of all synchronized outputs should be programmed to 1. When a chip is in FOLLOW mode, the programmed setting of the FLDRVx bits is ignored.

The timing diagram in Figure 19 illustrates multichip output synchronization of the circuit shown in Figure 18. The configurations of both the CONTROLLER LTC6950 and the FOLLOWER LTC6950 are as described in the preceding paragraphs. Figure 19 highlights that once the SYNC input transitions to a logic low, both outputs of the FOLLOWER (FOLLOWER.PECL0 and FOLLOWER.PECL1) have their first rising edges aligned with each other, as well as with the follower-synchronous output of the CONTROLLER (CONTROLLER.PECL1).

Table 9. Synchronization Configuration Bits for Different Synchronization Modes

SYNCMD [1:0]	SYNC_ENx		PDPLL		FLDRVx		DELx[5:0]
	VALUE	EFFECT ON OUTPUT x	VALUE	EFFECT ON OUTPUT x	VALUE	EFFECT ON OUTPUT x	EFFECT ON OUTPUT x
CONTROL [0:0]	0	Undisturbed	Don't Care	None	Don't Care	None	None
	1	Synchronized	0	Synchronized to N Divider (Repeatable Phase Alignment Relative to N Divider)	0	Follower-Synchronous	Allows 0 to 63 Cycle Delay
					1	Follower-Driver	None
			1	Not Synchronized to N Divider (N Divider is OFF)	0	Follower-Synchronous	Allows 0 to 63 Cycle Delay
					1	Follower-Driver	None
STANDALONE [0:1]	0	Undisturbed	Don't Care	None	Don't Care	None	None
	1	Synchronized	0	Synchronized to N Divider (Delayed 6 Cycles Relative to N Divider when DELx[5:0] = 0)	Don't Care	None	Allows 0 to 63 Cycle Delay
			1	Not Synchronized to N Divider (N Divider is OFF)	Don't Care	None	Allows 0 to 63 Cycle Delay
FOLLOW [1:0] [1:1]	0	Undisturbed	Don't Care	None	Don't Care	None	None
	1	Synchronized	Don't Care	None	Don't Care	None	Allows 0 to 63 Cycle Delay

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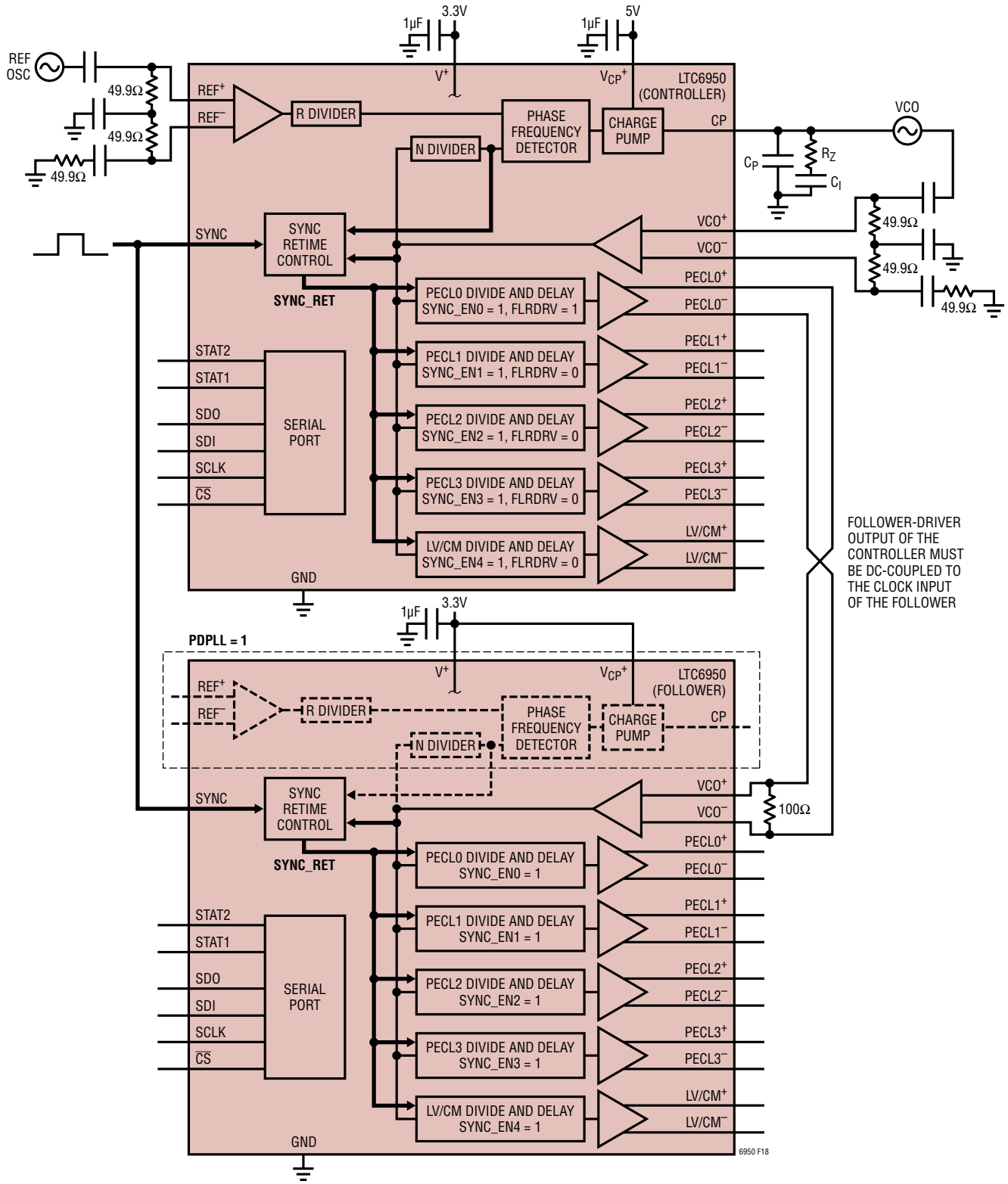


Figure 18. Two LTC6950 Chips Configured for Synchronization. The PECL0 Output of the CONTROLLER LTC6950 Drives the FOLLOWER LTC6950. All Other CONTROLLER Outputs Are Programmed as Follower-Synchronous, Enabling All Nine Outputs to Be Rising Edge Synchronized

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As described in the previous Single Chip Synchronization section, arbitrary phase relationships between different synchronized outputs may be created by programming the DELx[5:0] bits. However, programming DEL0[5:0] of the CONTROLLER device shown in Figures 18 and 19 will have no effect because it is in follower-driver mode. Any output configured as a follower-driver on a CONTROLLER LTC6950 will disregard programming to its DELx[5:0] bits.

The example in Figures 18 and 19 shows a CONTROLLER LTC6950 configured with a single follower-driver output and an output divider in bypass mode (M0[5:0] programmed to 1). An LTC6950 in CONTROL mode may have up to five outputs configured in follower-driver mode. Furthermore, any output configured as a follower-driver may have any divide modulus less than or equal to 8. If a follower-driver output is programmed to divide by more than 8, internal circuitry forces the divider to only divide by 8. There are no divide modulus limitations for outputs configured as follower-synchronous or for outputs of the FOLLOWER device.

The operation of the LTC6950 when programmed to FOLLOW mode differs from that of the STANDALONE mode described previously. Unlike operation in STANDALONE mode, the LTC6950 in FOLLOW mode does not retime the SYNC input with respect to the N divider output. In fact, most applications should power down the PLL of an LTC6950 in FOLLOW mode by programming its PDPLL bit to 1.

As illustrated in Figures 18 and 19, the EZSync feature of the LTC6950 allows a device configured in CONTROL mode to generate appropriately gated clock signals that guarantee all devices in FOLLOW mode will be synchronized with each other and with any follower-synchronous outputs of the CONTROLLER, making multichip synchronization easy.

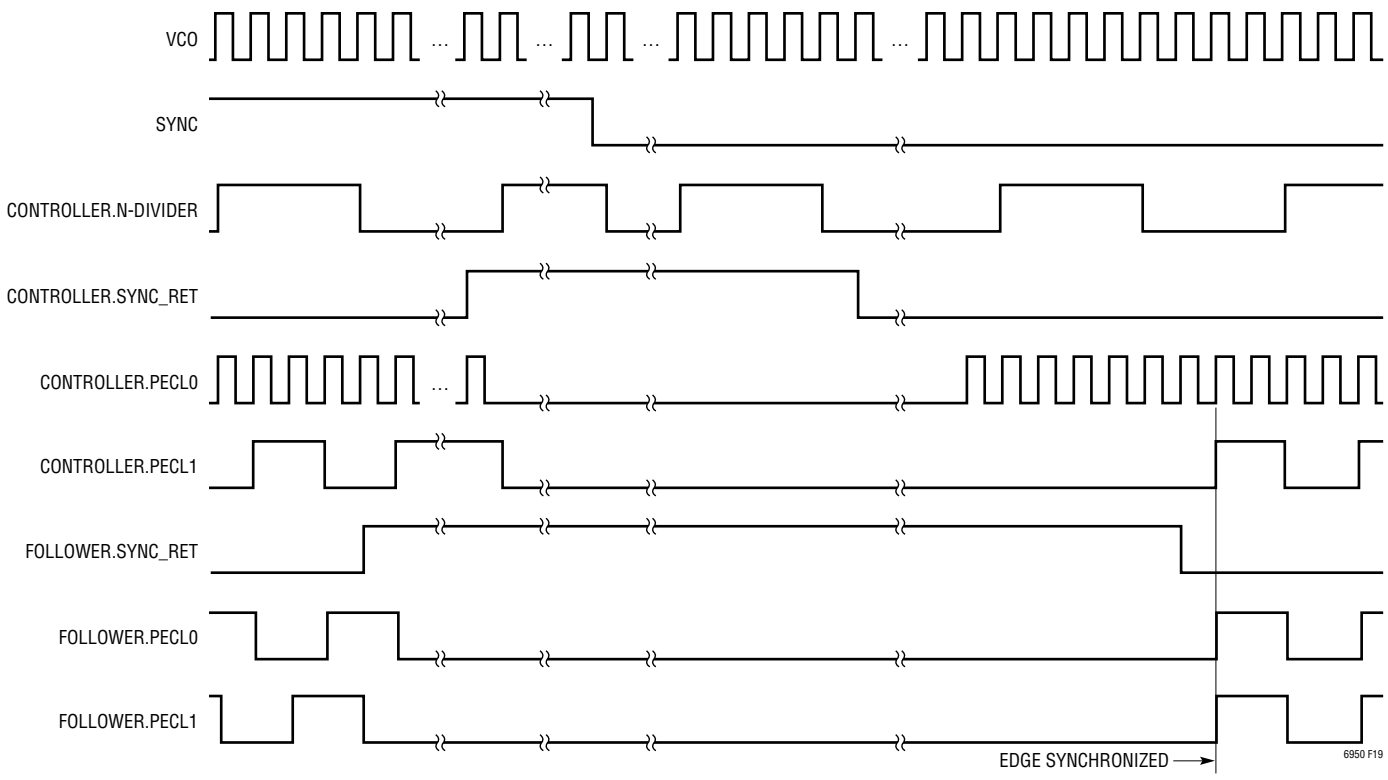


Figure 19. Timing Diagram of Circuit Shown in Figure 18 with Edge Synchronized Outputs Highlighted
CONTROLLER CHIP: M0[5:0] = 1, M1[5:0] = 4, DEL1[5:0] = 0, FLDRV0 = 1, FLDRV1 = 0, SYNC_EN0 = SYNC_EN1 = 1, N = 8
FOLLOWER CHIP: M0[5:0] = 4, M1[5:0] = 4, DEL0[5:0] = DEL1[5:0] = 0, SYNC_EN0 = SYNC_EN1 = 1

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SYNCHRONIZATION TO THE N DIVIDER IN CONTROL MODE

Applications requiring multiple devices' clock outputs to have a known, repeatable phase relationship with respect to the CONTROLLER's N divider may also be easily implemented with the LTC6950. However, understanding the precise phase alignment of the N divider output to the synchronized clock outputs requires understanding some of the internal EZSync operation of the LTC6950.

Like an LTC6950 in STANDALONE mode, an LTC6950 in FOLLOW mode retimes the SYNC input with respect to its VCO input. Due both to the retiming and other circuitry within its output divider, the clock outputs of a FOLLOWER LTC6950 only start transitioning after 7 cycles of its VCO input, regardless of the frequency of that signal. Since the VCO input of a FOLLOWER LTC6950 is a gated clock coming from the CONTROLLER, the SYNC_RET signal inside the FOLLOWER chip shown in Figure 18 will include several cycles of CONTROLLER.PECL0 delay. The timing diagram in Figure 20 illustrates this. Note that 7 cycles of CONTROLLER.PECL0 transition before the first rising edge of the FOLLOWER device's clock outputs. Functionally, an LTC6950 operating in FOLLOW mode propagates whatever VCO clock input it receives, just delayed by 7 cycles.

As already noted, there will always be a 7 cycle delay of a FOLLOWER output relative to its VCO input, which is independent of the frequency of that input. Since the VCO input of a FOLLOWER is actually a gated clock output from the CONTROLLER and the CONTROLLER must be able to provide follower-driver clock signals to multiple FOLLOWER devices, the relationship of the CONTROLLER's N divider output to other signals is more complicated than described for STANDALONE operation.

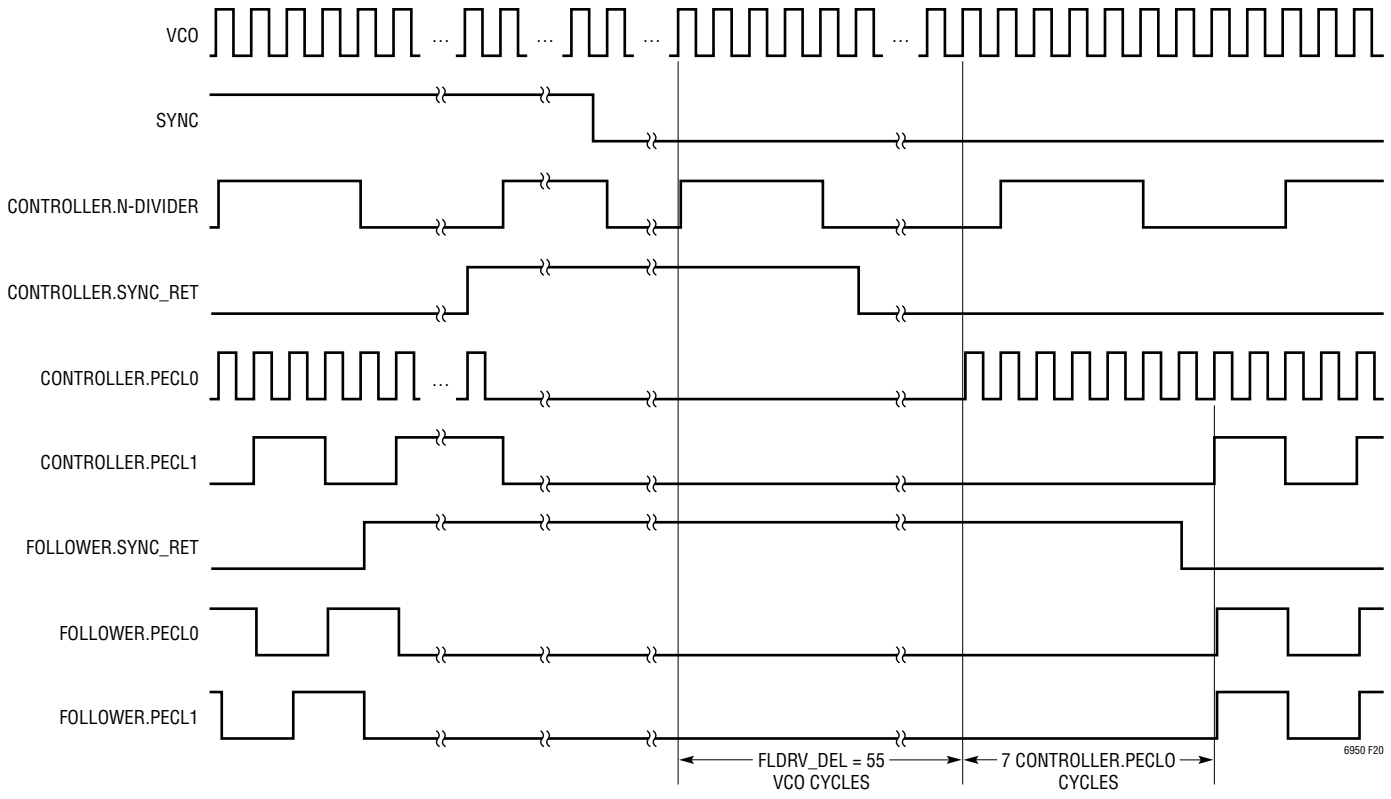


Figure 20: Timing Diagram of Circuit Shown in Figure 18 with N divider Synchronization Highlighted
CONTROLLER CHIP: M0[5:0] = 1, M1[5:0] = 4, DEL1[5:0] = 0, FLDRV0 = 1, FLDRV1 = 0, SYNC_EN0 = SYNC_EN1 = 1, N = 8
FOLLOWER CHIP: M0[5:0] = 4, M1[5:0] = 4, DEL0[5:0] = DEL1[5:0] = 0, SYNC_EN0 = SYNC_EN1 = 1

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An output of a CONTROL mode LTC6950 that has been configured as a follower-driver will have a first rising edge FLDRV_DEL number of VCO cycles after the N divider output transitions high. For the example shown in Figure 20, the follower-driver signal is CONTROLLER.PECL0 and FLDRV_DEL equals 55. The value of FLDRV_DEL depends on the output divider configuration of the specific follower-driver output (see Table 10).

Table 10. VCO Cycles Between N Divider Rising Edge and Specific Follower-Driver 1st Rising Edge

Mx[5:0]	DIVIDER MODULUS	FLDRV_DEL (VCO CYCLES)
≥8	8	6
7	7	13
6	6	20
5	5	27
4	4	34
3	3	41
2	2	48
1	1	55
0	1	55

As stated in the previous section, a CONTROLLER LTC6950 may have multiple outputs configured as follower-drivers, and each of these may be configured with a different output divider modulus. The only constraint is no output configured as a follower-driver can divide by more than 8.

Figure 20 illustrates another aspect of the synchronized clock output to N divider phase relationship worth noting. The FOLLOWER LTC6950's clock outputs, FOLLOWER.PECL0 and FOLLOWER.PECL1, have their first rising edges 62 VCO cycles after CONTROLLER.N-DIVIDER's rising edge. Similarly, the follower-synchronous output of the CONTROLLER LTC6950, CONTROLLER.PECL1, has its first rising edge 62 VCO cycles after the N divider's rising edge. For any CONTROLLER LTC6950, the number of VCO cycles between the rising edge of the N divider and the first rising edge of a follower-synchronous output with a DELx[5:0] value of 0 is a constant: *it will always be 62 cycles regardless of output divider setting*. This also implies there will always be 62 cycles of the CONTROLLER chip's VCO between the rising edge of the N divider to the first rising edge of any FOLLOWER device's synchronized output, assuming the DELx[5:0] value of the FOLLOWER device's output is 0. To achieve different alignments between the N divider output and the synchronized clock outputs, the DELx[5:0] bits may be programmed to values other than 0.

As is the case in STANDALONE mode, it is important to ensure the PFD frequency, f_{PFD}, is greater than or equal to 50kHz when synchronizing to the N divider in CONTROL mode.

Lastly, like a STANDALONE LTC6950, synchronization to the N divider requires the CONTROLLER's PLL be powered up. The LTC6950 will always disable the circuitry that retimes its SYNC input with respect to its N divider output if the PLL is powered down. In this case, all sync enabled clock outputs will transition high simultaneously, but with no relationship to the N divider output.

SERIAL PORT

The LTC6950 SPI-compatible serial port provides chip control and monitoring functionality. Two status output pins, STAT1 and STAT2, may be configured to allow real-time monitoring of the chip status.

COMMUNICATION SEQUENCE

The serial bus is comprised of chip select bar ($\overline{CS}$), serial clock (SCLK), serial data input (SDI) and serial data output (SDO) signals. Data transfers to the LTC6950 are accomplished by the serial bus master device first taking $\overline{CS}$ low, which enables the LTC6950's serial port. Input data applied on SDI is clocked on the rising edge of SCLK, *with most significant bits transferred first.* The communication burst is terminated by the serial bus master device returning $\overline{CS}$ high. See Figure 21 for details.

Data is read from the part during a communication burst using SDO. Read back may be multidrop (more than one LTC6950 connected in parallel on the serial bus), as SDO is three-stated (Hi-Z) either when $\overline{CS}$ is a logic high or when data is not being read from the part. See Figure 22 for details. *If the LTC6950 is not used in a multidrop configuration, or if the serial port master is not capable of setting the SDO line level between read sequences, attaching a high value resistor of at least 200k between SDO and GND to ensure the line returns to a known level during Hi-Z states is highly recommended.*

OPERATION

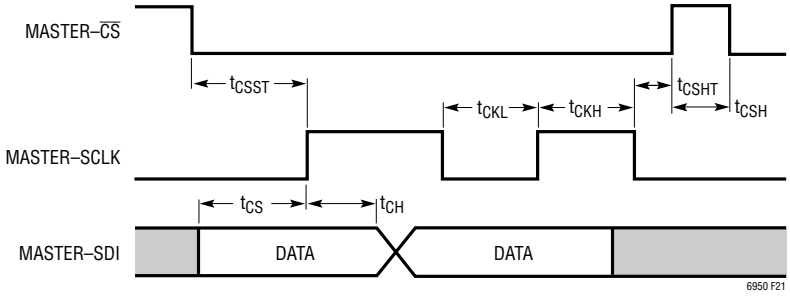


Figure 21. Serial Port Write Timing Diagram

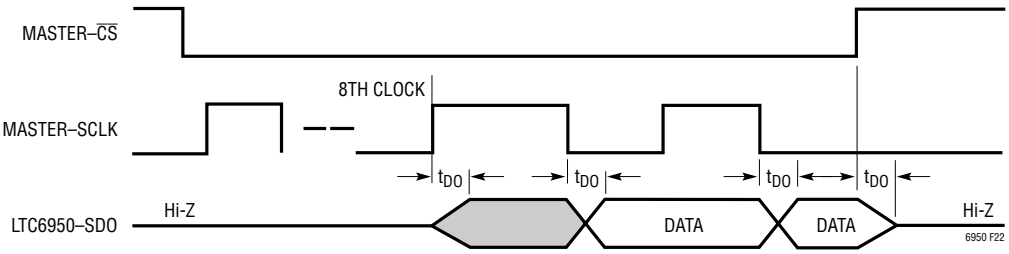


Figure 22. Serial Port Read Timing Diagram

SINGLE BYTE TRANSFERS

The serial port is arranged in a straightforward memory map, with status and control available in 23 byte-wide registers. All data bursts are comprised of at least two bytes. The 7 most significant bits (MSB) of the first byte are the register address, with a least significant bit (LSB) of 1 indicating a read from the part, and an LSB of 0 indicating a write to the part. The subsequent byte, or bytes, is data from/to the specified register address. See Figure 23 for an example of a detailed write sequence, and Figure 24 for a read sequence.

Figure 25 shows an example of two write communication bursts. The first communication burst from the serial bus master device contains a first byte of data on SDI that includes the seven-bit destination register address (Addr0) and an LSB of 0 indicating a write operation. The second byte on SDI is the data to be written into address Addr0. To terminate the first communication burst, $\overline{CS}$ is taken high.

The second communication burst is structured the same way as the first. The first byte on SDI contains a seven-bit destination register address (Addr1) and an LSB of 0 to indicate a write operation. The next byte on SDI is the data intended for the register at address Addr1. And finally, the transfer is terminated by taking $\overline{CS}$ high.

MULTIPLE BYTE TRANSFERS

More efficient data transfer of multiple bytes is accomplished by using the LTC6950's register address auto-increment feature as shown in Figure 26. Like Figure 25, Figure 26 shows the serial bus master device sending the destination register address and an LSB of 0 in the first byte, followed by a second byte of data for that destination register. But instead of terminating the burst by taking $\overline{CS}$ back high, the serial port master device continues sending bytes destined for subsequent registers. Byte 1's destination address is Addr0+1, Byte 2's destination address is Addr0+2 and so on. If the register address pointer attempts to increment past 22 (h16), it is automatically reset to 0.

An example of an auto-increment read from the part is shown in Figure 27. The first byte of the burst from the serial bus master device contains the seven-bit destination register address (Addr0) and an LSB of 1 to indicate a read operation. Once the LTC6950 detects a read burst, it takes SDO out of the Hi-Z condition and begins to send data bytes sequentially, starting with data from register Addr0. The part ignores all other data on SDI until the burst is terminated by taking $\overline{CS}$ high.

OPERATION

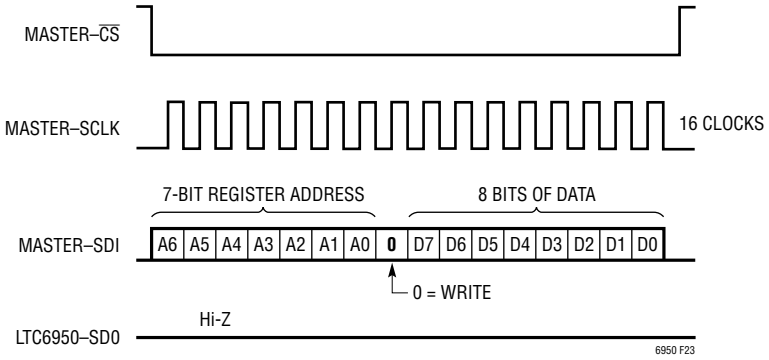


Figure 23. Serial Port Write Sequence

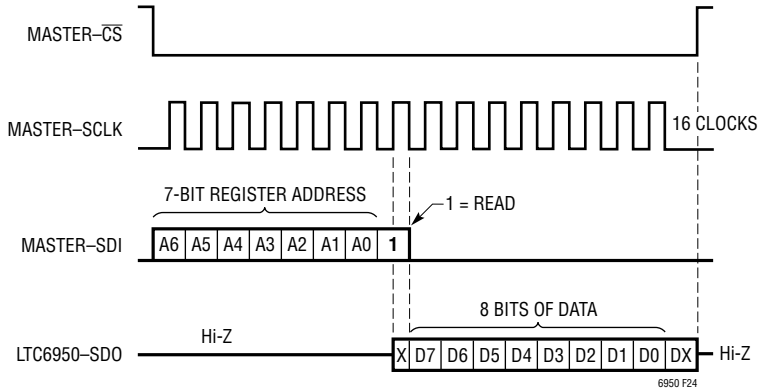


Figure 24. Serial Port Read Sequence

OPERATION

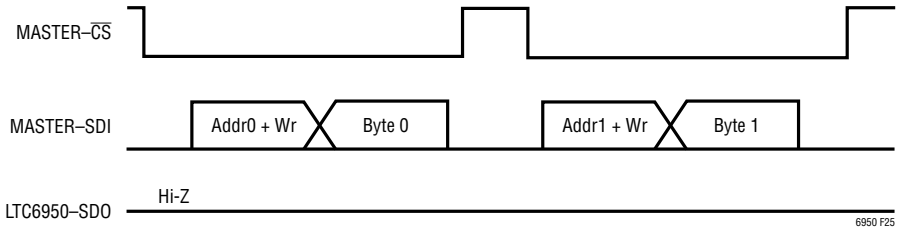


Figure 25. Serial Port Single Byte Write

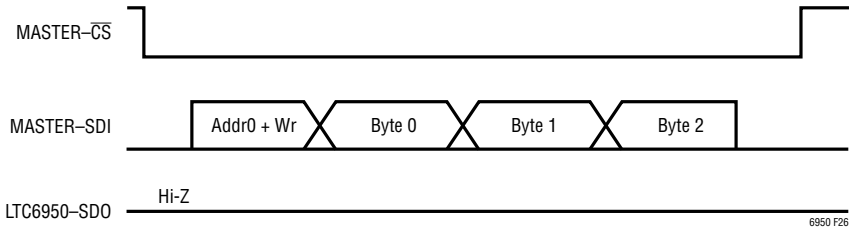


Figure 26. Serial Port Auto-Increment Write

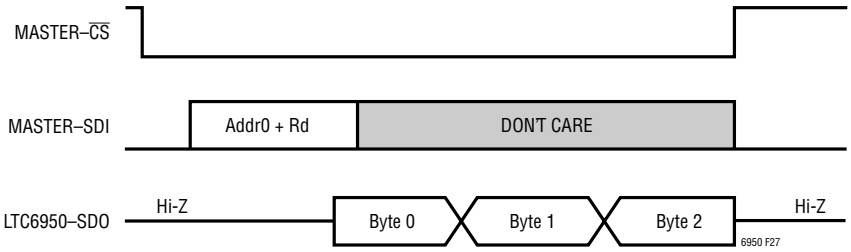


Figure 27. Serial Port Auto-Increment Read

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MULTIDROP CONFIGURATION

Several LTC6950's may share the serial bus. In this multidrop configuration SCLK, SDI and SDO are common between all parts. The serial bus master must use a separate $\overline{CS}$ for each LTC6950 and ensure that only one device has $\overline{CS}$ asserted at any time. It is recommended to attach a high value resistor from SDO to GND to ensure the line returns to a known level during Hi-Z states.

SERIAL PORT REGISTERS

The LTC6950's register map is shown in Table 11. Detailed bit descriptions are shown in Table 13.

The ADDR column in Table 11 specifies each register address in hexadecimal format. Each register is denoted as either read-only (R) or read-write (R/W). The register's default value on device power-up or after a reset is shown at the right.

The read-only register at address h00 is used to monitor the different status flags. These flags may provide instant output on either the STAT1 or STAT2 pins by configuring registers h01 and h02, respectively. See the Status Outputs section for more information.

The read-only register at address h16 is a ROM byte for user informational purposes only.

STATUS OUTPUTS

The STAT1 and STAT2 output pins are configured with the bits SM1[5:0] and SM2[5:0], respectively. These bits are used to bit-wise mask, or enable, the corresponding status flags of status register h00. See Figures 28 and 29 for simplified schematics of STAT1 and STAT2.

Table 11. Serial Port Register Mapping

ADDR (HEX)	[7] MSB	[6]	[5]	[4]	[3]	[2]	[1]	[0] LSB	R/W	DEFAULT (HEX)
00	*	*	NO_VCO	NO_REF	UNLOCK	LOCK	THI	TLO	R	NA
01	INV_ST1	*	SM1[5]	SM1[4]	SM1[3]	SM1[2]	SM1[1]	SM1[0]	R/W	04
02	INV_ST2	*	SM2[5]	SM2[4]	SM2[3]	SM2[2]	SM2[1]	SM2[0]	R/W	3B
03	PDALL	PDPLL	PDVCOAC	PDREFAC	LKEN	RES6950	PD_OUT0	PD_DIV0	R/W	08
04	PD_OUT4	PD_DIV4	PD_OUT3	PD_DIV3	PD_OUT2	PD_DIV2	PD_OUT1	PD_DIV1	R/W	00
05	LKWIN1	LKWIN0	LKCT1	LKCT0	CP[3]	CP[2]	CP[1]	CP[0]	R/W	9B
06	CPCHI	CPCLO	CPMID	CPINV	CPWIDE	CPRST	CPUP	CPDN	R/W	E4
07	*	*	*	*	RESET_R	*	R[9]	R[8]	R/W	00
08	R[7]	R[6]	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	R/W	01
09	*	*	*	RESET_N	*	N[10]	N[9]	N[8]	R/W	00
0A	N[7]	N[6]	N[5]	N[4]	N[3]	N[2]	N[1]	N[0]	R/W	32
0B	SYNCMD[1]	SYNCMD[0]	FILTV	FILTR	CMSINV	LVCMS	*	*	R/W	41
0C	SYNC_EN0	FLDRV0	DEL0[5]	DEL0[4]	DEL0[3]	DEL0[2]	DEL0[1]	DEL0[0]	R/W	80
0D	IBIAS0	*	M0[5]	M0[4]	M0[3]	M0[2]	M0[1]	M0[0]	R/W	02
0E	SYNC_EN1	FLDRV1	DEL1[5]	DEL1[4]	DEL1[3]	DEL1[2]	DEL1[1]	DEL1[0]	R/W	80
0F	IBIAS1	*	M1[5]	M1[4]	M1[3]	M1[2]	M1[1]	M1[0]	R/W	04
10	SYNC_EN2	FLDRV2	DEL2[5]	DEL2[4]	DEL2[3]	DEL2[2]	DEL2[1]	DEL2[0]	R/W	80
11	IBIAS2	*	M2[5]	M2[4]	M2[3]	M2[2]	M2[1]	M2[0]	R/W	08
12	SYNC_EN3	FLDRV3	DEL3[5]	DEL3[4]	DEL3[3]	DEL3[2]	DEL3[1]	DEL3[0]	R/W	80
13	IBIAS3	*	M3[5]	M3[4]	M3[3]	M3[2]	M3[1]	M3[0]	R/W	10
14	SYNC_EN4	FLDRV4	DEL4[5]	DEL4[4]	DEL4[3]	DEL4[2]	DEL4[1]	DEL4[0]	R/W	00
15	RDIVOUT	*	M4[5]	M4[4]	M4[3]	M4[2]	M4[1]	M4[0]	R/W	A0
16	REV[2]	REV[1]	REV[0]	PART[4]	PART[3]	PART[2]	PART[1]	PART[0]	R	65

*Unused.

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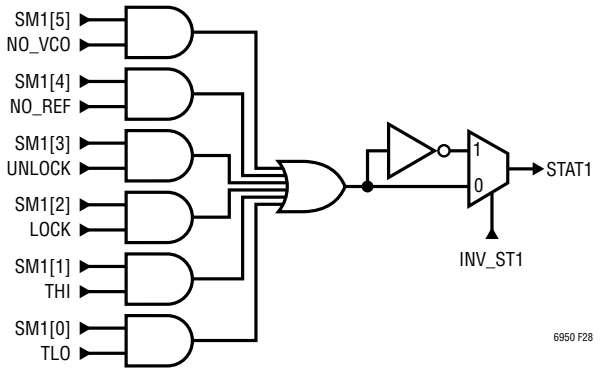


Figure 28. STAT1 Simplified Schematic

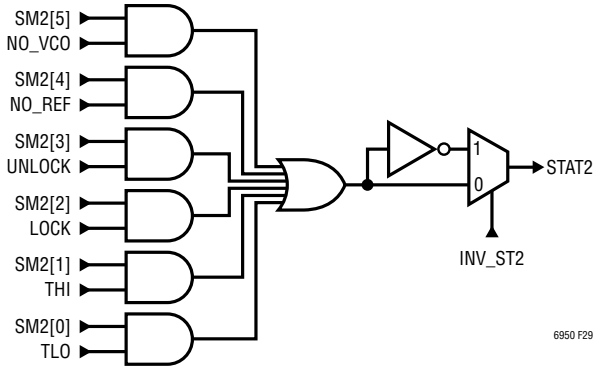


Figure 29. STAT2 Simplified Schematic

For example, to have STAT1 go to a logic high whenever the loop has been locked for the programmed number of LKCT[1:0] counts (i.e. LOCK = 1), then bit 2 of register h01 should be set to 1. All other bits in register h01 should be programmed to 0, thereby giving a register value of h04.

The INV_ST1 and INV_ST2 configuration bits found in registers h01 and h02, respectively, allow inversion of the normal status output flag. For example, to have STAT2 go to a logic high when the loop first achieves lock (i.e. UNLOCK = 0), bits 7 and 3 of register h02 should be set to 1. The remaining bits should be programmed to 0, thereby giving a register value of h88.

BLOCK POWER-DOWN

The LTC6950 provides considerable flexibility to power-down unused blocks. A summary of the different power-down bits is shown in Table 12. To determine the power savings in shutting down a particular section, consult the Supply Current Delta section of the Electrical Characteristics table.

To achieve maximum power savings when a PECLx output is unused and powered down, it is recommended that no terminations or other bias circuitry be connected to the output driver pins.

Table 12. Block Power-Down Descriptions

BIT NAME	DESCRIPTION
PDALL	Power Down Whole Chip
PDPLL	Power Down REF Input Buffer, R Divider, N Divider, PFD and Charge Pump
PDVCOAC	Power Down VCO Signal Present Circuit
PDREFAC	Power Down REF Signal Present Circuit
PD_OUT4	Power Down LV/CM Output Buffer
PD_DIV4	Power Down LV/CM Output Buffer and Output Divider
PD_OUT3	Power Down PECL3 Output Buffer
PD_DIV3	Power Down PECL3 Output Buffer and Output Divider
PD_OUT2	Power Down PECL2 Output Buffer
PD_DIV2	Power Down PECL2 Output Buffer and Output Divider
PD_OUT1	Power Down PECL1 Output Buffer
PD_DIV1	Power Down PECL1 Output Buffer and Output Divider
PD_OUT0	Power Down PECL0 Output Buffer
PD_DIV0	Power Down PECL0 Output Buffer and Output Divider

FULL PART RESET

The LTC6950 includes capability to perform a full part reset. This is equivalent to the power-on-reset (POR) that occurs when power is first applied to the LTC6950. The reset is controlled via the serial port by asserting the configuration bit, RES6950, found in register h03. Note that setting RES6950 to 1 forces a full reset of the chip, including resetting the serial port registers to their default values. As a result, the RES6950 bit is automatically cleared, or set to its default value of 0, once the reset completes.

OPERATION

Table 13. Serial Port Register Bit Descriptions

NAME	DESCRIPTION	REG ADDR (HEX)	BIT(s)	DEFAULT VALUE (b: BINARY h: HEX)
CMSINV	When CMSINV = 1, the CMOS outputs are complementary (LV/CM$^-$ is inverted relative to LV/CM$^+$).	0B	[3]	b 0
CP[3:0]	CP[3:0] sets the charge pump output current.	05	[3:0]	h B

CP[3]	CP[2]	CP[1]	CP[0]	I (mA)
0	0	0	0	0.25
0	0	0	1	0.35
0	0	1	0	0.50
0	0	1	1	0.70
0	1	0	0	1.00
0	1	0	1	1.40
0	1	1	0	2.00
0	1	1	1	2.80
1	0	0	0	4.00
1	0	0	1	5.60
1	0	1	0	8.00
1	0	1	1	11.20
1	1	0	0	4.00
1	1	0	1	5.60
1	1	1	0	4.00
1	1	1	1	5.60

CPCHI	When CPCHI = 1, the charge pump high voltage output clamp is enabled.	06	[7]	b 1
CPCLO	When CPCLO = 1, the charge pump low voltage output clamp is enabled.	06	[6]	b 1
CPDN	When CPDN = 1, the charge pump output forces a sink current based on CP[3:0].	06	[0]	b 0
CPINV	When CPINV = 1, the PFD phase is inverted.	06	[4]	b 0
CPMID	When CPMID = 1, the charge pump output is forced to $V_{CP}^+/2$.	06	[5]	b 1
CPRST	When CPRST = 1, the PFD is reset.	06	[2]	b 1
CPUP	When CPUP = 1, the charge pump output forces a source current based on CP[3:0].	06	[1]	b 0
CPWIDE	When CPWIDE = 1, the charge pump output current pulse width is increased.	06	[3]	b 0
DEL0[5:0]	DEL0[5:0] sets the PECL0 output divider delay to any integer from 0 to 63 cycles.	0C	[5:0]	h 00
DEL1[5:0]	DEL1[5:0] sets the PECL1 output divider delay to any integer from 0 to 63 cycles.	0E	[5:0]	h 00
DEL2[5:0]	DEL2[5:0] sets the PECL2 output divider delay to any integer from 0 to 63 cycles.	10	[5:0]	h 00
DEL3[5:0]	DEL3[5:0] sets the PECL3 output divider delay to any integer from 0 to 63 cycles.	12	[5:0]	h 00
DEL4[5:0]	DEL4[5:0] sets the LV/CM output divider delay to any integer from 0 to 63 cycles.	14	[5:0]	h 00

OPERATION

Table 13. Serial Port Register Bit Descriptions

NAME	DESCRIPTION	REG ADDR (HEX)	BIT(s)	DEFAULT VALUE (b: BINARY h: HEX)
FILTR	When FILTR = 1, the internal REF input filter is turned on (set FILTR = 1 when REF input slew rate < 100 V/µs).	0B	[4]	b 0
FILTV	When FILTV = 1, the internal VCO input filter is turned on (set FILTV = 1 when VCO input slew rate < 300 V/µs).	0B	[5]	b 0
FLDRV0	FLDRV0 sets the PECL0 output behavior when an input is applied to SYNC. When SYNCMD[1:0] is set to CONTROL mode, FLDRV0 = 1 forces the PECL0 output to be in follower-driver mode. When SYNCMD[1:0] is set to CONTROL mode, FLDRV0 = 0 forces the PECL0 output to be in follower-synchronous mode. In all other SYNCMD[1:0] modes, FLDRV0 has no effect on the PECL0 output.	0C	[6]	b 0
FLDRV1	FLDRV1 sets the PECL1 output behavior when an input is applied to SYNC. When SYNCMD[1:0] is set to CONTROL mode, FLDRV1 = 1 forces the PECL1 output to be in follower-driver mode. When SYNCMD[1:0] is set to CONTROL mode, FLDRV1 = 0 forces the PECL1 output to be in follower-synchronous mode. In all other SYNCMD[1:0] modes, FLDRV1 has no effect on the PECL1 output.	0E	[6]	b 0
FLDRV2	FLDRV2 sets the PECL2 output behavior when an input is applied to SYNC. When SYNCMD[1:0] is set to CONTROL mode, FLDRV2 = 1 forces the PECL2 output to be in follower-driver mode. When SYNCMD[1:0] is set to CONTROL mode, FLDRV2 = 0 forces the PECL2 output to be in follower-synchronous mode. In all other SYNCMD[1:0] modes, FLDRV2 has no effect on the PECL2 output.	10	[6]	b 0
FLDRV3	FLDRV3 sets the PECL3 output behavior when an input is applied to SYNC. When SYNCMD[1:0] is set to CONTROL mode, FLDRV3 = 1 forces the PECL3 output to be in follower-driver mode. When SYNCMD[1:0] is set to CONTROL mode, FLDRV3 = 0 forces the PECL3 output to be in follower-synchronous mode. In all other SYNCMD[1:0] modes, FLDRV3 has no effect on the PECL3 output.	12	[6]	b 0
FLDRV4	FLDRV4 sets the LV/CM output behavior when an input is applied to SYNC When SYNCMD[1:0] is set to CONTROL mode and RDIVOUT = 0, FLDRV4 = 1 forces the LV/CM output to be in follower-driver mode. When SYNCMD[1:0] is set to CONTROL mode and RDIVOUT = 0, FLDRV4 = 0 forces the LV/CM output to be in follower-synchronous mode. In all other SYNCMD[1:0] modes or if RDIVOUT = 1, FLDRV4 has no effect on the LV/CM output.	14	[6]	b 0
IBIAS0	When IBIAS0 = 1, the internal bias for the output emitter followers on PECL0 is enabled (no external bias resistors on PECL0± are required).	0D	[7]	b 0
IBIAS1	When IBIAS1 = 1, the internal bias for the output emitter followers on PECL1 is enabled (no external bias resistors on PECL1± are required).	0F	[7]	b 0
IBIAS2	When IBIAS2 = 1, the internal bias for the output emitter followers on PECL2 is enabled (no external bias resistors on PECL2± are required).	11	[7]	b 0
IBIAS3	When IBIAS3 = 1, the internal bias for the output emitter followers on PECL3 is enabled (no external bias resistors on PECL3± are required).	13	[7]	b 0

OPERATION

Table 13. Serial Port Register Bit Descriptions

NAME	DESCRIPTION	REG ADDR (HEX)	BIT(s)	DEFAULT VALUE (b: BINARY h: HEX)
INV_ST1	When INV_ST1 = 1, the STAT1 polarity is inverted.	01	[7]	b 0
INV_ST2	When INV_ST2 = 1, the STAT2 polarity is inverted.	02	[7]	b 0
LKCT[1:0]	LKCT[1:0] sets the number continuous PFD cycle counts that the PLL must be in lock before the lock indicator flag, LOCK, is asserted after UNLOCK is de-asserted.	05	[5:4]	b 01
	LKCT[1] / LKCT[0] / Number of Cycles			
	0 / 0 / 32			
	0 / 1 / 128			
	1 / 0 / 512			
	1 / 1 / 2048			
LKEN	When LKEN = 1, the PLL lock indicator flag, LOCK, is enabled.	03	[3]	b 1
LKWIN[1:0]	LKWIN[1:0] sets the duration of the PLL lock indicator window.	05	[7:6]	b 10
	LKWIN[1] / LKWIN[0] / Lock Window Duration (ns)			
	0 / 0 / 3			
	0 / 1 / 10			
	1 / 0 / 30			
	1 / 1 / 90			
LOCK	LOCK is a read-only bit that is forced to 1 when the PLL is locked if LKEN = 1.	00	[2]	
LVCMS	When LVCMS = 1, the LV/CM output buffer is configured in LVDS mode. When LVCMS = 0, the output buffer is configured as two single-ended CMOS outputs.	0B	[2]	b 0
M0[5:0]	M0[5:0] sets the PECL0 output divider modulus to any integer from 1 to 63. Programming M0[5:0] to a value of hex 0 or 1 results in a divide modulus of 1.	0D	[5:0]	h 02
M1[5:0]	M1[5:0] sets the PECL1 output divider modulus to any integer from 1 to 63. Programming M1[5:0] to a value of hex 0 or 1 results in a divide modulus of 1.	0F	[5:0]	h 04
M2[5:0]	M2[5:0] sets the PECL2 output divider modulus to any integer from 1 to 63. Programming M2[5:0] to a value of hex 0 or 1 results in a divide modulus of 1.	11	[5:0]	h 08
M3[5:0]	M3[5:0] sets the PECL3 output divider modulus to any integer from 1 to 63. Programming M3[5:0] to a value of hex 0 or 1 results in a divide modulus of 1.	13	[5:0]	h 10
M4[5:0]	M4[5:0] sets the LV/CM output divider modulus to any integer from 1 to 63. Programming M4[5:0] to a value of hex 0 or 1 results in a divide modulus of 1.	15	[5:0]	h 20
N[10:0]	N[10:0] sets the N divider modulus to any integer from 1 to 2047. Programming N[10:0] to a value of hex 0 or 1 results in a divide modulus of 1.			h 032
	N[10] N[9] N[8]	09	[2:0]	
	N[7] N[6] N[5] N[4] N[3] N[2] N[1] N[0]	0A	[7:0]	
NO_REF	NO_REF is a read-only bit that is forced to 1 when the signal present circuitry detects there is no REF input. Note that NO_REF is forced to 0 if the signal present circuitry is powered down (PDREFAC = 1).	00	[4]	
NO_VCO	NO_VCO is a read-only bit that is forced to 1 when the signal present circuitry detects there is no VCO input. Note that NO_VCO is forced to 0 if the signal present circuitry is powered down (PDVCOAC = 1).	00	[5]	

OPERATION

Table 13. Serial Port Register Bit Descriptions

NAME	DESCRIPTION	REG ADDR (HEX)	BIT(s)	DEFAULT VALUE (b: BINARY h: HEX)
PART[4:0]	PART[4:0] are read-only bits showing the part number code.	16	[4:0]	h 05
PDALL	When PDALL = 1, the full chip is powered down.	03	[7]	b 0
PD_DIV0	When PD_DIV0 = 1, the PECL0 output divider and buffer are both powered down.	03	[0]	b 0
PD_DIV1	When PD_DIV1 = 1, the PECL1 output divider and buffer are both powered down.	04	[0]	b 0
PD_DIV2	When PD_DIV2 = 1, the PECL2 output divider and buffer are both powered down.	04	[2]	b 0
PD_DIV3	When PD_DIV3 = 1, the PECL3 output divider and buffer are both powered down.	04	[4]	b 0
PD_DIV4	When PD_DIV4 = 1, the LV/CM output divider and buffer are both powered down.	04	[6]	b 0
PD_OUT0	When PD_OUT0 = 1, the PECL0 output buffer is powered down.	03	[1]	b 0
PD_OUT1	When PD_OUT1 = 1, the PECL1 output buffer is powered down.	04	[1]	b 0
PD_OUT2	When PD_OUT2 = 1, the PECL2 output buffer is powered down.	04	[3]	b 0
PD_OUT3	When PD_OUT3 = 1, the PECL3 output buffer is powered down.	04	[5]	b 0
PD_OUT4	When PD_OUT4 = 1, the LV/CM output buffer is powered down.	04	[7]	b 0
PDPLL	When PDPLL = 1, the REF input buffer, the R divider, the phase-frequency detector, the charge pump and the N divider are all powered down.	03	[6]	b 0
PDREFAC	When PDREFAC = 1, the REF input signal present circuit is powered down.	03	[4]	b 0
PDVCOAC	When PDVCOAC = 1, the VCO input signal present circuit is powered down.	03	[5]	b 0
R[9:0]	R[9:0] sets the R divider modulus to any integer from 1 to 1023. Programming R[10:0] to a value of hex 0 or 1 results in a divide modulus of 1.			h 001
	R[9] R[8]	07	[1:0]	
	R[7] R[6] R[5] R[4] R[3] R[2] R[1] R[0]	08	[7:0]	
RDIVOUT	When RDIVOUT = 1, the LV/CM output divider has the R divider as its input. All delay/synchronization functions are disabled for the LV/CM output in this mode.	15	[7]	b 1
RES6950	When RES6950 = 1, a reset of the entire chip to default values is performed.	03	[2]	b 0
RESET_R	When RESET_R = 1, a reset of the R divider is forced. Once a reset has been performed, RESET_R must be programmed to 0 to activate the R divider again.	07	[3]	b 0
RESET_N	When RESET_N = 1, a reset of the N divider is forced. Once a reset has been performed, RESET_N must be programmed to 0 to activate the N divider again.	09	[4]	b 0
REV[2:0]	REV[2:0] are read-only bits showing the revision code.	16	[7:5]	b 011
SM1[5:0]	SM1[5:0] bit-wise masks the corresponding status flags in register h00 to create the STAT1 logic output.	01	[5:0]	h 04
SM2[5:0]	SM2[5:0] bit-wise masks the corresponding status flags in register h00 to create the STAT2 logic output.	02	[5:0]	h 3B
SYNCMD[1:0]	SYNCMD[1:0] sets the synchronization mode for the chip.	0B	[7:6]	b 01
	SYNCMD[1] / SYNCMD[0] / Mode			
	0 / 0 / CONTROL			
	0 / 1 / STANDALONE			
	1 / 0 / FOLLOW			
	1 / 1 / FOLLOW			

OPERATION

Table 13. Serial Port Register Bit Descriptions

NAME	DESCRIPTION	REG ADDR (HEX)	BIT(s)	DEFAULT VALUE (b: BINARY h: HEX)
SYNC_EN0	When SYNC_EN0 = 1, the PECL0 output will respond to an input to the SYNC pin, depending on the configuration of the SYNCMD[1:0], DEL0[5:0] and FLDRV0 inputs. Otherwise, the PECL0 output ignores inputs to the SYNC pin.	0C	[7]	b 1
SYNC_EN1	When SYNC_EN1 = 1, the PECL1 output will respond to an input to the SYNC pin, depending on the configuration of the SYNCMD[1:0], DEL1[5:0] and FLDRV1 inputs. Otherwise, the PECL1 output ignores inputs to the SYNC pin.	0E	[7]	b 1
SYNC_EN2	When SYNC_EN2 = 1, the PECL2 output will respond to an input to the SYNC pin, depending on the configuration of the SYNCMD[1:0], DEL2[5:0] and FLDRV2 inputs. Otherwise, the PECL2 output ignores inputs to the SYNC pin.	10	[7]	b 1
SYNC_EN3	When SYNC_EN3 = 1, the PECL3 output will respond to an input to the SYNC pin, depending on the configuration of the SYNCMD[1:0], DEL3[5:0] and FLDRV3 inputs. Otherwise, the PECL3 output ignores inputs to the SYNC pin.	12	[7]	b 1
SYNC_EN4	When SYNC_EN4 = 1, the LV/CM output will respond to an input to the SYNC pin, depending on the configuration of the SYNCMD[1:0], DEL4[5:0], RDIVOUT and FLDRV4 inputs. Otherwise, the LV/CM output ignores inputs to the SYNC pin.	14	[7]	b 0
THI	THI is a read-only bit that is forced to 1 when the CP pin voltage exceeds V_{CP}^+ – 0.9V if CPCHI = 1.	00	[1]	
TLO	TLO is a read-only bit that is forced to 1 when the CP pin voltage is less than 0.9V if CPCLO = 1.	00	[0]	
UNLOCK	UNLOCK is a read-only bit that is forced to 1 when the PLL is unlocked.	00	[3]	

APPLICATIONS INFORMATION

PLL INTRODUCTION

A PLL is a complex feedback system that may conceptually be considered as a frequency multiplier. The system multiplies the frequency input at REF± and outputs a higher frequency at the PECL0±, PECL1±, PECL2±, PECL3± and LV/CM± outputs.

The phase/frequency detector (PFD), charge pump, N divider, external VCO and loop filter form a feedback loop to accurately control the output frequency (see Figure 30). The R divider and M divider are used to set the output frequency resolution but are outside of the feedback loop. The delay circuit block does not affect the output frequency.

OUTPUT FREQUENCY

When the loop is locked, the frequency f_{VCO} (in Hz) produced at the output of the VCO is determined by the reference frequency, f_{REF}, and the R divider and N divider values, given by Equation 2:

$$f_{VCO} = \frac{f_{REF} \bullet N}{R} \quad (2)$$

The PFD frequency, f_{PFD}, produced is given by the following equation:

$$f_{PFD} = \frac{f_{REF}}{R} \quad (3)$$

and f_{VCO} may be alternatively expressed as:

$$f_{VCO} = f_{PFD} \bullet N \quad (4)$$

The output frequency, f_{OUT}, produced at the output of each output divider (M = 1 to 63) is given by Equation 5:

$$f_{OUT} = \frac{f_{VCO}}{M} \quad (5)$$

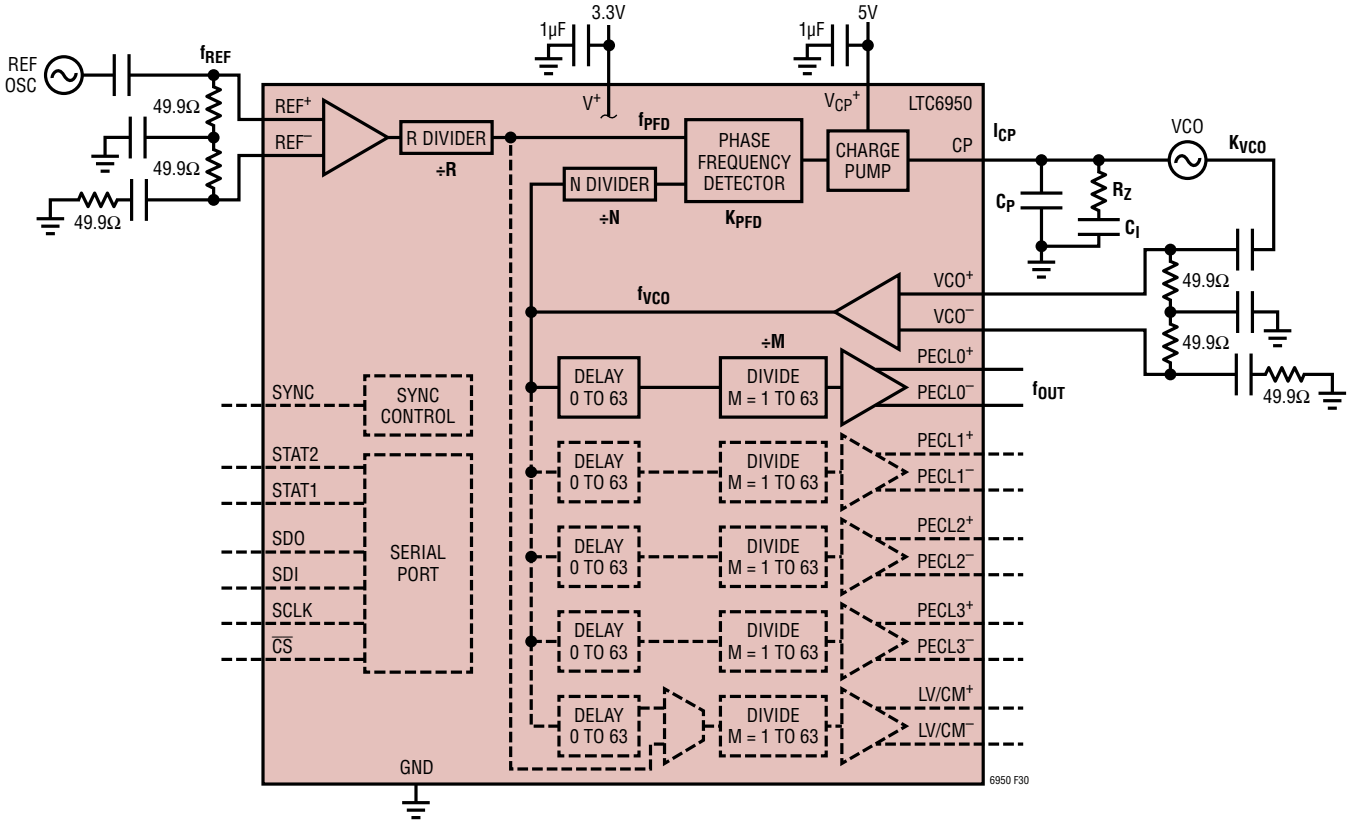


Figure 30. The LTC6950's PLL Loop Diagram and Important Parameters

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Using equations 2 to 5, the output frequency resolution f_{STEP} produced by a unit change in N is given by Equation 6:

$$f_{STEP} = \frac{f_{REF}}{R \bullet M} \quad (6)$$

LOOP FILTER DESIGN

A stable PLL system requires care in selecting the external loop filter values. The Linear Technology ClockWizard™ CAD tool, available from www.linear.com, aids in designing and simulating the complete LTC6950 system. The following design procedure is a useful guide; however, the ClockWizard tool takes care of all of the details automatically and yields an optimized result with minimal effort. Using ClockWizard is highly recommended.

The loop design should use the following algorithm:

1. Determine the output frequency, f_{OUT}, and frequency step size, f_{STEP}, based on application constraints. Using Equations 2, 3, 4, 5 and 6, change f_{REF}, N, R and M until the application frequency constraints are met. For the lowest phase noise, use the minimum R value that satisfies the constraints.

2. Select the open loop bandwidth (BW). A stable loop requires BW to be less than f_{PFD} divided by 10. Because the LTC6950 has very low additive noise, in most applications it is desirable, if possible, to select a loop bandwidth near the crossover frequency of the VCO's phase noise and the output referred reference phase noise (see Figure 31). The *phase noise floor* of the reference, referred to the PLL output, is calculated as follows:

   $$L_{M(REF_OUT)} = L_{M(REF_IN)} - 10 \bullet \log_{10}(R) + 20 \bullet \log_{10}(N)$$

   Whereas the *close-in phase noise* of the reference, referred to the PLL output, uses the following equation:

   $$L_{M(REF_OUT)} = L_{M(REF_IN)} - 20 \bullet \log_{10}(R) + 20 \bullet \log_{10}(N)$$

   To minimize the reference noise at the output, N should be minimized. As seen in Equation 4, the equivalent to minimizing N is maximizing f_{PFD}.

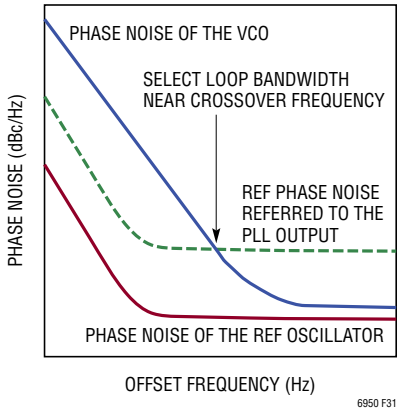


Figure 31. Selecting the PLL's Loop Bandwidth

3. Select the loop filter component R_Z and the charge pump current I_{CP} based on BW and the VCO gain factor (K_{VCO}). BW (in Hz) is approximated by the following equation:

   $$BW \cong \frac{I_{CP} \bullet R_Z \bullet K_{VCO}}{2 \bullet \pi \bullet N} \quad (7)$$

   Which leads to the following equation for R_Z:

   $$R_Z = \frac{2 \bullet \pi \bullet N \bullet BW}{I_{CP} \bullet K_{VCO}} \quad (8)$$

   where K_{VCO} is in Hz/V, I_{CP} is in Amps and R_Z is in Ohms. A larger I_{CP} can result in lower in-band noise due to the lower R_Z resistance and resultant lower thermal noise.

4. Select the loop filter components C_I and C_P based on BW and R_Z. A reliable loop can be achieved by using the following equations for the loop capacitors (in Farads):

   $$C_I = \frac{3.5}{2 \bullet \pi \bullet BW \bullet R_Z} \quad (9)$$

   $$C_P = \frac{1}{7 \bullet \pi \bullet BW \bullet R_Z} \quad (10)$$

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DESIGN AND PROGRAMMING EXAMPLE

For this example, assume the following parameters:

f_{REF} = 19.44MHz CMOS logic signal

f_{VCO} = 622.08MHz

K_{VCO} = 12kHz/V to 18kHz/V

f_{OUT} = 155.52MHz

In this application, the desired output frequency is fixed at 155.52MHz, therefore frequency agility, and hence f_{STEP}, is not an important design parameter. Additionally, the example assumes that the VCO is connected directly to the charge pump output and that PECL0 is enabled as the desired output with all other outputs shut down.

Determining Divider Values

Following the loop filter design algorithm, Equations 2, 3, 4 and 5 can be used to calculate the following values:

M = 4

R = 1

f_{PFD} = 19.44MHz

N = 32

Figure 32 illustrates the configuration.

The next step is to determine the open loop bandwidth (BW). BW should be at least 10x smaller than f_{PFD}. Wider loop bandwidths may have lower integrated phase noise, depending on the VCO phase noise characteristics, while narrower bandwidths will likely have lower spurious power. For this example assume that the optimum loop bandwidth (BW) is 20kHz.

Loop Filter Component Selection

To compute the loop filter resistor R_Z using Equation 8, two additional parameters are required: K_{VCO} and I_{CP}. Because K_{VCO} varies over the VCO's frequency range, using a geometric mean of K_{VCO} gives good results. And to achieve better in-band noise, assume an I_{CP} of 11.2mA:

$$K_{VCO} = 10^3 \bullet \sqrt{12 \bullet 18} = 14.7\text{kHz/V}$$

$$R_Z = \frac{2 \bullet \pi \bullet 32 \bullet 20k}{11.2m \bullet 14.7k} = 24.4k\Omega \approx 24.3k\Omega$$

Using Equations 9 and 10, C_I and C_P may be computed:

$$C_I = \frac{3.5}{2 \bullet \pi \bullet 20k \bullet 24.3k} = 1.15nF \approx 1.2nF$$

$$C_P = \frac{1}{7 \bullet \pi \bullet 20k \bullet 24.3k} = 93.5pF \approx 100pF$$

Status Output Programming

The default configuration for the STAT1 and STAT2 pins can be used to monitor the PLL's lock condition. Register h01 by default is programmed to h04, which results in the STAT1 pin being forced high whenever the LOCK bit asserts. Register h02 by default is programmed to h3B, which results in the STAT2 pin being forced high whenever the NO_VCO, NO_REF, UNLOCK, THI or TLO bits assert.

Power Register Programming

For correct PLL operation, the PDPLL bit in register h03 should be programmed to 0, otherwise the PLL is powered down. The PDALL bit powers down the entire part, so it must also be set to 0. All output sections required to be active must also have the PD bits set to 0 for them to be active. Additionally, the reference and VCO AC detection circuits are enabled, as well as the lock indicator:

register h03 = h08

To power down any unused outputs, set the appropriate PD_OUTx and PD_DIVx bits to 1:

register h04 = hFF

R and N Divider Programming

Program registers h07 to h0A with the previously determined R-divider and N-divider values:

register h07 = h00

register h08 = h01

register h09 = h00

register h0A = h20

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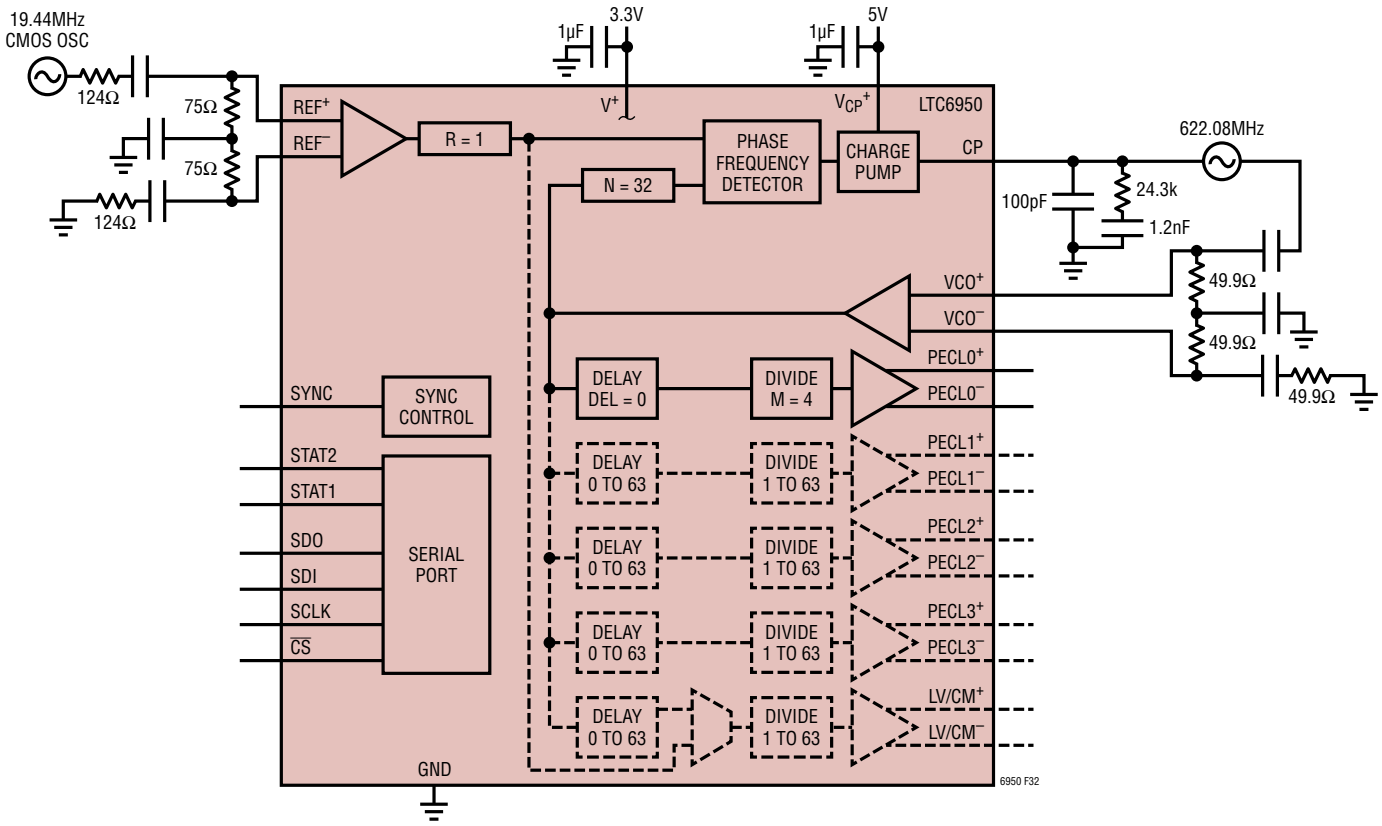


Figure 32. Design Example Configuration

Output Divider Programming

This design example sets the PECL0 output active and set to a divide by 4 with 0 delay. The internal bias IBIAS0 is also enabled on the PECL0 output. The other outputs are powered down and do not need to be programmed:

register h0C = h00

register h0D = h84

Reference and VCO Input Settings and SYNC Mode Settings

The VCO signal has sufficient slew rate that activating the filter is not necessary. However, if the 19.44MHz reference is supplied by a sine wave oscillator, the reference filter will need to be activated. See Tables 14 and 15 for information on FILTR programming. In this example, the reference is provided by an oscillator with a CMOS logic output having sufficient slew rate, so both FILTR and FILTV are set to 0. This example is a standalone application so the SYNC mode is set accordingly:

register h0B = h40

This register also controls the mode of the LV/CM output. As this output is not being used in the example, these bits are set to 0.

Lock Detect and Charge Pump Current Programming

The lock indicator window is determined from f_{PFD}. From Table 1, the appropriate setting is 3ns, or LKWIN[1:0] = 0. The LTC6950 will consider the loop locked as long as the phase coincidence at the PFD is within 21°, as calculated below:

$$\text{phase} = 360° \bullet t_{LWW} \bullet f_{PFD} = 360 \bullet 3n \bullet 19.44M \cong 21°$$

Choosing the correct LOCK_COUNT value depends upon the ratio of the bandwidth of the loop to the PFD frequency

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(BW/f_{PFD}). Smaller ratios dictate larger LOCK_COUNT values. In this example, the ratio is very small at roughly 1/1000 indicating the largest LOCK_COUNT value should be used. Setting LKCT[1:0] = h3 yields a lock count of 2048.

The charge pump current is set to 11.2mA in this example giving CP[3:0] = hB:

register h05 = h3B

Charge Pump Function Programming

For this example, the charge pump's programming features are not utilized. Make certain that the CPDN, CPMID, CPRST and CPUP bits are all set to 0 as the loop will never lock if these bits are asserted:

register h06 = h00

Summary

Here are all of the register settings for this example to lock and function properly:

register h01 = h04

register h02 = h3B

register h03 = h08

register h04 = hFF

register h05 = h3B

register h06 = h00

register h07 = h00

register h08 = h01

register h09 = h00

register h0A = h20

register h0B = h40

register h0C = h00

register h0D = h84

While this design example is illustrative, using the Clock-Wizard CAD tool is strongly recommended to design with the LTC6950.

PHASE NOISE IN A PLL

Since a PLL is a servo with a finite loop bandwidth, working in the frequency domain is the best way to approach noise analysis. Thus, phase noise is the preferred measure. A typical phase noise plot of the output from a PLL is shown in Figure 33. The plot is composed of four distinct regions.

Regions 1 and 2 are inside the PLL's loop bandwidth. In these regions the loop responds to any variation in the reference oscillator's frequency since the loop's purpose is to track the reference. If the reference frequency drifts with time or temperature, the loop makes certain that the output frequency does so as well. As the rate of frequency variation increases, the loop continues to track these changes until the point is reached where the variations are beyond the loop's bandwidth. Beyond the PLL's loop bandwidth, the PLL is unable to track frequency or phase changes and this noise is essentially ignored.

Regions 3 and 4 are outside the PLL's loop bandwidth. In these regions the reference oscillator and the LTC6950's PLL core have little or no influence on the phase noise. Here the phase noise is determined by the VCO and the additive noise of the LTC6950's output dividers and drivers.

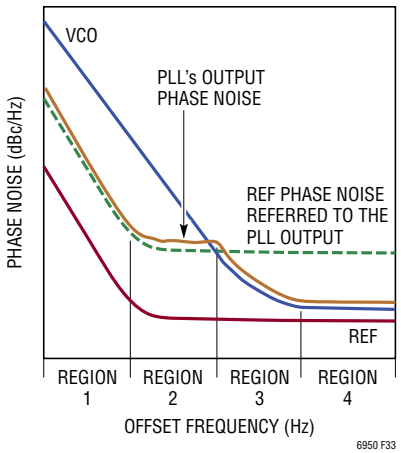


Figure 33. Selecting the PLL's Loop Bandwidth

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Phase Noise in Region 1

The phase noise in region 1 is composed of a combination of the reference oscillator's close-in phase noise, the PLL's 1/f noise and the output divider's additive phase noise. Most of the PLL's 1/f noise in the LTC6950 comes from the charge pump, although there are minor contributions from the R divider, the N divider and the phase/frequency detector. Fortunately, the LTC6950's 1/f noise is very low and this region is usually dominated by the close-in phase noise of the reference.

If the reference oscillator has extremely low close-in phase noise, the in-band phase noise at very low offset frequencies may be influenced by the LTC6950's 1/f noise. Use the normalized in-band 1/f noise of –274dBc/Hz with Equation 11 to approximate the output 1/f phase noise of the LTC6950 at a given frequency offset f_{OFFSET}:

$$L_{M(OUT\ –\ 1/f)}\ (f_{OFFSET}) = \quad (11)$$
$$–274 + 20 \bullet \log_{10}\ (f_{OUT}) – 10 \bullet \log_{10}\ (f_{OFFSET})$$

Unlike the in-band noise floor $L_{M(OUT)}$ (see region 2), the 1/f noise $L_{M(OUT\ –1/f)}$ does not change with f_{PFD} and is not constant over offset frequency. See Figure 34 for an example of in-band phase noise for f_{PFD} equal to 3MHz and 100MHz. The LTC6950's contribution to the total in-band phase noise will be the summation of $L_{M(OUT)}$ and $L_{M(OUT\ –1/f)}$.

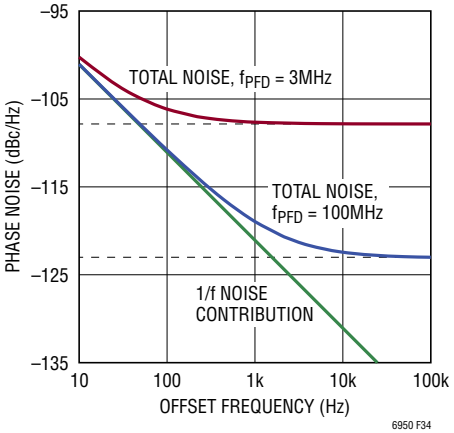


Figure 34. Theoretical In-Band Phase Noise, f_{OUT} = 1.4GHz

Phase Noise in Region 2

The phase noise in region 2 is composed of a combination of the reference oscillator's flatband phase noise (noise floor), the PLL's in-band phase noise and the output divider's additive phase noise. The additive noise of the LTC6950's output dividers is usually not an issue in this region though.

The in-band phase noise produced at the PLL's output may be calculated by using Equation 12:

$$L_{M(OUT)} = \quad (12)$$
$$–226 + 10 \bullet \log_{10}(f_{PFD}) + 20 \bullet \log_{10}\left(\frac{f_{OUT}}{f_{PFD}}\right)$$

which can be rewritten:

$$L_{M(OUT)} =$$
$$–226 + 10 \bullet \log_{10}(f_{PFD}) + 20 \bullet \log_{10}\left(\frac{N}{M}\right)$$

The PLL's in-band phase noise increases at a 20dB per decade rate with N and only a 10dB per decade rate with f_{PFD}. For the lowest phase noise, f_{PFD} should be as large as possible while still satisfying the application's frequency step size requirements.

To calculate the LTC6950 PLL's equivalent *input* referred in-band phase noise floor $L_{M(IN)}$, use Equation 13:

$$L_{M(IN)} = –226 + 10 \bullet \log_{10}\left(\frac{f_{REF}}{R}\right) \quad (13)$$

For example, using a 10MHz reference frequency with R = 1 gives an input phase noise floor of –156dBc/Hz. The reference frequency source's phase noise must be at least 6dB better than this to prevent its noise from limiting the overall system performance. Refer to the Reference Source Phase Noise Considerations section for more information.

Phase Noise in Region 3

The phase noise in region 3 is outside of the PLL's loop bandwidth and is a combination of the VCO's close-in phase noise and the output divider's additive phase noise. The

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additive noise of the LTC6950's output dividers is usually not an issue in this region and the VCO's noise dominates in most cases.

Phase Noise in Region 4

The phase noise in region 4 is composed of a combination of the VCO's flatband phase noise (noise floor) and the output divider's additive phase noise. As noted in the Electrical Characteristics table, the LTC6950's output dividers and drivers have very low phase noise that varies somewhat depending on which logic type output is selected (LVPECL, LVDS or CMOS). The PECLx outputs have the lowest 1/f noise and the lowest noise floor. The LTC6950's additive noise and the VCO's noise floor add in an RMS sense, thus the VCO's floor should be at least 6dB below the LTC6950's divider noise floor to prevent the VCO noise from limiting the overall system performance.

Optimal Loop Bandwidth

As noted earlier, the optimal loop bandwidth for minimal output phase noise is near the crossover of the VCO's phase noise and the output referred reference phase noise. VCOs are frequency tunable and typically have worse close-in phase noise than fixed frequency oscillators. A low noise reference oscillator coupled with the low in-band noise of the LTC6950's PLL results in an extended optimal loop bandwidth, thus relaxing the VCO's close-in phase noise requirement and yielding lower integrated phase noise.

Alternatively, if the application must work with a noisy reference oscillator, the output phase noise can be minimized by selecting a high quality, low noise VCO (perhaps a VCXO or VCSO) and setting a very low loop bandwidth. The loop then locks to what is essentially the average frequency of the reference, ignores most of the reference noise and relies on the VCO to provide low phase noise and jitter. This is how jitter cleaning PLLs work and is only possible if the VCO has considerably lower noise than the reference oscillator.

I/O INTERFACE

The LTC6950 is a high performance PLL and clock distribution chip. To achieve the best performance, it is important to select the proper circuitry to interface to the various inputs and outputs.

REFERENCE INPUT

The LTC6950's reference input buffer provides a flexible interface to either differential or single-ended frequency sources. The frequency range for the reference input is from 2MHz to 250MHz. The reference input signal swing must be less than $1.5V_{P-P}$ to avoid turning on the input buffer's protection diodes (see Figure 35). If the input signal is too large, it should be attenuated. Any reference signal source may also be directly coupled (DC), as long as its common mode voltage is approximately the self-bias voltage of the input buffer (see Figure 35). If the common mode voltage is too high or low, the signal must be level shifted or AC-coupled.

Common signals that may be DC-coupled into the LTC6950's reference input include 2.5V CML and 3.3V LVPECL. Common signals that must be AC-coupled into the LTC6950's reference input include 3.3V CML, LVDS, CMOS and RF style, 50Ω output sine wave oscillators (<7.5dBm signal). 2.5V CML and 3.3V LVPECL signals may optionally be AC-coupled if system design considerations require it. Figures 36 and 37 show many common reference signal interfaces. Note that all signal traces are assumed to be 50Ω transmission lines.

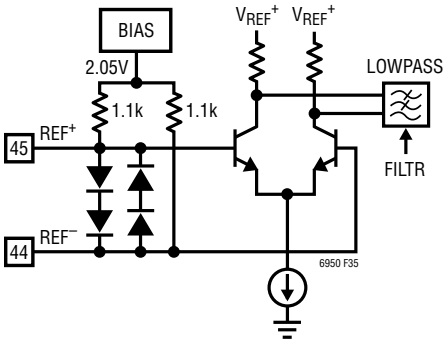


Figure 35. Simplified Reference Input Schematic

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Because the signal applied to the REF± inputs provides the frequency reference for the PLL, it is important that this frequency source has low phase noise and a high slew rate. Using a reference source with an output slew rate of at least 100V/µs will deliver the best phase noise performance; however, the LTC6950 will operate with a reference having an output slew rate of at least 10V/µs. For applications where using a reference source with an output slew rate of at least 100V/µs is not possible, better phase noise performance will be achieved by enabling the internal broadband noise filtering circuit within the reference input buffer. This is accomplished by asserting the configuration bit FILTR in serial port register h0B. Note that setting FILTR = 1 when the slew rate of the reference frequency source is greater than 100V/µs will degrade the overall PLL phase noise performance. Table 14 illustrates how to set the FILTR bit based on the reference input's slew rate.

Table 14. FILTR Programming (Register h0B)

FILTR BIT	REF INPUT SLEW RATE
0	> 100V/µs
1	≤ 100V/µs

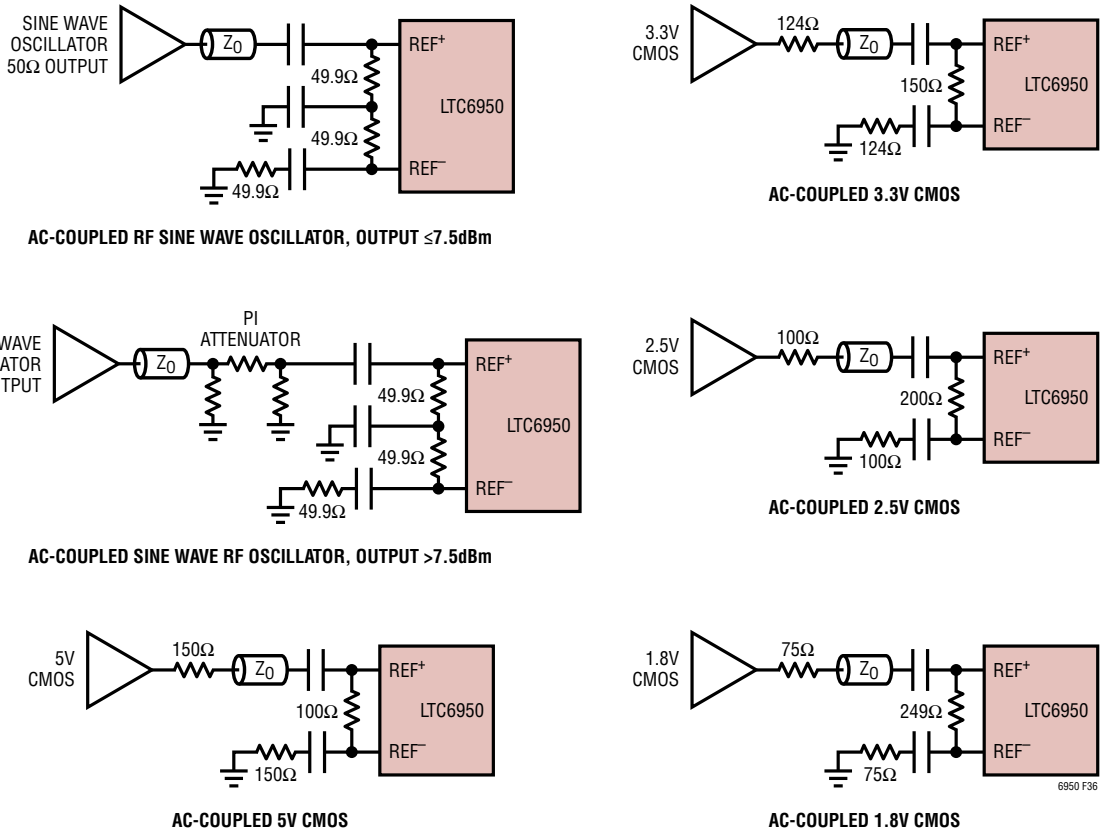


Figure 36. Common Single-Ended Reference Input Interface Configurations. All Z_O Signal Traces Are 50Ω Transmission Lines. All Capacitors Are 0.1µF. All Resistors and Capacitors Are Placed as Close as Possible to the Driver or Receiver with the Transmission Line in Between

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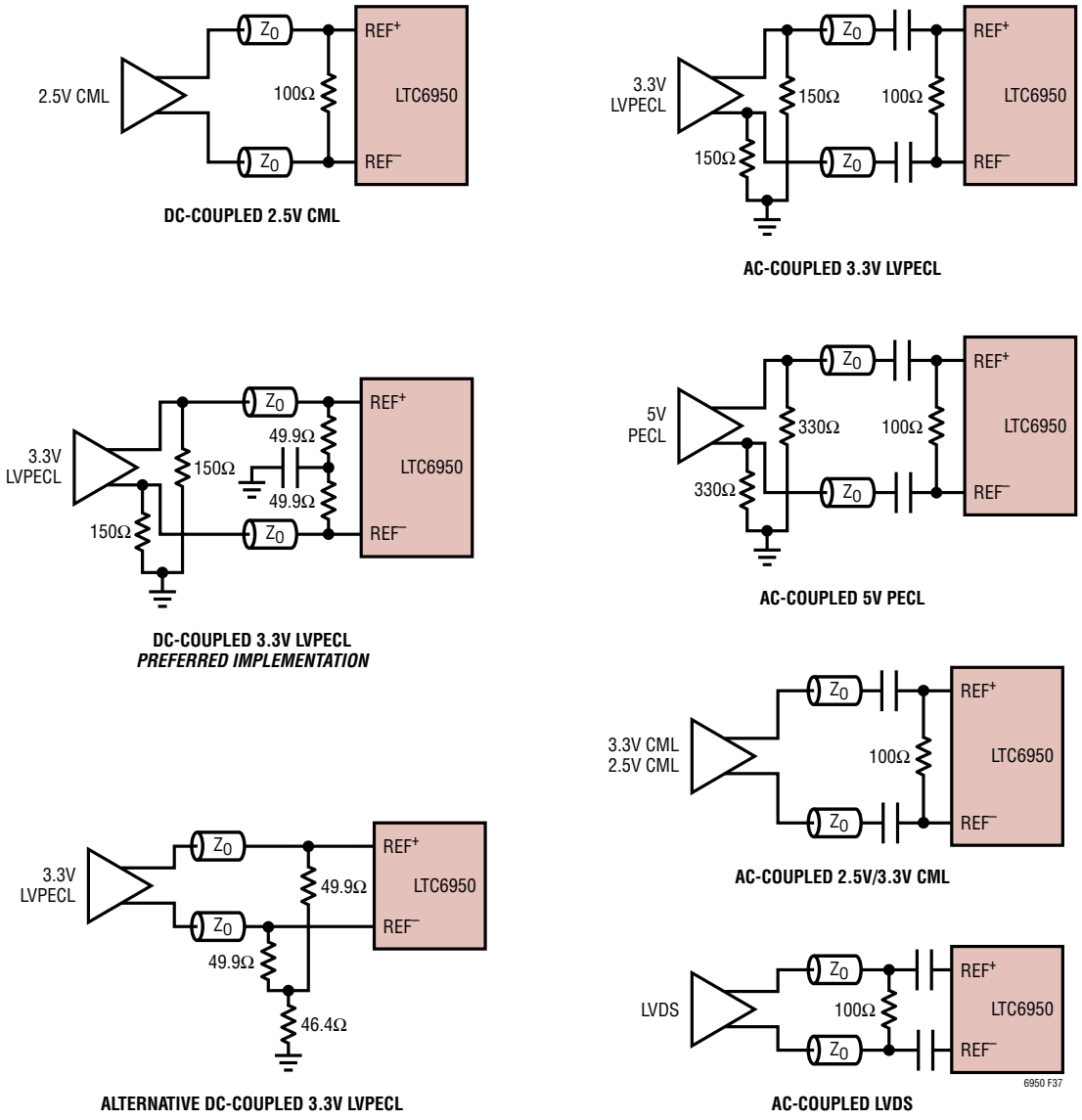


Figure 37. Common Differential Reference Input Interface Configurations. All Z_0 Signal Traces Are 50Ω Transmission Lines. All Capacitors Are 0.1µF. All Resistors and Capacitors Are Placed as Close as Possible to the Driver or Receiver with the Transmission Line in Between

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Typically the FILTR bit is only enabled for relatively low frequency sine wave signals. Logic signals typically have sufficient slew rate as long as there is not excessive capacitive loading, thus the FILTR bit should be disabled when the reference is a logic signal. Table 15 provides guidance for how to set the FILTR bit for sine wave input signals.

Table 15. FILTR Programming for a Sine Wave Reference Input

SINE WAVE INPUT POWER (AMPLITUDE)	FREQUENCY FOR FILTR = 1	FREQUENCY FOR FILTR = 0
7.5dBm (1.5V_{P-P})	≤ 21MHz	> 21MHz
6dBm (1.262V_{P-P})	≤ 25MHz	> 25MHz
0dBm (632mV_{P-P})	≤ 50MHz	> 50MHz
–6dBm (317mV_{P-P})	≤ 100MHz	> 100MHz
–10dBm (200mV_{P-P})	≤ 159MHz	> 159MHz

REFERENCE SOURCE PHASE NOISE CONSIDERATIONS

A high quality signal must be applied to the REF± inputs since they provide the frequency reference to the entire PLL. Consider the analogy of creating a 25V DC source with a low noise op amp and a noisy 1.25V reference. This combination yields a noisy result as the voltage reference's noise is multiplied by the amplifier's gain of 20. In a similar way, applying a noisy reference oscillator signal to the low noise LTC6950 also results in a noisier output signal than could be achieved.

A moderate quality fixed frequency crystal oscillator typically has lower close-in phase noise than most VCOs, even when referred to the PLL's output. To achieve the maximum performance, a low phase noise reference is needed. Using a poor reference oscillator followed by a jitter cleaning PLL usually results in performance far inferior to that attained by using a moderate cost crystal oscillator. Jitter cleaning PLLs are useful in systems where the reference signal is recovered from a data stream but are not a good choice in most other cases.

As stated earlier, the phase noise inside the PLL's loop bandwidth is determined by a combination of the reference oscillator's phase noise and the in-band phase noise of the PLL core. The LTC6950 achieves an in-band normalized phase noise floor of –226dBc/Hz (typical). To calculate its equivalent input referred phase noise floor $L_{M(IN)}$, use Equation 13 repeated here.

$$L_{M(IN)} = -226 + 10 \bullet \log_{10}\left(\frac{f_{REF}}{R}\right) \quad (13)$$

For example, using a 10MHz reference frequency with R = 1 gives an input phase noise floor of –156dBc/Hz. The reference frequency source's phase noise must be at least 6dB better than this to prevent its noise from limiting the overall system performance. In addition, the input should have a slew-rate of at least 100V/µs in order to achieve the part's in-band noise performance, as mentioned previously.

VCO INPUT BUFFER

The LTC6950's VCO input buffer provides a flexible interface to either differential or single-ended frequency sources and is similar in operation to the reference input. The maximum input signal frequency is 1.4GHz. The VCO input signal swing must be less than 1.5V_{P-P} to avoid turning on the input buffer's protection diodes (see Figure 38). If the input signal is too large, it should be attenuated. Any VCO signal source may also be directly coupled (DC), as long as its common mode voltage is approximately the self-bias voltage of the input buffer (see Figure 38). If the common mode voltage is too high or low, the signal must be level shifted or AC-coupled.

Common signals that may be DC-coupled into the LTC6950's VCO input include 2.5V CML and 3.3V LVPECL. Common signals that must be AC-coupled into the LTC6950's VCO input include 3.3V CML, LVDS and RF style, 50Ω output sine wave oscillators (<7.5dBm signal). 2.5V CML and 3.3V LVPECL signals may optionally be AC-coupled if system design considerations require

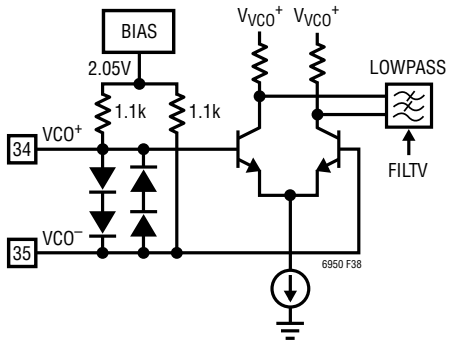
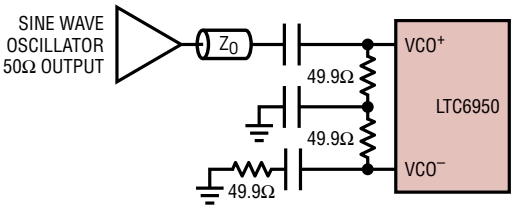
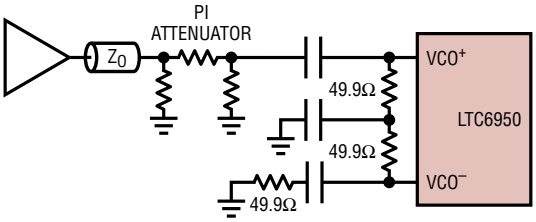


Figure 38. Simplified VCO Input Schematic

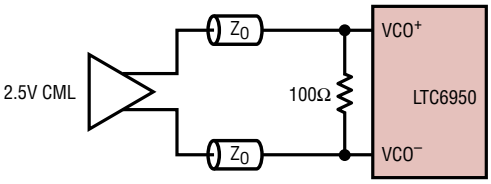
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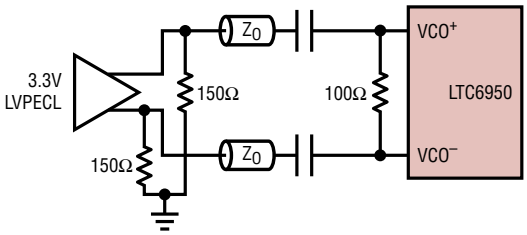
AC-COUPLED RF SINE WAVE OSCILLATOR, OUTPUT ≤7.5dBm



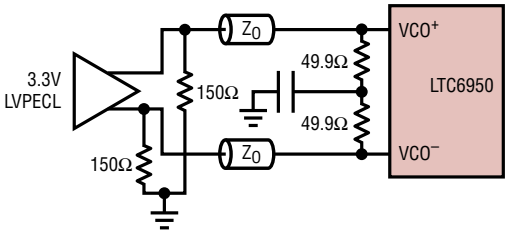
AC-COUPLED RF SINE WAVE OSCILLATOR, OUTPUT >7.5dBm



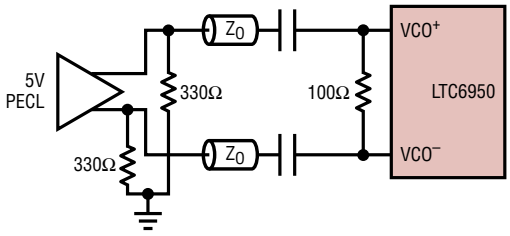
DC-COUPLED 2.5V CML



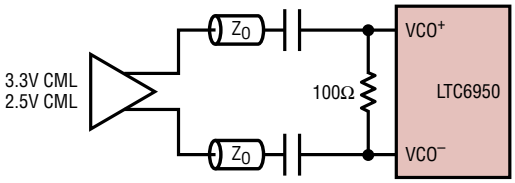
AC-COUPLED 3.3V LVPECL



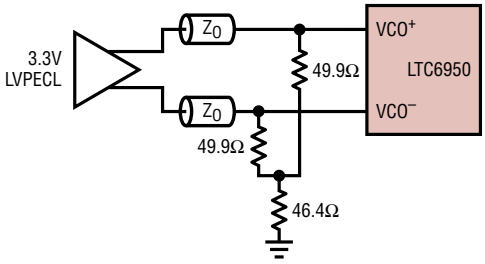
DC-COUPLED 3.3V LVPECL
PREFERRED IMPLEMENTATION



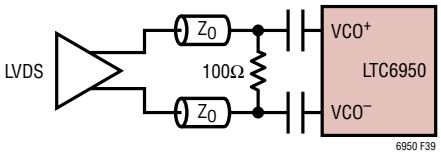
AC-COUPLED 5V PECL



AC-COUPLED 2.5V/3.3V CML



ALTERNATIVE DC-COUPLED 3.3V LVPECL



AC-COUPLED LVDS

Figure 39. Common VCO Input Interface Configurations. All Z_0 Signal Traces Are 50Ω Transmission Lines. All Capacitors Are 0.1µF. All Resistors and Capacitors Are Placed as Close as Possible to the Driver or Receiver with the Transmission Line in Between

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it. Figure 39 shows many common VCO input signal interfaces. Note that all signal traces are assumed to be 50Ω transmission lines. Additionally, the input signal transmission line should be terminated as close to the input as possible to minimize reflections.

It is also important that the VCO± inputs be low noise and have a high slew rate. Using a VCO/VCXO/VCSO with an output slew rate of at least 300V/µs will deliver the best phase noise performance; however, the LTC6950 will operate with a signal having a slew rate of at least 100V/µs. For applications where using a VCO/VCXO/VCSO with an output slew rate of at least 300V/µs is not possible, better phase noise performance will be achieved by enabling the internal broadband noise filtering circuit within the VCO input buffer. This is accomplished by asserting the configuration bit FILTV in serial port register h0B. Note that setting FILTV = 1 when the slew rate of the reference frequency source is greater than 300V/µs will degrade the overall PLL phase noise performance. Table 16 illustrates how to set the FILTV bit based on the VCO input's slew rate.

Table 16. FILTV Programming (Register h0B)

FILTV BIT	VCO INPUT SLEW RATE
0	> 300V/µs
1	≤ 300V/µs

Typically, the FILTV bit is only enabled for relatively low frequency sine wave signals. Logic signals typically have sufficient slew rate as long as there is not excessive capacitive loading, thus the FILTV bit should be disabled when the VCO's output is a logic signal. Table 17 provides guidance for how to set the FILTV bit for sine wave input signals.

Table 17. FILTV Programming for a Sine Wave VCO Input

SINE WAVE INPUT POWER (AMPLITUDE)	FREQUENCY FOR FILTV = 1	FREQUENCY FOR FILTV = 0
7.5dBm (1.50V_{P-P})	≤ 63MHz	> 63MHz
6dBm (1.262V_{P-P})	≤ 75MHz	> 75MHz
0dBm (632mV_{P-P})	≤ 150MHz	> 150MHz
–6dBm (317mV_{P-P})	≤ 300MHz	> 300MHz
–10dBm (200mV_{P-P})	≤ 475MHz	> 475MHz

PECLx OUTPUT DRIVER

The LTC6950 contains four low noise, low skew LVPECL compatible output drivers designed for frequencies up to 1.4GHz. The output driver provides considerable flexibility for biasing and termination. Internal biasing for the output emitter followers may be selected by programming IBIASx to 1 for the appropriate output driver block. See Figure 40 for a simplified schematic.

Enabling the internal bias will usually reduce the number of passive components required off-chip. In many cases, a single 100Ω differential termination at the far end is all that is required. In addition, more symmetrical rise/fall times may result from using the constant current internal bias.

Setting IBIASx to 0 disables the internal bias and allows the PECLx output driver to be configured using standard LVPECL bias and termination networks.

See Table 18 for a summary of the registers containing the internal bias control bits for each PECLx output driver. See Table 11, Serial Port Register Mapping, for complete register mapping information.

The LTC6950 allows powering down of many blocks, including the PECLx output drivers. When a PECLx output driver is powered down, the output pins will float to approximately 0.8V below V_{Px}^+. Depending on the external bias and termination circuits connected to the PECLx output pins, the output driver may actually source current in this mode. To achieve maximum power savings, it is recommended that no terminations or other bias circuitry be connected to an unused PECLx output that will be powered down. Additionally, if the output is expected to be turned on and off, using the internal bias with a single 100Ω differential far end termination gives the lowest power consumption in the powered down state.

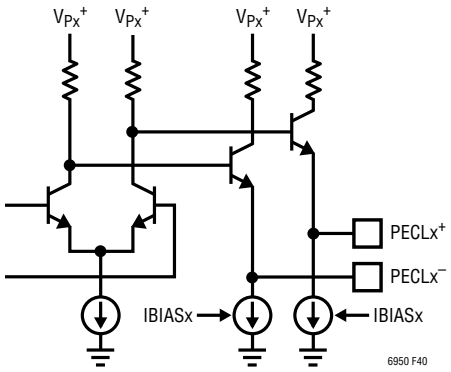


Figure 40. Simplified PECLx Output Schematic

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Table 18. PECLx Internal Bias Control Registers

PECLx OUTPUT	INTERNAL BIAS CONTROL	BIT	REG ADDR (HEX)
PECL0	IBIAS0	[7]	0D
PECL1	IBIAS1	[7]	0F
PECL2	IBIAS2	[7]	11
PECL3	IBIAS3	[7]	13

The PECLx outputs are emitter followers and thus have a low output impedance. The PECLx output signals also have very fast rise and fall times. To maintain proper signal integrity (sharp rise and fall times with minimal ringing), route signals with well controlled transmission lines with proper far end termination. In cases where the full LVPECL compatible signal swing is not required, consider using a series resistor to provide additional near end transmission line termination. With both near and far end termination, manufacturing variations of the transmission lines in production are more easily tolerated. This configuration is also recommended for driving ADCs as discussed in the Using the LTC6950 to Drive ADC Sample Clock Inputs section.

Figure 41 shows how to interface the PECLx outputs to many typical input receivers. Driving an LVDS input is a somewhat special case. Most LVDS inputs are designed to accept a wide range of input signal swings and common

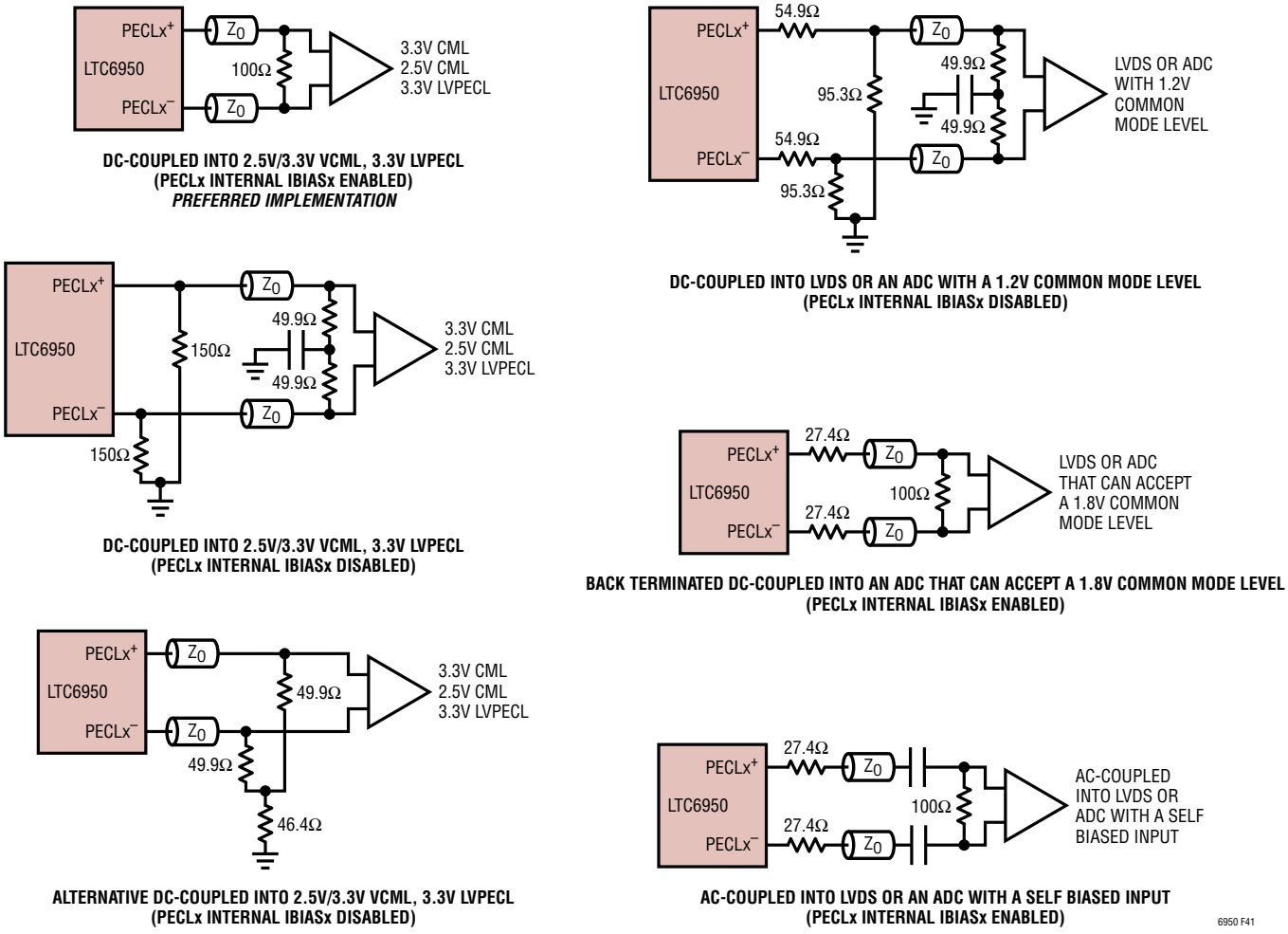


Figure 41. Common PECLx Output (PECL0, PECL1, PECL2 and PECL3) Interface Configurations. All Z_0 Signal Traces Are 50Ω Transmission Lines. All Capacitors Are 0.01µF. All Resistors and Capacitors Are Placed as Close as Possible to the Driver or Receiver with the Transmission Line in Between

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mode levels. For many LVDS inputs, a simple connection is fine. For LVDS inputs operating on a lower power supply voltage, a 1.2V common mode level is required. This requirement is easily met by using a few resistors to level shift the signal from approximately 1.8V down to 1.2V. In this configuration, the signal's peak-to-peak amplitude is also reduced but because a PECLx signal is much larger than an LVDS signal (1600mV$_{P-P(DIFF)}$ vs 800mV$_{P-P(DIFF)}$), the signal at the LVDS receiver is at the correct level for both the common mode level and the voltage swing. As a side benefit, this configuration also provides both near and far end transmission line termination.

LV/CM OUTPUT DRIVER

The LTC6950 contains one output driver capable of being configured as an LVDS or CMOS logic output driver (see Figures 42 and 43 for simplified schematics). Programming the LVCMS bit in register h0B to 1 allows LVDS compatible operation at frequencies up to 800MHz. Setting it to 0 configures two CMOS compatible output drivers with a maximum operating frequency of 250MHz.

When the output driver is configured for CMOS operation, programming the bit CMSINV in register h0B to 1 provides an inverted CMOS logic output on LV/CM$^-$ (pin 21) with respect to the CMOS logic signal at LV/CM$^+$ (pin 22). Setting CMSINV to 0 results in both LV/CM$^+$ and LV/CM$^-$ being in phase.

While the CMOS output is rated to 250MHz, it is recommended that the LVDS output mode be used for operation at frequencies beyond 50MHz. The nature of CMOS signaling (single-ended, large current spikes, large signal swing, poor capacitive load driving) makes it most useful for lower frequencies and short interconnection length. For higher frequencies or longer interconnection lengths, LVDS output mode is a much better choice. LVDS is designed to drive transmission lines and its inherent differential nature provides superior noise immunity.

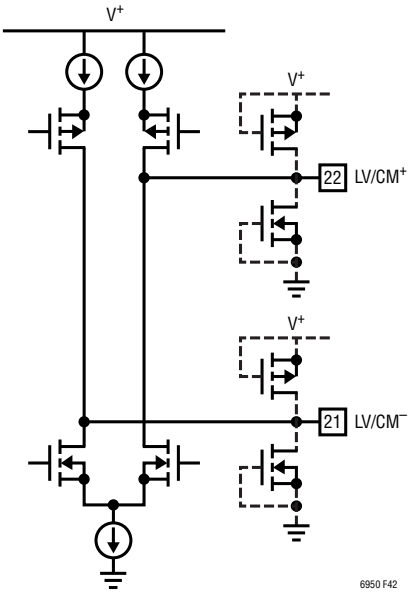


Figure 42. Simplified LV/CM Output Schematic (LVDS Mode, CMOS Circuit Shutdown)

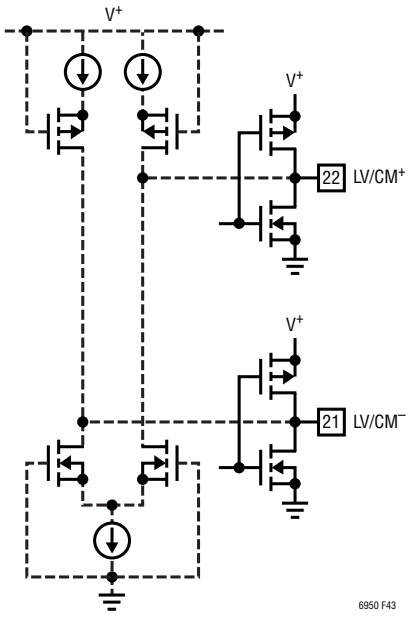


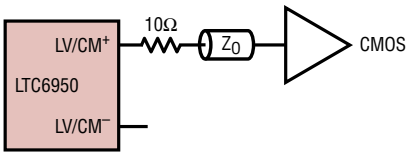
Figure 43. Simplified LV/CM Output Schematic (CMOS Mode, LVDS Circuit Shutdown)

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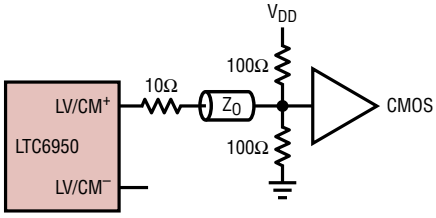
When a CMOS signal is required, Figure 44 shows some common interfaces. The use of the series termination is the most common configuration and is suitable for short interconnection lengths since the transmission line and CMOS input's capacitance will reduce the rise and fall times. The doubly terminated circuits suffer from reduced signal swing at the far end that may not be acceptable with some CMOS input circuits.

When the LVCMS bit is set to 1, the LV/CM outputs are configured for LVDS operation. Figure 44 shows common LVDS output interfaces to various logic types of inputs.

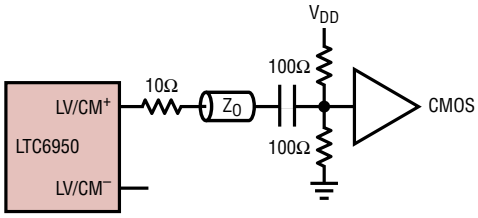
When the LV/CM output is powered down through either the PD_OUT4 or PD_DIV4 bits, the output is placed in a Hi-Z state regardless of the output mode being LVDS or CMOS.



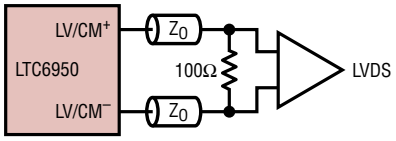
CMOS OUTPUT MODE, DC-COUPLED INTO CMOS WITH A SOURCE TERMINATION
(TRANSMISSION LINE SHOULD BE NO LONGER THAN 10cm)



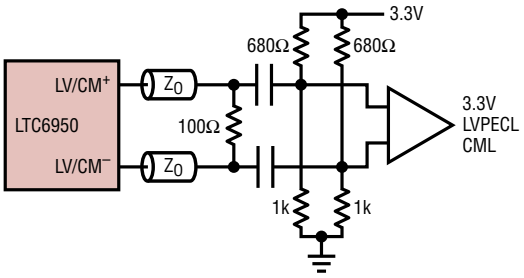
CMOS OUTPUT MODE, DC-COUPLED AND DOUBLY TERMINATED INTO CMOS
(SIGNAL SWING AT THE LOAD WILL BE REDUCED)



CMOS OUTPUT MODE, AC-COUPLED AND DOUBLY TERMINATED INTO CMOS
(SIGNAL SWING AT THE LOAD WILL BE REDUCED)



LVDS OUTPUT MODE, DC-COUPLED AND FAR END TERMINATED INTO LVDS



LVDS OUTPUT MODE, AC-COUPLED INTO LVPECL OR CML

THIS CIRCUIT WORKS WITH MANY LVPECL RECEIVER PARTS THAT CAN ACCEPT THE SMALLER LVDS SIGNAL SWING
($800mV_{P-P(DIFF)}$ FOR LVDS COMPARED TO $1600mV_{P-P(DIFF)}$ FOR LVPECL)

6950 F44

Figure 44. Common LV/CM Output Interface Configurations. All Z_0 Signal Traces Are 50Ω Transmission Lines. All Capacitors Are 0.1µF. All Resistors and Capacitors Are Placed as Close as Possible to the Driver or Receiver with the Transmission Line in Between

APPLICATIONS INFORMATION

LOOP FILTERS USING AN OP AMP

Some VCO tune voltage ranges are greater than the LTC6950's charge pump voltage range. An active loop filter using an op amp allows the LTC6950 to interface with these VCOs. To maintain the LTC6950's high performance, care must be given to picking an appropriate op amp.

The op amp input common mode voltage should be biased at the LTC6950 charge pump's mid-supply ($V_{CP}^+/2$), while its output voltage should achieve the VCO tuning range. See Figure 45 for an example op amp loop filter.

The op amp's input bias current is supplied by the charge pump; minimizing this current keeps spurs related to f_{PFD} low. The input bias current should be less than the charge pump leakage (found in the Electrical Characteristics section) to avoid increasing spurious products.

Op amp noise sources are highpass filtered by the PLL loop filter and should be kept at a minimum, as their effect raises the total system phase noise beginning near the loop bandwidth. Choose a low noise op amp whose input-referred voltage noise is less than the thermal noise of R_Z. Additionally, the gain bandwidth of the op amp should be at least 15 times the loop bandwidth to limit phase margin degradation. The LT1678 is an op amp that works well in most applications. An additional R-C lowpass filter (formed by R_{P2} and C_{P2} in Figure 45) connected at the input of the VCO will limit the op amp noise sources. The bandwidth of this filter should be placed approximately 15 to 20 times the PLL loop bandwidth to limit loop phase margin degradation. R_{P2} should be small (preferably much less than R_Z) to minimize its noise impact on the loop. However, picking too small of a value can make the op amp unstable as it has to drive the capacitor in this filter.

Note that using an op amp at the charge pump output increases the voltage range available to tune the VCO. However, it also adds an inversion in the loop transfer function. When using an op amp, the CPINV bit in register

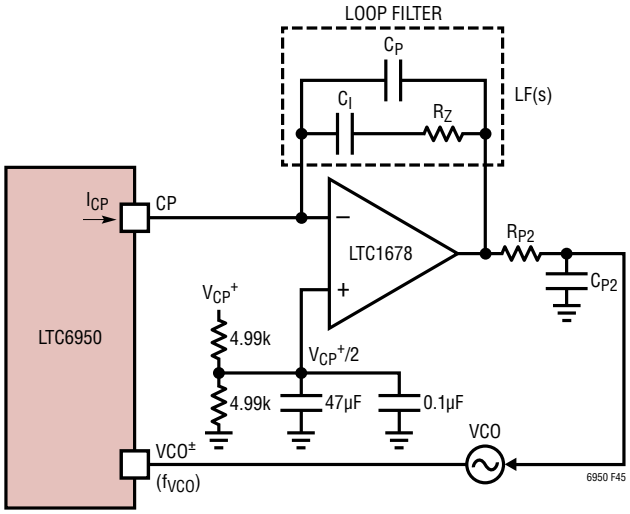


Figure 45. Op Amp Loop Filter

h06 must be set to 1 to compensate for this inversion, assuming a positive VCO transfer function (a positive K_{VCO}). If the loop polarity is incorrect, the loop will have positive feedback and will not work. Most VCOs have a positive K_{VCO} and should have the CPINV bit set to a 1 for proper loop operation with an op amp at the charge pump's output.

PCB LAYOUT GUIDELINES

The LTC6950 requires a printed circuit board (PCB) with a clean unbroken ground plane in the first layer beneath the part. A multilayer board with an internal ground plane is recommended. Care must be taken when creating a PCB layout to minimize power supply and ground inductances and to prevent signals from interfering with each other.

Layout for the printed circuit board should ensure that digital signals (serial port, SYNC and STAT pins) and analog signals (all other signal pins) are separated as much as possible. Additionally, top layer ground fill and grounded vias should be used as barriers to isolate signals from each other.

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The LTC6950 reference input, VCO input and all signal outputs must be routed using transmission lines. Traces should be as short as possible to minimize capacitance and interference pickup.

The LTC6950's demonstration circuit, DC1795, provides a good example of proper PCB layout. The files for this demo circuit are found on the Linear Technology (www.linear.com) website's LTC6950 landing page.

REFERENCE SIGNAL ROUTING AND SPURS

The routing of the reference oscillator input, the charge pump output and the VCO input requires special attention. The charge pump operates at the PFD's update frequency f_{PFD}. The resultant output spurious energy is small and is further reduced by the loop filter before it modulates the VCO frequency. However, improper PCB layout can degrade the LTC6950's inherent spurious performance. Care must be taken to prevent the reference signal from coupling onto the VCO's tune line, or into other loop filter signals. Below are some suggestions.

1. Use separate ground vias for each power supply decoupling capacitor, especially those connected to V_{REF}^+, V_{CP}^+, and V_{VCO}^+.
2. Physically separate the reference frequency signal from the loop filter and VCO.
3. Ground fill and grounded vias should be used as barriers to isolate the reference signal from the charge pump output and loop filter.

SUPPLY BYPASSING

High quality ceramic bypass capacitors such as X5R, X7R or X6S dielectrics should be used at all of the supply pins (V^+, V_{P0}^+, V_{P1}^+, V_{P2}^+, V_{P3}^+, V_{VCO}^+, V_{CP}^+ and V_{REF}^+). Each pin should have its own bypass cap if possible. This is easily achieved with 0201 size capacitors located on the top side layer with the LTC6950. A good strategy is to use one 0.01µF size 0201 capacitor per pin on the top side of the PCB with additional 0.1µF size 0402 connected to selected pin pairs on the back side of the PCB. This provides good, high frequency bypassing and minimizes channel-to-channel crosstalk. The one exception would be the V_{CP}^+ pin which is best bypassed with a 0.1µF size 0402 capacitor connected directly to the pin on the top side of the PCB. Demo circuit 1795 provides a good example of good supply connections, proper bypassing and capacitor ground connections.

Bypass capacitors must be located as close to the pins as possible and connected to ground through a low impedance path. The traces connecting the pins and bypass capacitors must be kept short and should be made as wide as possible. The ground connection for each capacitor must have its own ground via and should also be connected to the top layer ground pour.

THE EXPOSED PAD CONNECTION – SIGNAL GROUNDING AND HEAT TRANSFER

The exposed pad on the bottom of the package is the primary ground connection for the LTC6950 and its connection is as important as any other pin on this part. The inductance to the ground plane must be kept to a minimum to ensure peak performance and good signal integrity. The exposed pad must be soldered directly to a matching PCB land. The PCB land pattern should be connected to the internal ground planes by an array of vias as shown in Figure 46. Consult the QFN Package User's Guide on the Linear Technology website's Packaging Information page for specific recommendations concerning land patterns and land via solder masks.

Additionally, most of the heat generated by the LTC6950 is removed from the die through the bottom side exposed pad onto the printed circuit board. Fortunately, the above guidelines for signal grounding also yield the best thermal assembly and layout. Soldering of the exposed pad to a matching PCB land provides the most direct thermal connection. Connecting this PCB land to all ground layers through an array of vias also is the best way to add thermal mass and to spread the heat as much as possible.

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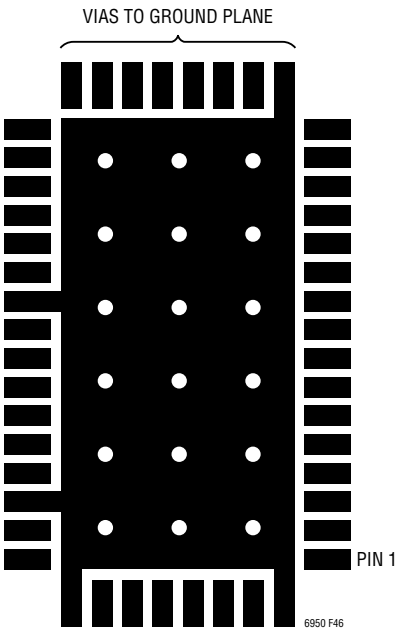


Figure 46. PCB Top Metal Layer Pin and Exposed Ground Pad Design Highlighting the Array of Ground Vias. Also Note Pins 17, 31, 38, 41 and 48 Are Signal Ground and Connected Directly to the Exposed Pad Metal

For the best thermal transfer, the array of vias should extend to the back side of the PCB where a sizable area of the solder mask should be cleared to open the plated copper directly to the air. The exposed area should be at least as large as the land pattern on the top of the PCB. Again, demo circuit 1795 provides a good example of grounding the LTC6950 from both the signal and thermal standpoints.

Following these guidelines achieves a good ground signal connection and a good thermal connection. However, much of this good practice can be undone if the ground plane has a significant void or narrowing near the part. This often occurs inadvertently when there is a long row of adjacent signal or power vias. The clearance around these vias can be very close to each other, or overlapping, creating a void in the plane. In extreme cases a small ground island can form.

One area on the LTC6950 where a ground plane void could occur is on the side of the part with the PECLx outputs, PECL0 through PECL3 (pins 1 to 16). The most difficult case is when all four outputs are to be routed using stripline transmission lines (transmission lines buried between ground planes inside the PCB). Figure 47 illustrates the issue. Using stripline transmission lines necessitates vias to a lower layer preferably located close to each output pin. Additionally, all of the V_{PX}^+ power pins require a via to the power plane that should ideally also be located close to each pin. As shown in Figure 47, when all of these vias are located as close to each pin as possible (which is good for many reasons) and in a row, there is a significant void in the ground plane in this area. This void is undesirable both electrically and thermally. The empty space increases the ground inductance for the PECLx outputs' return signal path and decreases the flow of heat in that direction.

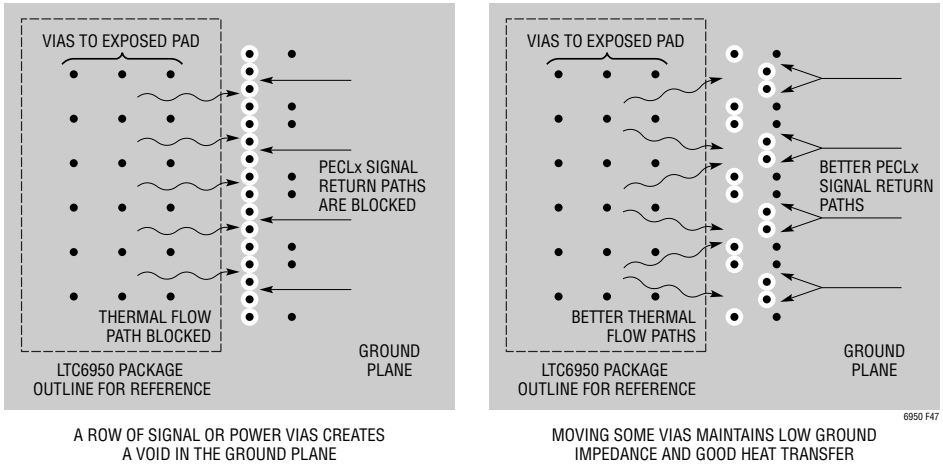


Figure 47. The Ground Plane Can Be Inadvertently Split by a Row of Vias Resulting in Higher Ground Impedance and Poor Heat Transfer. Moving or Staggering Some Vias Fixes the Problem

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Figure 47 also illustrates that by pulling some of the vias away from the part, in this case the PECLx output vias, significant paths for current and heat flow are opened. This is not ideal from the transmission line design standpoint, but definitely improves the ground path inductance and the thermal flow. Alternatively, the V_{Px}^+ supply vias could be pulled further away from the part or a microstrip transmission line on layer 1 of the PCB could be utilized instead of the stripline traces, thereby eliminating the need for PECLx output vias entirely.

ADC CLOCKING AND JITTER REQUIREMENTS

Adding noise directly to a clean signal clearly reduces its signal to noise ratio (SNR). In data acquisition applications, digitizing a clean signal with a noisy clock signal also degrades the SNR. This issue is best explained in the time domain using jitter instead of phase noise. For this discussion, assume that the jitter is white (flat with frequency) and of Gaussian distribution.

Figure 48 shows a sine wave signal entering a typical data acquisition circuit composed of an ADC, an input signal amplifier and a sampling clock. Also shown are three signal sampling scenarios for sampling the sine wave at its zero crossing.

In the first scenario, a perfect sine wave input is buffered by a noiseless amplifier to drive the ADC. Sampling is performed by a perfect, zero jitter clock. Without any added noise or sampling clock jitter, the ADC's digitized output value is very clearly determined and perfectly repeatable from cycle to cycle.

In the second scenario, a perfect sine wave input is buffered by a noisy amplifier to drive the ADC. Sampling is performed by a perfect, zero jitter clock. The added noise results in an uncertainty in the digitized value, causing an error term which degrades the SNR. The degraded SNR in this scenario, from adding noise to the signal, is expected.

In the third scenario, a perfect sine wave input is buffered by a noiseless amplifier to drive the ADC. Sampling is performed by a clock signal with added jitter. Note that as the signal is slewing, the jitter of the clock signal leads to an uncertainty in the digitized value and an error term just as in the previous scenario. Again, this error term degrades the SNR.

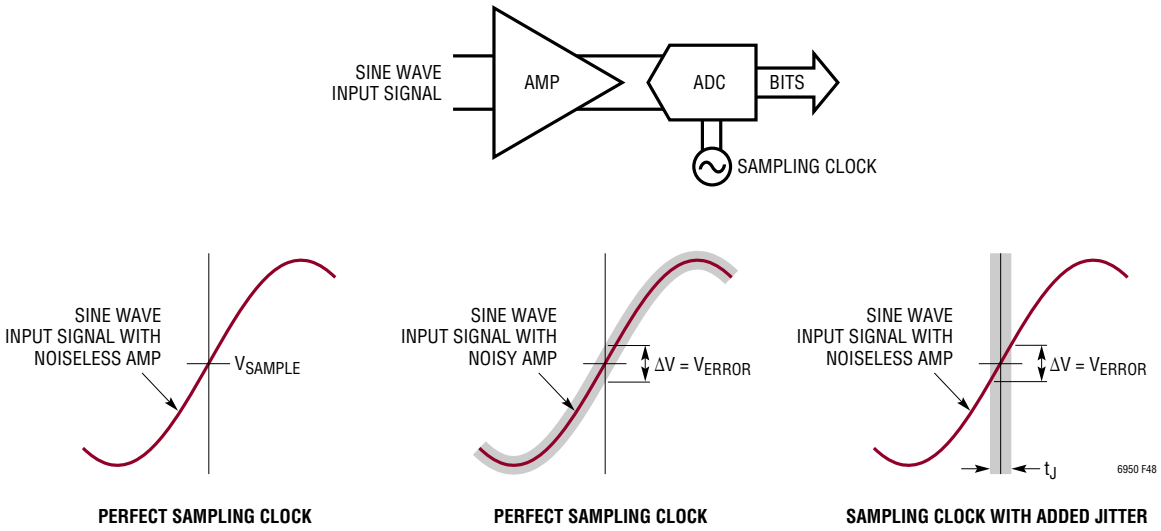


Figure 48. A Typical Data Acquisition Circuit Showing the Sampling Error Effects of a Noisy Amplifier and a Jittery Sampling Clock

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A real world system will have both some additive amplifier noise and some sample clock jitter. Once the signal is digitized, determining the root cause of any SNR degradation – amplifier noise or sampling clock jitter – is essentially impossible.

Degradation of the SNR due to sample clock jitter only occurs if the input signal is slewing. If the input signal is stationary (DC) then it does not matter when in time the sampling occurs. Additionally, a faster slewing signal yields a greater error (more noise) than a slower slewing signal. Figure 49 demonstrates this effect. Note how much larger the error term is with the fast slewing signal than with the slow slewing signal. To maintain the data converter's SNR performance, digitization of high input frequency signals requires a clock with much less jitter than applications with lower frequency input signals.

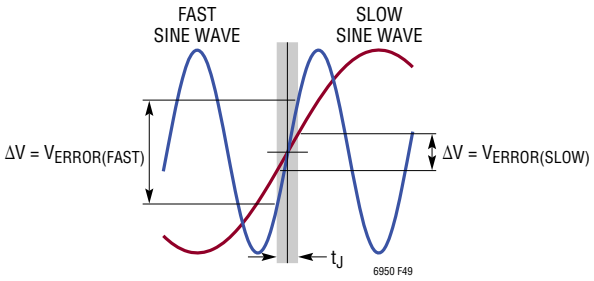


Figure 49. Fast and Slow Sine Wave Signals Sampled with a Jittery Clock

It is important to note that *the frequency of the input signal determines the sample clock's jitter requirement. The actual sample clock frequency does not matter.* Many ADC applications that undersample high frequency signals have especially challenging sample clock jitter requirements.

The previous discussion was useful for gaining an intuitive feel for the SNR degradation due to sampling clock jitter. Quantitatively, the actual sample clock jitter requirement for a given application is calculated as follows:

$$t_{J(TOTAL)} = \frac{10^{\frac{-SNR_{dB}}{20}}}{2 \bullet \pi \bullet f_{SIG}}$$

Where f_{SIG} is the highest frequency signal to be digitized expressed in Hz, SNR_{dB} is the SNR requirement in decibels and $t_{J(TOTAL)}$ is the total RMS jitter in seconds. The total jitter is the RMS sum of the ADC's aperture jitter and the sample clock jitter calculated as follows:

$$t_{J(TOTAL)} = \sqrt{t_{J(CLK)}^2 + t_{J(ADC)}^2}$$

Alternatively, for a given total jitter, the attainable SNR is calculated as follows:

$$SNR_{dB} = -20\log_{10}\left(2 \bullet \pi \bullet f_{SIG} \bullet t_{J(TOTAL)}\right)$$

These calculations assume a full-scale sine wave input signal. If the input signal is a complex, modulated signal with a moderate crest factor, the peak slew rate of the signal may be lower and the sample clock jitter requirement may be relaxed.

These calculations are also theoretical. They assume a noiseless ADC with infinite resolution. All realistic ADCs have both added noise and a resolution limit. The limitations of the ADC must be accounted for to prevent over specifying the sampling clock.

Figure 50 plots the previous equations and provides a simple, quick way to estimate the sampling clock jitter requirement for a given input signal or the expected SNR performance for a given sample clock jitter.

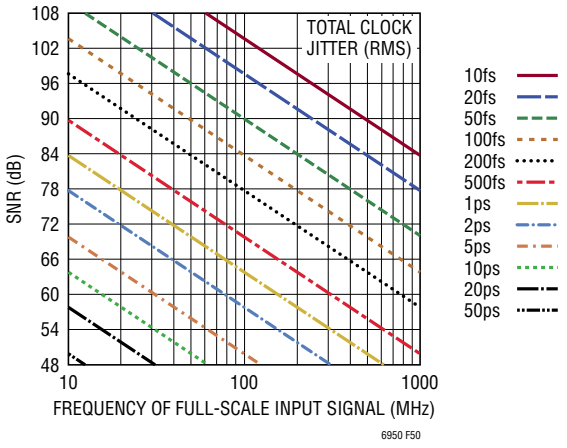


Figure 50. SNR vs Input Signal Frequency vs Sample Clock Jitter

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ADC SAMPLE CLOCK INPUT DRIVE REQUIREMENTS

Modern high speed, high resolution ADCs are incredibly sensitive components able to match laboratory instruments in many regards. With wide bandwidth and wide dynamic range, any noise or interfering signals on the analog signal input, the voltage reference or the sampling clock input of the ADC can easily appear in the digitized data. To deliver the full performance of any ADC, the sampling clock input must be driven with a clean, low jitter signal.

Figure 51 shows a simplified version of a typical ADC sample clock input. In this case the input pins are labeled ENC±, for Encode, while some ADCs label the inputs CLK± for Clock. The input is composed of a differential limiting amplifier stage followed by a buffer that directly controls the ADC's track and hold stage.

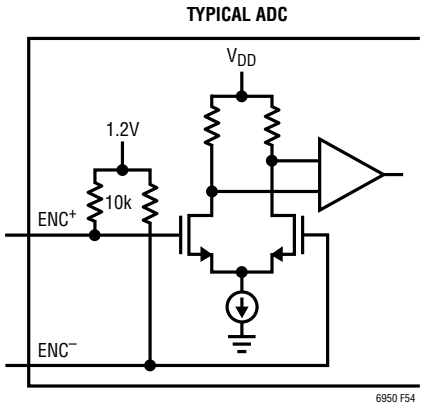


Figure 51. Simplified Sample Clock Input Circuit

The input amplifier requires a minimum input signal amplitude to enter limiting. The sampling clock signal's amplitude should be somewhat greater than the minimum requirement to assure that the amplifier is limiting under all conditions, but not so large as to damage the ADC. A typical minimum input signal level is in the $300mV_{P-P(DIFF)}$ to $400mV_{P-P(DIFF)}$ range.

The sample clock input amplifier also benefits from a fast slewing input signal as the amplifier has noise of its own. By slewing through the crossover region quickly, the amplifier noise creates less jitter than if the transition were slow.

As shown in Figure 51, the ADC's sample clock input is typically differential. Although the amplifier will work fine with a single-ended input signal, a differential sampling clock typically delivers the best performance.

The LTC6950 meets all of these sample clock input requirements. The output signals are differential, low phase noise (thus low jitter), have sharp rise and fall times and drive high speed transmission lines with more than enough signal swing.

The LTC6950's PECLx outputs are recommended for the best phase noise performance. While the LVDS and CMOS signals provide good phase noise performance, the PECLx outputs have the lowest phase noise.

TRANSMISSION LINES AND TERMINATION

Interconnection of high speed signaling with fast rise and fall times requires the use of transmission lines with properly matched termination. The transmission lines may be stripline, microstrip or any other design topology. A detailed discussion of transmission line design is beyond the scope of this data sheet. Any mismatch between the transmission line's characteristic impedance and the terminating impedance results in a portion of the signal reflecting back toward the other end of the transmission line. In the extreme case of an open or short circuit termination, all of the signal is reflected back.

This signal reflection leads to overshoot and ringing on the waveform. The frequency of ringing is inversely proportional to the propagation delay through the transmission line, which is mostly dependent on the length of the line. The amplitude of the ringing is dependent on the degree of mismatch between the transmission line's characteristic

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impedance and the termination impedance at each end of the line. The greater the mismatch, the larger the reflection and the greater the amplitude of the ringing. Figure 52 shows three methods of transmission line termination with a low impedance driver and a high impedance receiver.

Far end termination is sometimes referred to as parallel or shunt termination of the transmission line. Its purpose is to match the transmission line's impedance and prevent signal reflection back to the driver. Any mismatch at the far end results in a portion of the initial signal being reflected back to the driver. As the low impedance driver is poorly matched to the transmission line, most of this reflected signal is re-reflected back to the receiver. This back-and-forth signaling continues until the reflected signal energy eventually dies out.

Near end termination is sometimes referred to as source, series or back termination. Its purpose is to match the transmission line and prevent any of the reflected signal from the far end from being re-reflected back to the receiver. The far end receiver is a high impedance and is poorly matched to the transmission line, resulting in most of the signal being reflected back to the driver. The termination at the source absorbs most of this reflected signal, but if there is a mismatch in the impedance, some of the signal is re-reflected back to the receiver. This back-and-forth signaling continues until the reflected signal energy eventually dies out.

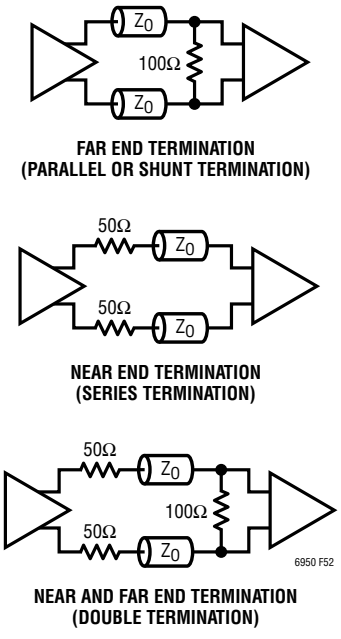


Figure 52. Transmission Line Termination Methods (Z_0 = 50Ω)

Near and far end termination is sometimes referred to as double termination. The advantage of double termination over the simpler far end or near end termination is if there is any mismatch at the far end, its reflection will be largely absorbed by the near end termination. Therefore, the reflected energy dies out rapidly as each re-reflected signal is considerably smaller at each turn.

The disadvantage of double termination is that the signal level at the receiver is only half the amplitude of the source's signal. However, this loss of signal amplitude is acceptable in many cases. The series resistor used in near end termination also adds some noise to the signal.

Double termination makes for a more robust and forgiving system design. Production variation of the printed circuit board (PCB) that would affect the transmission line's characteristic impedance is more easily accommodated. Variation of the termination resistor value and its non-idealities are also less critical. Delivering good signal integrity is more easily achieved with double termination of transmission lines at the cost of some added noise.

ADC SAMPLE CLOCK INPUT SIGNAL INTEGRITY REQUIREMENTS

Figure 51 is a simplified ADC sample clock input circuit. The simplification omits many of the circuit details and also omits parasitic elements in the circuit. These parasitic elements play an important role in the ADC's sample clock input signal integrity requirements.

Logic applications can tolerate a significant amount of signal overshoot and ringing. For a logic system to work properly, the only requirement is that logic 0 and logic 1 states are separable. A logic 0 or logic 1 state signal with large amounts of ringing, ripple and interference causes little concern in a logic system.

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The ADC sample clock input has a different signal integrity requirement than a logic input. In fact, *the ADC sample clock should never be thought of as a logic signal*. It is more like the local oscillator (LO) input signal of a mixer where signal noise, ringing and interferers are imprinted onto the signal of interest. However, in a mixer application, undesired out of band signals are often easily filtered away at the output. Due to the sampling nature of an ADC, undesired high frequency signals can fold back into the frequency band of interest and corrupt the desired signal. In the case of an ADC, noise, ringing and interference can appear in the digitized data along with the analog input signal and are not easily removed with digital filtering.

Without considering parasitic signal paths, it appears that once the input amplifier is limiting, any noise or ringing at the ADC's sample clock input has no effect. However, the ADC's sample clock input has several parasitic elements that provide a signal path to the track and hold circuit and ultimately to the digitized data. On-chip layout and device parasitic capacitance present one path for undesired high frequency signals to couple into the track and hold. Another path is the ADC's substrate resistance. As this resistance is finite, coupling through this path is also possible. The coupling through these paths is heavily attenuated, but with SFDR in excess of 100dB in modern ADCs, it does not take very much coupled signal to appear in the digitized data.

USING THE LTC6950 TO DRIVE ADC SAMPLE CLOCK INPUTS

As noted earlier, the LTC6950's PECLx outputs are recommended for the best phase noise performance. These outputs are designed to interface with standard LVPECL devices while driving transmission lines with far end termination only. Configured this way, the signal conforms to the LVPECL standard and the swing is very large at $1.6V_{P-P(DIFF)}$. The use of far end termination only in LVPECL systems presents trade-offs of power consumption, signal swing and signal integrity (overshoot and ringing).

When driving the sample clock inputs of an ADC with the LTC6950's PECLx outputs, it is typically not necessary to provide a full LVPECL logic compatible signal, due to the very fast rise and fall times provided by the PECLx outputs (typically less than 150ps). One approach to consider is using the PECLx outputs with *both* near and far end terminations of the transmission line. The signal is attenuated at the far end and does not meet the LVPECL signal level specifications, but most ADC sample clock inputs do not require a proper LVPECL level signal.

Figure 53 shows three PECLx output configurations that satisfy this requirement. One configuration has the standard LVPECL common mode voltage and the other is level shifted down to a 1.2V common mode voltage. Because the PECLx outputs are 50% duty cycle signals, AC-coupling the outputs is also a viable solution as shown in the last configuration.

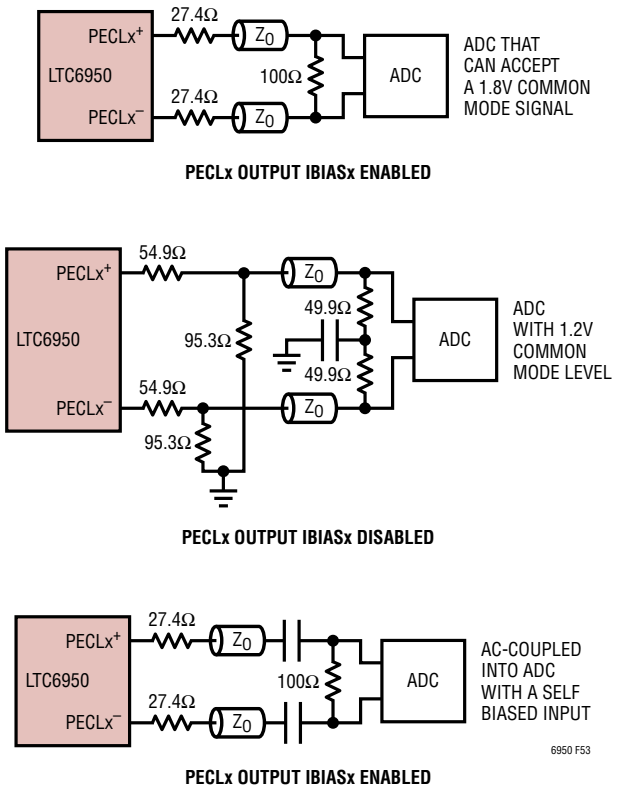
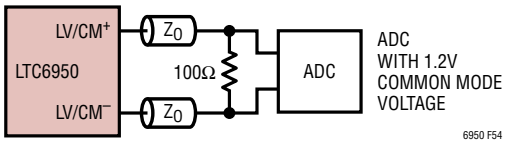


Figure 53. PECLx Output Connections to ADC Sample Clock Inputs (Z_0 = 50Ω)

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Note that the series, near end termination is 27.4Ω, not 50Ω. The LTC6950's PECLx output impedance is about 5Ω and must also be taken into account, but the biggest reason the near end termination resistor is less than 50Ω is because it adds noise to the signal. So, the near end termination shown here presents a trade off of transmission line impedance matching over production variations (signal integrity) against the added noise. If the far end termination is perfectly matched to the transmission line's characteristic impedance, then the near end termination is not needed at all. However, perfect matching is elusive and making provisions in the PCB layout for near end series termination, even if initially populated with zero ohm resistors, is highly recommended.

While the PECLx outputs provide the best ADC sample clock driver performance, the LVDS output can still provide very good performance. Compared to the PECLx output, the LVDS output has higher 1/f phase noise and a slightly higher phase noise floor. This slightly higher phase noise and jitter are still suitable for many ADC applications. When driving the sample clock input of an ADC with the LVDS output driver, it is best to use a single 100Ω resistor at the far end of the transmission line as shown in Figure 54.

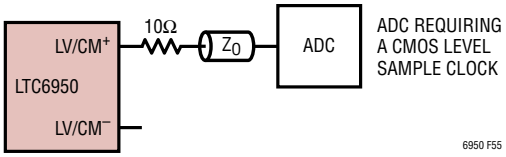


LVDS OUTPUT MODE, DC-COUPLED WITH A FAR END TERMINATION INTO THE ADC'S SAMPLE CLOCK INPUT

Figure 54. LVDS Output Connections to ADC Sample Clock Inputs (Z_O = 50Ω)

Using the CMOS output to drive the sample clock input of high performance, high frequency ADCs is not recommended. Using the same output pins in LVDS output mode is a better performing choice and certainly better for routing the signal any significant length. However, some ADCs require a CMOS level sample clock signal.

In these cases, the connection between the LTC6950 and the ADC should be as short as possible with partial source termination as shown in Figure 55.



CMOS OUTPUT MODE, DC-COUPLED INTO AN ADC REQUIRING A CMOS LEVEL SAMPLE CLOCK (TRANSMISSION LINE SHOULD BE NO LONGER THAN 10cm)

Figure 55. CMOS Output Connections to ADC Sample Clock Inputs (Z_O = 50Ω)

TYPICAL APPLICATIONS

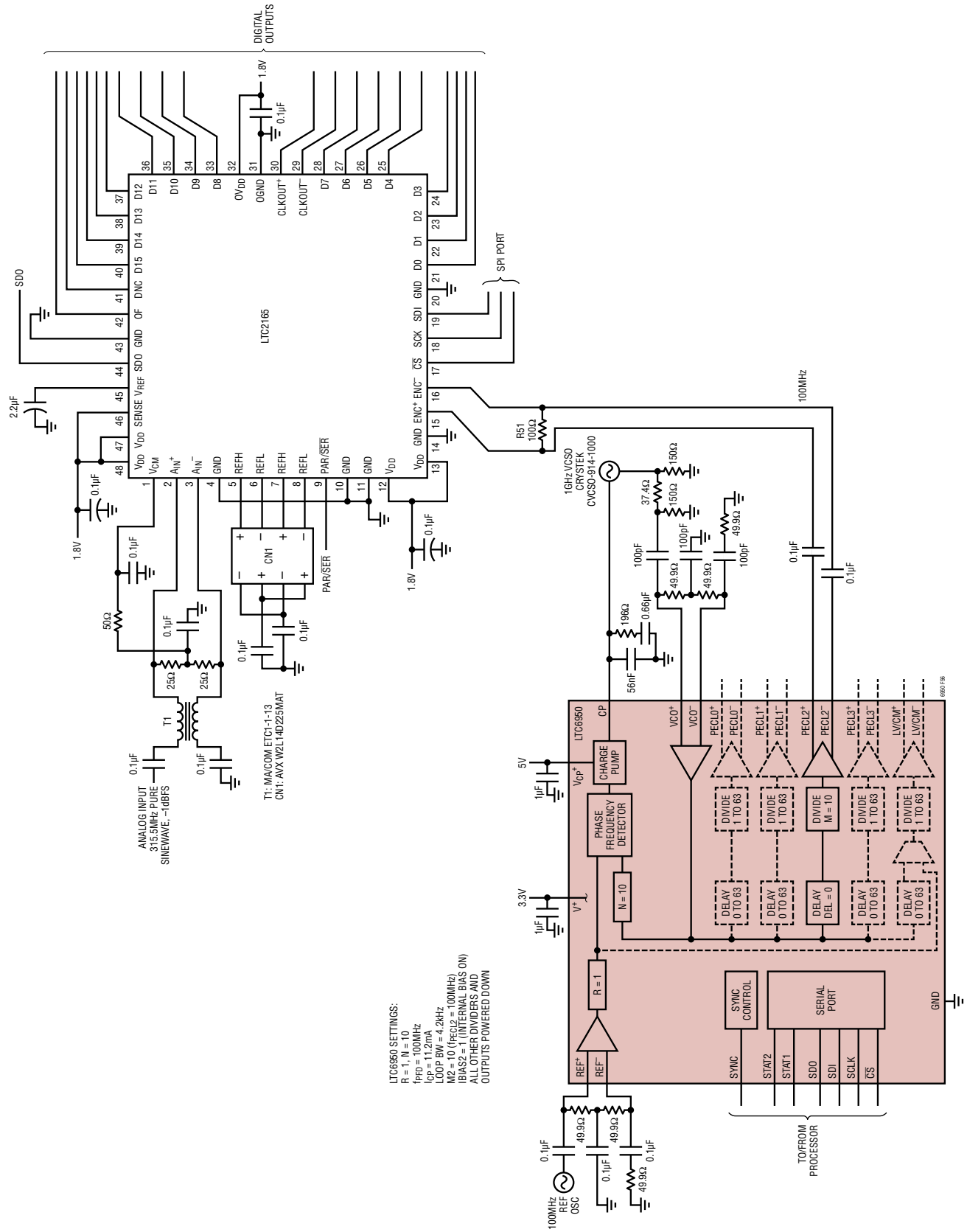


Figure 56. LTC6950 Driving the Encode Sample Clock Input of an LTC2165 100MSPS, 16-Bit ADC

TYPICAL APPLICATIONS

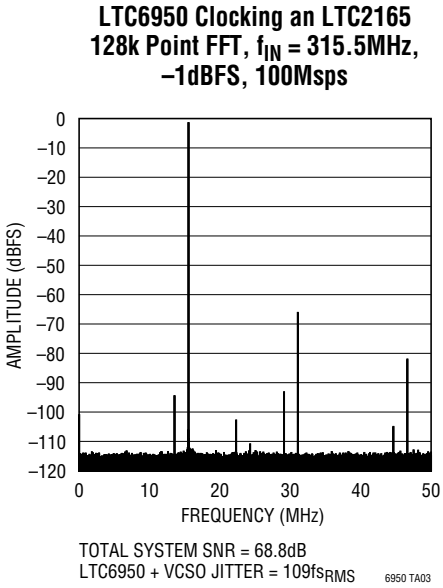
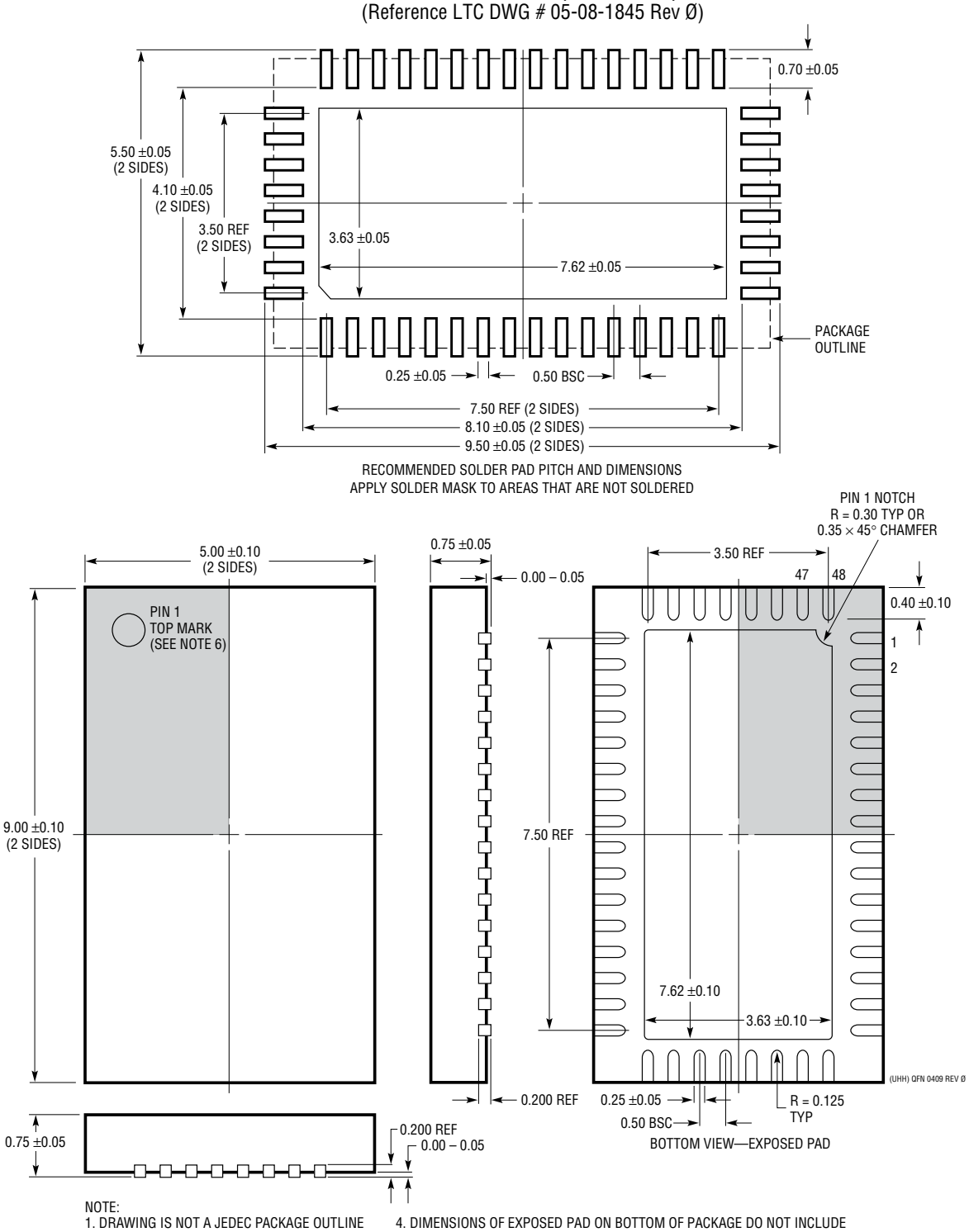


Figure 57. FFT from the LTC2165 at f_{IN} = 315.5MHz, Sample Clock Provided by the LTC6950 at 100MHz

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

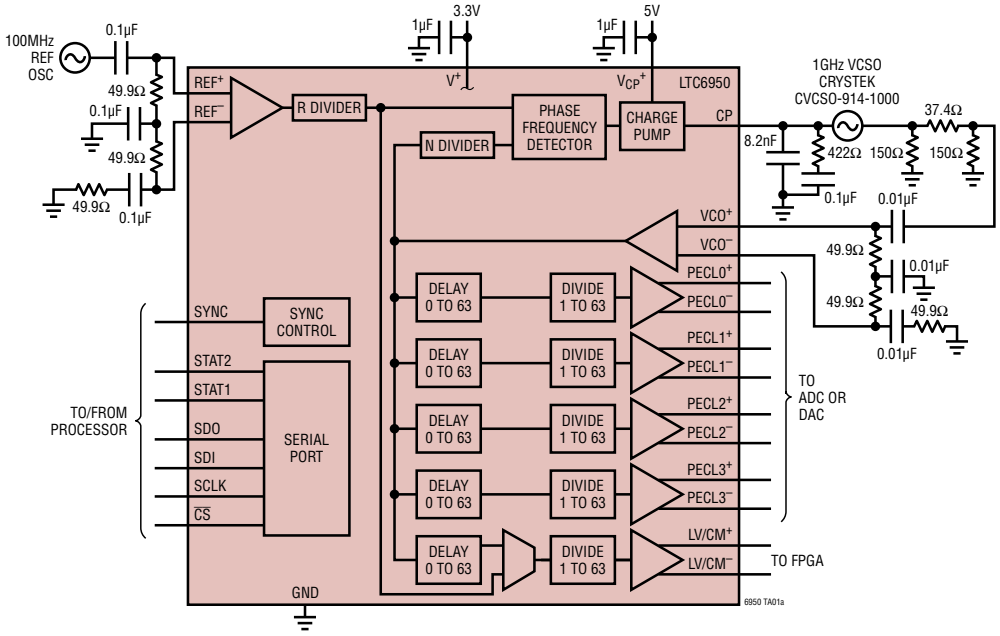
UHH Package
48-Lead Plastic QFN (5mm × 9mm)
(Reference LTC DWG # 05-08-1845 Rev Ø)



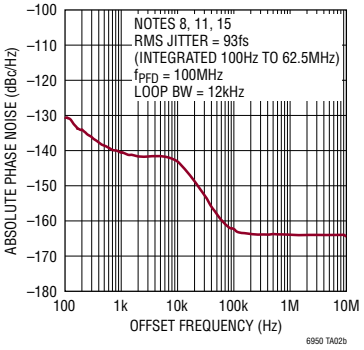
NOTE:
1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

TYPICAL APPLICATION



PECLx Closed-Loop Phase Noise, f_{VCSO} = 1GHz, Mx[5:0] = 8, f_{PECLx} = 125MHz



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
PLLs and Clock Buffer		
LTC6945	350MHz to 6GHz PLL Synthesizer	Integer-N PLL, –226dBc/Hz Normalized In-Band Phase Noise Floor
LTC6946-1/ LTC6946-2/ LTC6946-3	374MHz to 3.7GHz PLL + VCO/514MHz to 4.8GHz PLL + VCO/638MHz to 5.8GHz PLL + VCO	Integer-N PLL, –157dBc/Hz Wideband Output Phase Noise Floor, –226dBc/Hz, Normalized In-Band Phase Noise Floor, < –100dBc Spurious Output.
LTC6957	Low Phase Noise, Dual Output Buffer	Phase Noise Floor < –160dBc/Hz
ADCs		
LTC2208	16-Bit, 130Msps, 3.3V ADC, LVDS Outputs	1250mW, 77.7dB SNR, 100dB SFDR, 64-Lead QFN Package
LTC2157-14/ LTC2156-14/ LTC2155-14	14-Bit, 250Msps/210Msps/170Msps, 1.8V Dual ADC, DDR LVDS Output	650mW/616mW/567mW, 70dB SNR, 90dB SFDR, 64-Lead QFN Package
LTC2157-12/ LTC2156-12/ LTC2155-12	12-Bit, 250Msps/210Msps/170Msps, 1.8V Dual ADC, LVDS DDR Outputs	588mW/543mW/495mW, 68.5dB SNR, 90dB SFDR
Receiver Subsystems		
LTM®9002	14-Bit Dual Channel IF/Baseband Receiver Subsystem	Integrated High Speed ADC, Passive Filters and Fixed Gain Differential Amplifier
LTM9003	12-Bit Digital Pre-Distortion Receiver	Integrated 12-Bit ADC Down-Converter Mixer with 0.4GHz to 3.8GHz Input Frequency Range

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