LX3302A

Inductive Sensor Interface IC with Embedded MCU

Features

- Built-In Oscillator for Driving Primary Coil
- Two Independent Analog Channels with Demodulation
- 32-Bit Cortus APS1 RISC MCU
- Two 13-Bit ADCs
- One 12-Bit DAC
- One 16-Bit PWM
- Fault Detection and Protection
- Digital Calibration with Nonvolatile Configuration Storage (EEPROM)
- Protected Watchdog Timer
- Low-Temperature Drift
- Wide Range Supply Voltage (4.0V to 11.0V)
- -40°C to +150°C Operation
- Excellent Long-Term Stability
- SENT Output
- Asynchronous PSI5 Output
- AEC-Q100 Certification
- ISO26262 ASIL B Support

Applications

- Automotive Control
- ATE Equipment
- Industrial Process Control
- Smart Energy Saving Control

Description

The LX3302A is a highly integrated programmable data conversion IC designed for interfacing to, and managing of, inductive sensors. The device includes an integrated oscillator circuit for driving the primary coil of an inductive sensor, along with two independent analog conversion paths for conditioning, converting and processing of two analog signals from the secondary coils of the sensor. Each path includes an EMI filter, demodulator, anti-alias filter, programmable amplifier and a 13-bit Sigma-Delta Analog-to-Digital Converter.

Each analog signal path includes digital calibration capability, which allows the complete analog path (including the external sensors) to be calibrated during the system manufacturing process. The calibration information is written to internal EEPROM resulting in improved production yields and in-line system upgrades.

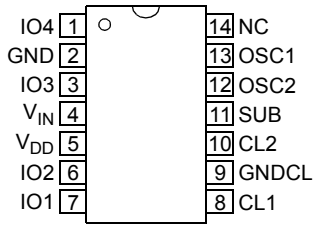
The LX3302A integrates a 32-bit RISC processor, which provides programmable digital filtering and signal processing functions.

System interfaces include a SENT or PSI5 serial port, programmable PWM output and a 12-bit Digital-to-Analog Converter analog buffed output.

The LX3302A is offered in a 14-lead TSSOP package. The device is specified over a temperature range of -40°C to +150°C, making it suitable for a wide range of commercial, industrial, medical and/or automotive sensor applications.

Package Types

14-Pin TSSOP
(Top View)



System Block Diagrams

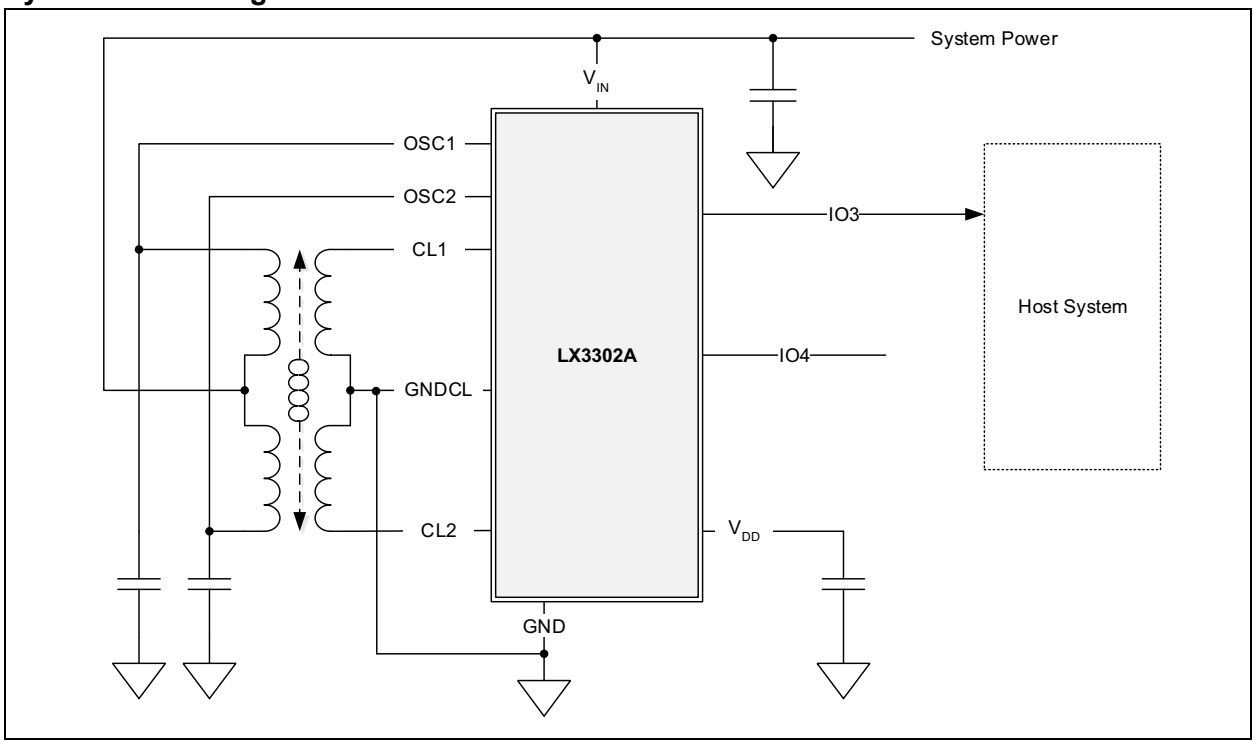


FIGURE 1: *System Block Diagram: LX3302A.*

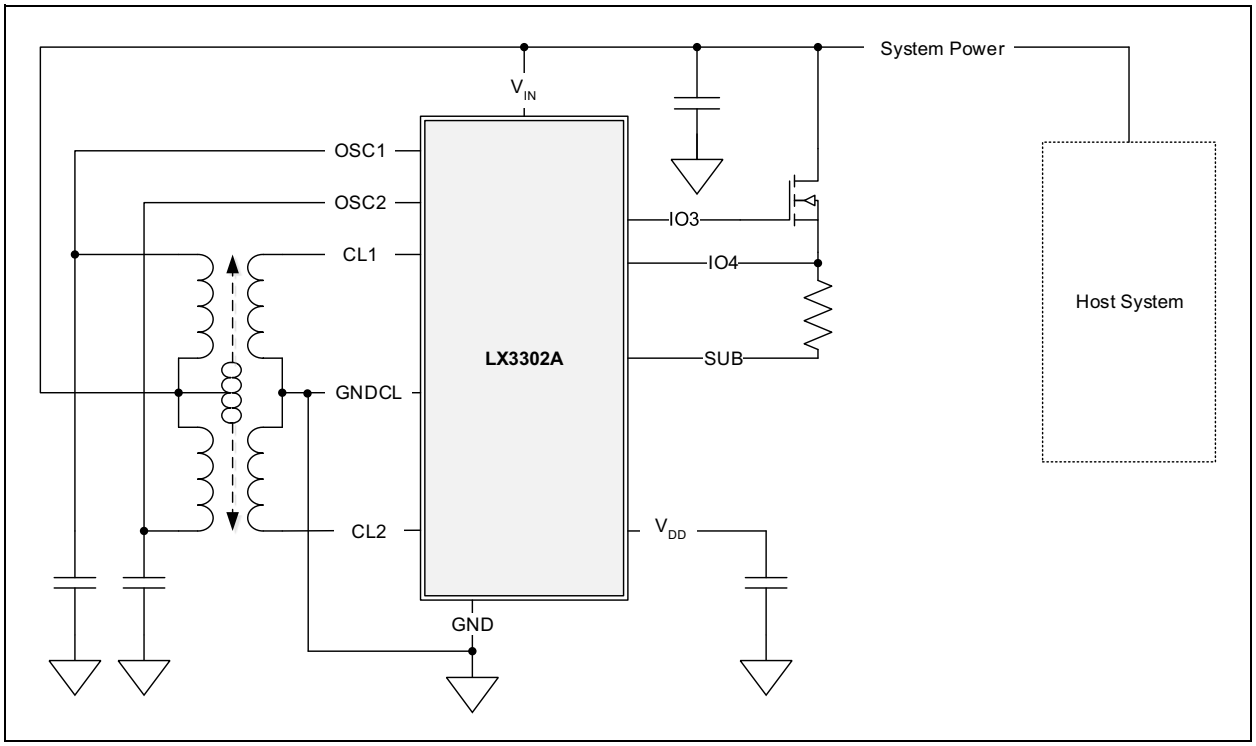


FIGURE 2: *System Block Diagram with PSI5 Output: LX3302A.*

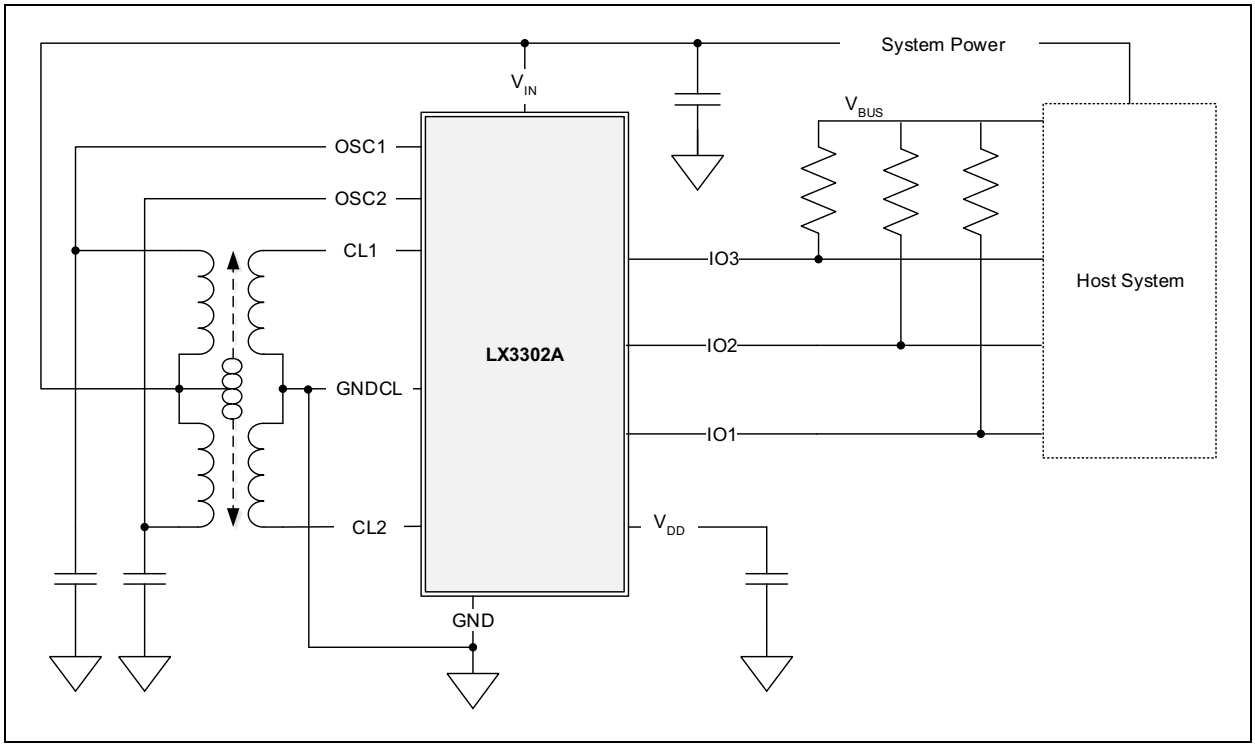


FIGURE 3: *System Block Diagram with Open-Drain Outputs: LX3302A.*

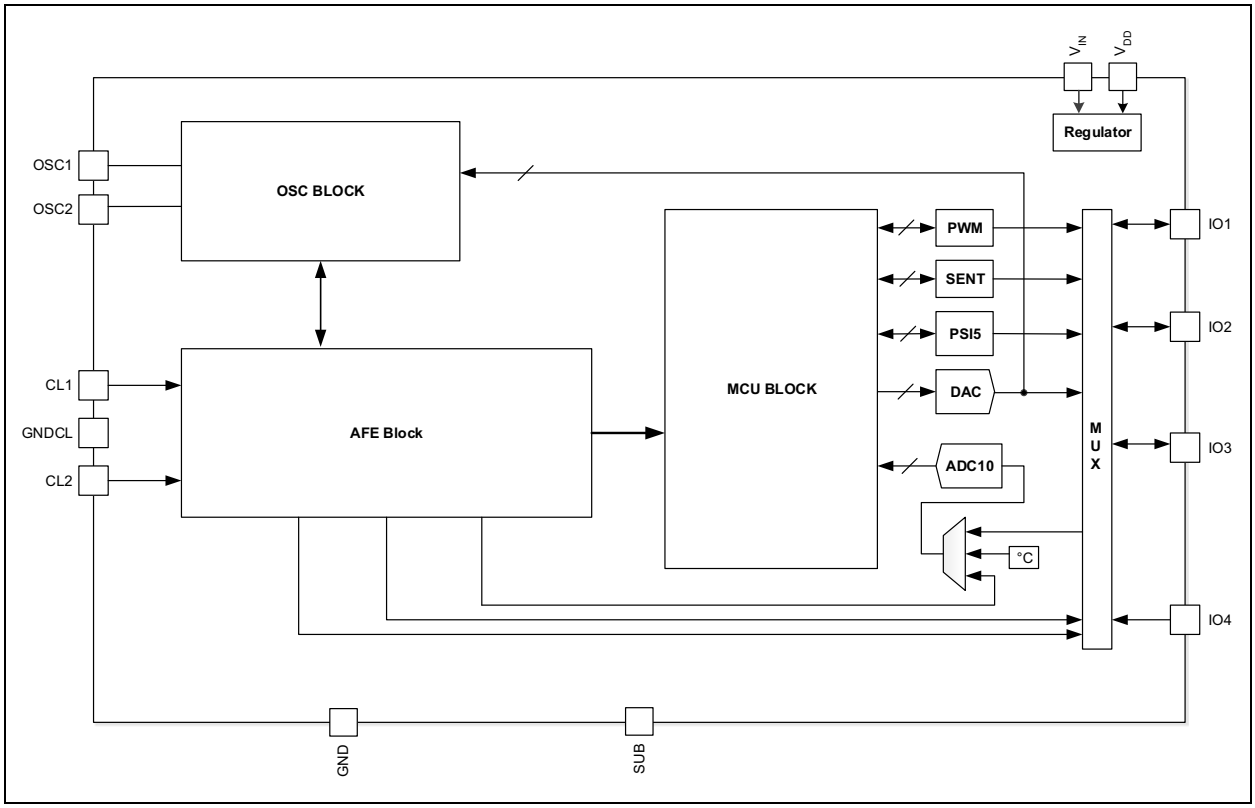


FIGURE 4: *LX3302A Block Diagram.*

Ordering Information

Ambient Temperature	Type	Package	Part Number	Packaging Type
-40°C to +150°C	RoHS2 Compliant, Pb-Free MSL1, AEC-Q100 Grade 0	14-Lead TSSOP	LX3302AQPW	Tube
			LX3302AQPW-TR	Tape and Reel

1.0 ELECTRICAL CHARACTERISTICS

1.1 Electrical Specifications

Absolute Maximum Ratings†

Supply Input Voltage Pin (V_{IN}) ..... -7V to 20V
Load Current on V_{DD} Pin ..... -1 mA to 15 mA
Voltage on OSC1, OSC2 and IO3 Pins ..... -0.3V to 20V
Voltage on IO3 Pin ..... -0.3V to 17V
Voltage on IO1 and IO2 Pins ..... -0.5V to 6.5V
Current on IO1 and IO2 Pins ..... -10 mA to 10 mA
Voltage on IO4, V_{DD}, CL1 and CL2 Pins ..... -0.5V to 3.6V
Operating Humidity (non-condensing) ..... 0% to 95%
Operating Temperature ..... -40°C to +150°C
Storage Temperature ..... -65°C to +150°C
Lead Temperature (soldering, 10 seconds) ..... +300°C
Package Peak Temperature for Solder Reflow (40 seconds exposure) ..... +260°C
ESD Rating – All Pins – HBM (AEC-Q100-002D) ..... ±2 kV
ESD Rating – All Pins – CDM (AEC-Q100-011) ..... ±1.5 kV

† **Notice**: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to above maximum rating conditions for extended periods may affect device reliability. All voltages are with respect to GND. All voltages on ESD are with respect to SUB.

Recommended Operating Range

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Supply Voltage	V_{IN}	4.0	5.0	6.0	V	For normal operation
V_{IN} EEPROM Program High	VIN_PH	—	—	18	V	
Supply Current	I_{IN}	—	—	15	mA	For normal operation, excluding oscillator tail current
Output Current	I_IO3_AN0	-15	—	-8	mA	IO3 = Analog mode, 0V
	I_IO3_AN5	6	—	15		IO3 = Analog mode, 0V
	I_IO3_OD	—	—	28		IO3 = OD mode, 0V
Internal Clock Frequency	F_{OSC}	8.0	8.2	8.4	MHz	
Operating Temperature	T_{OP}	-40	—	+150	°C	

Electrical Characteristics

Electrical Specifications: Unless otherwise indicated, the following specifications apply over the operating temperature range of -40°C ≤ T_A ≤ +150°C and the following test conditions: V_{IN} = 5V, f = 8.2 MHz, I_{DD} = 1 mA, I/O = 0 mA. Typical values are at +25°C.

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Power						
V_{IN} Input Voltage	V_{IN1}	4.0	5.0	11	V	For normal operation, IO3 = PSI5
	V_{IN2}	4.0	5.0	6	V	For normal operation, IO1,2,3 = PWM, analog
V_{IN} Supply Current	I_{IN}	—	12.3	15	mA	For normal operation, excluding oscillator tail current, I_{DD} = 0 mA, IO1,2,3,4 = 0 mA, f = 8.2 MHz
V_{IN} Threshold Disabling of IO1 and IO2 Push-Pull Buffers	VIN_DIS_IO	6	6.4	7	V	
V_{IN} Hysteresis of VIN_DIS_IO	VIN_DIS_IOhys	—	0.25	—	V	
V_{IN} UVLO High Threshold	VIN_UVLO_HI	3.7	3.8	3.95	V	V_{IN} POR error enabled
V_{IN} UVLO Hysteresis	VIN_HYST	—	0.05	—	V	
V_{IN} EEMode (EEPROM Programming)						
Programming Mode Threshold	VIN_TH_EE	11.5	12	12.5	V	For EEPROM mode
Program Low	VIN_PL	12.6	13	13.6	V	For EEPROM Programming mode
Program Idle	VIN_PI	14.9	15.3	15.8	V	For EEPROM Programming mode
Program High	VIN_PH	17.1	17.5	18.0	V	For EEPROM Programming mode
Duration Time	td	20	—	110	µs	Duration time for each voltage state
Rise Time	tr	—	—	2.5	ms	To enter EEPROM mode, V_{IN} = 15.3V, 10-90%
Digital EEMode (EEPROM Programming (IO1, IO2, IO4))						
Programming Mode Threshold	VEN_DEE	2.5	—	—	V	For Digital EEMode with IO4
CLK High Threshold	V_EECLK_HI	2.5	—	—	V	IO1 input for Digital EEMode
CLK Low Threshold	V_EECLK_LO	—	—	0.8	V	IO1 input for Digital EEMode
CLK Rise/Fall Time	tr_CLK	—	1	—	µs	
CLK Duty	Duty_CLK	—	50	—	%	
Data High Threshold	V_EEDATA_HI	—	2.5	—	V	IO2 input for Digital EEMode
Data Low Threshold	V_EEDATA_LO	—	—	0.8	V	IO2 input for Digital EEMode
Data Rise/Fall Time	Tr_DATA	—	1	—	µs	
Duration Time for CLK	Td_CLK	20	—	110	µs	Duration time for each state
VEN_DEE Rise Time	Tr_CLK	—	10	—	µs	To enter Digital EEMode with IO4
V_{DD} Reference Voltage						
Output Voltage	V_{DD}	3.24	3.3	3.36	V	I_{DD} = 5 mA, after trimming
Output Current	I_{DD}	—	—	5	mA	Additional current sourced to external load(s)
V_{DD} POR Threshold	VDD_POR	—	2.9	—	V	Monitor V_{DD}, rising edge
V_{DD} UVLO Hysteresis	VDD_Hyst	—	0.20	—	V	V_{DD} UVLO hysteresis
Short Current V_{DD} to GND	IDD_SC_5V	—	120	—	mA	Shorted to GND, V_{IN} = 5V, +25°C
V_{DD} Over Ripple Threshold	VDD_RIPPLE	—	300	—	mVpp	Noise frequency > 10 MHz

Note 1: For 3 µs nominal clock tick including clock accuracy. For higher clock tick, times need to be increased proportionally.

Electrical Characteristics (Continued)

Electrical Specifications: Unless otherwise indicated, the following specifications apply over the operating temperature range of -40°C ≤ T_A ≤ +150°C and the following test conditions: V_{IN} = 5V, f = 8.2 MHz, I_{DD} = 1 mA, I/O = 0 mA. Typical values are at +25°C.

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Oscillator OSC1 and OSC2						
Center Tap Voltage	V_{TAP}	—	5	—	V	V_{IN} = 5V
Center Tap Output Voltage Detection Threshold	VTAP_OPEN	—	3.3	—	V	V_{IN} = 5V
IO1, IO2, IO3 Voltage from OSC1, OSC2 Pins	VOSC_OV	—	0	—	V	V_{IN} = 0V and OSC pins driven by external signal
OSC AC Swing Peak Overvoltage Detection	VOSC_OV	10	—	—	Vpp	AC coupled
OSC AC Swing Peak Undervoltage Detection	VOSC_UV	—	—	3	Vpp	AC coupled
Total Tank DC Tail Current	ITK	0	—	10	mA	V_{TAP} = 5V
Amplitude of OSC1, OSC2	V_{OSC}	3.1	—	9.9	Vpp	V_{TAP} = 5V
Oscillation Frequency Range	FOSC_R	1	—	6	MHz	V_{TAP} = 5V
Frequency Variation	FOSCTOL	-5	—	5	%	V_{TAP} = 5V
Oscillator Inductance	LOSC	3	6	12	µH	V_{TAP} = 5V
Tank Circuit Quality Factor	QOSC	10	22	30	—	V_{TAP} = 5V (|X|/R)
Harmonics	HOSC	—	—	2	%	V_{TAP} = 5V, GDNT
Resistance Between OSC1 and OSC2	ROSC1&2_HI	500	1000	—	kΩ	OSC1 = 1 Vpp, OSC2 = GND
Resistance Between OSC1 and GND	ROSC1_GND	500	2000	—	kΩ	V_{IN} = 0V, OSC1 = 5V, measure current from OSC1 to 5V
Resistance Between OSC2 and GND	ROSC2_GND	500	2000	—	kΩ	V_{IN} = 0V, OSC1 = 5V, measure current from OSC1 to 5V
Resistance Between OSC1 and V_{DD}	ROSC1_VDD	500	1000	—	kΩ	
Resistance Between OSC2 and V_{DD}	ROSC2_VDD	500	1000	—	kΩ	
Oscillator Tail Current Digital Control OSCDAC						
OSCDAC Resolution	—	—	11	—	bits	
OSCDAC Range	—	0	—	2047	bits	
OSCDAC Allowable Max. Tail Current	Imax	—	—	15	mA	Over process and temperature range
Zero Code Error Current	Izero	—	25	—	µA	
Step Current	Istep	4.88	6.9	8.88	µA	IOSCDAC/VALOSCDAC
ADC1 and ADC2						
Resolution	ADC_Res	—	13	—	bits	
Integral Nonlinearity	ADC_INL	-1	—	1	LSB	GDNT
SINC or SINC+FIR Filter 1 and 2						
Crosstalk Rejection	FLTR_CTR	—	—	-44	dB	
PSRR	FLTR_PSRR	—	—	-50	dB	GDNT
Digital-to-Analog Converter (DAC)						
DAC Resolution	DACR	—	12	—	bits	
Output Load (RL)						
Output Load Range	RL	0.9	10	100	kΩ	
Maximum Allowable Output Voltage	V_{OHmax}	—	85	—	%VIN	RL = 0.9 ~ 3 kΩ

Note 1: For 3 µs nominal clock tick including clock accuracy. For higher clock tick, times need to be increased proportionally.

Electrical Characteristics (Continued)

Electrical Specifications: Unless otherwise indicated, the following specifications apply over the operating temperature range of -40°C ≤ T_A ≤ +150°C and the following test conditions: V_{IN} = 5V, f = 8.2 MHz, I_{DD} = 1 mA, I/O = 0 mA. Typical values are at +25°C.

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
IO1, IO2 Analog Outputs						
Low-Level Output Voltage	V_{OLA}	0	—	0.3	V	Pull-up load ≥ 10 kΩ to V_{IN}
High-Level Output Voltage	V_{OHA}	V_{IN} – 0.3	—	VIN	V	Pull-down load ≥ 10 kΩ to GND, Gain = V_{IN}/V_{DD}
Output Short-Circuit Current	ISHORT_12A	9	—	20	mA	Short to 0 or short to 5V
IO1, IO2 Digital Outputs						
Low-Level Output Voltage	V_{OLD}	—	—	3	%VIN	Pull-up load ≥ 10 kΩ to V_{IN}
High-Level Output Voltage	V_{OHD}	97	—	—	%VIN	Pull-down load ≥ 10 kΩ to GND
Output Short-Circuit Current	ISHORT_12D	9	—	20	mA	Short to 0 or short to 5V
IO1, IO2 Digital Inputs (Address for V_{IN} EEMode)						
High-Level Input Voltage	V_{IHD}	2.5	—	—	V	
Low-Level Input Voltage	V_{ILD}	—	—	0.8	V	
Input Impedance	RIN_12	200	—	—	kΩ	
Input Capacitance	CIN_12	—	—	5	pF	
IO3 Analog Output						
Output Load	RL_3	0.9	10	100	kΩ	
Output Low	VLO_IO3	—	40	—	mV	Pull-up load ≥ 10 kΩ to V_{IN}
Output Short-Circuit Current	SHORT1_3A	—	12	17	mA	Short to GND or short to V_{IN}
	SHORT2_3A	—	—	45	mA	Short to 14V
V_{IN} Ratiometric Error	RaErr_3A	-0.5	0	0.5	%VIN	
IO3 Digital Output						
High-Level Output Voltage	VOH_3	98	—	—	%VIN	Pull-up load ≥ 10 kΩ to V_{IN}
Low-Level Output Voltage	VOL_3	—	—	2	%VIN	Pull-down load ≥ 10 kΩ to GND
Output Short-Circuit Current	ISHORT_3A	25	—	35	mA	Short to 0 or short to 5V
IO3 Input						
High-Level Input Voltage	VIH_3IN	2.5	—	—	V	Pull-up load ≥ 10 kΩ to V_{IN}
Low-Level Input Voltage	VIL_3IN	—	—	0.8	V	Pull-down load ≥ 10 kΩ to GND
Input Impedance	RIN_4	450	—	—	kΩ	
Input Capacitance	CIN_3	—	—	5	pF	
IO4 Digital Input						
High-Level Input Voltage	VIH_4	2.5	—	V_{DD}	V	Pull-up load ≥ 10 kΩ to V_{IN}
Low-Level Input Voltage	VIL_4	0	—	0.8	V	Pull-down load ≥ 10 kΩ to GND
Input Impedance	RIN_4	450	—	—	kΩ	
Input Capacitance	CIN_4	—	—	5	pF	
IO3 Fault Output						
Ground Off Output High Level	VOH_IO3GF1	99	100	—	%VIN	Broken GND, 100 kΩ ≥ RL_IO3 to V_{IN}
V_{IN} Open Output Low Level	VOL_IO3_IN	—	0	1	%VIN	Broken V_{IN}, RL_IO3 = 10 kΩ to GND
V_{IN} Open Output High Level	VOH_IO3_VIN1	97	99	—	%VIN	Broken V_{IN}, RL_IO3 ≥ 3 kΩ to V_{IN}
	VOH_IO3_VIN2	97	99	—	%VIN	Broken V_{IN} and pull-up load to V_{IN}, 1 kΩ ≤ RL ≤ 3 kΩ, with 3 kΩ between V_{IN} and GND
Fault Output Low Level	VIO3_FL10K	—	—	3	%VIN	RL_IO3 = 10 kΩ to V_{IN}
Main Oscillator						
Main Oscillator Frequency	F_{CLK}	—	8.2	—	MHz	
Tolerance	FCLK_TOL	-1.5	—	1.5	%	T_A = +25°C

Note 1: For 3 µs nominal clock tick including clock accuracy. For higher clock tick, times need to be increased proportionally.

Electrical Characteristics (Continued)

Electrical Specifications: Unless otherwise indicated, the following specifications apply over the operating temperature range of -40°C ≤ T_A ≤ +150°C and the following test conditions: V_{IN} = 5V, f = 8.2 MHz, I_{DD} = 1 mA, I/O = 0 mA. Typical values are at +25°C.

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Processor Resources						
Data Bus	PR_DBUS	—	32	—	bits	
Instruction Size	PR_INSS	—	32	—	bits	
EEPROM Size	PR_EEPRMS	—	32	—	words	16-bit words
Number of EEPROM Erase/Write Cycles	PR_NEEWC1	100	—	—	cycles	T_A = +25°C, GDNT
	PR_NEEWC2	100	—	—	cycles	T_A = +125°C, GDNT
Max. Temperature for Erase/Write EEPROM	PR_TmaxEW	—	+125	—	°C	
EEPROM Data Retention	PR_DataR1	10	—	—	Years	T_A = +85°C
	PR_DataR2	1	—	—	Years	T_A = +125°C
	PR_DataR3	0.3	—	—	Years	T_A = +150°C
PWM Controller						
Clock Prescale Bit	PWM_CPSB	—	2	—	bits	Divider = 1, 2, 4, 8
PWM Clock	PWM_CLK	—	8.2	—	MHz	
PWM Period	PWM_PER	—	16	—	bits	
PWM Duty	PWM_Duty	—	16	—	bits	
PWM Jitter	PWM_Jitter	—	0.2	—	%D	No clamped output
Single-Edge Nibble Transmission (SENT) Interface and Driver						
Low State Voltage	SENTVOL	—	—	0.5	V	IL = 5 mA
High State Voltage	SENTVOH	4.1	—	—	V	IL = 5 mA, V_{IN} = 5V
Average Current Consumption	SENTIS	—	—	15	mA	Average current consumption from receiver supply over one message
Supply Current Ripple	SENTISCR	—	—	9	mApp	Peak-to-peak variation
Square Wave Rising Time	SENTTR	—	0.3	—	µs	From 1.1V to 3.8V. Load = 5 mA, C_{OUT} = 1 nF, SENTCLK = 3 µs **(Note 1)**
Square Wave Falling Time	SENTTF	—	0.3	—	µs	From 3.8V to 1.1V. Load = 5 mA, C_{OUT} = 1 nF, SENTCLK = 3 µs **(Note 1)**
Edge-to-Edge Jitter with Static Environment for Any Pulse Period	SENTJIT	—	—	0.1	µs	**Note 1**
Nominal Clock Period (Tick)	SENTCLK	3.0	—	24.0	µs	By two program bits
Clock Accuracy	SENTCLKAC	-10	—	+10	%	
Clock Jitter and Drift Error	SENTCLKJIT	—	—	0.05	µs	**Note 1**
PSI5 (Asynchronous Mode Only)						
Absolute Bit Time Range	ATBitR1	7.6	8.0	8.4	µs	125 kbps
	ATBitR2	5.0	5.3	5.6	µs	189 kbps
Absolute Gap Time	ATGAP1	8.4	—	—	µs	125 kbps, $T_{GAP} > T_{BIT}$
	ATGAP2	5.6	—	—	µs	189 kbps, $T_{GAP} > T_{BIT}$
Current Regulation Ref.	V_{REF}	390	412.5	435	mV	For PSI5 operation
Fall/Rise Time Driver Voltage Slope	PSI5_Tr_Tf	0.33	—	1	µs	20% to 80%, RL = 12.5Ω, CL = 100 nF, L = 0 µH
Total Overshoot Time per Cycle	PSI5_TOTPC	—	—	0.52	µs	Voltage over 10%, RL = 2.5Ω, CL = 47 nF, L = 8.7 µH
Total Undershoot Time per Cycle	PSI5_TUTPC	—	—	0.52	µs	Voltage under 10%, RL = 2.5Ω, CL = 47 nF, L = 8.7 µH

Note 1: For 3 µs nominal clock tick including clock accuracy. For higher clock tick, times need to be increased proportionally.

Electrical Characteristics (Continued)

Electrical Specifications: Unless otherwise indicated, the following specifications apply over the operating temperature range of -40°C ≤ T_A ≤ +150°C and the following test conditions: V_{IN} = 5V, f = 8.2 MHz, I_{DD} = 1 mA, I/O = 0 mA. Typical values are at +25°C.

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
PSI5 (Asynchronous Mode Only) (Continued)						
Overshoot Voltage	PSI5_OV	—	—	10	%	RL = 2.5Ω, CL = 47 nF, L = 8.7 µH
Undershoot Voltage	PSI5_UV	-10	—	—	%	RL = 2.5Ω, CL = 47 nF, L = 8.7 µH
Embedded Temperature Sensor						
Temperature Sensing Range	Tsnsrng	-40	—	+175	°C	
Temperature Sensing Accuracy	Tsnsacc	—	±12	—	°C	T_A = +25°C
Sensor Output at +25°C	Tsnsout25	—	500	—	LSB	T_A = +25°C, GBNT
Temperature Coefficient	TCsns	—	1.681	—	LSB/°C	-40°C ≤ T_A ≤ +175°C

Note 1: For 3 µs nominal clock tick including clock accuracy. For higher clock tick, times need to be increased proportionally.

Temperature Specifications[(1)]

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Thermal Resistance, Junction to Ambient	θ_{JA}	—	117	—	°C/W	
Thermal Resistance, Junction to Case	θ_{JC}	—	22	—	°C/W	

Note 1: The θ_{JA} numbers assume no forced airflow. Junction temperature is calculated using the formula: $T_J = T_A + (P_D \times \theta_{JA})$. In particular, θ_{JA} is a function of the PCB construction. The stated number above is for a four-layer board in accordance with JESD-51-7 (JEDEC) with thermal vias on V_{IN}, IO3 and GND pins.

2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1.

TABLE 2-1: PIN DESCRIPTIONS

14-Lead TSSOP	Symbol	Description
1	IO4	I/O Pin 4. External FET current limits sensing. Pulled high to overwrite EEWR when one of the EELOCK bits is set to '1'. Pulled high to enable EEPROM programming via the IO1, IO2 or IO3 pins (hereafter Digital EEMode).
2	GND	Ground pin.
3	IO3	I/O Pin 3. Can be programmed to provide DAC output, PWM output, reverse PWM output, SENT output, PSI5 external FET drive and µP digital output. Alternatively, IO3 can be configured as an address pin for V_{IN} EEMode and Digital EEMode.
4	V_{IN}	Power Supply and Internal EEPROM Programming Pin. DC input power is applied to this pin for normal operation. Also used for EEPROM programming (refer to application information). Bypass this pin to GND pin with a low-ESR capacitor, not lower than 100 nF.
5	V_{DD}	Regulator Output Pin. This is the output of the internal voltage regulator providing power to the analog and digital blocks. Bypass this pin to the SUB pin with a low-ESR capacitor, not lower than 100 nF. A maximum load of 5 mA is allowed.
6	IO2	I/O Pin 2. When configured as an output: PGA1 or PGA2 analog output, digital push-pull output (PWM/PWMB/SENT/µP GPO) or open-drain output (PWM/PWMB/µP GPO). Configured as an input: for V_{IN} EEMode as address pin or for Digital EEMode as data input.
7	IO1	I/O Pin 1. When configured as an output: PGA1 or PGA2 analog output, digital push-pull output (PWM/PWMB/SENT/µP GPO) or open-drain output (PWM/PWMB/µP GPO). Configured as an input: for V_{IN} EEMode as an address pin or for Digital EEMode as a CLK input.
8	CL1	Sensor Signal from Secondary Coil 1 of Inductive Sensor Pin.
9	GNDCL	Reference Ground for CL1 and CL2 Pin. Connect directly to GND on board via a star connection.
10	CL2	Sensor Signal from Secondary Coil 2 of Inductive Sensor Pin.
11	SUB	Substrate Pin. It should not be connected to GND. For normal applications, V_{DD} bypass capacitor is connected.
12	OSC2	LC Oscillator Pin. Connects to the second side of the primary inductor coil. An external capacitor is connected between this pin and GND as part of the LC oscillator tank circuit. External capacitor should be C0G or NP0, or equivalent type and low-ESR at 1 MHz to 6 MHz, rated voltage 50V or higher.
13	OSC1	LC Oscillator Pin. Connects to the first side of the primary inductor coil. An external capacitor is connected between this pin and GND as part of the LC oscillator tank circuit. External capacitor should be C0G or NP0, or equivalent type and low-ESR at 1 MHz to 6 MHz, rated voltage 50V or higher.
14	NC	Not Connected.

NOTES:

3.0 CONFIGURATION EEPROM

The LX3302A integrates a 32 words by 16 bits (512-bit) user-programmable EEPROM for storing calibration and configuration parameters. The calibration parameters enable the production sensor assembly to be customer-factory calibrated, assuring consistent unit to unit performance. Table 3-2 shows the LX3302A EEPROM Configuration map and Table 3-1 itemizes the LX3302A Configuration EEPROM contents.

TABLE 3-1: LX3302A CONFIGURATION EEPROM(1)

Name	Description	Size (bits)	Words and Bits (MSB:LSB)	Sign	Min. Value	Max. Value	Factory Default
ID	Part ID	18	W0[15:0]W1[15:14]	—	—	—	Serial #
Reserved	Reserved	3	W1[13:11]	—	—	—	0
GADJ	PGA Gain	4	W1[10:7]	No	0000 b	1111 b	0
IOSC	Oscillator Tail Current	2	W1[6:5]	No	0	3	0
Reserved	Reserved	1	W1[4]	—	—	—	0
Reserved	Reserved	1	W1[3]	—	—	—	0
REFRESH	ADC Clock and PWM Clock	3	W1[2:0]	No	011 b	110 b	011 b
FILTER	Select Digital Filter	1	W2[15]	No	0	1	0
CLSEL	Select CL1 and CL2	1	W2[14]	No	0	1	0
GMTCH	Channel Gain Mismatch Correction	7	W2[13:7]	Yes	-12.1%	12.1%	0
DCOS	Cosine Channel Dynamic Offset Correction	10	W2[6:0]W3[15:13]	Yes	-511	511	0
SCOS	Cosine Channel Offset Correction	10	W3[12:3]	Yes	-511	511	0
DSIN	Sine Channel Dynamic Offset Correction	10	W3[2:0]W4[15:9]	Yes	-511	511	0
SSIN	Sine Channel Offset Correction	10	W4[8:0]W5[15]	Yes	-511	511	0
OSCOMP	Max. Oscillator Swing	10	W5[14:5]	No	0	1023	1023
Reserved	—	5	W5[4:0]	—	—	—	00000 b
ORIGIN	Origin	12	W6[15:4]	No	0	4095	0
HCLMP	High Plateau Value	12	W6[3:0]W7[15:8]	No	0	4095	4095
LCLMP	Low Plateau Value	12	W7[7:0]W8[15:2]	No	0	4095	0
S0	Initial Slope	12	W8[11:0]	No	0	4095	511
X1	Linearization Point 1 X-Coordinate	12	W9[15:4]	No	0	4095	511
X2	Linearization Point 2 X-Coordinate	12	W9[3:0]W10[15:8]	No	0	4095	1023
X3	Linearization Point 3 X-Coordinate	12	W10[7:0]W11[15:12]	No	0	4095	1535
X4	Linearization Point 4 X-Coordinate	12	W11[11:0]	No	0	4095	2047
X5	Linearization Point 5 X-Coordinate	12	W12[15:4]	No	0	4095	2559

Note 1: ‘xxx b’ stands for ‘xxx’ binary numbers.

TABLE 3-1: LX3302A CONFIGURATION EEPROM[(1)] (CONTINUED)

Name	Description	Size (bits)	Words and Bits (MSB:LSB)	Sign	Min. Value	Max. Value	Factory Default
X6	Linearization Point 6 X-Coordinate	12	W12[3:0]W13[15:8]	No	0	4095	3071
X7	Linearization Point 7 X-Coordinate	12	W13[7:0]W14[15:12]	No	0	4095	3583
Y1	Linearization Point 1 Y-Coordinate	12	W14[11:0]	No	0	4095	511
Y2	Linearization Point 2 Y-Coordinate	12	W15[15:4]	No	0	4095	1023
Y3	Linearization Point 3 Y-Coordinate	12	W15[3:0]W16[15:8]	No	0	4095	1535
Y4	Linearization Point 4 Y-Coordinate	12	W16[7:0]W17[15:12]	No	0	4095	2047
Y5	Linearization Point 5 Y-Coordinate	12	W17[11:0]	No	0	4095	2559
Y6	Linearization Point 6 Y-Coordinate	12	W18[15:4]	No	0	4095	3071
Y7	Linearization Point 7 Y-Coordinate	12	W18[3:0]W19[15:8]	No	0	4095	3583
S7	Final Slope	12	W19[7:0]W20[15:12]	No	0	4095	511
TD	Threshold Detect	13	W20[11:0]W21[15]	No	0	8191	8191
TDPOL	TD Output Logic Level	1	W21[14]	No	0	1	0
DIAGMK	Diagnostic Error Mask	12	W21[13:2]	No	0	0xFFF	0xFFF
SENTCLK	SENT Clock Tick	2	W21[1:0]	No	00 b	11 b	00 b
SENTFCM	SENT Protocol Select	4	W22[15:12]	No	0000 b	1100 b	0000 b
SENTREFR	SENT Constant Clock Ticks Sync. with Pause Pulse	11	W22[11:1]	No	0	0x7FF	0
SENTPPE	SENT Pause Pulse	1	W22[0]	No	0	1	0
SENTSCM	SENT Serial Message	2	W23[15:14]	No	00 b	11 b	00 b
MSGMUX	Message MUX	1	W23[13]	No	0	1	0
DIAGPOL	Diagnostic Level	1	W23[12]	No	0	1	0
PSI5FR	PSI5 Frame	3	W23[11:9]	No	000 b	100 b	000 b
PSI5STS	PSI5 Status	2	W23[8:7]	No	00 b	10 b	00 b
PSI5MSG	PSI5 Serial Message	2	W23[6:5]	No	00 b	11 b	00 b
PSI5ERRCS	PSI5 Error Check Selection	1	W23[4]	No	0	1	0
PSI5DRB	PSI5 Data Region B	4	W23[3:0]	No	0000 b	1100 b	0000 b
PSI5DRA	PSI5 Data Region A	4	W24[15:12]	No	0000 b	1110 b	0000 b
PSI5REFR	PSI5 Refresh Rate	11	W24[11:1]	No	0	0x7FF	0
PSI5BR	PSI5 Bit Time	1	W24[0]	No	0	1	0
IOSEL	Output Selection	15	W25[15:1]	No	0	FBBD	E000
OSCDFB	Oscillator DAC Control	1	W25[0]	No	0	1	0
OSCDAC	Oscillator DAC Data	12	W26[15:4]	No	0	0xFFF	0
TD MASK	TD Input Source Select	2	W26[3:2]	No	0	3	0
EELOCK	EEPROM Lock	2	W26[1:0]	No	0	3	0

Note 1: ‘xxx b’ stands for ‘xxx’ binary numbers.

TABLE 3-1: LX3302A CONFIGURATION EEPROM(1) (CONTINUED)

Name	Description	Size (bits)	Words and Bits (MSB:LSB)	Sign	Min. Value	Max. Value	Factory Default
MESSAGE	Message	16	W27[15:0]	No	0	0xFFF	0
MSGID	Message ID	8	W28[15:8]	No	0	0xFF	0
TDHYST	Threshold Detect Hysteresis	8	W28[7:0]	No	0	255	255
ADC10IN	ADC10_IN	1	W29[15]	No	0	1	1
CLCHK	Range Check Ignore	1	W29[14]	No	0	1	0
WDSCALE	Watchdog Timer Scale	3	W29[13:11]	No	0	7	001 b
Reserved	—	43	W29[10:0]W30[15:0] W31[15:0]	—	—	—	—

Note 1: ‘xxx b’ stands for ‘xxx’ binary numbers.

TABLE 3-2: LX3302A CONFIGURATION EEPROM MAP

	MSB 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	LSB 0
WORD0	ID[17..2]															
WORD1	ID[1..0]		Reserved			GADJ				IOSC		Reserved		REFRESH		
WORD2	Filter	CLSEL	GMTCH[6..0]							DCOS[9..3]						
WORD3	DCOS[2..0]			SCOS[9..0]										DSIN[9..7]		
WORD4	DSIN[6..0]							SSIN[9..1]								
WORD5	SSIN[0]	OSCOMP[9..0]										Reserved				
WORD6	ORIGIN[11..0]												HCLMP[11..8]			
WORD7	HCLMP[7..0]								LCLMP[11..4]							
WORD8	LCLMP[3..0]				S0[11..0]											
WORD9	X1[11..0]												X2[11..8]			
WORD10	X2[7..0]								X3[11..4]							
WORD11	X3[3..0]				X4[11..0]											
WORD12	X5[11..0]												X6[11..8]			
WORD13	X6[7..0]								X7[11..4]							
WORD14	X7[3..0]				Y1[11..0]											
WORD15	Y2[11..0]												Y3[11..8]			
WORD16	Y3[7:0]								Y4[11:4]							
WORD17	Y4[3..0]				Y5[11..0]											
WORD18	Y6[11..0]												Y7[11..8]			
WORD19	Y7[7..0]								S7[11..4]							
WORD20	S7[3..0]				TD[12..1]											
WORD21	TD[0]	TDPOL	DIAGMK[11..0]												SENTCLK	
WORD22	SENTFCM[3..0]				SENTREFR[10..0]											SENT PPE
WORD23	SENTSCM[1..0]		MSG MUX	DIAG POL	PSI5FR[2..0]			PSI5STS[1..0]		PSI5MSG[1..0]		PSI5 ERRCS	PSI5DRB[3..0]			
WORD24	PSI5DRA[3..0]				PSI5REFR[10..0]											PSI5BR
WORD25	IOSEL[14..0]															OSC DFB
WORD26	OSCDAC[11..0]												TDMASK	EELOCK		
WORD27	MESSAGE[15..0]															
WORD28	MSGID[7..0]								TDHYST[7..0]							
WORD29	ADC10 IN	CLCHK	WD SCALE	Reserved												
WORD30	Reserved															
WORD31	Reserved															

3.1 GADJ (Four Bits, W1[10:7])

This parameter is used to adjust the gain of the Programmable Gain Amplifier (PGA). The bit, WORD1[10], is the polarity bit. The remaining three bits ([9:7]) adjust gains. The default gain ('00000 b') is 3.125. The gain can be adjusted in increments of approximately 3%. The smallest number is '1000' and the largest number is '0111'.

3.2 IOSC (Two Bits, W1[6:5])

The IOSC bits set the oscillator tail current value, as shown in Table 3-3.

TABLE 3-3: IOSC CONFIGURATION

IOSC Bits	Tail Current	Feedback
00	Normal mode	Enabled
01	1/2	Enabled
10	1/4	Enabled
11	1/8	Enabled

3.3 REFRESH (Three Bits, W1[2:0])

This parameter sets the value of the refresh rate of the ADC update. If the PWM output is selected then the PWM frequency is always equal to the ADC update rate. Also WDSCALE should be selected, as shown in Table 3-4.

TABLE 3-4: REFRESH CONFIGURATION

Bit Value	ADC1 and ADC2 Sampling Clock	PWM Frequency	WDSCALE
011	$F_{CLK}/8$	2 kHz	001
100	$F_{CLK}/16$	1 kHz	001
101	$F_{CLK}/32$	500 Hz	010
110	$F_{CLK}/64$	250 Hz	011

3.4 FILTER (One Bit, W2[15])

This bit selects the digital filter type. Setting the bit to '0' will set the filter type to SINC, while assigning a value of '1' will set the filter to SINC+FIR, as shown in Table 3-5.

TABLE 3-5: FILTER CONFIGURATION

FILTER Bit	Filter Type
0	SINC
1	SINC+FIR

3.5 CLSEL (One Bit, W2[14])

When the CLSEL bit is set to '1', it swaps the Sine and Cosine inputs (CL1 and CL2).

3.6 GMTCH (Seven Bits, W2[13:7])

The GMTCH bits set the value of the input channel gain mismatch correction used in input correction calculations.

3.7 DCOS (Ten Bits, W2[6:0]W3[15:13])

These bits set the dynamic offset correction of the CL1 input channel used in input correction calculations.

3.8 SCOS (Ten Bits, W3[12:3])

These bits set the offset correction of the CL1 input channel used in input correction calculations.

3.9 DSIN (Ten Bits, W3[2:0]W4[15:9])

These bits set the offset correction of the CL2 input channel used in input correction calculations.

3.10 SSIN (Ten Bits, W4[8:0]W5[15])

These bits set the dynamic offset correction of the CL2 input channel used in input correction calculations.

3.11 OSCOMP (Ten Bits, W5[14:5])

These bits set the maximum amplitude of the oscillator swing used in the input correction calculations. The maximum value of the OSCOMP setting is 1023 at Step 1.

3.12 ORIGIN (Twelve Bits, W6[15:4])

Offset value of the system origin relative to fore-and-after position. This is not a DC output offset adjustment.

3.13 HCLMP (Twelve Bits, W6[3:0]W7[15:8])

This parameter sets the high plateau level of output. When HCLMP > 0, the output will be clamped at this HCLMP value if the output swing (Pre_Clamp value) can go above this level. It reduces the maximum output swing. Full-scale swing is achieved with HCLMP = 4095 and LCLMP = 0.

3.14 LCLMP (Twelve Bits, W7[7:0]W8[15:12])

This parameter sets the low plateau level of output. The output is clamped at this level if the output swing can go below this level. The LCLMP value raises the minimum output value from zero. An output value of 'zero' is achieved with LCLMP = 0. Setting the value of LCLMP will override the HCLMP setting if both settings are crossed over.

3.15 S0 (Twelve Bits, W8[11:0])

This parameter sets the slope of the first linearization segment.

3.16 Xn and Yn (n = 1 to 7, Twelve Bits Each)

Refer to the EEPROM map in Table 3-2. The value of the X and Y coordinates for the “n”-th linearization point.

3.17 S7 (Twelve Bits, W19[7:0]W20[15:12])

These bits set the slope of the last linearization segment.

3.18 TD (Thirteen Bits, W20[11:0]W21[15])

This parameter is reserved.

3.19 TDHYST (Eight Bits, W28[7:0])

TDHYST is reserved.

3.20 TDPOL (One Bit, W21[14])

This bit is reserved.

3.21 TDMASK (Two Bits, W26[3:2])

This parameter is reserved. The value must be ‘00’.

TABLE 3-6: TDMASK CONFIGURATION

Bit Value	Frame	Remarks
00	None	TD is off
01	Reserved	
10	Reserved	
11	Reserved	

3.22 DIAGMK (Twelve Bits, W21[13:2])

DIAGMK enables Fault detection, as shown in Table 3-7. When a bit is set to ‘1’, Fault detection is enabled. When a bit is set to ‘0’, the result is masked.

TABLE 3-7: DIAGMK CONFIGURATION

Bit	Diagnostic Mask
0	EEPROM reading back error **(Note 1)**
1	MCU integrity check, ROM checksum, peripheral test, RAM test **(Note 2)**
2	Firmware flow **(Note 3)**
3	CL1, CL2 signal too low
4	CL1, CL2 signal too high
5	Reserved
6	V_{IN} POR error
7	V_{DD} failure
8	CL1, CL2 open
9	OSC1, OSC2 open
10	OSC undervoltage
11	OSC overvoltage

Note 1: EEPROM reading match failure.
2: Hardware integrity check failure.
3: Firmware not executed in the correct order.

3.23 SENTCLK (Two Bits, W21[1:0])

This parameter sets the SENT clock tick time period, as shown in Table 3-8.

TABLE 3-8: SENTCLK CONFIGURATION

Bit Value	Tick Clock (µs)
00	3
01	6
10	12
11	24

3.24 SENTFCM (Four Bits, W22[15:12])

This parameter sets the sensor type and serial protocol, as shown in Table 3-9.

TABLE 3-9: SENTFCM CONFIGURATION

Bit Value	Protocol
0000	Standard SENT
0001	A1 – single sensor with error sets data nibble feature
0011	A1 – single sensor without error sets data nibble feature
0100	Reserved
0101	
0110	
0111	
1000	A3 or A4 with counter and invert copy of Data Nibble 1 at Data Nibble 6
1001	A4 with counter and '0' at Data Nibble 6
1010	A4 with no counter and invert copy of Data Nibble 1 at Data Nibble 6
1011	A4 with no counter and '0' at Data Nibble 6
1100	A3 with counter and Data Nibble 6 as in 15- n1. Slow channel sends out ram_DIAG

3.25 SENTREFR (Eleven Bits, W22[11:1]), SENTPPE (One Bit, W22[0])

The SENTREFR and SENTPPE parameters are SENT constant clock ticks synced with the pause pulse. W22[0] is used to set the pause pulse. If this bit is set to '0', it disables the SENT pause pulse. If the bit is set to '1', the SENT pause pulse is enabled. The SENT message is synced with a selectable constant period of clock ticks. The SENT message syncs with selectable length based on clock ticks and is defined in 11 bits on SENTREFR.

Bits[10:0] set the number of clock ticks. All '0's set 0 clock ticks and all '1's set 2023 clock ticks.

3.26 SENTSCM (Two Bits, W23[15:14])

This parameter sets the SENT serial message, as shown in Table 3-10.

TABLE 3-10: SENTSCM CONFIGURATION

Bit Value	Configuration
00	Serial message is off
01	Serial message is on in short format
10	Serial message is on with enhanced format, 12-bit data and 8-bit ID
11	Serial message is on with enhanced format, 16-bit data and 4-bit ID

3.27 MSGMUX (One Bit, W23[13])

If the bit is set to '0', message MUX is disabled. Set this bit to '1' if PSI5 and the SENT serial channel message are enabled.

3.28 DIAGPOL (One Bit, W23[12])

This bit sets the Fault mode output level. It must be kept '0':

- '0': Fault mode outputs logic low
- '1': Fault mode outputs logic high

3.29 PSI5FR (Three Bits, W23[11:9])

This parameter sets the PSI5 frame, as shown in Table 3-11.

TABLE 3-11: PSI5FT CONFIGURATION

Bit Value	Frame
000	Disable PSI5 frame
001	Enable PSI5 frame and set the size to 1
010	Enable PSI5 frame and set the size to 2
011	Enable PSI5 frame and set the size to 3
100	Enable PSI5 frame and set the size to 4

3.30 PSI5STS (Two Bits, W23[8:7])

This parameter sets the PSI5 status, as shown in Table 3-12.

TABLE 3-12: PSI5STS CONFIGURATION

Bit Value	Status
00	Disable PSI5 status
01	Enable PSI5 status and set the size to 1
10	Enable PSI5 status and set the size to 2

3.31 PSI5MSG (Two Bits, W23[6:5])

This parameter sets the PSI5 serial message, as shown in Table 3-13.

TABLE 3-13: PSI5MSG CONFIGURATION

Bit Value	Configuration
00	Serial message is off
01	Serial message is on, size is set to 2
10	Serial message format is set to 12-bit data with 8-bit ID
11	Serial message format is set to 16-bit data with 4-bit ID

3.32 PSI5ERRCS (One Bit, W23[4])

This parameter is the PSI5 error check selection bit. Configuration is shown in Table 3-14.

TABLE 3-14: PSI5ERRCS SELECTION

Bit Value	Error Check
0	3-bit CRC
1	1-bit parity

3.33 PSI5DRB (Four Bits, W24[3:0])

This parameter sets PSI5 Data Region B and its size, as shown in Table 3-15.

TABLE 3-15: PSI5DRB CONFIGURATION

Bit Value	Description
0000	Disable PSI5 Data Region B
0001	Enable PSI5 Data Region B and set the size to 1 bit
0010	Enable PSI5 Data Region B and set the size to 2 bits
0011	Enable PSI5 Data Region B and set the size to 3 bits
0100	Enable PSI5 Data Region B and set the size to 4 bits
0101	Enable PSI5 Data Region B and set the size to 5 bits
0110	Enable PSI5 Data Region B and set the size to 6 bits
0111	Enable PSI5 Data Region B and set the size to 7 bits
1000	Enable PSI5 Data Region B and set the size to 8 bits
1001	Enable PSI5 Data Region B and set the size to 9 bits
1010	Enable PSI5 Data Region B and set the size to 10 bits
1011	Enable PSI5 Data Region B and set the size to 11 bits
1100	Enable PSI5 Data Region B and set the size to 12 bits

3.34 PSI5DRA (Four Bits, W24[15:12])

This parameter sets Data Region A, as shown in Table 3-16.

TABLE 3-16: PSI5DRA CONFIGURATION

Bit Value	Description
0000	Set PSI5 Data Region A size of 10 bits
0001	Set PSI5 Data Region A size of 11 bits
0010	Set PSI5 Data Region A size of 12 bits
0011	Set PSI5 Data Region A size of 13 bits
0100	Set PSI5 Data Region A size of 14 bits
0101	Set PSI5 Data Region A size of 15 bits
0110	Set PSI5 Data Region A size of 16 bits
0111	Set PSI5 Data Region A size of 17 bits
1000	Set PSI5 Data Region A size of 18 bits
1001	Set PSI5 Data Region A size of 19 bits
1010	Set PSI5 Data Region A size of 20 bits
1011	Set PSI5 Data Region A size of 21 bits
1100	Set PSI5 Data Region A size of 22 bits
1101	Set PSI5 Data Region A size of 23 bits
1110	Set PSI5 Data Region A size of 24 bits

3.35 PSI5REFR (Eleven Bits, W24[11:1])

This parameter sets the PSI5 refresh rate. Bits[10:0] set the bit time. All '0's set 0 bit times and all '1's set 2023 bit times. Single PSI5 frame length is from 13 bit times to 33 bit times, plus at least 3 bit times for gap time. The refresh rate is defined as the user-selected single PSI5 frame length including gap time. The hardware takes this number, minus the user-selected format length, with a minimum gap time of three bit times, then compensates the rest as gap time.

3.36 PSI5BR (One Bit, W24[0])

This bit sets the PSI5 bit time rate, as shown in Table 3-17.

TABLE 3-17: PSI5BR CONFIGURATION

Bit Value	Bit Time Rate
0	125 kbps
1	189 kbps

3.37 IOSEL (Fifteen Bits, W25[15:1])

The IOSEL bits provide the various output selection options. Table 3-18 shows the IOSEL bits versus output option. Factory default is Safety mode on.

TABLE 3-18: IOSEL BITS CONFIGURATION

IO1 Output		IO2 Output		IO3 Output	
Bits	**Remarks**	**Bits**	**Remarks**	**Bits**	**Remarks**
bit 12	1 = IO1 Safety mode on 0 = IO1 Safety mode off	bit 13	1 = IO2 Safety mode on 0 = IO2 Safety mode off	bit 14	1 = IO3 Safety mode on 0 = IO3 Safety mode off
bits 3-0		**bits 7-4**		**bits 11-8**	
Bit Values	**Setting**	**Bit Values**	**Setting**	**Bit Values**	**Setting**
1101	TD	1101	TD	1101	TD
1100	Reserved	1100	Reserved	1100	OD SENTB
1011	Reserved	1011	Reserved	1011	OD PWMB
1010	OD SENT	1010	OD SENT	1010	OD SENT
1001	OD PWM	1001	OD PWM	1001	OD PWM
0111	PP PWM	0111	PP PWM	0111	PP PWM
0110	PP PWMB	0110	PP PWMB	0110	PP PWMB
0101	PP SENT	0101	PP SENT	0101	PP SENT
0100	PP IO1	0100	PP IO2	0100	PP IO3
0011	Analog, PGA2, $V_{IN}/2$	0011	Analog, PGA2, $V_{IN}/2$	0011	Reserved
0010	Analog, PGA1, $V_{IN}/2$	0010	Analog, PGA1, $V_{IN}/2$	0010	Reserved
0001	Analog, PGA2, $V_{DD}/2$	0001	Analog, PGA2, $V_{DD}/2$	0001	PSI5
0000	Analog, PGA1, $V_{DD}/2$	0000	Analog, PGA1, $V_{DD}/2$	0000	Analog DAC

3.38 OSCDFB (One Bit, W25[0])

This bit is used to set the oscillator tail current feedback control loop. If the bit is set to '0', the analog signal is fed to the oscillator circuit. If the bit is set to '1', then the value on the OSCDAC of the EEPROM is fed to the oscillator circuit. This functionality is not available when Analog mode on IO3 is selected.

3.39 OSCDAC (Twelve Bits, W26[15:4])

This parameter is used to set the value of the oscillator tail current control when the OSCDFB bit is set to '1'. The lower 11 bits determine the oscillator tail current. The upper bit must be set to '0'. This functionality is not available when Analog mode on IO3 is selected.

3.40 EELOCK (Two Bits, W26[1:0])

There are two lock bits (W26[1:0]). If the LSB lock bit is set to '1', then the EEPROM cannot be written unless IO4 is pulled high to overwrite the EELOCK setting.

3.41 MESSAGE (Sixteen Bits, W27[15:0])

SENT/PSI5 Serial Message Configuration bits. The hardware takes data from the MSB to the LSB. The user inputs the contents of the serial message.

3.42 MSGID (Eight Bits, W28[15:8])

Serial Message ID for SENT or PSI5 serial message. The user inputs the Serial Message ID content from the MSB to the LSB.

3.43 ADC10IN (One Bit, W29[15])

ADC10 monitor selection bit. The default setting of '1' configures the device to monitor exciter voltage. Setting this bit to '0' enables the internal temperature sensor.

3.44 CLCHK (One Bit, W29[14])

The CLCHK bit sets the CL1/CL2 input range check. The CL1/2 input range check is disabled when the CLCHK bit is set to '1'.

3.45 WDSCALE (Three Bits, W29[13:11])

WDSCALE is used to adjust the Watchdog Timer when the various refresh rate options are selected.

TABLE 3-19: WDSCALE CONFIGURATION

Bit Value	WDSCALE	Refresh	Remarks
000	0	—	
001	1	2 kHz 1 kHz	Default
010	2	500 Hz	
011	3	250 Hz	
100	4	—	
101	5	—	
110	6	—	
111	7	—	

4.0 THEORY OF OPERATION

4.1 General Information

The LX3302A is a highly integrated programmable data conversion IC designed for interfacing to, and managing of, inductive sensors. The device includes an integrated oscillator circuit for driving the primary coil of an inductive sensor, along with two independent analog conversion paths for conditioning, converting and processing of two analog signals from the secondary coils of the PCB sensor. Each path includes an EMI filter, demodulator, anti-alias filter, programmable amplifier, and a 13-bit Sigma-Delta Analog-to-Digital converter before the DSP. DSP peripherals include a SENT serial interface, PSI5 serial interface, programmable PWM controller and a 12-bit Digital-to-Analog Converter.

4.2 Oscillator

The on-chip oscillator provides a carrier signal for driving the primary coil of the inductive sensor via pins, OSC1 and OSC2. The carrier signal is generated by an internal current source, which resonates with the primary inductor and external capacitors (which form a tank circuit). The oscillator operates over a frequency range from 1 MHz to 5 MHz, as shown in Equation 4-1.

EQUATION 4-1:

$$f = \frac{1}{2\pi\sqrt{LC}}$$

Where:

L = Inductance of Coil

C = Tanking Capacitance

The value of the inductor L is the most critical element in the cross-coupled LC tank oscillator. Because the inductance is relatively low, the parasitic resistance of L can dominate and impact the ability to maintain oscillation. As such, the value of inductor L should be as large as possible and with a high Q factor. Small clearance of PCB traces of primary coil contributes significant parasitic capacitance to the tank circuit. The resonant frequency is the result of total equivalent capacitance in the circuit. An external capacitor for the tanking circuit should be C0G or NP0-type, low-ESR at 1 to 6 MHz and rated 50V.

In most applications, the inductor L is implemented as traces on a Printed Circuit Board (PCB). Depending on the processing of the PCB, the height and width of the trace will vary, resulting in a variation of the inductance L and of the parasitic resistance. Because these variations will change from PCB to PCB, it is necessary to calibrate each sensor PCB independently. Care should be taken to select a PCB source which can achieve manufacturing tolerances required by a given set of system requirements.

The amplitude of the carrier signal is a function of the primary coil tank circuit configuration, and feedback of the secondary coil signals from the CL1 and CL2 inputs. The shoulder signals of the tank circuit are protected by an internal clamp circuit. It will distort the sinusoidal waveform if the tank circuit and secondary coil feedback signal are not within design limits.

In order to detect system Faults, the IC monitors the amplitude of the carrier signal on pin OSC1. When the amplitude is above or below the specified amplitude (reference the VOSC_OV and VOSC_UV parameters in the **Electrical Characteristics** section), the output pin will be forced either to 0V or high, depending on the DIAGPOL setting, if the DIAGMK parameter is set to 0xFFF and IOSEL is set to Safety mode. This output level indicates a system Fault. When initially calibrating a sensor, the voltage on OSC1 should be monitored in order to verify that the amplitude is within the specified range. If the OSC1 voltage is too high, the signal levels at CL1 and CL2 may be too low. If the OSC1 voltage is too low, the signal levels at CL1 and CL2 may be too high. The optimal level of OSC1 is about 6.5 Vpp, at typical airgap distance, from the target surface to the sensor coil surface.

4.3 Demodulator, Programmable Gain Amplifier and Anti-Alias Filter

Pins, CL1 and CL2, are the inputs to the AFE block. The programmable gain amplifier features four bits of range, where the '0000' default value corresponds to a gain of 3.125 (total gain is 21.875). Bit value percentage changes that can be applied to the 3.125 default gain value are shown in Table 4-1.

TABLE 4-1: PROGRAMMABLE GAIN AMPLIFICATION SETTING

Bit #	Function
0	3% Amplification
1	6% Amplification
2	12% Amplification
3	24% Amplification

The output of the amplifier goes through a low-pass anti-aliasing filter prior to input to the Sigma-Delta ADC.

4.4 Sigma-Delta ADC with Digital Filters

Each analog path includes a 13-bit Sigma-Delta Analog-to-Digital Converter (ADC). The sampling frequency for the ADC is derived from the main clock by the REFRESH bits in the Configuration EEPROM.

The ADC decimation filter includes a SINC filter and a half-band FIR filter. The SINC filter provides -40 dB of stop-band attenuation. Because the SINC filter does not provide the same sharp response as a finite/infinite filter response, a half-band FIR filter is also provided. The drawback of the FIR filter is that it adds delay to the input signal, and this delay depends on the number of coefficients and the output data rate. The half-band FIR filter can be selected by the “FILTER” setting in the Configuration EEPROM.

4.5 Embedded CPU

The LX3302A includes an embedded 32-bit micro-controller core, which is used to perform filtering and math functions on the digitized samples from the ADCs. The MCU executes a set of preprogrammed filtering and math functions which can be selected by setting the appropriate bits in the on-chip Configuration EEPROM. Also included in the on-chip Configuration EEPROM are system calibration and linearization coef-ficient bits. The device includes a Watchdog Timer, which will reset the chip if the MCU is unable to reset the Watchdog Timer within the preprogrammed period. Note that the Watchdog Timer time-out is automatically scaled with the refresh rate of the ADCs.

4.6 Configuration EEPROM

The LX3302A includes a user-programmable, 32 x 16 bits EEPROM for storing configuration parameters into nonvolatile memory. Two EEPROM Programming modes are provided: V_{IN} EEMode and Digital EEMode.

4.6.1 V_{IN} EEMODE

V_{IN} EEMode uses V_{IN} as the power line communication with CLK and DATA. The device is placed into EEPROM Programming mode (V_{IN} EEMode) by increasing the voltage on the V_{IN} pin to 15.3V. Note that a delay of 200 µs (t_2) from power-on must be observed before EEPROM Programming mode is entered. Also, maximum delay time should be less than 12 ms.

Data are represented by one of two voltage levels on the V_{IN} pin: a ‘1’ is represented by increasing the V_{IN} voltage to 17.5V, while a ‘0’ is represented by decreasing the V_{IN} voltage to 13V. The voltage for a given bit must be held for a minimum duration of 20 µs (t_3), and between each bit, the voltage must return to 15.3V for a minimum of 20 µs (t_4) (see Figure 4-1).

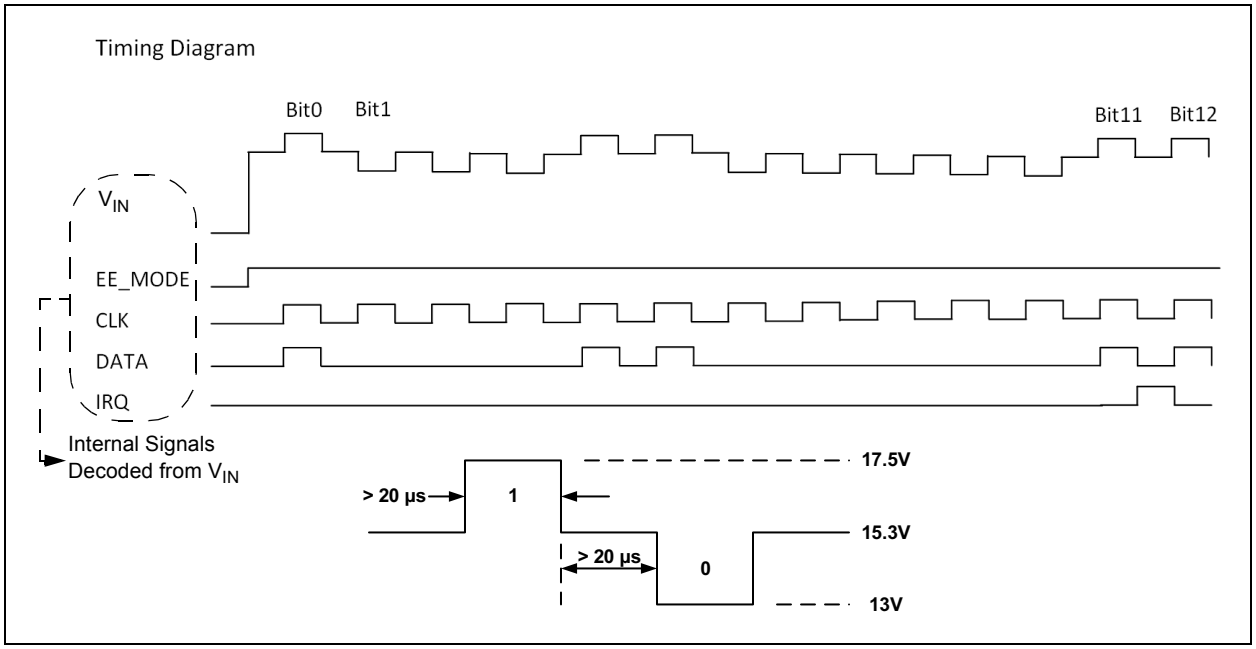


FIGURE 4-1: *EEPROM Decoder Block Diagram.*

The first five bits sent in EEMode are the command bits, followed by the address bits, which correspond to the logic level of the selected I/O pin and to the reversed five command bits. The programming commands are only executed if the address bits and selected I/O pin logic level match.

The LX3302A uses the Watchdog Timer to provide the timer for Programming Write/Read or Test mode operation. It is required to complete the EEPROM programming or ADC test before the Watchdog Timer time-out. If the timer times out before the programming operation has been completed, IC operation will be locked and it may be unable to access the device due to an incomplete data write.

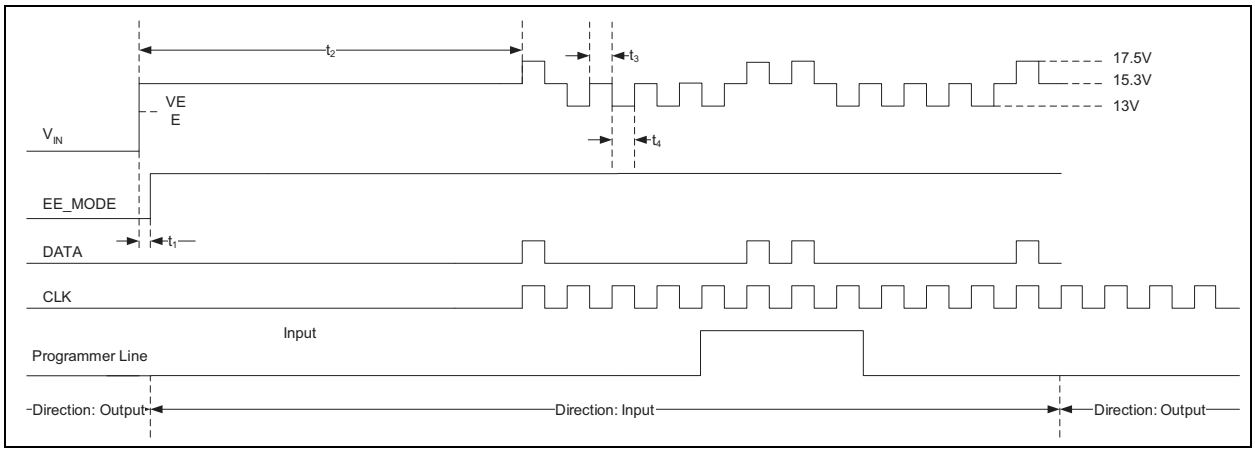


FIGURE 4-2: *V_{IN} EEMode Programming Diagram.*

4.6.2 DIGITAL EEMode

Digital EEMode uses IO4 as EEMode enable, IO1 as CLK and IO2 as data. IO3 is used as an address pin and EEPROM data output pin. The device is placed into EEPROM Programming mode (Digital EEMode) by increasing the voltage on the IO4 pin to 3.3V. The timing diagram between IO4, IO1, IO2 and IO3 is shown in Figure 4-3. IO4 must be present prior to V_{IN} being applied (t_{1a}). Note that a delay of 200 µs (t_{2a}) from power-on must be observed after clocking. Also, maximum delay time should be less than 12 ms. Data/clock should be a minimum duration of 20 µs (t_3) and the off duration should be a minimum of 20µ (t_4).

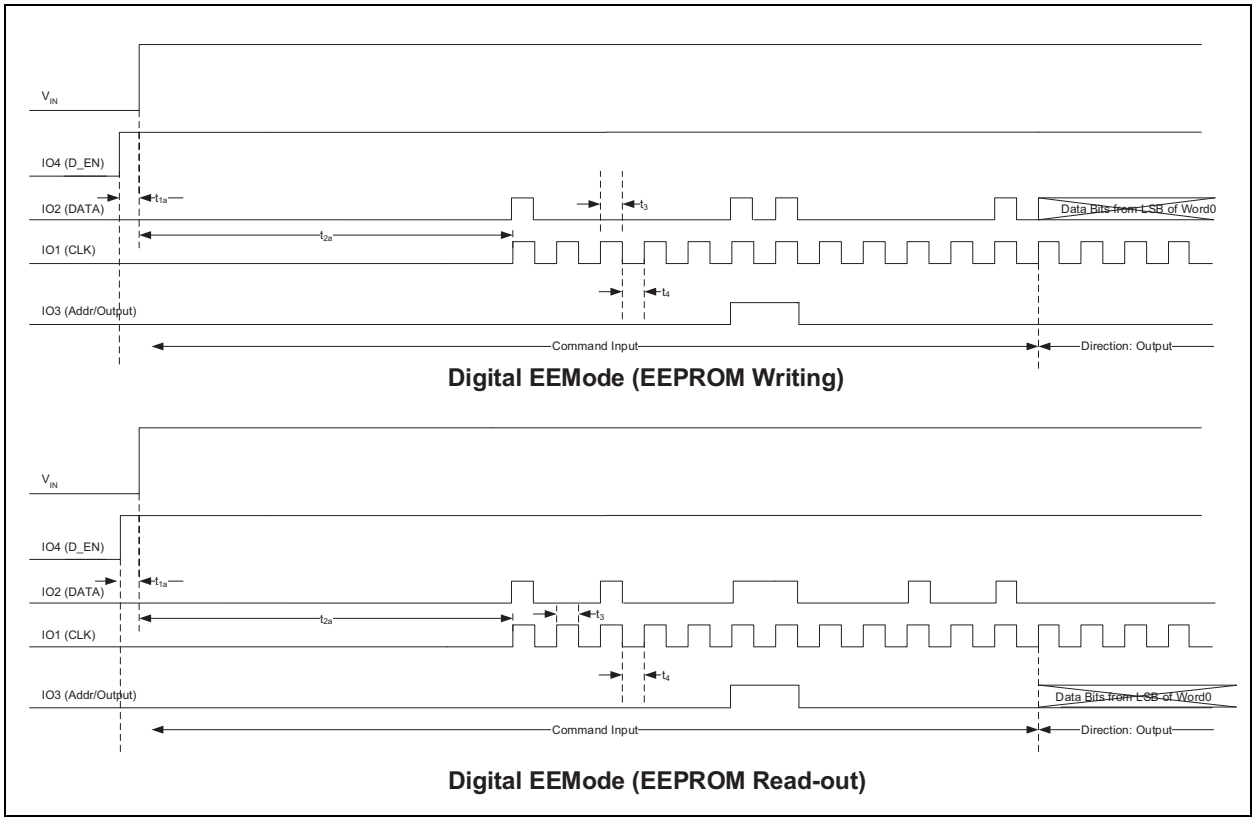


FIGURE 4-3: *Digital EEPROM Timing Diagram.*

The first five bits sent in EEMode are the command, followed by the address bits, which correspond to the logic level of the IO3 pin and the reversed five command bits. The programming commands are only executed if the address bits and IO3 pin logic level match.

The LX3302A employs the Watchdog Timer to provide a timer for Programming Write/Read or Test mode operation. It is required to complete the EEPROM programming or ADC test before the Watchdog Timer time-out. If the timer times out before the programming operation completion, then it will lock IC operation and it may be unable to access the device due to an incomplete data write. After completion of EEPROM writing, in order to read written EEPROM parameters, V_{IN} has to be disabled until the IC enters Reset. Reset time is dependent upon V_{DD} bypass capacitance and V_{IN} bypass capacitance discharge time.

4.6.3 EEMode COMMANDS AND OPERATION

To enter the EEPROM Writing mode, with selected I/O without PSI5 mode for V_{IN} EEMode or with IO3 for Digital EEMode, the user has to enter the EEMode and send the command as shown below. The user must first enter a 12-bit command, followed by 32 words, starting from the LSB of WORD0 and finishing with the MSB of WORD31, and 21 bits of checksum of the 32 words. If the checksum is wrong, the EEPROM will not be erased or written. The address input is the selected I/O pin for V_{IN} EEMode or the IO3 pin for Digital EEMode. Note that the command starts from B0, B1, B2, B3, B4, Addr, Addr, B4, B3, B2, B1, B0 and so on. The following tables show an example of EEPROM writing with Addr = 1.

EXAMPLE 4-1:

Command					Addr	Addr	Command					WORD0			WORD1			...	WORD31			Checksum		
B0	B1	B2	B3	B4			B4	B3	B2	B1	B0	B0	...	B15	B0	...	B15	...	B0	...	B15	B0	...	B20
1	0	0	0	0	0/1	0/1	0	0	0	0	1	0/1	...	0/1	0/1	...	0/1	...	0/1	...	0/1	0/1	...	0/1

To enter the EEPROM Writing mode with IO3 and PSI5 mode (V_{IN} EEMode only), the user must enter EEMode and send the command as shown below. Send the 12-bit command, '0010 0000 0100', followed by 32 words, starting from the LSB of WORD0 and ending with the MSB of WORD31, then followed by a 21-bit checksum of the 32 words. If the checksum is wrong, the EEPROM will not be erased or written. The address input is the IO3 pin. Note that the command starts from B0, B1, B2, B3, B4, Addr, Addr, B4, B3, B2, B1, B0 and so on. An example of writing to EEPROM with IO3 and Addr(CS) = 0 follows.

EXAMPLE 4-2:

Command					Addr	Addr	Command					WORD0			WORD1			...	WORD31			Checksum		
B0	B1	B2	B3	B4			B4	B3	B2	B1	B0	B0	...	B15	B0	...	B15	...	B0	...	B15	B0	...	B20
0	0	1	0	0	0	0	0	0	1	0	0	0/1	...	0/1	0/1	...	0/1	...	0/1	...	0/1	0/1	...	0/1

To enter the EEPROM Read-Out mode from the selected I/O pin, no PSI5 mode enabled, the user must first enter EEMode and send the 12-bit command as shown below (for example: '1010 0xx0 0101').

EXAMPLE 4-3:

Command					Addr	Addr	Command					WORD0			WORD1			...	WORD31			Checksum		
B0	B1	B2	B3	B4			B4	B3	B2	B1	B0	B0	...	B15	B0	...	B15	...	B0	...	B15	B0	...	B20
1	0	1	0	0	0/1	0/1	0	0	1	0	1	0/1	...	0/1	0/1	...	0/1	...	0/1	...	0/1	0/1	...	0/1

Once the 12 command bits have been sent, the outputs are reactivated and the selected I/O pins will have transitioned to logic high. To serial out the data, a clock pulse has to be sent on V_{IN}. After each clock, the next bit is sent to the output, starting with bit 0 of WORD0 to bit15 of WORD31. After bit 15 of WORD31 has been read, it will send the 21-bit checksum of WORD0 to WORD31 of EEPROM. An extra clock at the end will output logic low.

To enter the EEPROM Read-out mode from IO3, PSI5 mode enabled, the user has to enter EEMode and send the command ('0001 0000 1000') as shown below.

EXAMPLE 4-4:

Command					Addr	Addr	Command					WORD0			WORD1			...	WORD31			Checksum		
B0	B1	B2	B3	B4			B4	B3	B2	B1	B0	B0	...	B15	B0	...	B15	...	B0	...	B15	B0	...	B20
0	0	0	1	0	0	0	0	1	0	0	0	0/1	...	0/1	0/1	...	0/1	...	0/1	...	0/1	0/1	...	0/1

Once this 12-bit command has been sent, the outputs are reactivated and the IO3 pin will have transitioned to logic high. To serial out the data, a clock pulse must be sent on V_{IN}. After each clock, the next bit is sent to the output, starting with bit 0 of WORD0 to bit 15 of WORD31. After bit 15 of WORD31 has been read, the 21-bit checksum of WORD0 to WORD31 of EEPROM will be sent. An extra clock at the end will output logic low. Note that when the data outputs high to IO3, it will turn on the PSI5 current sink; so if the power supply cannot provide enough current, V_{IN} will be dropped. If it falls below the UVLO threshold, the IC operation will be reset.

Table 4-2 lists the 12-bit commands for EEPROM programming.

TABLE 4-2: EEPROM PROGRAMMING COMMANDS(1)

	#	B0	B1	B2	B3	B4	B5 (c/s)	B6 (c/s)	B7	B8	B9	B10	B11	Command	Description
V/D	1	1	0	0	0	0	0/1	0/1	0	0	0	0	1	Write EEPROM on IO3, no PSI5 enabled	V_{IN} or Data sends the 12-bit command, then 512 EEPROM bits to be written, plus 21 bits of checksum. Use IO3 as address bit input.
V	2	0	1	0	0	0	0/1	0/1	0	0	0	1	0	Write EEPROM on IO1	V_{IN} sends the 12-bit command, then 512 EEPROM bits to be written, plus 21 bits of checksum. Use IO1 pin as address bit input.
V	3	1	1	0	0	0	0/1	0/1	0	0	0	1	1	Write EEPROM on IO2	V_{IN} sends the 12-bit command, then 512 EEPROM bits to be written, plus 21 bits of checksum. Use IO2 pin as address bit input.
V	4	0	0	1	0	0	0	0	0	0	1	0	0	Write EEPROM on IO3, PSI5 mode	V_{IN} sends the 12-bit command, then 512 EEPROM bits and the 21-bit checksum. IO3 is the CS input. Addr(c/s) must be '0'.
V/D	5	1	0	1	0	0	0/1	0/1	0	0	1	0	1	Read out EEPROM on IO3, no PSI5 enabled	V_{IN} or Data sends the 12-bit command, then 512 EEPROM bits plus the 21-bit checksum. Clocked out on IO3.
V	6	0	1	1	0	0	0/1	0/1	0	0	1	1	0	Read out EEPROM on IO1	V_{IN} sends the 12-bit command, then 512 bits of EEPROM plus 21 bits of checksum. Clocked out on IO1.
V	7	1	1	1	0	0	0/1	0/1	0	0	1	1	1	Read out EEPROM on IO2	V_{IN} sends the 12-bit command, then 512 EEPROM bits plus the 21-bit checksum. Clocked out on IO2.
V	8	0	0	0	1	0	0	0	0	1	0	0	0	Read out EEPROM on IO3, PSI5 mode	V_{IN} sends the 12-bit command, then 512 EEPROM bits plus the 21-bit checksum. IO3 is the CS input. Addr(c/s) must be '0'.
V/D	9	1	0	0	1	0	0/1	0/1	0	1	0	0	1	Read back temperature data	V_{IN} or Data sends the 12-bit command, then 10 bits of temperature data are clocked out on IO3.

Note 1: V = V_{IN} EEMode, D = Digital EEMode.

4.6.4 CHECKSUM CALCULATION

The checksum of the 512-bit EEPROM data can be calculated as shown in Example 4-5. “wordn” is the EEPROM word number from 0 to 31. By adding 32 words of EEPROM data, 21 bits of checksum data will be generated as Hex.

EXAMPLE 4-5:

```
Uint32 check_sum =0U;
for(wordn=0U;wordn<32U;wordn++)
{
   a = read_word((uint32_t)wordn, EEPROM_RD);
   check_sum += a;  /* EEPROM checksum */
}
```

4.7 PWM Controller

A 16-bit digital PWM controller is implemented on the chip. The module allows the user to time and control different events. It can generate a pulse-width modulated signal of varying period and duty cycle. The PWM module has a 3-bit prescalar to divide down the MCU clock signal. PWM frequency is selected by “REFRESH” on the Configuration EEPROM. PWM mode can be set by “IOSEL”. When PWM is selected, a pull-up resistor between the IO1/2/3 pin and V_{IN} or V_{DD} is needed; 10 kΩ is recommended. PWM frequency is trimmed at factory.

4.8 12-Bit DAC

A 12-bit Digital-to-Analog Converter (DAC) is implemented on the chip. When the OSCFB bit is set to ‘0’ and the IO3 pin is set for “Analog”, this DAC provides the analog output of the measured sensor data. In this mode, the voltage reference for the DAC is V_{IN}. When the OSCFB bit is set to ‘1’, this DAC sets the magnitude of oscillator tail current based upon the value of the OSCDAC bits in the Configuration EEPROM. Note that DAC control of the oscillator tail current is not available when Analog Output mode on IO3 is selected.

4.9 SENT (SAE J2716)

The LX3302A supports the SAE J2716 JAN2010 SENT standard. It is implemented with the inductive sensor requirement only, with one 16-bit serial message.

SENT is an acronym for Single-Edge Nibble Transmission, which consists of transmitting eight nibbles (one nibble equals four bits) in sequence. Each nibble is coded using a PWM output referenced to the falling edge. SENT is a point-to-point unidirectional scheme from sensor device to controller. The series of transmitted pulses are measured from falling edge to falling edge (clock tick) with a programmable time granularity of 3 µs, 6 µs, 12 µs and 24 µs.

Each nibble has a defined PWM cycle output. The output is driven low (after the falling edge) for five clock ticks first and then driven high for seven clock ticks, plus N clock ticks, where N is the decimal value of the nibble. For example, when transmitting a nibble value of 0 (minimum), the output is driven low for five clock ticks then driven high for seven clock ticks. The total period for the shortest nibble (n = 0) is therefore, 12 clock ticks, as shown in Figure 4-4.

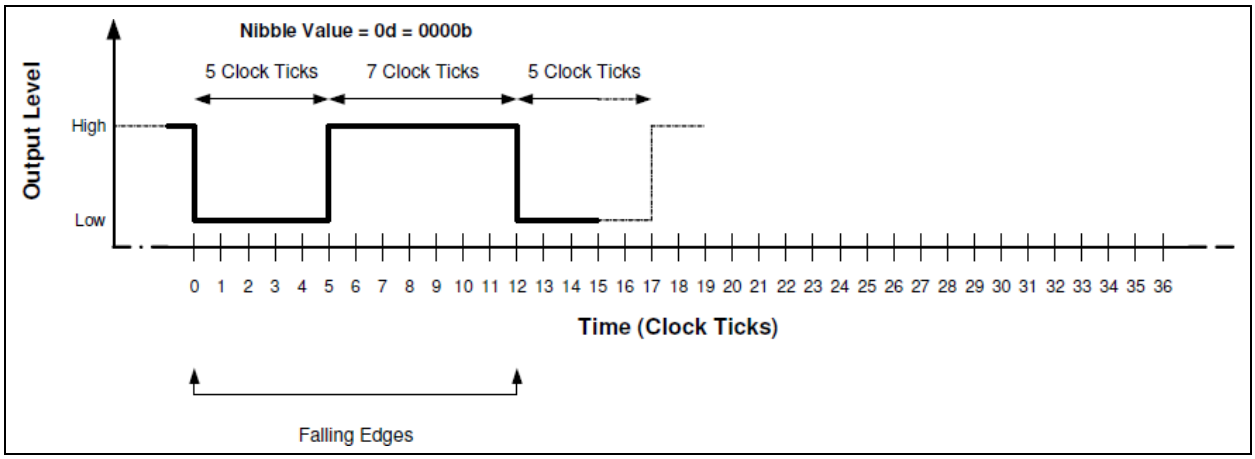


FIGURE 4-4: *Timing Diagram for Nibble Value = 0d.*

For example, when transmitting a nibble value of 15 (maximum), the output is driven low for five clock ticks, then driven high for 22 (7+15) clock ticks. The total period for the longest nibble (n = 15) is therefore, 27 clock ticks as shown in the following figure.

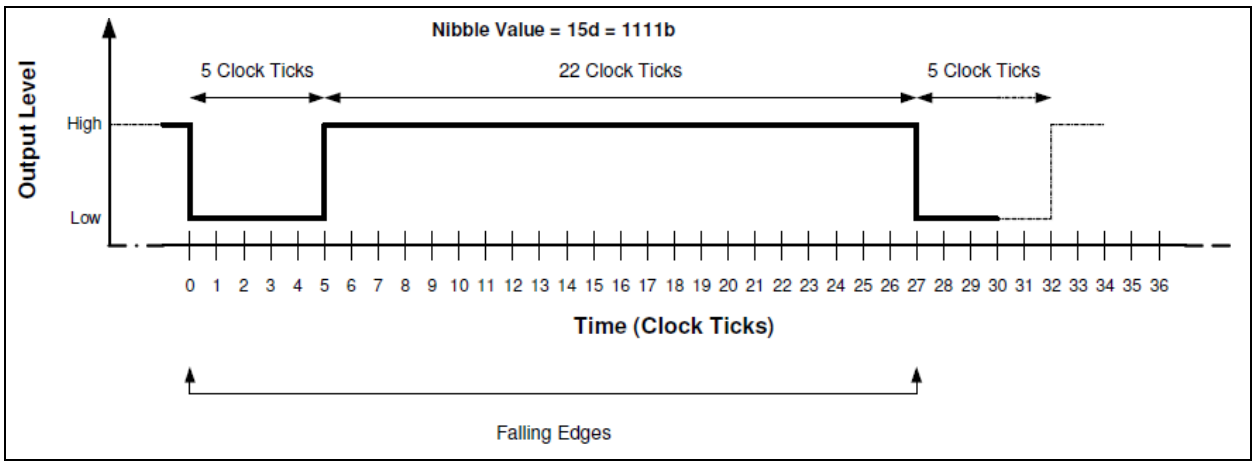


FIGURE 4-5: *Timing Diagram for Nibble Value = 15d.*

4.9.1 TRANSMISSION SEQUENCE

The transmission sequence for the SENT feature is:

1. Calibration/synchronization pulse period of 56 clock ticks.
2. One 4-bit status and serial communication nibble pulse of 12 to 27 clock ticks.
3. A sequence of six 4-bit data nibble pulses (12 to 27 clock ticks each) representing the values of the signal(s) to be communicated.
4. One 4-bit checksum nibble pulse of 12 to 27 clock ticks.

Without a pause pulse, one transmission consists of 154 to 270 clock ticks. The transmission rate depends on firmware operation.

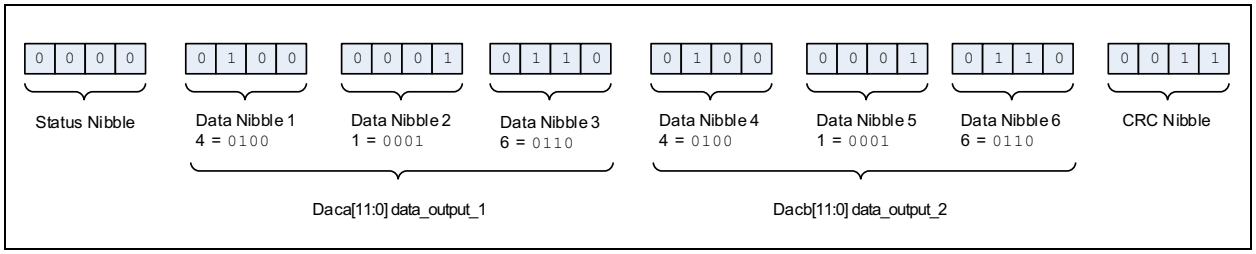


FIGURE 4-6: *Encoded SENT Format for 0x416.*

4.9.2 CALIBRATION PULSE

1. The 56 clock ticks period consists of 5 clock ticks driven low plus 51 clock ticks driven high.
2. The period is measured by the receiving module to calibrate/synchronize the clock time.

4.9.3 STATUS NIBBLE

The status bits represent the sensor error status, as follows:

- Bit 3 (MSB): Message start = 1, otherwise '0' or serial data message bit
- Bit 2: Serial data message bit
- Bits 1, 0: Reserved for specific application. See Table 4-3.

TABLE 4-3: STATUS NIBBLE(1)

Status Nibble	Bit 3	Bit 2	Bit 1	Bit 0
SENT Mode '000' Standard	Reserved as '0'	Reserved as '0'	Reserved as '0'	Reserved as '0'
SENT Mode A.1	Reserved as '0'	Reserved as '0'	TPS2 Error = 1	TPS1 Error = 1
SENT Mode A.3	Reserved as '0'	Reserved as '0'	Always '0'	Error = 1
SENT Mode A.4	Reserved as '0'	Reserved as '0'	Always '0'	Error = 1

Note 1: For proper detection of sensor error, status bits 1 and 0 must be used for error detection. Using Standard mode (SENTCFM = 0000) for error detection required applications is not recommended.

The LX3302A supports two serial message formats:

1. Short Serial Message Format:

   Serial data are transmitted in a 16-bit sequence in Status Nibble Bit 2, as shown in Figure 4-7. The starting bit of a serial message is indicated by a '1' in bit 3, then for the next 15 frames, bit 3 = 0.

   The 16-bit message consists of a 4-bit Message ID nibble, 8 bits of data and a 4-bit CRC checksum. The CRC checksum is derived for the Message ID and 8-bit data, and is the same checksum algorithm as used to calculate the SENT CRC nibble. The Message ID is used to identify the type of data being communicated in the 8-bit data transmission. Please refer to JAE2716 JAN 2010 for details.

   Data transmitted in bit 2 are sent from Most Significant Bit to Least Significant Bit.

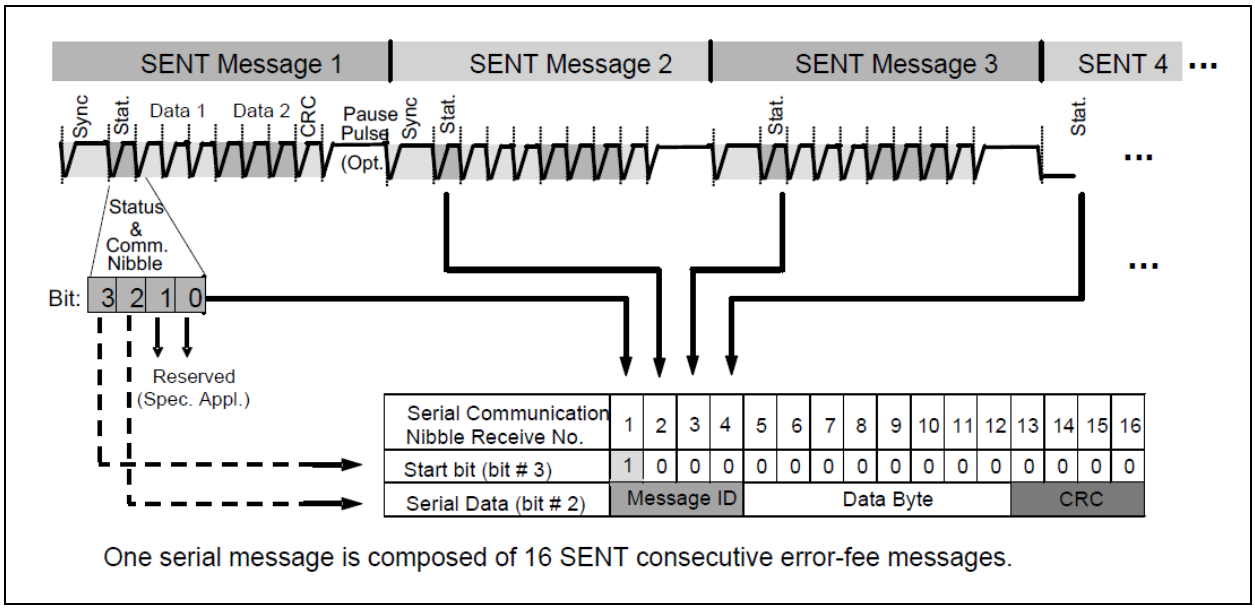


FIGURE 4-7: *Short Serial Message Format.*

2. Enhanced Serial Message Format:

   The other serial message format option is enhanced serial message format. It is used for a larger data field and larger ID message. Both bit 2 and bit 3 are used for this format. It stretches over 18 consecutive SENT messages, as shown in Figure 4-8.

   This 18 consecutive messages start with the fixed pattern, '1111110', in bit 3. Bit 3 of the 7th, 13th and 18th message frames is set to '0'. All data are transferred from MSB to LSB.

   The serial message frame contains 21 bits of payload data. Two different configurations can be chosen determined by bit 3 of the 8th frame.

   - 12-bit data and 8-bit Message ID (Configuration bit = 0, Figure 4-9)
   - 16-bit data and 4-bit Message ID (Configuration bit = 1, Figure 4-10)

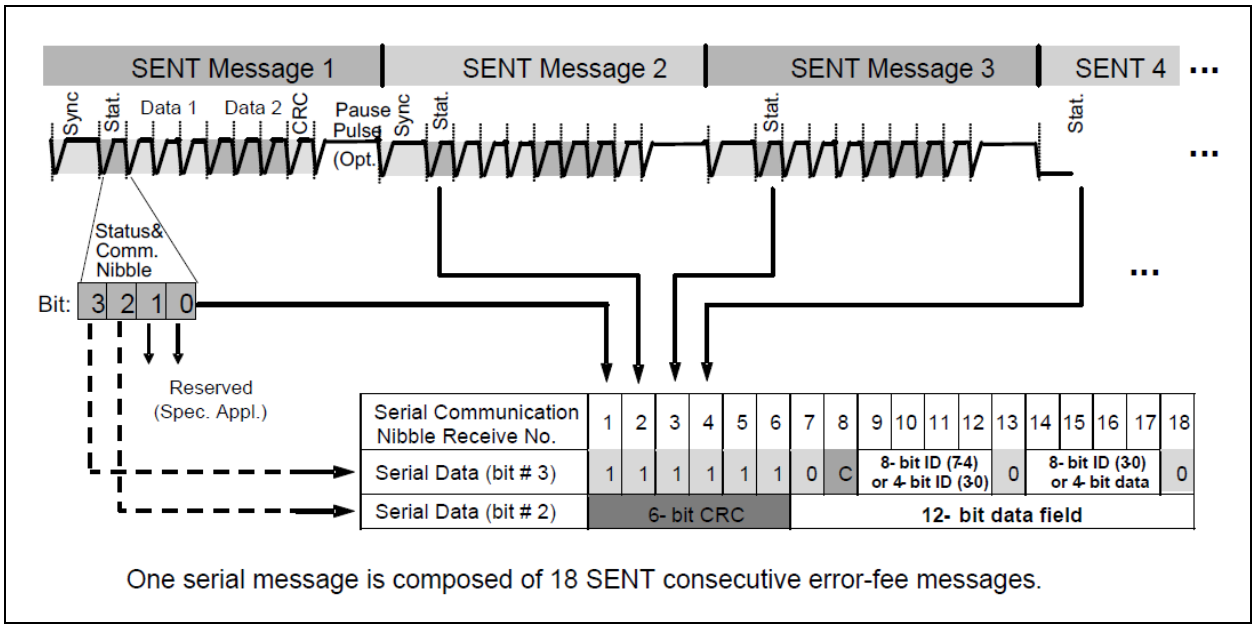


FIGURE 4-8: *Enhanced Serial Message Format.*

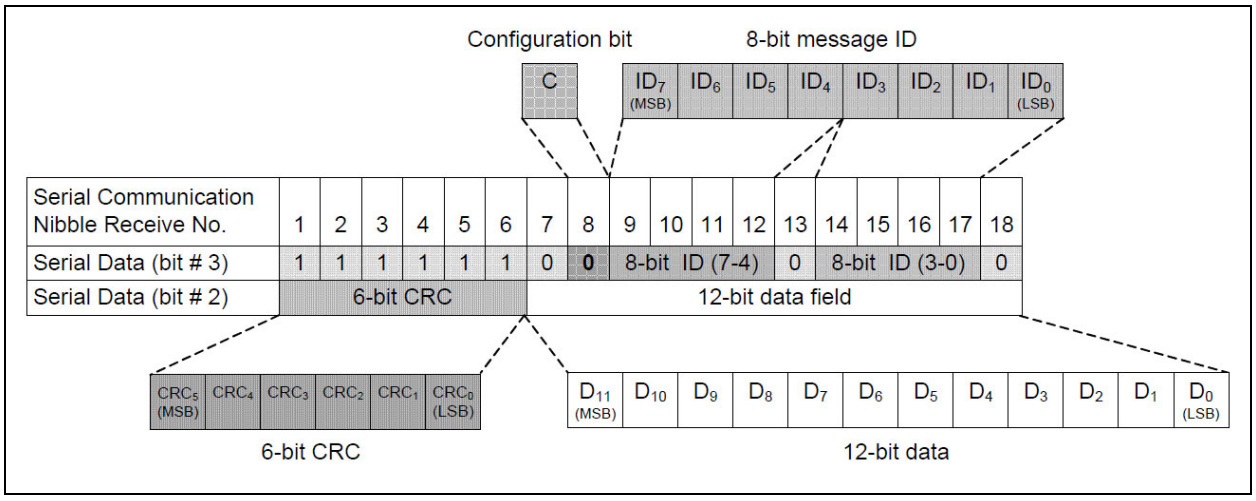


FIGURE 4-9: *12-Bit Data and 8-Bit Message ID.*

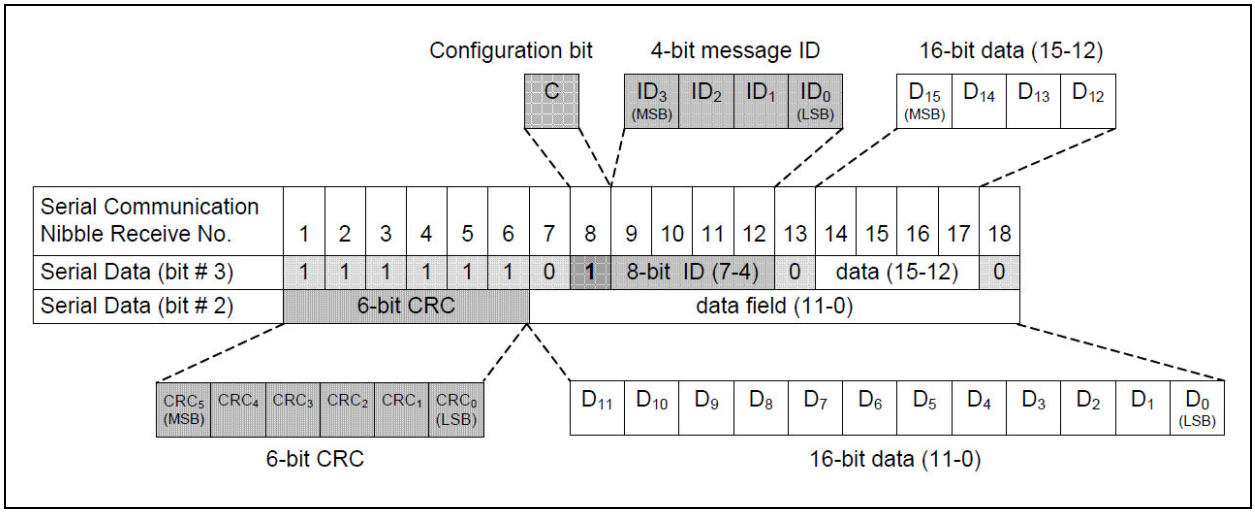


FIGURE 4-10: *16-Bit Data and 4-Bit Message ID.*

The CRC for the enhanced serial message format is described in Figure 4-11. This CRC value is computed as a function of the contents of serial data message bits #2 and #3 for frames 7 to 18. See Figure 4-11 for CRC order and details.

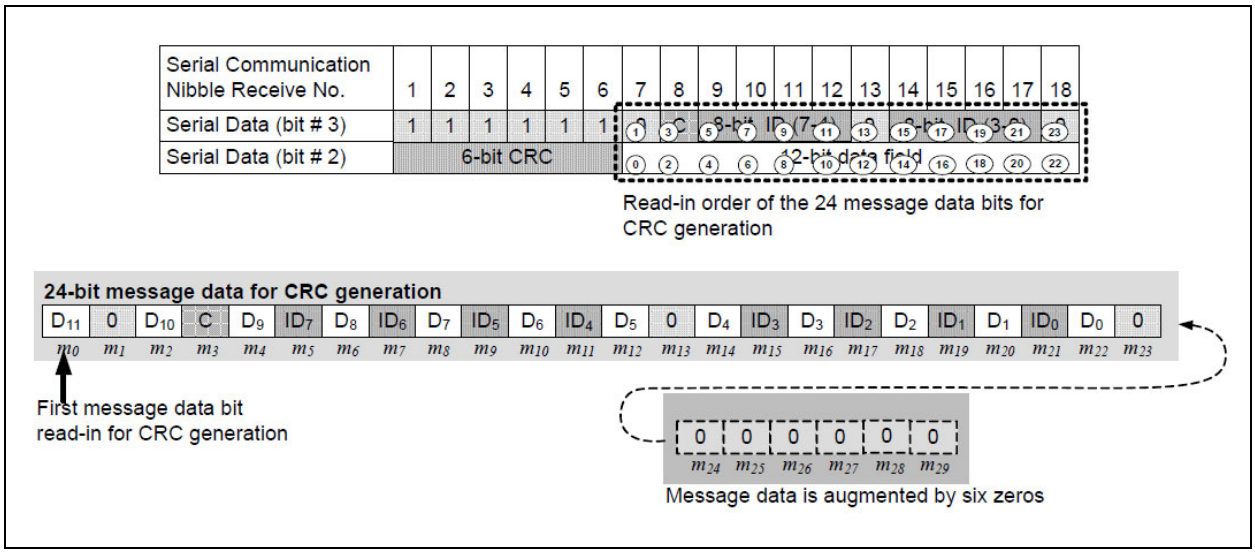


FIGURE 4-11: *CRC for Enhanced Serial Message.*

The encoding is defined by the generating polynomial, $G(x) = x^6 + x^4 + x^3 + 1$, with seed value, '010101'. For CRC generation, the message will be augmented by six zeros:
M_{CRC} = [m0 m1 m2 ……. m21 m22 m23 0 0 0 0 0 0].

4.9.4 DATA NIBBLE

SENT has six data nibbles. Register SENT_data1 content is sent out as data nibbles 1 to 3. Register SENT_data2 content is sent out as data nibbles 4 to 6.

For standard SENT protocol, 12-bit sensor position information can be stored in the SENT_data1 register and the same data are replicated in the SENT_data2 register. The most significant nibble of each data is transmitted first. After the status nibble pulse, the first data nibble is transmitted, starting with five ticks driven low, followed by seven ticks driven high, then extended by the data nibble decimal ticks. The rest of the data nibbles are transmitted in the same manner.

The LX3302A supports SENT A3 and A4 protocols and meets the following requirements:

1. Sensor value is transmitted as a 12-bit value in this nibble order:
   Data nibble 1: MSN,
   Data nibble 2: MidN,
   Data nibble 3: LSN.
2. Data nibbles 4 and 5 are an 8-bit rolling counter (0 to 255) with rollover back to 0. Data nibble 4 is the MSN and data nibble 5 is the LSN of the counter value. There is a register bit in the internal EEPROM that can manually reset the counter.
3. For the A3 protocol, data nibble 6 is the inverted copy of nibble 1 (15 minus nibble 1 value).
4. For the A4 protocol, data nibble 6 can be the same format as the A3 protocol or can be reset to zero. Data nibbles 4 and 5 are the rolling counter or set to all zeros.

4.9.5 CRC NIBBLE

This section describes the recommended implementation and the legacy implementation of the CRC nibble.

1. Recommended Implementation:

   The CRC nibble contains a 4-bit CRC of the data nibbles only. The "Status and Communication Nibble" is not included in the CRC calculation. The CRC is calculated using polynomial, $x^4 + x^3 + x^2 + 1$, with a binary initialization value of '0101'. The augment message data are extended with four extra zero bits.

2. Legacy Implementation:

   The CRC checksum can also be implemented as a series of shift left by 4, followed by a 256 array look-up. (For detailed support, contact Microchip Technology.)

4.9.6 PAUSE PULSE (OPTIONAL)

A pause pulse is an extra fill pulse which is transmitted after the CRC nibble. It is mainly used to create a SENT transmission with a constant number of clock ticks. Its length varies from 12 ticks (5 driven low plus 7 driven high) to 768 ticks (5 driven low plus 763 driven high).

Once the pause pulse is enabled, two options are used to determine the length of the pause pulse. The first one is to sync the entire single SENT message length to either ADC_SYNC or PWM. The second option is to sync the entire single SENT with a certain constant number of clock ticks, ranging from 166 to 1038.

4.9.7 PHYSICAL LAYER REQUIREMENTS

The physical layer requirements are described in this section.

1. Transmission Rate:

   Transmission bit rate is variable depending on the clock tick period, data value and clock variance. The longest transmission time is 270 clock ticks or 972 µs at a 3 µs clock time period. At, 24.7 kbps, this is also the worst transmission rate. The shortest is 154 message clocks with a 64.9 kbps rate (not including serial data).

2. Clock Tolerance:

   Variation of maximum nibble time compared to the expected time derived from the calibration pulse time at a 3 µs clock tick is ≤ 0.05 µs.

3. Electrical Interface Requirements:

   The SENT signal is seen as a nominal 5V square wave signal, but for low radiated emissions purpose, signal shaping is required. To minimize ground and supply offset effects, the receiving device must provide a regulated 5V supply and ground reference to the LX3302A SENT pin.

Figure 4-12 shows an example SENT test topology. The transmitter portion of these circuits is an example only and should not be taken as a direct implementation requirement.

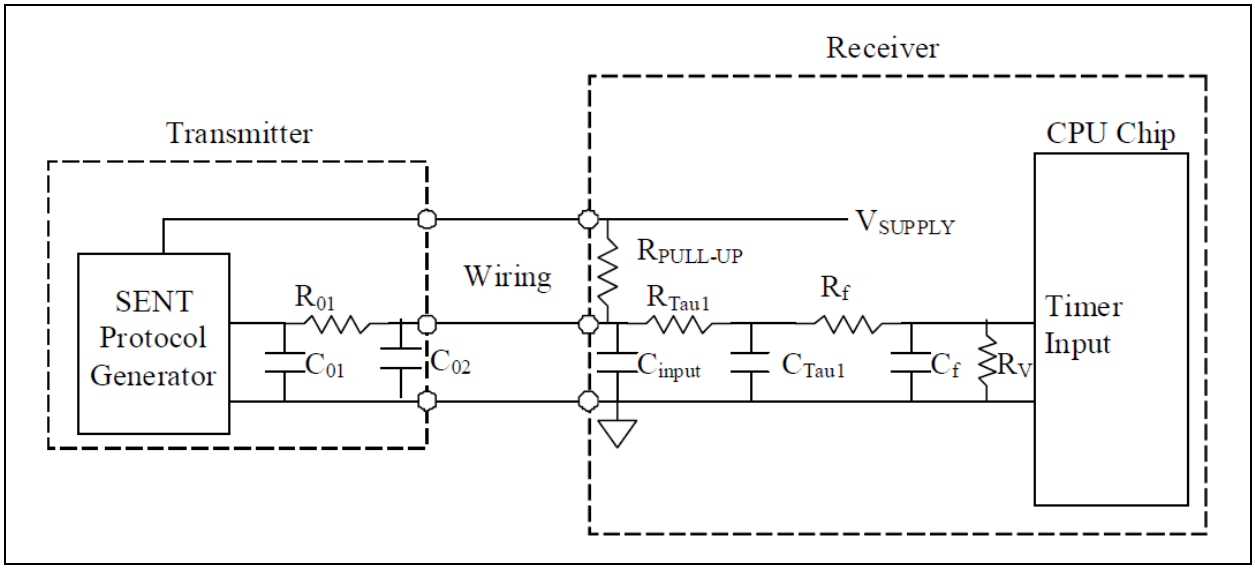


FIGURE 4-12: *Example SENT Test Topology.*

4. SENT Driver Requirements:

   The LX3302A's Single-Edge Nibble Transmissions need a push-pull pin as an output pin. The LX3302A SENT driver ensures that the signal rise and fall time requirements are met when driving into the receiver passive load. The LX3302A prevents damage from overvoltage or overcurrent conditions and switches off the SENT driver to prevent damage.

   In addition, an EMC filter consisting of a capacitor, followed by a resistor in series with the output pin, is recommended to attenuate RF energy coupled on the external signal line.

5. Fault Protection Modes:

   Short to GND. An impedance of less than 50Ω between the line and ground is considered a short to ground. Upon removal of the Fault, the LX3302A resets and resumes normal operation

   Short to Supply. An impedance of less than 50Ω between the line and V_{OUT} is considered a short to V_{IN}. Upon removal of the Fault, the LX3302A resets and resumes normal operation.

4.10 PSI5 (Peripheral Sensor Interface)

The LX3302A supports PSI5 technical specification V2.0 and substandard power train v2.0 with PSI5-AddP/CRC-tttt/n/L/H, where:

- A = Asynchronous mode
- dd = Number of data bits
- P/CRC = Error detection
- Parity or CRC
- tttt = Cycle time in µs (e.g., 500)
- L/H = Bit rate (L = 125 kbps/H = 189 kbps)

For error detection required applications, it is recommended to use status bit information to detect the error status of a sensor.

The Peripheral Sensor Interface (PSI5) is an interface developed for automotive applications. Key features include:

- Two-wire current interface
- Manchester coded digital data transmission
- High EMC immunity and low emissions
- 10 to 28-bit payload data word length
- Asynchronous mode

4.10.1 GENERAL REQUIREMENTS

The LX3302A's required input voltage to compile with the PSI5 protocol is from 4V to 11V.

Since PSI5 is an open protocol, each section of the frame format, including status, serial messaging channel, frame control, Data Region B and Data Region A, needs to have its own register to turn on and off the optional section, output any data and be able choose variable length. The goal is to ensure the LX3302A has the flexibility to meet any requirement within PSI5 protocol.

4.10.2 TRANSMISSION SEQUENCE

A “low” level is represented by the normal quiescent current consumption of the sensor. A “high” level is generated by an increased current sink of the sensor. The current modulation is detected within the Electronics Control Unit receiver. Manchester coding represents logic ‘0’ by the rising edge and logic ‘1’ by the falling edge of the sending current. Figure 4-13 shows the current level thresholds.

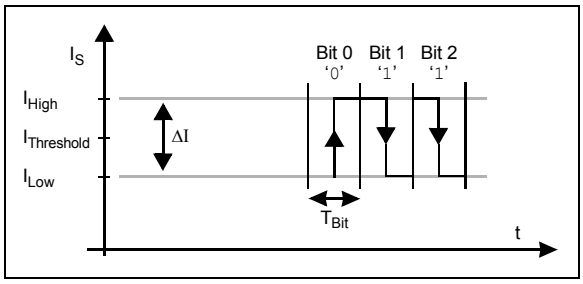


FIGURE 4-13: *Bit Encoding by Current Modulation.*

The LX3302A PSI5 Asynchronous mode operation consists of the following sequence (see Figure 4-14):

- Mandatory two Start bits: S1, S2
- Serial messaging channel: M0, M1 (optional 0 or 2-bit)
- Frame control: F0, … F[q-1] (optional 0, 1, 2, 3 or 4-bit)
- Status: E0, … E[r-1] (optional, 0, 1 or 2-bit)
- Data Region B: B0, … B[m-1] (optional 0 or scalable m = 1 to 12 with 1-bit increment)
- Mandatory Data Region A: A0, … A[n-1] (scalable n = 10 to 24 with 1-bit increment)
- Mandatory error check bit (3-bit CRC C2, C1, C3 or 1-bit parity)

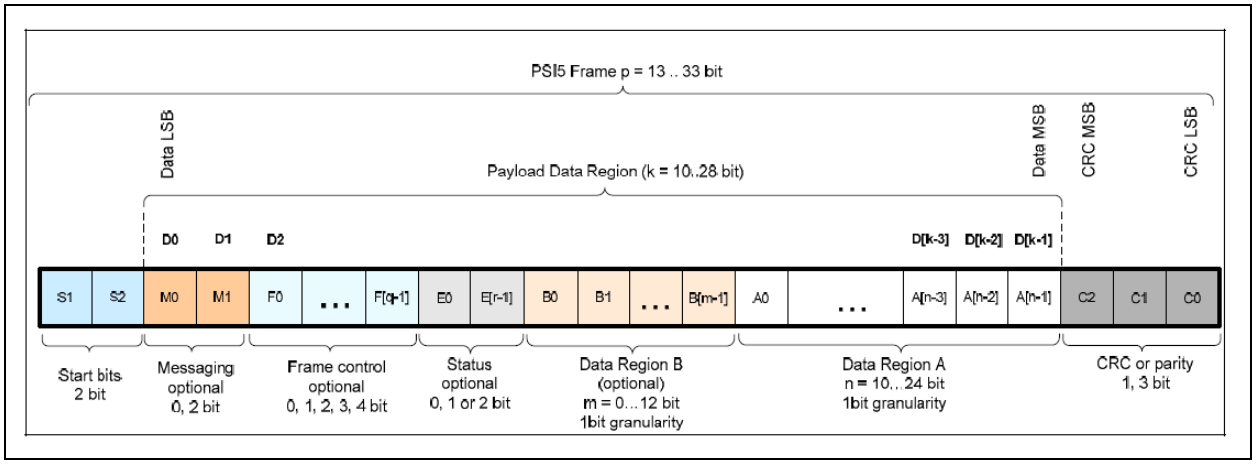


FIGURE 4-14: *PSI5 Single Frame Sequence Format.*

The single PSI5 message length ranges from 13 to 33 bits, including any optional format of payload data region, Start bits and CRC/parity. The payload data region length can range from 10 to 28 bits. One example shows what the format looks like if optional bits are enabled. If the sensor position information is 0xB54 (binary: ‘1011 0101 0100’), it will be encoded as shown in Figure 4-15.

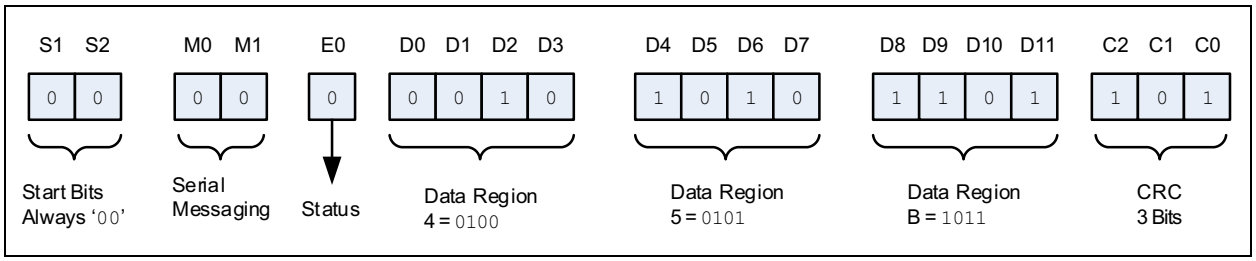


FIGURE 4-15: *Encoded PSI5 Format for 0xB54.*

4.10.2.1 Start Bits

Two Start bits are defined as '00 b' at all times and are transmitted at the beginning of the sequence.

4.10.2.2 Serial Messaging Channel

The serial messaging channel is used to transmit data messages over 18 consecutive PSI5 frames. Once it is enabled, it is transmitted following the Start bits. The serial messaging channel is optional. It has its own register and can be fully controlled to meet requirements.

Figure 4-16 shows how M1 transient serial data start from the 1st PSI5 frame and end at the 18th frame, then repeat from Frame 1. Serial data (M1) bit 8 determines the serial format. Setting this bit to '0' will select the serial format option with a 12-bit data field and an 8-bit ID.

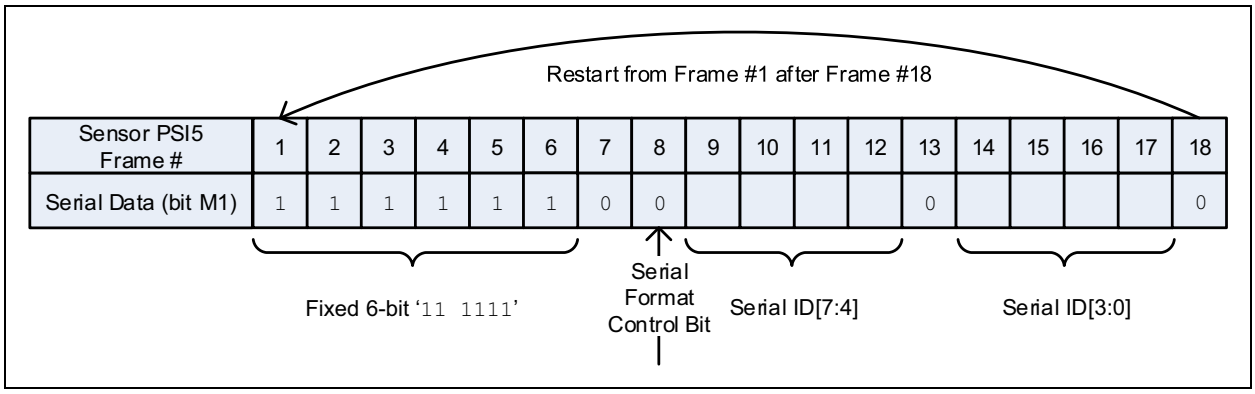


FIGURE 4-16: *Serial Data Frame Generated by [M1] When M1[8] = 0.*

Figure 4-17 shows M0 transient serial data starting from PSI5 Frame 1 to Frame 18 and then repeating from Frame 1.

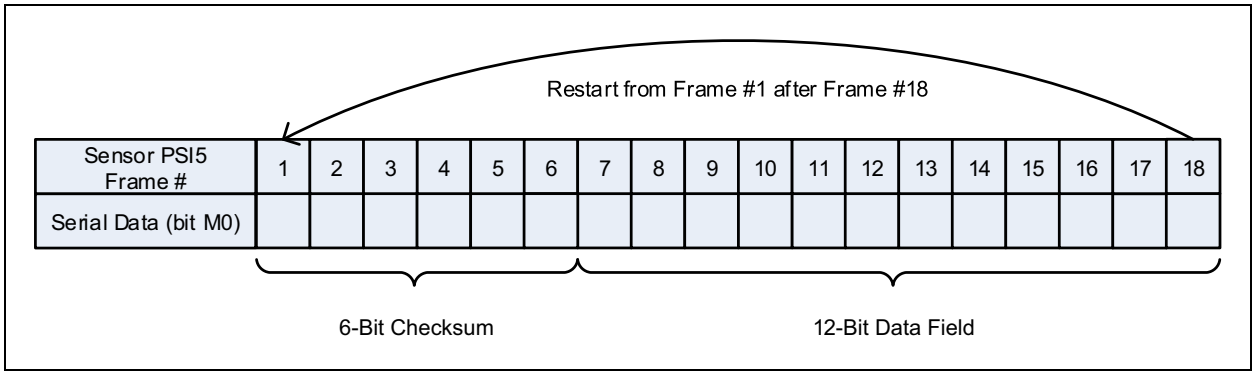


FIGURE 4-17: *Serial Data Frame Generated by [M0] When M1[8] = 0.*

If M1[8] was set to '1', the serial format with a 16-bit data field and a 4-bit ID is selected. Figure 4-18 and Figure 4-19 show M0 and M1 being formatted.

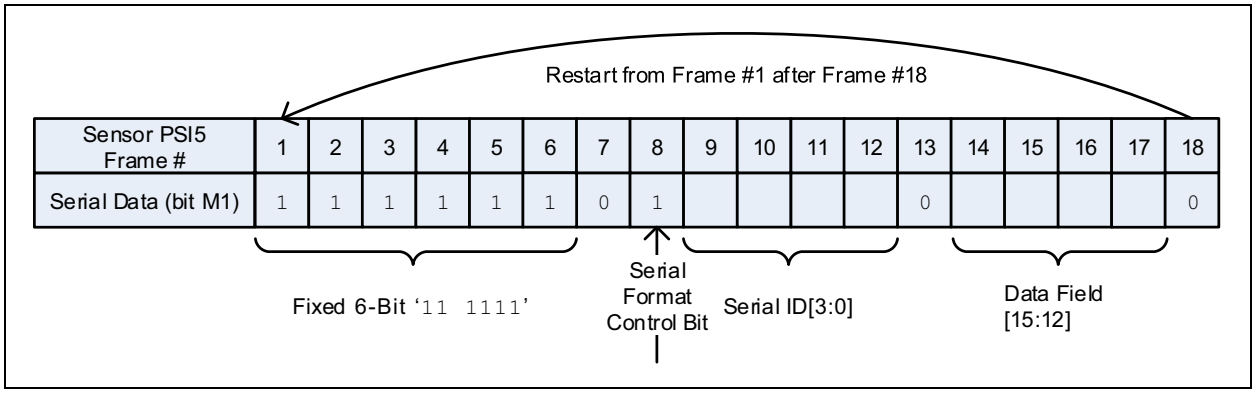


FIGURE 4-18: *Serial Data Frame Generated by [M1] When M1[8] = 1.*

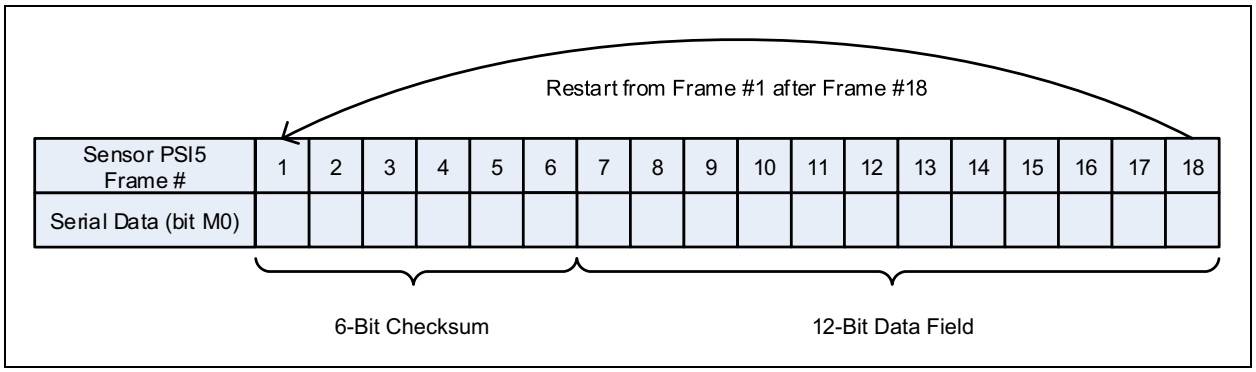


FIGURE 4-19: *Serial Data Frame Generated by [M0] When M1[8] = 1.*

The generator polynomial of the 6-bit checksum for both serial formats described in Figure 4-18 and Figure 4-19 is $g(x) = 1 + x^3 + x^4 + x^6$ with a binary initialization value of '010101'. The CRC value is derived from the serial messaging contents of sensor PSI5 Frames 7 to 18. The bits are read into a newly generated message data word, starting with the serial data bit M0 of sensor PSI5 Frame 7 and ending with the serial data bit M1 of sensor PSI5 Frame 18.

For CRC generation, the transmitter extends the message data by six zeros. This augmented data word is fed into the shift registers of the CRC check. When the last zero of the augmentation is pending on the input adder, the shift registers contain the CRC checksum. These six check bits are transmitted MSB first: [C5, C4, ... C0]. The following figure shows the reading order.

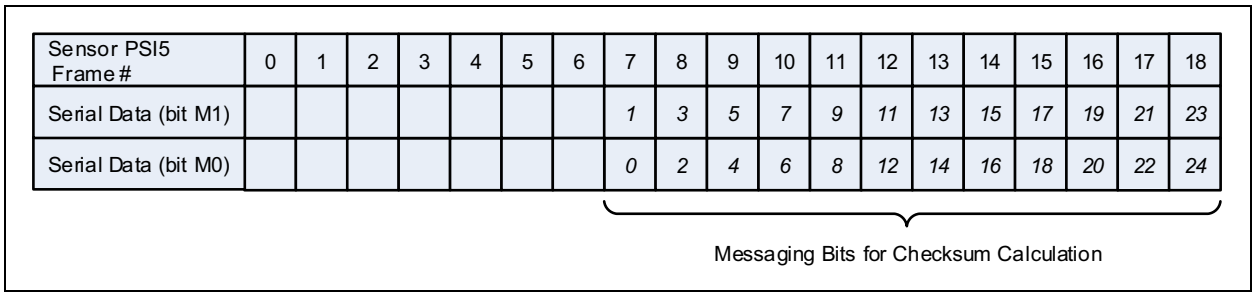


FIGURE 4-20: *Read Order of Serial Data Checksum.*

Note:	The serial data checksum is not the same as the 3-bit checksum of the total PSI5 frame.

4.10.3 FRAME CONTROL

Frame control bits are used to indicate the type of frame or data content, or to identify the sensor. Once this function is enabled, the information is transmitted following the serial message channel bits. Frame control is optional; it has its own register. The length of the frame control can be selected from 1 bit to 4 bits, with a 1-bit increment.

4.10.4 STATUS BITS

Status bits are used to indicate if an error has occurred on the sensor. Once this function is enabled, it is transmitted following the frame control bits. Status bits are optional and have their own register. The length of the status is selectable and can be either 1 bit or 2 bits.

4.10.5 DATA REGION B

Data Region B serves as an additional data region. Once it is enabled, it is transmitted following the status bits, ordered from LSB to MSB. Data Region B is optional; it has its own register. Once it is enabled, the length of Data Region B can be selected from 1 bit to 12 bits, with a 1-bit increment.

4.10.6 DATA REGION A

Data Region A is the main data region. It is transmitted following Data Region B and ordered from LSB to MSB. Data Region A is mandatory; it has its own register. The length of Data Region A can be selected from 10 bits to 12 bits, with a 1-bit increment.

4.10.7 INITIALIZATION

Sensor identification data are sent after each Power-on Reset. The LX3302A supports PSI5 initialization via serial channel messaging.

For immediate access to measurement data, identification data are transmitted in parallel to sensor data via serial channel bits, M0 and M1. The sensor immediately starts parallel transmission of measurement and sensor identification data.

4.10.8 META INFORMATION

At the very beginning of the identification phase, a “meta information” header is transmitted at least once indicating the PSI5 version and the method used for identification data transmission. Irrespective of the applied identification procedure, the header data field is sent in status data format (10-bit value out of Data Range 3).

The meta code of the LX3302A is `0111` = PSI5 2.0 serial channel initialization.

4.10.9 ERROR CHECK

Error detection in PSI5 transmission is realized by a single bit even parity or 3-bit CRC [C2 C1 C0]. It can be selected by a Toggle register bit.

Once the 3-bit CRC is selected, the generator polynomial of the CRC is ($x^3 + x + 1$) with a binary CRC initialization value, ‘`111`’. The transmitter extends the data bits by three zeros as MSBs. This augmented data word is fed into the shift register CRC check as LSB first. The Start bits are ignored in this check. When the last zero of the augmentation is pending on the input adder, the shift registers contain the CRC checksum. These three check bits are transmitted in reverse order (MSB first: C2, C1, C0).

4.10.10 PSI5 SENSOR POWER-ON REQUIREMENT

A maximum start-up time is specified to make sure the LX3302A sinks to quiescent current (see Figure 4-21).

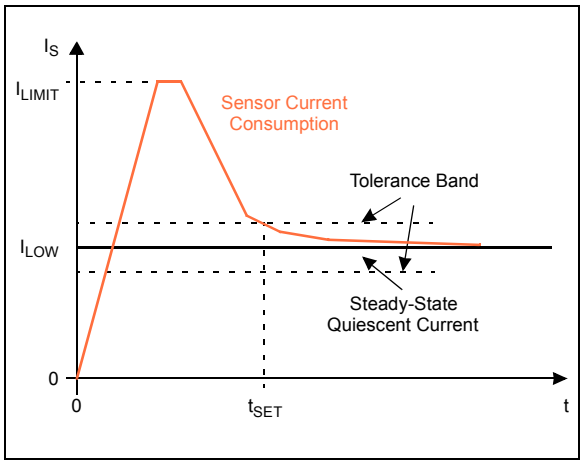


FIGURE 4-21: *Current Settling During Start-Up.*

4.10.11 PSI5 SENSOR DAMPING BEHAVIOR

The LX3302A's PSI5 pin damping behavior is described in Figure 4-22. The complex impedance, Z_S, consists of an equivalent resistance, $R_{eq,S}$, an equivalent capacitance, $C_{eq,S}$, connected in serial and a given frequency range of 10 kHz to 2000 kHz.

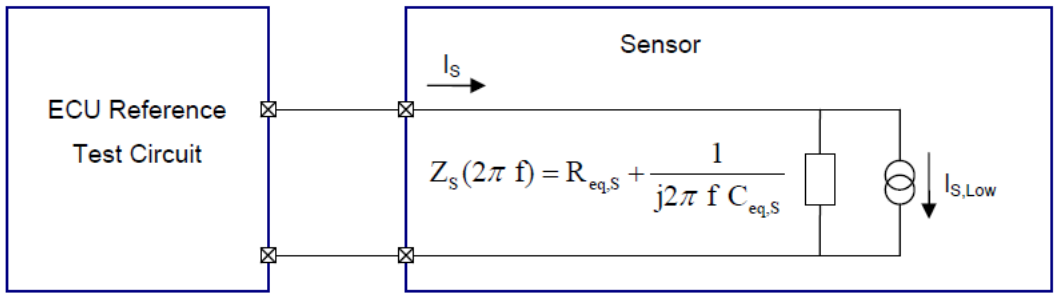


FIGURE 4-22: *LX3302A Damping Behavior Model.*

4.10.12 PSI5 SENSOR CURRENT REQUIREMENT

The LX3302A's PSI5 sensor current requirement is described in Figure 4-23.

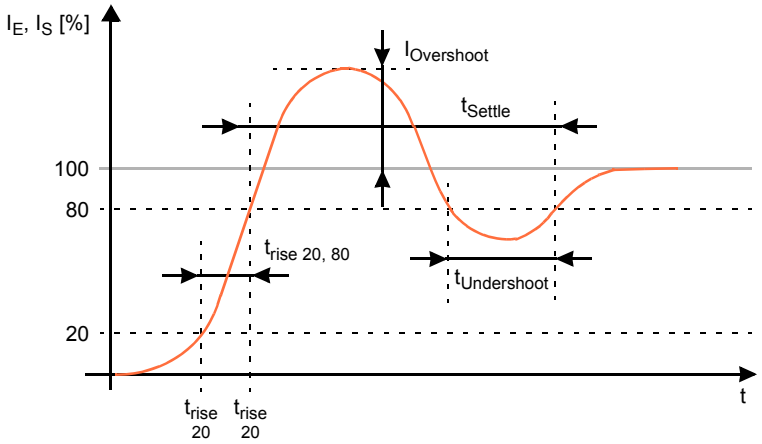


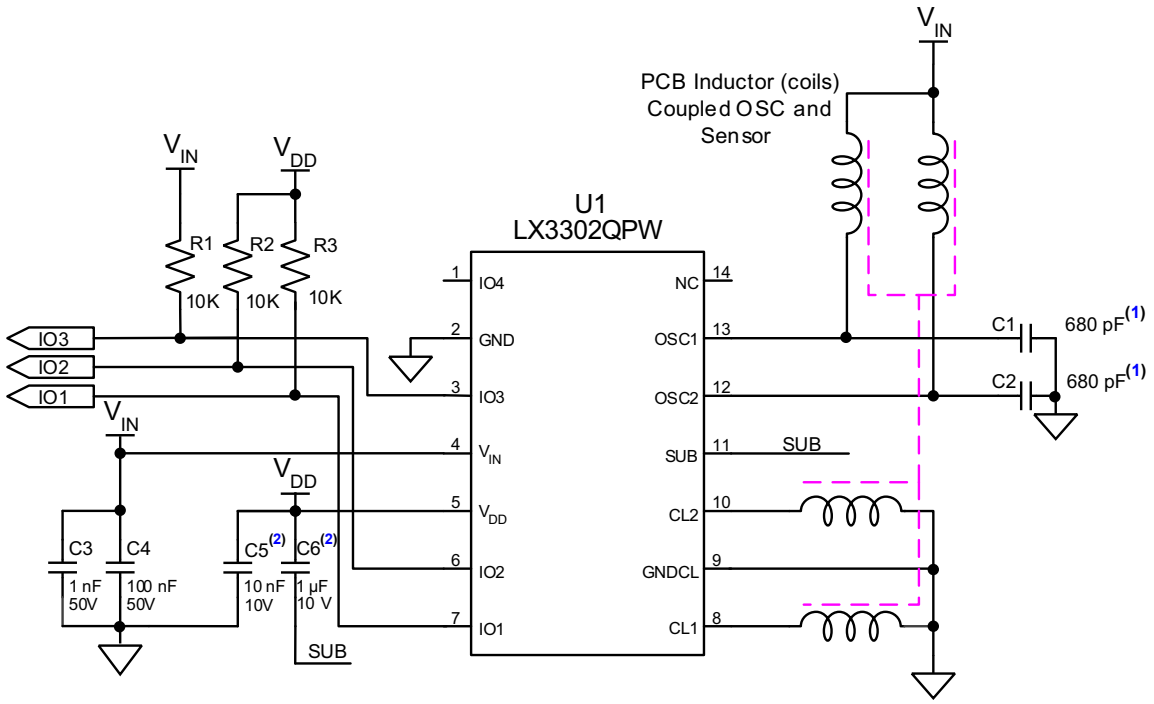
FIGURE 4-23: *LX3302A PSI5 Current Model.*

4.10.13 HIGH-VOLTAGE LDO

The LX3302A includes an internal voltage regulator that provides the core operating voltage for the chip and the power for external components, such as pull-up resistors. Overcurrent protection is implemented with the regulator. Decoupling caps are required to ensure high-performance analog measurements (minimum 100 nF, recommended value is 1 µF). V_{DD} is pretrimmed at the factory.

5.0 REFERENCE SCHEMATICS

The LX3302A 14-pin reference schematic is shown in Figure 5-1.



Note 1: Cap value is for reference only. The user must select it to set the desired oscillation frequency. C0G or NP0-type, 50V, low-ESR at 1 MHz to 6 MHz caps should be used.

2: C5 is recommended for digital output applications (PWM/SENT/PSI5) and C6 is recommended for analog output application.

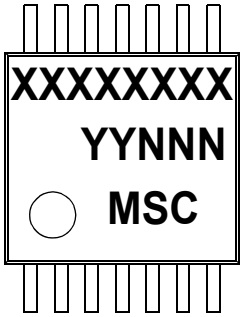
FIGURE 5-1: *LX3302A 14-Pin Reference Schematic.*

NOTES:

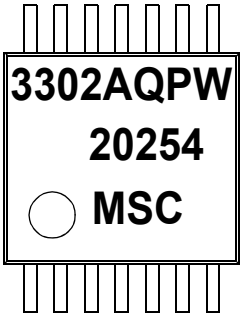
6.0 PACKAGING SPECIFICATIONS

6.1 Package Marking Information

14-Lead TSSOP (4.4 mm body)



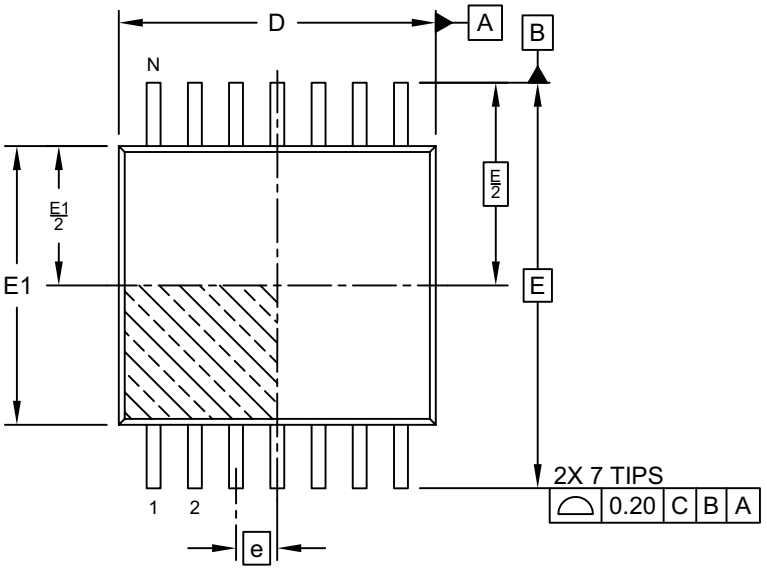
Example



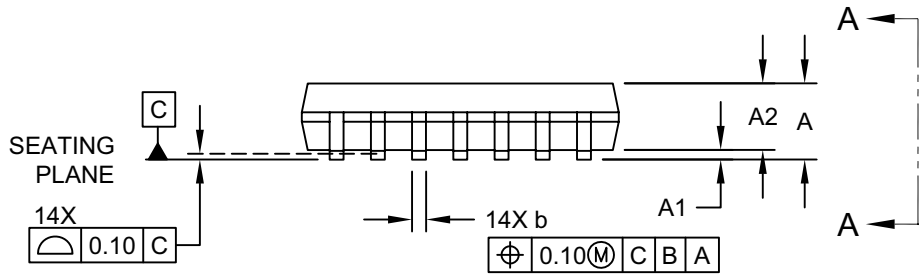
Legend:	XX...X	Device-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	NNN	Alphanumeric traceability code
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
Note:	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.	

14Lead Thin Shrink Small Outline Package [ST] 4.4 mm Body [TSSOP]

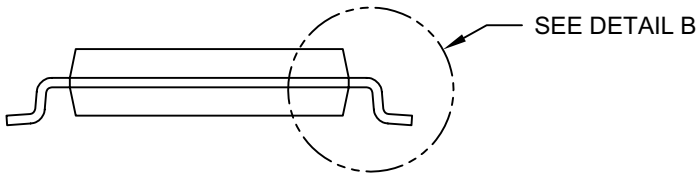
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW

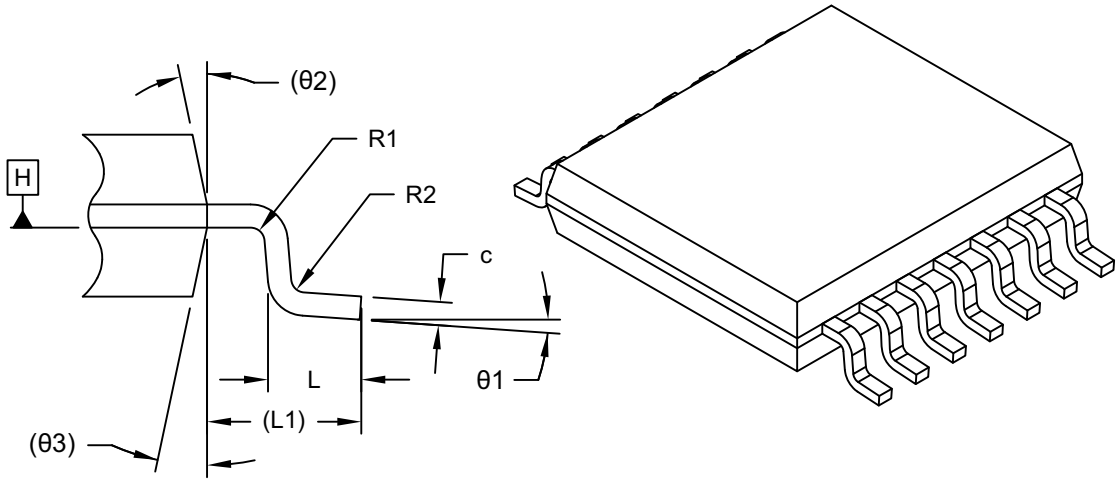


VIEW A–A

Microchip Technology Drawing C04-087 Rev D Sheet 1 of 2

14Lead Thin Shrink Small Outline Package [ST] 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



DETAIL B

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		14	
Pitch	e		0.65 BSC	
Overall Height	A	–	–	1.20
Standoff	A1	0.05	–	0.15
Molded Package Thickness	A2	0.80	1.00	1.05
Overall Length	D	4.90	5.00	5.10
Overall Width	E		6.40 BSC	
Molded Package Width	E1	4.30	4.40	4.50
Terminal Width	b	0.19	–	0.30
Terminal Thickness	c	0.09	–	0.20
Terminal Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Lead Bend Radius	R1	0.09	–	–
Lead Bend Radius	R2	0.09	–	–
Foot Angle	θ1	0°	–	8°
Mold Draft Angle	θ2	–	12° REF	–
Mold Draft Angle	θ3	–	12° REF	–

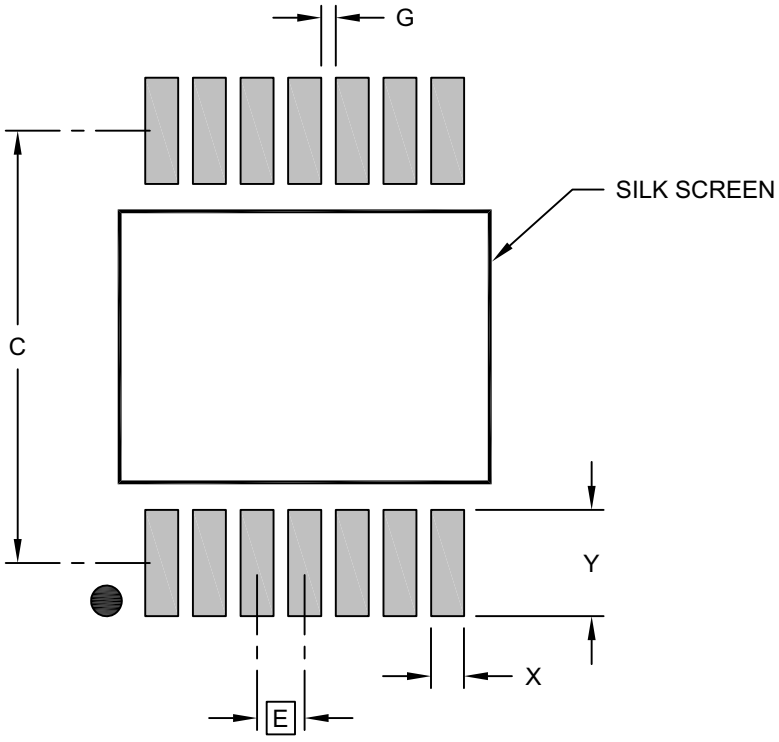
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-087 Rev D Sheet 2 of 2

14Lead Thin Shrink Small Outline Package [ST] 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C		5.90	
Contact Pad Width (Xnn)	X			0.45
Contact Pad Length (Xnn)	Y			1.45
Contact Pad to Contact Pad (Xnn)	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2087 Rev D

APPENDIX A: REVISION HISTORY

Revision B (June 2020)

The following is the list of modifications:

1. Updated **Table 3-1**.
2. Updated **Section 4.6.1, V_{IN} EEMode**.
3. Updated **Section 4.6.2, Digital EEMode**.
4. Updated **Table 4-2**.

Revision A (January 2020)

- Initial release of this document.
- This document replaces *"LX3302A Data Sheet – Inductive Sensor Interface IC with Embedded MCU"* (LX3302A V1.4/09.19, Microsemi, 2016-2019), with the following updates:
  - Updated **Section 2.0 "Pin Descriptions"**.
  - Updated Table 3-1 in **Section 3.0 "Configuration EEPROM"**.
  - Updated **Section 3.37 "IOSEL (Fifteen Bits, W25[15:1])"**.
  - Updated **Section 4.2 "Oscillator"**.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO. - XX[1]	Examples:
Device: Tape and Reel Option	a) LX3302AQPW: -40°C to +150°C Ambient Temperature, RoHS2 Compliant, Pb-free MSL1, AEC-Q100 Grade 0, 14-Lead TSSOP package
Device: LX3302AQPW: Inductive Sensor Interface IC with Embedded MCU	b) LX3302AQPW-TR: -40°C to +150°C Ambient Temperature, RoHS2 Compliant, Pb-free MSL1, AEC-Q100 Grade 0, 14-Lead TSSOP package, Tape and Reel
Tape and Reel: Blank = Standard Packaging (Tube); TR = Tape and Reel[1]	**Note 1:** Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with Microchip for package availability with the Tape and Reel option.

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Trademarks

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