NCS2300

Headset Detection Interface

The NCS2300 is a compact and cost effective headset detection interface IC. It integrates a comparator, OR gate, and N−channel MOSFET to detect the presence of a stereo headset with a microphone. Pull−up resistors for the detection pins are internalized. A built in resistor divider provides the reference voltage for detecting the left audio channel. The logic low output of the OR gate indicates the headset has been connected properly. The NCS2300 comes in a space saving UDFN6 package (1.2 x 1.0 mm).

Features

- Supply Voltage: 1.6 V to 2.75 V
- Low Quiescent Supply Current: 7.5 μA typical @ V_{DD} = 1.8 V
- Integrated Resistors, Comparator, OR Gate, and N−Channel MOSFET
- Space Saving UDFN6 Package
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

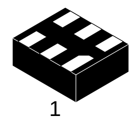
Typical Applications

- Cell Phones, Smartphones
- Tablets
- Notebooks

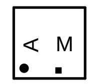
ON Semiconductor®

http://onsemi.com

MARKING DIAGRAM

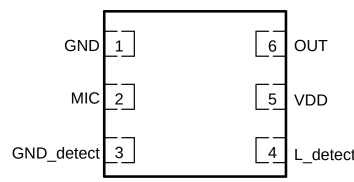


UDFN6
MU SUFFIX
CASE 517AA



A = Specific Device Code
M = Date Code
▪ = Pb−Free Package

PIN DIAGRAM



Top View

ORDERING INFORMATION

Device	Package	Shipping†
NCS2300MUTAG	UDFN6 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

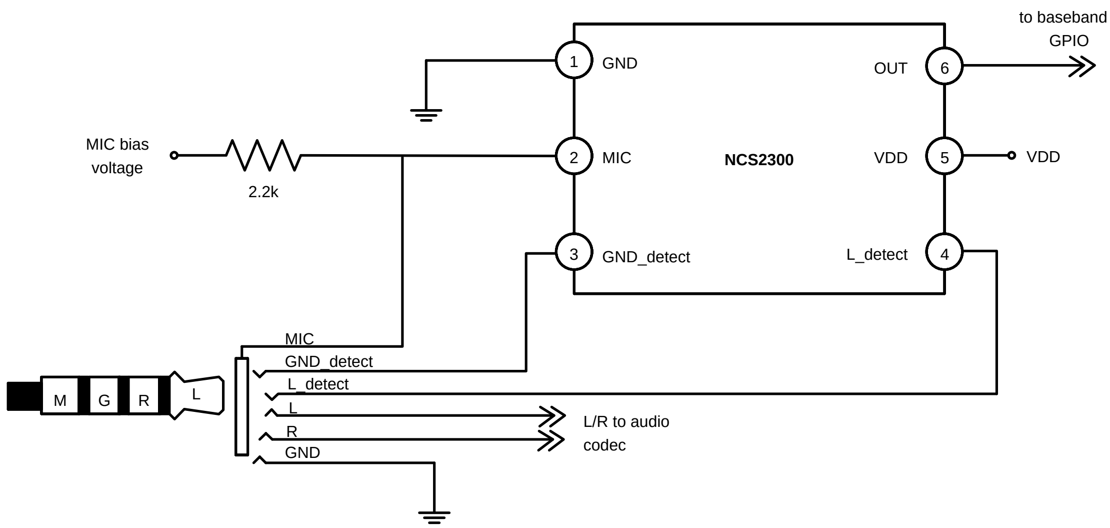


Figure 1. Typical Application Schematic

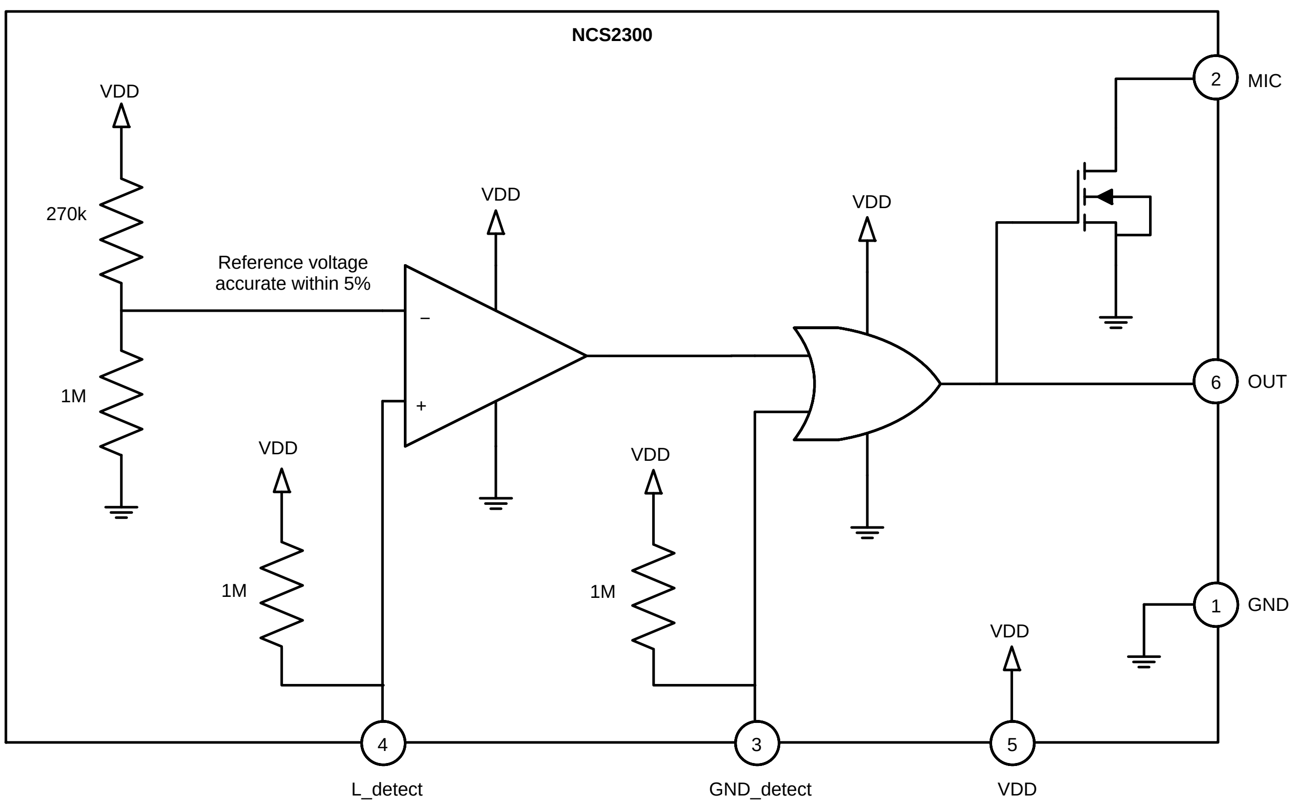


Figure 2. Block Diagram

Table 1. OUTPUT LOGIC

Inputs		Outputs		Headset
L_detect	GND_detect	OUT	MIC	
0	0	0	1 (external pull−up)	Detected
0	1	1	0	Not Detected
1	0	1	0	
1	1	1	0	

Table 2. PIN DESCRIPTION

Pin	Name	Type	Description
1	GND	Power	GND is connected to the system ground.
2	MIC	Output	The open drain MIC output controls the bias on the MIC line. When the headset is not present, MIC is pulled low. When the headset is present, MIC is pulled up to the MIC bias voltage through an external pull−up resistor.
3	GND_detect	Input	GND_detect is the OR gate input. An internal 1 MΩ pull−up resistor pulls this pin high when the headset is not present.
4	L_detect	Input	L_detect is the comparator input. An internal 1 MΩ pull−up resistor pulls this pin high when the headset is not present.
5	VDD	Power	VDD is connected to the system power supply. A 0.1 μF decoupling capacitor is recommended as close as possible to this pin.
6	OUT	Output	OUT is a logic output that indicates whether the headset has been properly connected. OUT will be logic low only when GND_detect and L_detect are low.

Table 3. ABSOLUTE MAXIMUM RATINGS (Note 1)

Rating	Symbol	Value	Unit
Supply Voltage Range	V_{DD}	0 to 2.75	V
L_detect Input Pin Voltage Range	V_{L_detect}	−0.1 to V_{DD} + 0.1	V
GND_detect Input Pin Voltage Range	V_{GND_detect}	−0.1 to V_{DD} + 0.1	
MIC Output Pin Voltage Range	V_{MIC}	0 to 6.0	V
Maximum MIC Current	I_{MIC}	2	mA
Maximum Junction Temperature	$T_{J(max)}$	+125	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
ESD Capability (Note 2) Human Body Model Machine Model	 ESD_{HBM} ESD_{MM}	 5000 250	V
Latch−up Current (Note 3)	I_{LU}	800	mA
Moisture Sensitivity Level (Note 4)	MSL	Level 1	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
2. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per AEC−Q100−002 (JEDEC standard: JESD22−A114)
   ESD Machine Model tested per AEC−Q100−003 (JEDEC standard: JESD22−A115)
3. Latch−up Current tested per JEDEC standard: JESD78
4. Moisture Sensitivity Level tested per IPC/JEDEC standard: J – STD – 020A

Table 4. OPERATING RANGES

Rating	Conditions	Symbol	Min	Typ	Max	Unit
Power Supply Voltage		V_{DD}	1.6	1.8	2.75	V
Input Voltage	L_detect and GND_detect pins	V_{IN}	0		V_{DD}	V
Input Transition Rise or Fall Rate	GND_detect pin	$\Delta t / \Delta V$	0		10	ns/V
Bias Voltage on MIC Output		V_{MIC}	0		3.0	V
Ambient Temperature		T_A	−40		85	°C
Junction Temperature		T_J	−40		125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Table 5. ELECTRICAL CHARACTERISTICS Typical values are referenced to T_A = 25°C, V_{DD} = 1.8 V, unless otherwise noted. Min/max values apply from T_A = −40°C to 85°C, unless otherwise noted. (Note 5)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
SUPPLY CHARACTERISTICS						
Quiescent Supply Current	V_{GND_detect} = 1.8 V or 0 V	I_{DD}		7.5	12	μA
INPUT CHARACTERISTICS OF L_DETECT						
Voltage Input Low	V_{DD} = 1.8 V	V_{IL}			1.33	V
Voltage Input High	V_{DD} = 1.8 V	V_{IH}	1.5			V
Propagation Delay to OUT	C_{out} = 15 pF, GND_detect = 0 V, L_detect = 1.31 V to 1.52 V	t_{pLH}, t_{pHL}		480		ns
Low Voltage Input Leakage	V_{L_detect} = 0 V	I_{IL}		1.8		μA
High Voltage Input Leakage	V_{L_detect} = 1.8 V	I_{IH}		500		pA
Input Capacitance	f = 1 MHz	C_{IN}		3		pF
INPUT CHARACTERISTICS OF GND_DETECT						
Voltage Input Low	V_{DD} = 1.8 V	V_{IL}			0.63	V
Voltage Input High	V_{DD} = 1.8 V	V_{IH}	1.17			V
Propagation Delay to OUT	C_{out} = 15 pF, R_L = 1 MΩ, L_detect = 0 V, GND_detect = 0 to 1.8 V	t_{pLH}, t_{pHL}		550		ps
Low Voltage Input Leakage	V_{GND_detect} = 0 V	I_{IL}		1.8		μA
High Voltage Input Leakage	V_{GND_detect} = 1.8 V	I_{IH}		500		pA
Input Capacitance	f = 1 MHz	C_{IN}		3		pF
OUTPUT CHARACTERISTICS OF OUT						
Voltage Output Low	V_{DD} = 1.8 V, I_{OH} = 0.1 mA	V_{OL}			0.10	V
Voltage Output High	V_{DD} = 1.8 V, I_{OH} = −0.1 mA	V_{OH}	1.70			V
Rise Time	C_{OUT} = 15 pF, R_L = 1 MΩ	t_{rise}		7		ns
Fall Time	C_{OUT} = 15 pF, R_L = 1 MΩ	t_{fall}		4		ns
CHARACTERISTICS OF MIC						
Drain−Source On Resistance of NMOS	V_{DD} = 1.8 V, I_{MIC} = 1 mA	$R_{DS(on)}$		0.9	1.4	Ω

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Guaranteed by characterization and/or design.

TYPICAL CHARACTERISTICS

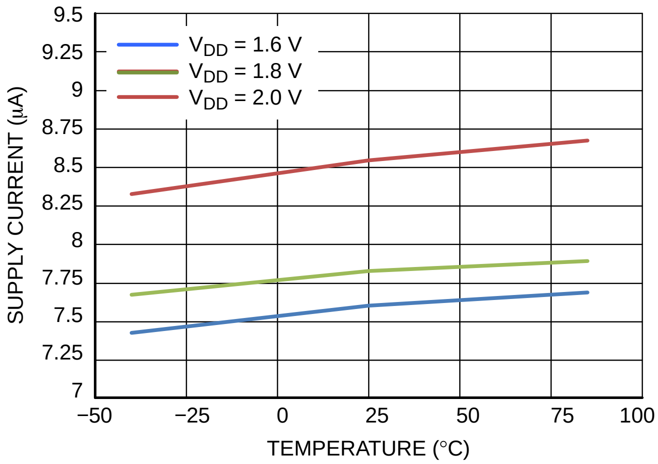


Figure 3. Supply Current vs. Temperature

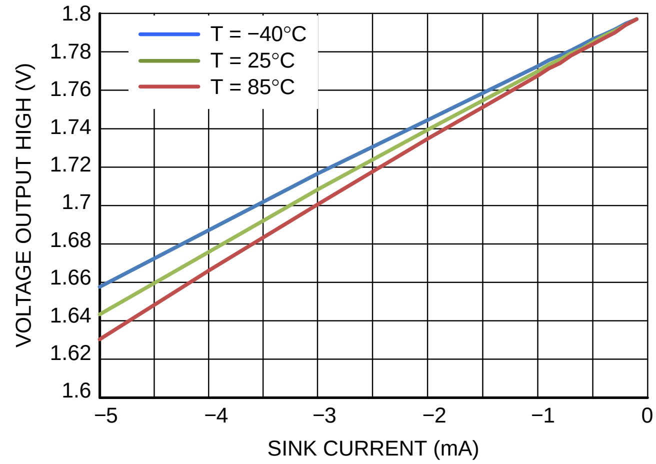


Figure 4. V_{OH} vs. I_{OH} of OUT Pin

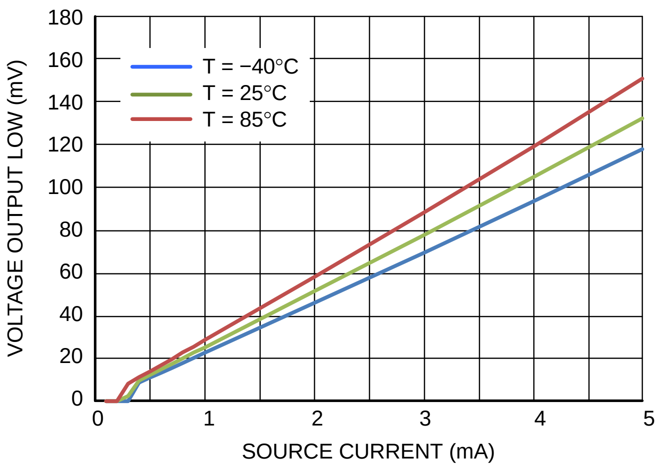


Figure 5. V_{OL} vs. I_{OL} of OUT Pin

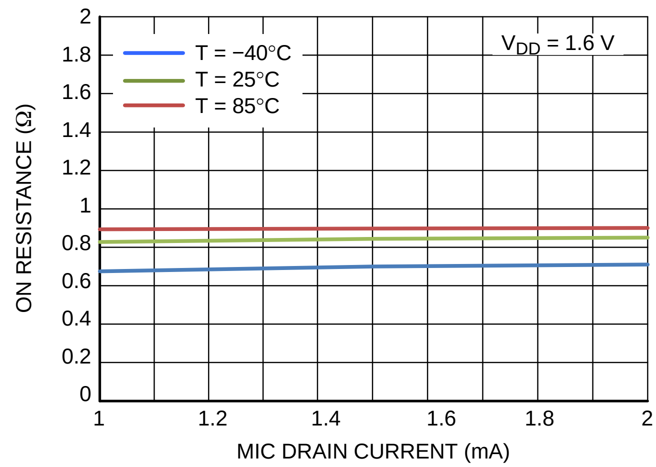


Figure 6. On Resistance vs. Drain Current at V_{DD} = 1.6 V

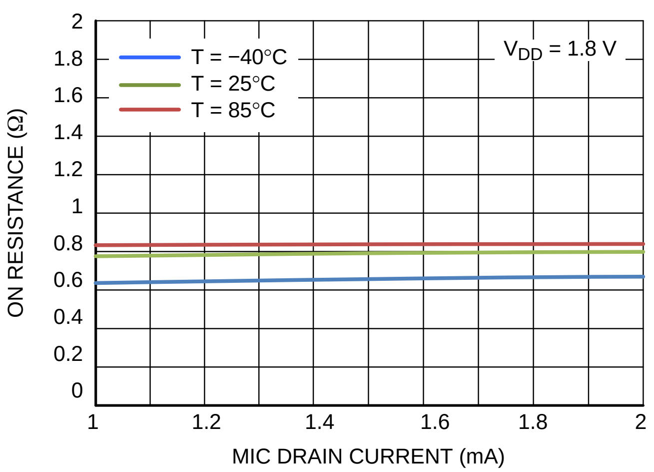


Figure 7. On Resistance vs. Drain Current at V_{DD} = 1.8 V

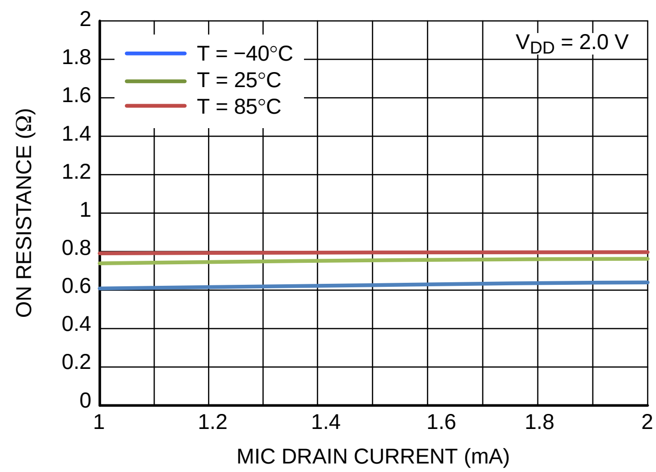


Figure 8. On Resistance vs. Drain Current at V_{DD} = 2.0 V

TYPICAL CHARACTERISTICS

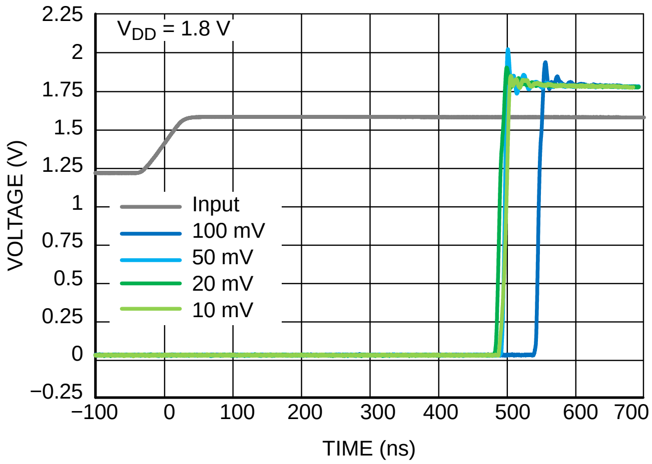


Figure 9. Low to High Propagation to OUT with Changing Input Overdrive of L_detect

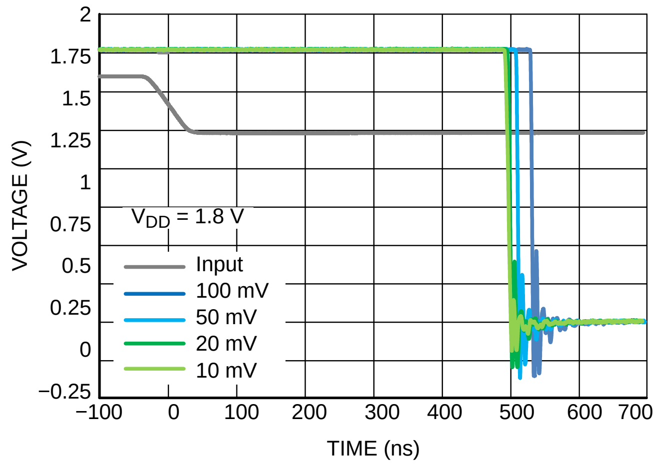


Figure 10. High to Low Propagation to OUT with Changing Input Overdrive of L_detect

APPLICATIONS INFORMATION

SUPPLY VOLTAGE

The NCS2300 works with a wide range of supply voltages from 1.6 V to 2.75 V. A 0.1 μF decoupling capacitor should be placed as close as possible to the VDD pin. Since the NCS2300 has built in latch-up immunity up to 800 mA, series resistors are not recommended on VDD.

AUDIO JACK DETECTION

The NCS2300 is designed to simplify the detection of a stereo audio connector with a microphone contact. When the headset is not connected, the internal pull−up resistors on L_detect and GND_detect pull those pins high. When the headset is connected to the switched audio jack, the headset ground and left audio channel trigger L_detect and GND_detect to logic low.

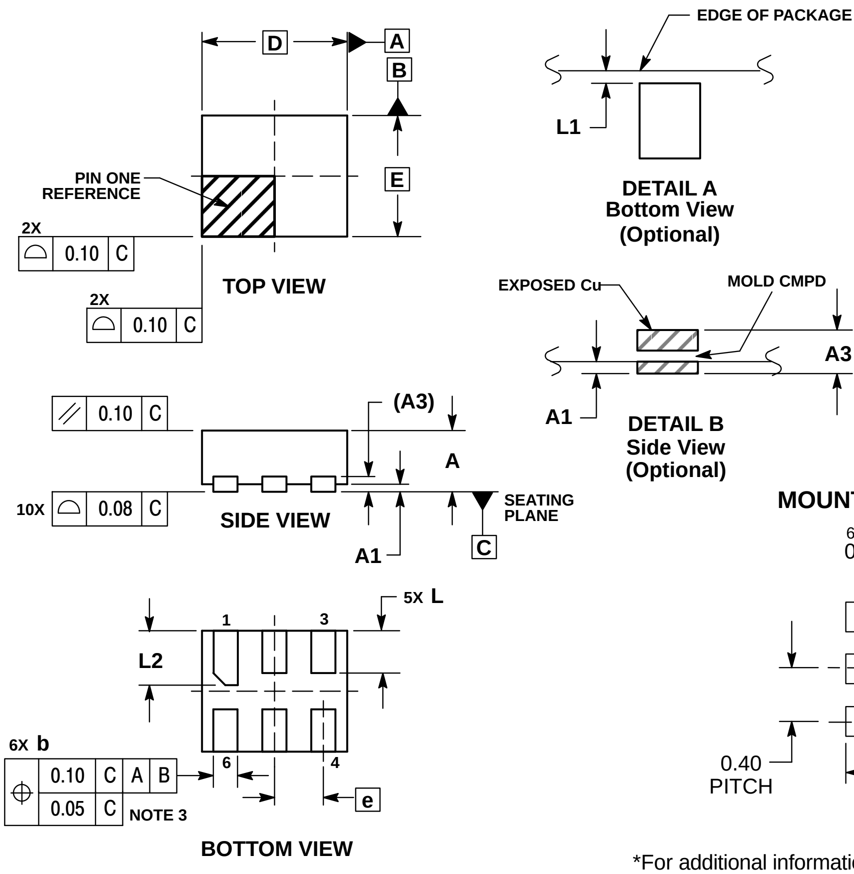
The NCS2300 can work with either the CTIA or OMTP standard. In order to support both standards simultaneously, a cross point switch and additional circuitry is necessary to detect and swap the ground and microphone pins.

MIC PIN BIASING

The typical application schematic in Figure 1 shows the recommended 2.2 kΩ pull−up resistor to the MIC bias voltage. The MIC bias voltage can exceed VDD and can go as high as 3 V. While the headset is not detected, the internal NMOS transistor is enabled to mute the MIC signal. In the typical application scenario with a 2.2 kΩ pull−up to a 2.3 V MIC bias voltage, the MIC pin is pulled near 1 mV when the headset is not present. The internal NMOS transistor is optimized to sink up to 2 mA of current, allowing some flexibility in the selection of the pull−up resistor and MIC bias voltage.

PACKAGE DIMENSIONS

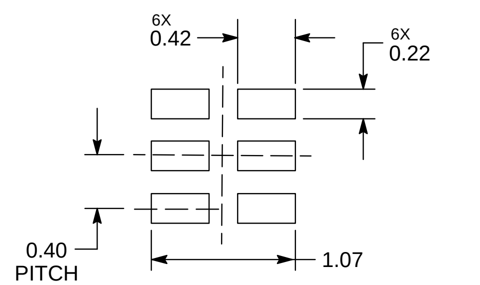
UDFN6, 1.2x1.0, 0.4P
CASE 517AA
ISSUE D



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 mm FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.127 REF	
b	0.15	0.25
D	1.20 BSC	
E	1.00 BSC	
e	0.40 BSC	
L	0.30	0.40
L1	0.00	0.15
L2	0.40	0.50

MOUNTING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81−3−5817−1050

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative