Click here for production status of specific part numbers.

MAXM17552

4V to 60V, 100mA, Compact Step-Down Power Module

General Description

The Himalaya series of voltage regulator ICs and power modules enable cooler, smaller, and simpler power-supply solutions. The MAXM17552 is a high-efficiency, synchronous, step-down DC-DC power module with integrated controller, MOSFETs, compensation components, and inductor that operates over a wide input-voltage range. The module operates from 4V to 60V input voltage and delivers up to 100mA output current over a programmable output voltage from 0.9V to 5.5V. The module significantly reduces design complexity, manufacturing risks and offers a true "plug and play" power supply solution, reducing the time-to-market.

The MAXM17552 employs peak-current-mode control architecture. To reduce input inrush current, the device offers a soft-start feature including the default soft-start time of 5.1ms.

The MAXM17552 is available in a low profile, compact 10-pin 2.6mm x 3mm x 1.5mm uSLIC™ package.

Applications

- Industrial Sensors and Encoders
- 4mA–20mA Current-Loop Powered Sensors
- LDO Replacement
- HVAC and Building Control
- Battery-Powered Equipment

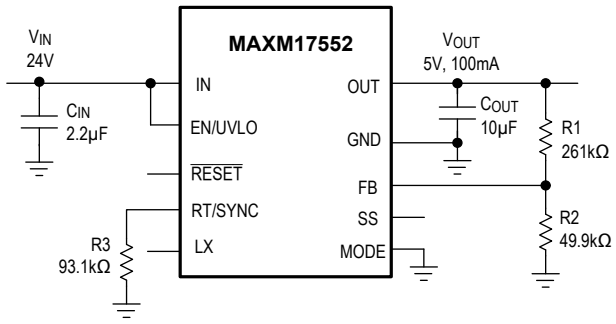
uSLIC is a trademark of Maxim Integrated Products, Inc.

Benefits and Features

- Easy to Use
  - Wide 4V to 60V Input
  - Adjustable 0.9V to 5.5V Output
  - ±1.75% Feedback-Voltage Accuracy
  - Up to 100mA Output Current
  - Internally Compensated
  - All Ceramic Capacitors
- High Efficiency
  - Fixed-Frequency PWM
  - Pulse Frequency Modulation (PFM) Mode to Enhance Light-Load Efficiency
  - Shutdown Current as Low as 1.2µA (typ)
- Flexible Design
  - Programmable Soft-Start and Prebias Startup
  - Open-Drain Power Good Output ($\overline{\text{RESET}}$ Pin)
  - Programmable EN/UVLO Threshold
- Rugged
  - Complies with CISPR22 (EN55022) Class B Conducted and Radiated Emissions.
  - Passes Drop, Shock, and Vibration Standards - JESD22–B103, B104, B111
- Robust Operation
  - Hiccup Overcurrent Protection
  - Overtemperature Protection
  - -40°C to +125°C Ambient OperatingTemperature/ -40°C to +150°C Junction Temperature

***Ordering Information* appears at end of data sheet.**

Typical Application Circuit



Absolute Maximum Ratings

IN, EN/UVLO to GND ..... -0.3V to +70V
LX to GND ..... -0.3V to IN +0.3V
OUT to GND ..... -0.3V to +7V
RT/SYNC, SS, FB, MODE to GND ..... -0.3V to +6V
$\overline{\text{RESET}}$ ..... -0.3V to +18V

Output Short-Circuit Duration ..... Continuous
Junction Temperature (Note 1) ..... +150°C
Storage Temperature Range ..... -55°C to +125°C
Lead Temperature (soldering, 10s) ..... +260°C
Soldering Temperature (reflow) ..... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

PACKAGE TYPE: 10-PIN uSLIC	
Package Code	M102A3+1
Outline Number	**21-100094**
Land Pattern Number	**90-100027**
THERMAL RESISTANCE FOUR-LAYER BOARD (Note 2)	
Junction to Ambient (θ_{JA})	30.6°C/W

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Note 1: Junction temperature greater than +125°C degrades operating lifetimes

Note 2: Package thermal resistance measured on Evaluation Board, Natural convection. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(V_{IN} = 24V, V_{GND} = 0V, V_{FB} = 0.85V, $V_{EN/UVLO}$ = 1.5V, RT/SYNC = 69.8kΩ, LX = SS = $\overline{RESET}$ = unconnected; MODE = GND T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to GND, unless otherwise noted) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT SUPPLY (IN)						
Input Voltage Range	V_{IN}		4		60	V
Input Shutdown Current	I_{IN-SH}	$V_{EN/UVLO}$ = 0V, T_A = +25°C	0.67	1.2	2.25	µA
Input Supply Current	I_{Q-PWM}	V_{FB} = Normal switching, V_{MODE} = 0V, V_{OUT} = 3.3V	800	1100	1950	µA
	I_{Q-PFM}	V_{MODE} = unconnected	30	62	110	µA
MODULE OUTPUT PIN (OUT)						
Output Line Regulation Accuracy		V_{IN} = 4V to 60V, V_{OUT} = 3.3V, I_{LOAD} = 0		0.1		mV/V
Output Load Regulation Accuracy		Tested with I_{OUT} = 0A and 100mA V_{OUT} = 3.3V		0.3		mV/mA
ENABLE/UVLO (EN/UVLO)						
EN/UVLO Threshold	V_{ENR}	$V_{EN/UVLO}$ rising	1.2	1.25	1.3	V
	V_{ENF}	$V_{EN/UVLO}$ falling	1.1	1.15	1.2	V
	$V_{EN-TRUESD}$	$V_{EN/UVLO}$ falling, true shutdown		0.72		V
EN/UVLO Leakage Current	I_{EN}	$V_{EN/UVLO}$ = 1.3V, T_A = +25°C	-100		+100	nA
LX						
LX Leakage Current	I_{LX-LKG}	V_{EN} = 0V, T_A = +25°C, V_{LX} = (V_{GND} + 1V) to (V_{IN} - 1V) V_{OUT} = float	-1		+1	µA
SOFT-START (SS)						
Soft-Start Time	t_{SS}	No SS cap	4.4	5.1	5.8	ms
SS Charging Current	I_{SS}	V_{SS} = 0.4V	4.7	5	5.3	µA
FEEDBACK (FB)						
FB Regulation Voltage	V_{FB-REG}	MODE = OPEN	0.786	0.812	0.830	V
		MODE = GND	0.786	0.8	0.814	V
FB Input Leakage Current	I_{FB}	V_{FB} = 0.81V, T_A = 25°C	-100		+120	nA
CURRENT LIMIT						
V_{OUT} Current-Limit	$I_{SOURCE-LIMIT}$		100	178		mA
V_{OUT} Current-Limit	$I_{SINK-LIMIT}$	MODE = OPEN		-1		mA
		MODE = GND		-74	-50	mA
OSCILLATOR (RT/SYNC)						
Switching Frequency	f_{SW}	R_{RT} = 422kΩ	85	100	120	kHz
		R_{RT} = 191kΩ	200	220	250	kHz
		R_{RT} = 130kΩ	295	322	350	kHz
		R_{RT} = 69.8kΩ	540	600	640	kHz
		R_{RT} = 45.3kΩ	813	900	973	kHz

Electrical Characteristics (continued)

(V_{IN} = 24V, V_{GND} = 0V, V_{FB} = 0.85V, $V_{EN/UVLO}$ = 1.5V, RT/SYNC = 69.8kΩ, LX = SS = $\overline{RESET}$ = unconnected; MODE = GND T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to GND, unless otherwise noted) (Note 3)

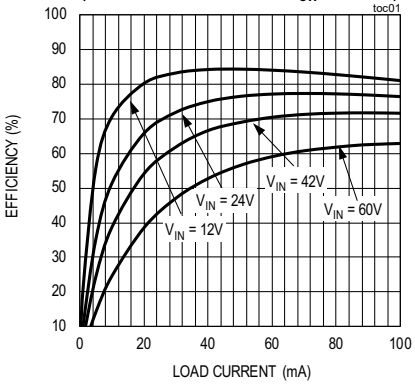
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Switching Frequency Adjustable Range		See the Switching Frequency (RT/SYNC) section for details	100		900	kHz
SYNC Input Frequency			1.1 x f_{SW}		900	kHz
SYNC Pulse Minimum Off-Time			40			ns
SYNC Rising Threshold	V_{SYNC-H}		1	1.22	1.48	V
Hysteresis	$V_{SYNC-HYS}$		0.115	0.18	0.265	
Number of SYNC Pulses to Enable Synchronization				1		Cycle
MODE						
MODE PFM Threshold	$V_{MODE-PFM}$		1	1.22	1.55	V
MODE Hysteresis	$V_{MODE-HYS}$			0.19		V
TIMING						
Minimum On-Time	t_{ON-MIN}		46	90	152	ns
Maximum Duty Cycle	D_{MAX}	V_{FB} = 0.98 x V_{FB-REG}, f_{SW} ≤ 600kHz	90	94	98	%
		600kHz < f_{SW} < 900kHz, V_{FB} = 0.98 x V_{FB-REG}	87	92		
Hiccup Timeout				51		ms
$\overline{RESET}$						
FB Threshold for $\overline{RESET}$ Rising	V_{FB-OKR}	V_{FB} rising	93	95	97	%
FB Threshold for $\overline{RESET}$ Falling	V_{FB-OKF}	V_{FB} falling	90	92	94	%
$\overline{RESET}$ Delay after FB Reaches 95% Regulation				2.08		ms
$\overline{RESET}$ Output Level Low		$I_{\overline{RESET}}$ = 1mA		0.23		V
$\overline{RESET}$ Output Leakage Current		V_{FB} = 1.01 x V_{FB-REG}, T_A = +25°C			1	µA
THERMAL SHUTDOWN						
Thermal-Shutdown Threshold		Temperature rising		160		°C
Thermal-Shutdown Hysteresis				20		°C

Note 3: All limits are 100% tested at +25°C. Limits over temperature are guaranteed by design.

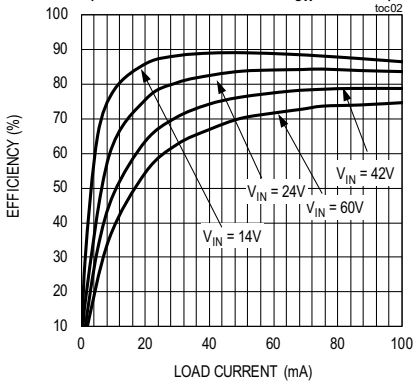
Typical Operating Characteristics

(V_{IN} = 24V, $V_{EN/UVLO}$ = 1.5V, RT/SYNC = 69.8kΩ, MODE = GND, T_A = +25°C unless otherwise noted)

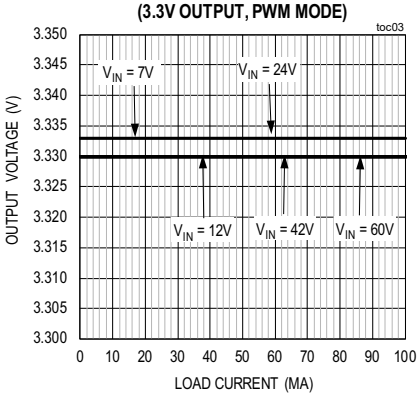
EFFICIENCY vs. LOAD CURRENT
(3.3V OUTPUT, PWM MODE, f_{SW} = 600kHz)



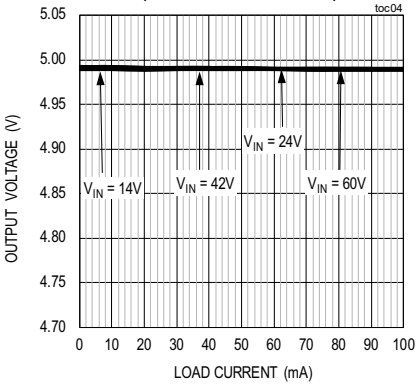
EFFICIENCY vs. LOAD CURRENT
(5V OUTPUT, PWM MODE, f_{SW} = 450kHz)



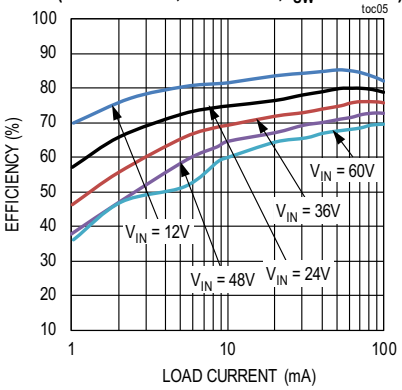
LOAD AND LINE REGULATION
(3.3V OUTPUT, PWM MODE)



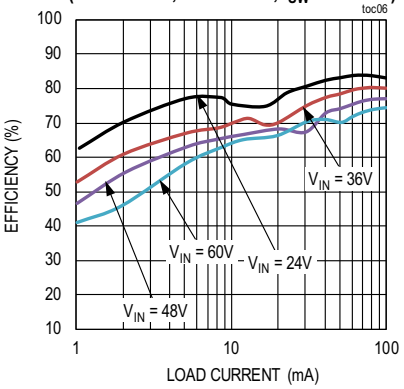
LOAD AND LINE REGULATION
(5V OUTPUT, PWM MODE)



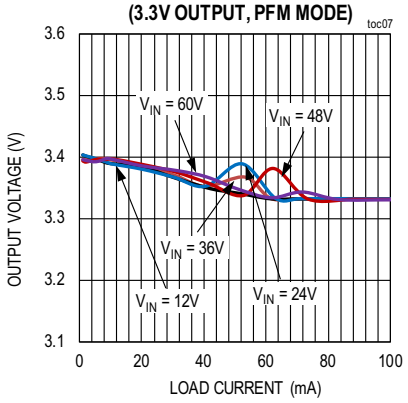
EFFICIENCY vs. LOAD CURRENT
(3.3V OUTPUT, PFM MODE, f_{SW} = 322kHz)



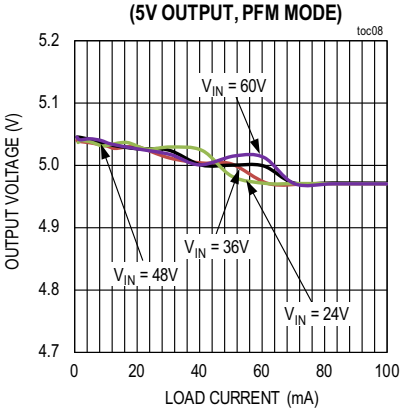
EFFICIENCY vs. LOAD CURRENT
(5V OUTPUT, PFM MODE, f_{SW} = 450kHz)



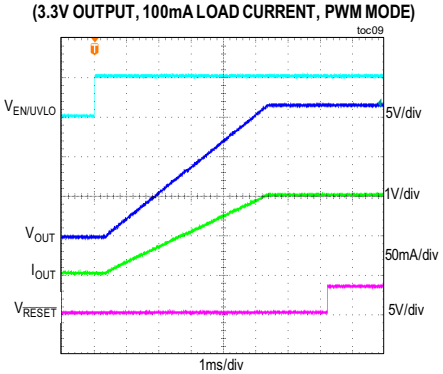
OUTPUT VOLTAGE vs. LOAD CURRENT
(3.3V OUTPUT, PFM MODE)



OUTPUT VOLTAGE vs. LOAD CURRENT
(5V OUTPUT, PFM MODE)



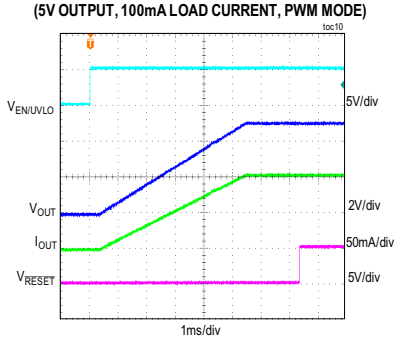
SOFT-START FROM EN/UVLO
(3.3V OUTPUT, 100mA LOAD CURRENT, PWM MODE)



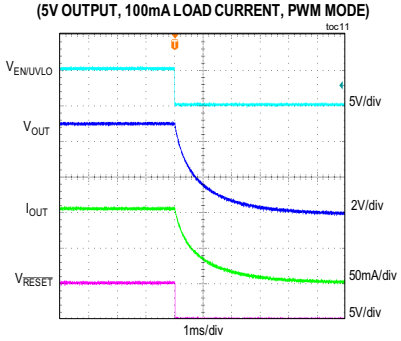
Typical Operating Characteristics (continued)

(V_{IN} = 24V, $V_{EN/UVLO}$ = 1.5V, RT/SYNC = 69.8kΩ, MODE = GND, T_A = +25°C unless otherwise noted)

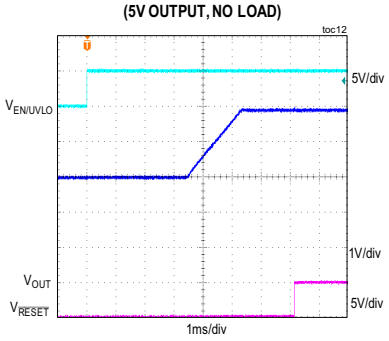
SOFT-START FROM EN/UVLO
(5V OUTPUT, 100mA LOAD CURRENT, PWM MODE)



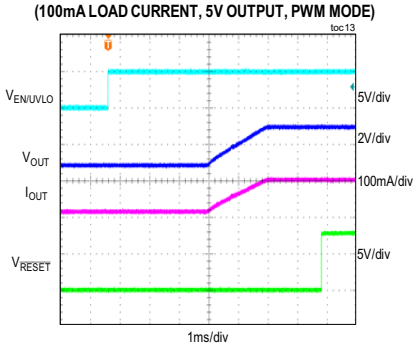
SHUTDOWN FROM EN/UVLO
(5V OUTPUT, 100mA LOAD CURRENT, PWM MODE)



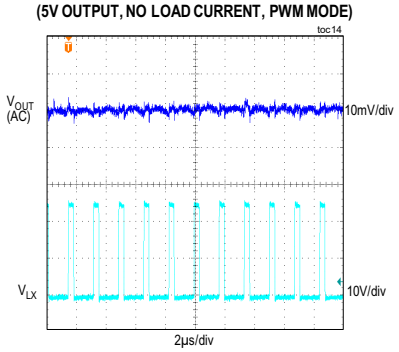
SOFT-START WITH 3V PREBIAS
(5V OUTPUT, NO LOAD)



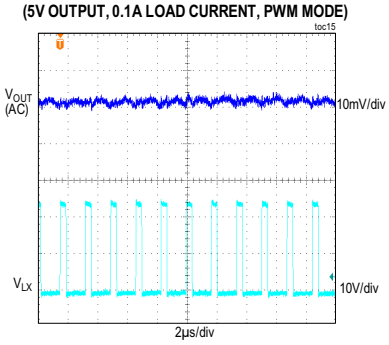
SOFT-START WITH 3V PREBIAS
(100mA LOAD CURRENT, 5V OUTPUT, PWM MODE)



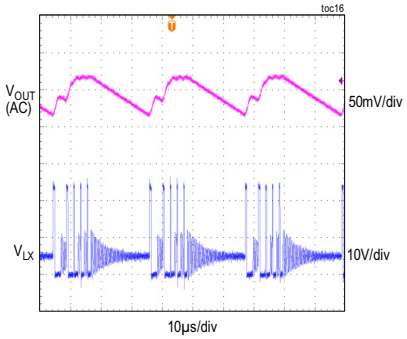
STEADY-STATE SWITCHING WAVEFORMS
(5V OUTPUT, NO LOAD CURRENT, PWM MODE)



STEADY-STATE SWITCHING WAVEFORMS
(5V OUTPUT, 0.1A LOAD CURRENT, PWM MODE)



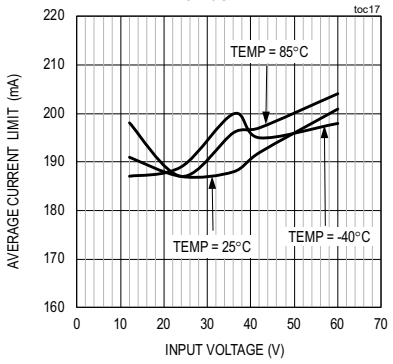
STEADY-STATE SWITCHING WAVEFORMS,
(5V OUTPUT, 0.01A LOAD CURRENT, PFM MODE)



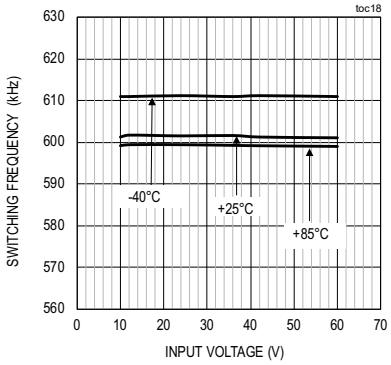
Typical Operating Characteristics (continued)

(V_{IN} = 24V, $V_{EN/UVLO}$ = 1.5V, RT/SYNC = 69.8kΩ, MODE = GND, T_A = +25°C unless otherwise noted)

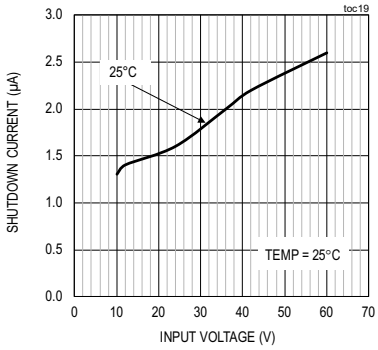
AVERAGE CURRENT LIMIT



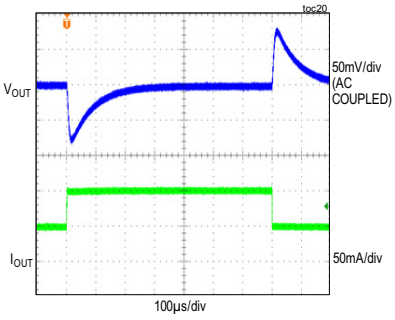
SWITCHING FREQUENCY vs. INPUT VOLTAGE



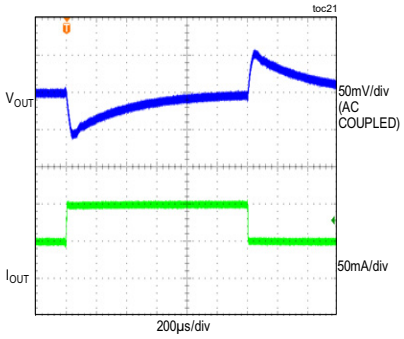
SHUTDOWN CURRENT vs. INPUT VOLTAGE



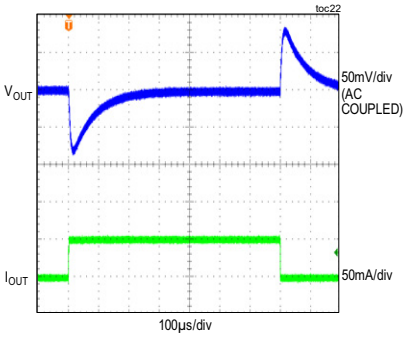
LOAD CURRENT TRANSIENT RESPONSE
(V_{IN} = 24V, V_{OUT} = 5V, I_{OUT} = 0.05A TO 0.1A)



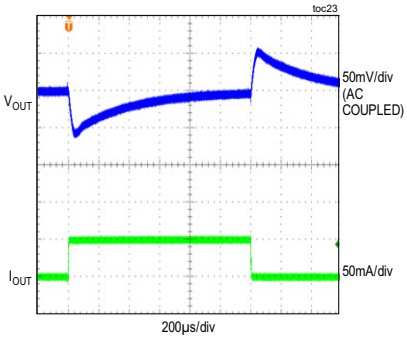
LOAD CURRENT TRANSIENT RESPONSE
(V_{IN} = 24V, V_{OUT} = 3.3V, I_{OUT} = 0.05A TO 0.1A)



LOAD CURRENT TRANSIENT RESPONSE
(V_{IN} = 24V, V_{OUT} = 5V, I_{OUT} = 0A TO 0.05A)



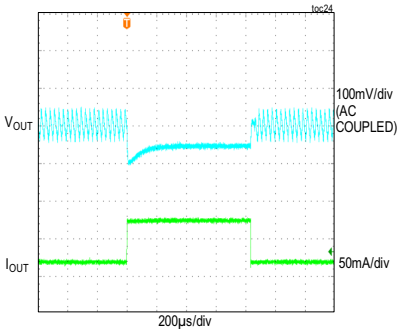
LOAD CURRENT TRANSIENT RESPONSE
(V_{IN} = 24V, V_{OUT} = 3.3V, I_{OUT} = 0A TO 0.05A)



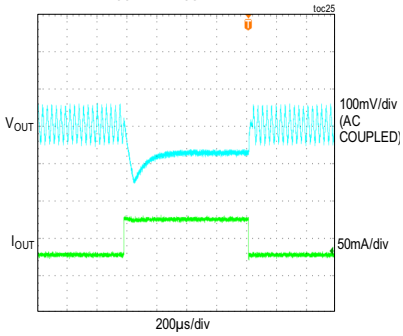
Typical Operating Characteristics (continued)

(V_{IN} = 24V, $V_{EN/UVLO}$ = 1.5V, RT/SYNC = 69.8kΩ, MODE = GND, T_A = +25°C unless otherwise noted)

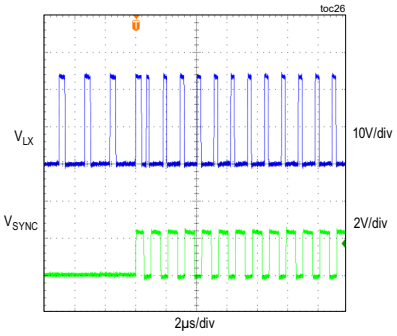
LOAD CURRENT TRANSIENT RESPONSE (PFM MODE)
V_{IN} = 24V, V_{OUT} = 3.3V, I_{OUT} = 20mA TO 75mA)



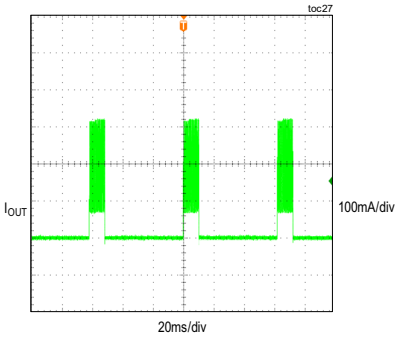
LOAD CURRENT TRANSIENT RESPONSE (PFM MODE
V_{IN} = 24V, V_{OUT} = 5V, I_{OUT} = 25mA TO 75mA)



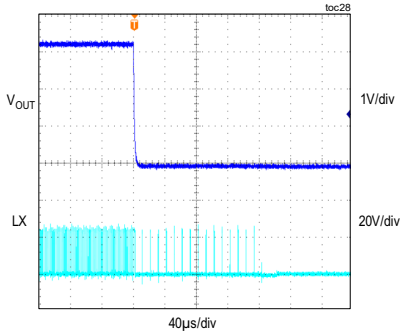
EXTERNAL SYNCHRONIZATION WITH 900kHz CLOCK FREQUENCY
(V_{IN} = 24V, V_{OUT} = 5V, I_{OUT} = 0.1A)



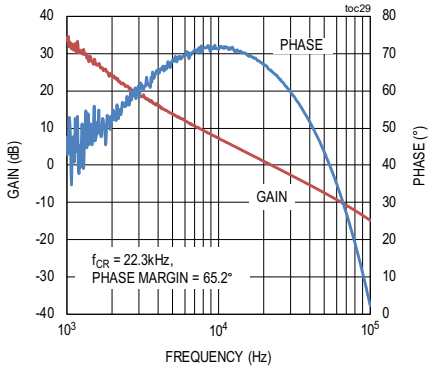
OVERLOAD PROTECTION STEADY STATE



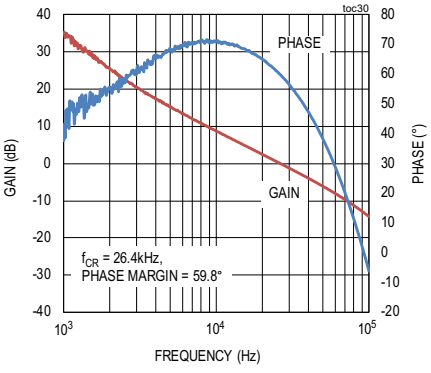
OVERLOAD PROTECTION OUT SHORT TO GROUND



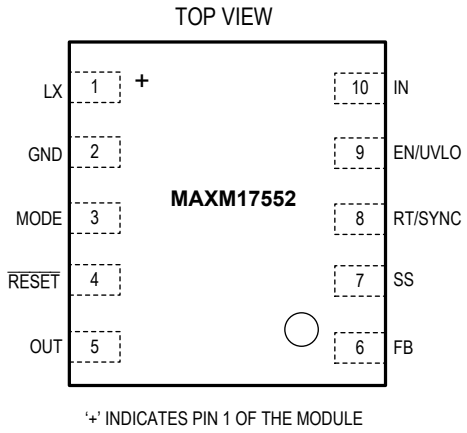
BODE PLOT
(V_{IN} = 24V, V_{OUT} = 5V, I_{OUT} = 0.1A)



BODE PLOT
(V_{IN} = 24V, V_{OUT} = 3.3V, I_{OUT} = 0.1A)



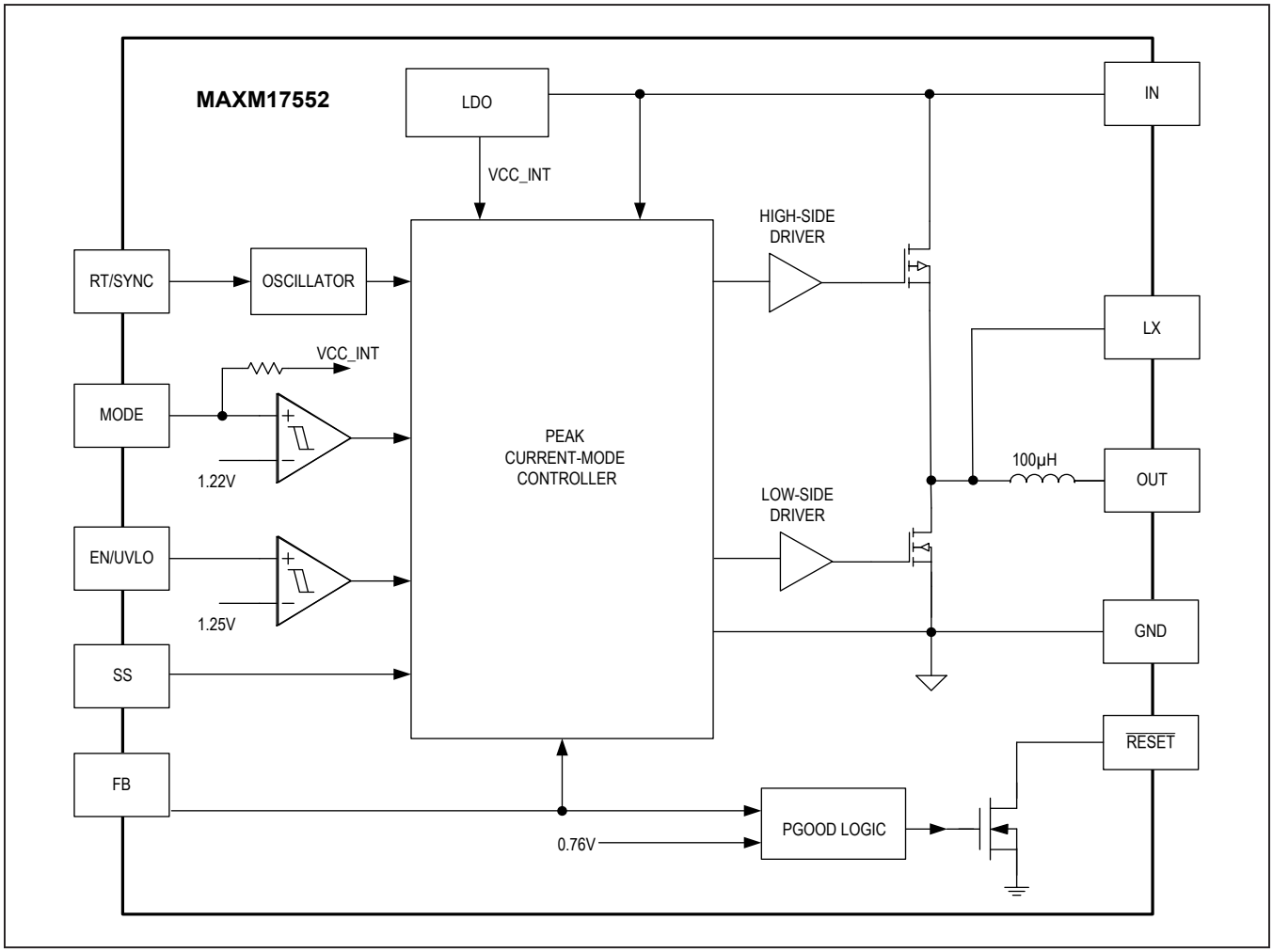
Pin Configuration



Pin Description

PIN NAME	PIN #	FUNCTION
LX	1	Switching Node. LX is high impedance when the device is in shutdown. Do not connect any external components to this pin.
GND	2	Ground. Connect GND to the power ground plane. Connect all the circuit ground connections together at a single point. See the *PCB Layout Guidelines* section.
MODE	3	PFM/PWM Mode Selection Input. Connect MODE to GND to enable the fixed-frequency PWM. Leave MODE unconnected for light-load PFM operation.
$\overline{\text{RESET}}$	4	Open-Drain Reset Output. Pull up $\overline{\text{RESET}}$ to an external power supply less than or equal to 16V with an external resistor. $\overline{\text{RESET}}$ pulls low if FB drops below 92% of its set value. $\overline{\text{RESET}}$ goes high 2ms after FB rises above 95% of its set value.
OUT	5	Module output pin. Connect a capacitor from OUT to GND. See PCB Layout Guidelines section for more connection details.
FB	6	Output Feedback Connection. Connect FB to a resistor-divider between OUT and GND to set the output voltage.
SS	7	Soft-Start Capacitor Input. Connect a capacitor from SS to GND to set the soft-start time. Leave SS unconnected for default 5.1ms internal soft-start.
RT/SYNC	8	Oscillator Timing Resistor Input. Connect a resistor from RT/SYNC to GND to program the switching frequency from 100kHz to 900kHz. See the *Switching Frequency (RT/SYNC)* section for details. An external pulse can be applied to RT/SYNC through a coupling capacitor to synchronize the internal clock to the external pulse frequency.
EN/UVLO	9	Active-High, Enable/Undervoltage-Detection Input. Pull EN/UVLO to GND to disable the module output. Connect EN/UVLO to IN for always-on operation. Connect a resistor-divider between IN, EN/UVLO, and GND to program the input voltage at which the module is enabled and turns on.
IN	10	Power Module Input. Connect a ceramic capacitor from IN to GND for bypassing. Place the capacitor close to the IN and PGND pins. See *Component Selection* tables for more details.

Functional Diagram



Detailed Description

The MAXM17552 high-voltage, synchronous step-down power module with integrated MOSFETs and inductor, operates over a 4V to 60V input voltage range. The module can deliver output current up to 100mA at output voltages of 0.9V to 5.5V. The feedback voltage is accurate to within ±1.75% over -40°C to +125°C.

The device uses an internally-compensated, peak current mode control architecture. On the rising edge of the internal clock, the high-side pMOSFET turns on. An internal error amplifier compares the feedback voltage to a fixed internal reference voltage and generates an error voltage. The error voltage is compared to a sum of the current-sense voltage and a slope-compensation voltage by a PWM comparator to set the “on-time.” During the on-time of the pMOSFET, the inductor current ramps up. For the remainder of the switching period (off-time), the pMOSFET is kept off and the low-side nMOSFET turns on. During the off-time, the inductor releases the stored energy as the inductor current ramps down, providing current to the output. Under overload conditions, the cycle-by-cycle current- limit feature limits inductor peak current by turning off the high-side pMOSFET and turning on the low-side nMOSFET.

Mode Selection (MODE)

The device features a MODE pin for selecting either forced-PWM or PFM mode of operation. If the MODE pin is left unconnected, the device operates in PFM mode at light loads. If the MODE pin is grounded, the device operates in a constant-frequency forced-PWM mode at all loads. The mode of operation cannot be changed on-the fly during normal operation of the device.

In PWM mode, the inductor current is allowed to go negative. PWM operation is useful in frequency-sensitive applications and provides fixed switching frequency at all loads. However, the PWM mode of operation gives lower efficiency at light loads compared to PFM mode of operation.

PFM mode disables negative inductor current and additionally skips pulses at light loads for high efficiency. In PFM mode, the inductor current is forced to a fixed peak of 72mA (typ) (IPFM) every clock cycle until the output rises to 102% (typ) of the nominal voltage. Once the output reaches 102% (typ) of the nominal voltage, both high-side and low-side FETs are turned off and the device enters hibernation mode until the load discharges the output to 101% (typ) of the nominal voltage. Most of the internal blocks are turned off in hibernation mode to save quiescent current. Once the output falls below 101% (typ) of the nominal voltage, the device comes out of hibernation mode, turns on all internal blocks, and again commences the process of delivering pulses of energy to the output until it reaches 102% (typ) of the nominal output voltage. The device naturally exits PFM mode when the inductor peak current increases to a magnitude approximately equal to IPFM.

Enable Input (EN/UVLO) and Soft-Start (SS)

When EN/UVLO voltage increases above 1.25V (typ), the device initiates a soft-start sequence and the duration of the soft-start depends on the status of the SS pin voltage at the time of power-up. If the SS pin is not connected, the device uses a fixed 5.1ms (typ) internal soft-start to ramp up the internal error-amplifier reference. If a capacitor is connected from SS to GND, a 5µA current source charges the capacitor and ramps up the SS pin voltage. The SS pin voltage is used as a reference for the internal error amplifier. Such a reference ramp up allows the output voltage to increase monotonically from zero to the final set value independent of the load current.

EN/UVLO can be used as an input voltage UVLO adjustment input. An external voltage-divider between IN and EN/UVLO to GND adjusts the input voltage at which the device turns on or off. See the *Setting the Input Undervoltage-Lockout Level* section for details. If input UVLO programming is not desired, connect EN/UVLO to IN (see the *Electrical Characteristics* table for EN/UVLO rising and falling-threshold voltages). Driving EN/UVLO low disables both power MOSFETs, as well as other internal circuitry, and reduces IN quiescent current to below 1.2µA. The SS capacitor is discharged with an internal pulldown resistor when EN/UVLO is low. If the EN/UVLO pin is driven from an external signal source, a series resistance of minimum 1kΩ is recommended to be placed between the signal source output and the EN/UVLO pin, to reduce voltage ringing on the line.

Switching Frequency (RT/SYNC)

Switching frequency of the device can be programmed from 100kHz to 900kHz by using a resistor connected from RT/SYNC to GND. The switching frequency (f_{SW}) is related to the resistor connected at the RT/SYNC pin (R_T) by the following equation, where R_T is in kΩ and f_{SW} is in kHz:

$$R_T = \frac{42000}{f_{SW}}$$

The switching frequency in ranges of 130kHz to 160kHz and 230kHz to 280kHz are not allowed for user programming to ensure proper configuration of the internal adaptive-loop compensation scheme.

External Synchronization

The RT/SYNC pin can be used to synchronize the device's internal oscillator to an external system clock. The external clock should be coupled to the RT/SYNC pin through a 47pF capacitor, as shown in Figure 1. The external clock logic high level should be higher than 3V, logic low level lower than 0.5V and the duty cycle of the external clock should be in the range of 10% to 70%. The RT resistor should be selected to set the switching frequency 10% lower than the external clock frequency. The external clock should be applied at least 500µs after enabling the device for proper configuration of the internal loop compensation.

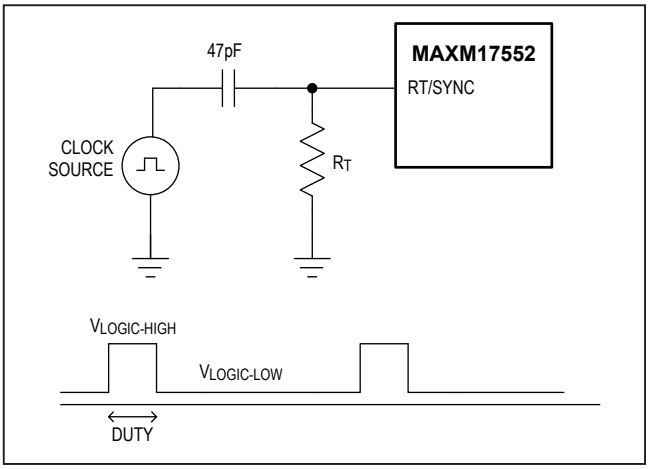


Figure 1. Synchronization to an External Clock

Reset Output ($\overline{RESET}$)

The device includes an open-drain $\overline{RESET}$ output to monitor output voltage. $\overline{RESET}$ should be pulled up with an external resistor to the desired external power supply less than or equal to 16V. $\overline{RESET}$ goes high impedance 2ms after the output rises above 95% of its nominal set value and pulls low when the output voltage falls below 92% of the set nominal output voltage. $\overline{RESET}$ asserts low during the hiccup timeout period.

Startup Into a Pre-biased Output

The device supports monotonic startup into a pre-biased output. When the module starts into a pre-biased output, both the high-side and low-side switches are turned off so that the module does not sink current from the output. High-side and low-side switches do not start switching until the PWM comparator commands the first PWM pulse, at which point switching commences. The output voltage is then smoothly ramped up to the target value in alignment with the internal reference. Such a feature is useful in applications where digital integrated circuits with multiple rails are powered.

Operating Input-Voltage Range

The maximum operating input voltage is determined by the minimum controllable on-time, while the minimum operating input voltage is determined by the maximum duty cycle and circuit voltage drops. The minimum and maximum operating input voltages for a given output voltage should be calculated as follows:

$$V_{IN(MIN)} = \frac{V_{OUT} + (I_{OUT} \times 8.6)}{D_{MAX}} + (I_{OUT} \times 2.5)$$

$$\text{for duty cycle, } D > 0.3: \; V_{IN(MIN)} > 4.8 \times V_{OUT} - \left(\frac{f_{SW}}{42000}\right)$$

$$V_{IN(MAX)} = \frac{V_{OUT}}{t_{ON(MIN)} \times f_{SW}}$$

where,

V_{OUT} = Steady-state output voltage

I_{OUT} = Maximum load current

f_{SW} = Switching frequency (max)

D_{MAX} = Maximum duty cycle

$t_{ON(MIN)}$ = Worst case minimum controllable switch on-time (152ns).

Overcurrent Protection (OCP), Hiccup Mode

The device implements a HICCUP-type overload protection scheme to protect the inductor and internal FETs under output short-circuit conditions. When the overcurrent event occurs, the part enters hiccup mode. In this mode, the part is initially operated with hysteretic cycle-by-cycle peak-current limit that continues for a time period equal to twice the soft-start time. The part is then turned off for a fixed 51ms hiccup timeout period. This sequence of hysteretic inductor current waveforms, followed by a hiccup timeout period, continues until the short/overload on the output is removed. Since the inductor current is bound between two limits, inductor current runway never happens.

Thermal Shutdown

Thermal shutdown limits the total power dissipation in the module. When the junction temperature exceeds +160°C, an on-chip thermal sensor shuts down the device, turns off the internal power MOSFETs, allowing the device to cool down. The device turns on after the junction temperature cools by approximately 20°C.

Application Information

Input Capacitor Selection

Small ceramic input capacitors are recommended. The input capacitor reduces peak current drawn from the power source and reduces noise and voltage ripple on the input caused by the switching circuitry. It is recommended to select the input capacitor of the module to keep the input-voltage ripple under 2% of the minimum input voltage, and to meet the maximum ripple-current requirements.

Output Capacitor Selection

Small ceramic X7R-grade output capacitors are recommended for the device. The output capacitor has two functions. It stores sufficient energy to support the output voltage under load transient conditions and stabilizes the device's internal control loop. Usually the output capacitor is sized to support a step load of 50% of the maximum output current in the application, such that the output voltage deviation is less than 3%. Calculate the minimum required output capacitance from the following equations:

FREQUENCY RANGE (kHZ)	MINIMUM OUTPUT CAPACITANCE (µF)
100 to 130	$\frac{50}{V_{OUT}}$
160 to 230	$\frac{25}{V_{OUT}}$
280 to 900	$\frac{17}{V_{OUT}}$

It should be noted that dielectric materials used in ceramic capacitors exhibit capacitance loss due to DC bias levels and should be appropriately de-rated to ensure the required output capacitance is obtained in the application.

Soft Start Capacitor Selection

The device offers a 5.1ms internal soft-start when the SS pin is left unconnected. When adjustable soft-start time is required, connect a capacitor from SS to GND to program the soft-start time. The minimum soft-start time is related to the output capacitance (C_{OUT}) and the output voltage (V_{OUT}) by the following equation:

$$t_{SS} > 0.05 \times C_{OUT} \times V_{OUT}$$

where t_{SS} is in milliseconds and C_{OUT} is in µF.

Soft-start time (t_{SS}) is related to the capacitor connected at SS (C_{SS}) by the following equation:

$$C_{SS} = 6.25 \times t_{SS}$$

where t_{SS} is in milliseconds and C_{SS} is in nanofarads.

Setting the Input Undervoltage-Lockout Level

The device offers an adjustable input undervoltage-lockout level. Set the voltage at which the device turns on with a resistive voltage-divider connected from IN to GND (see Figure 2). Connect the center node of the divider to EN/UVLO. Choose R1 to be 3.3MΩ max and then calculate R2 as follows:

$$R2 = \frac{1.25 \times R_1}{V_{INU} - 1.25}$$

where V_{INU} is the voltage at which the device is required to turn on.

Adjusting the Output Voltage

The output voltage can be programmed from 0.9V to 5.5V. Different output voltage needs to use different switching frequency (see Table 1). Set the output voltage by connecting a resistor-divider from output to FB to GND (see Figure 3). Choose R5 in the range of 25kΩ to 100kΩ and calculate R4 with the following equation:

$$R4 = R5 \times \left(\frac{V_{OUT}}{0.8} - 1 \right)$$

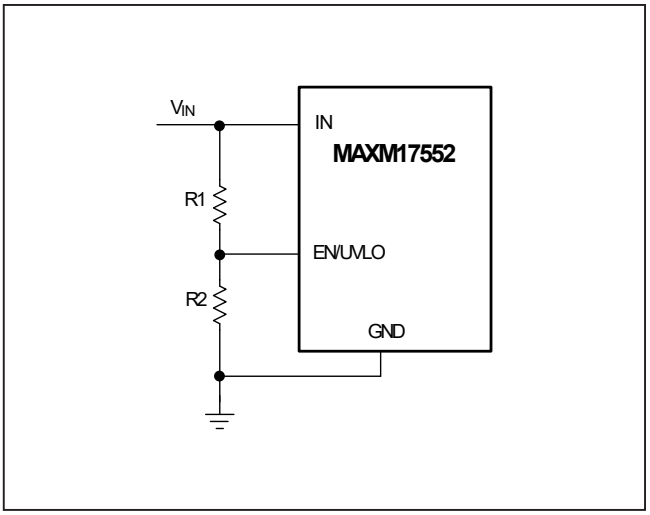


Figure 2. Adjustable EN/UVLO Network

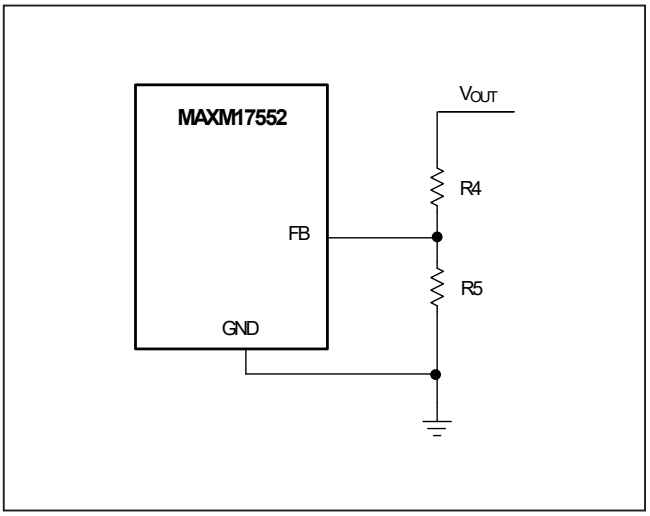


Figure 3 Circuit for Setting the Output Voltage.

Table 1. Selection Component Values

V_{OUT} (V)	V_{IN} (V)	C_{IN}	f_{SW} (kHz)	R_T (kΩ)	R_U (kΩ)	R_B (kΩ)	C_{OUT}
0.9	4 to 24	1 × 2.2µF 1206 50V X7R	220	191	6.19	49.9	2 × 10µF 0805 6.3V X7R
1	4 to 26	1 × 2.2µF 1206 50V X7R	220	191	12.4	49.9	2 × 10µF 0805 6.3V X7R
1.2	4 to 32	1 × 2.2µF 1206 50V X7R	220	191	24.9	49.9	2 × 10µF 0805 6.3V X7R
1.5	4 to 27	1 × 2.2µF 1206 50V X7R	322	130	43.2	49.9	1 × 10µF 0805 6.3V X7R
1.8	4 to 32	1 × 2.2µF 1206 50V X7R	322	130	61.9	49.9	1 × 10µF 0805 6.3V X7R
2.5	4.5 to 45	1 × 2.2µF 1206 100V X7R	322	130	107	49.9	1 × 10µF 0805 6.3V X7R
3.3	7 to 60	1 × 2.2µF 1206 100V X7R	322	130	158	49.9	1 × 10µF 0805 6.3V X7R
5	14 to 60	1 × 2.2µF 1206 100V X7R	450	93.1	261	49.9	1 × 10µF 0805 6.3V X7R
5.5	13 to 60	1 × 2.2µF 1206 100V X7R	500	84.5	294	49.9	1 × 10µF 0805 10V X7R

Transient Protection

In applications where fast line transients or oscillations with a slew rate in excess of 15V/µs are expected during power-up or steady-state operation, the MAXM17552 should be protected with a series resistor that forms a low pass filter with the input ceramic capacitor (Figure 4). These transients can occur in conditions such as hot-plugging from a low-impedance source or due to inductive load switching and surges on the supply lines.

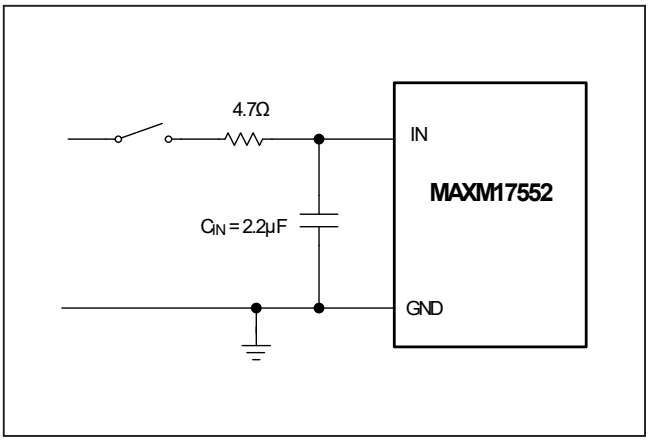


Figure 4. Circuit for Transient Protection

Power Dissipation

Ensure that the junction temperature of the devices do not exceed 125°C under the operating conditions specified for the power supply. At a particular operating condition, the power losses that lead to temperature rise of the device are estimated as follows:

$$P_{LOSS} = P_{OUT}(\frac{1}{\eta} - 1)$$

$$P_{OUT} = V_{OUT} \times I_{OUT}$$

where P_{OUT} is the output power, η is the efficiency of power conversion. See the *Typical Operating Characteristics* for the power-conversion efficiency or measure the efficiency to determine the total power dissipation. The junction temperature (T_J) of the device can be estimated at any ambient temperature (T_A) from the following equation:

$$T_J = T_A + \theta_{JA} \times P_{LOSS}$$

where θ_{JA} is the junction-to-ambient thermal impedance of the package.

PCB Layout Guidelines

Careful PCB layout (Figure 5) is critical to achieve clean and stable operation. The switching power stage requires particular attention. Follow these guidelines for good PCB layout:

- Place the input ceramic capacitor as close as possible to V_{IN} and GND pins
- Ensure that all feedback connections are short and direct
- Route high-speed switching node (LX) away from the signal pins

For a sample PCB layout that ensures the first-pass success, refer to the MAXM17552 evaluation kit data sheet.

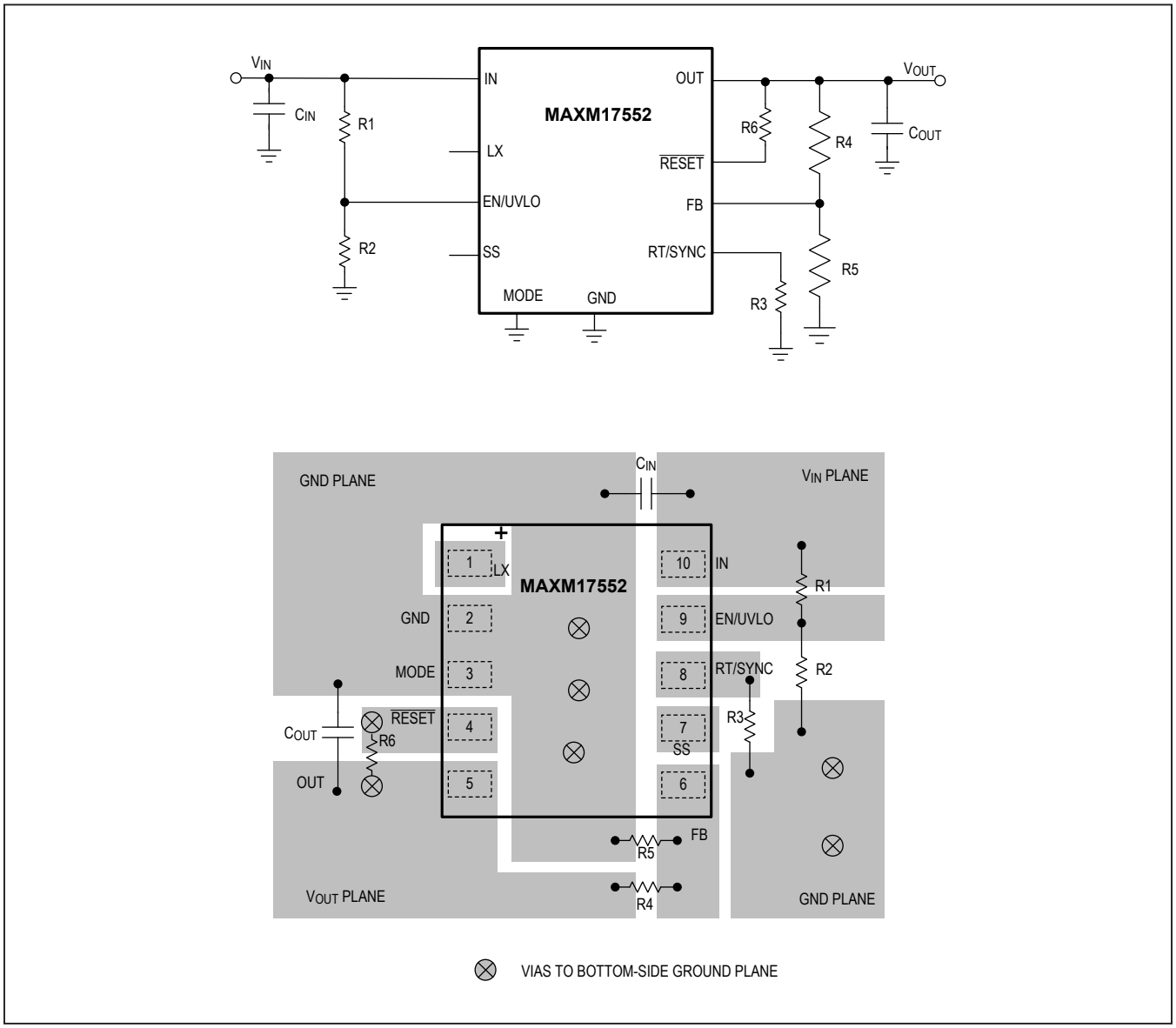


Figure 5. Layout Guidelines

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAXM17552AMB+	-40°C to +125°C	10-pin uSLIC
MAXM17552AMB+T	-40°C to +125°C	10-pin uSLIC

+Denotes a lead(Pb)-free/RoHS-compliant package.
T = Tape and reel.

Chip Information

PROCESS: BiCMOS

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	10/17	Initial release	—
1	9/18	Updated *General Description*, *Applications*, *Benefits and Features*, and *Absolute Maximum Ratings* sections; updated *Package Information*, *Electrical Characteristics*, *Pin Description*, and *Ordering Information* tables; replaced *Typical Application Circuit*, *Pin Configuration*, *Functional Diagram*, and Figure 5; added TOC05-TOC08, TOC16, and TOC21-TOC22 and renumbered remaining TOCs.	1-10, 14-15
2	12/19	Updated the *Absolute Maximum Ratings, Pin Description,* and *Reset Output (RESET)* sections.	2, 9, 12

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