Monolithic Power Systems, Inc.

PRODUCT RELIABILITY REPORT

Product: MPM3805/10

Reliability Department
Monolithic Power Systems
79 Great Oaks Boulevard
San Jose, CA 95119
Tel: 408-826-0600
Fax: 408-826-0601

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1. Device Information

Product:	MPM3805/10
Package:	FCM QFN MODULE (2.5mm×3.0mm×0.9mm)-12
Process Technology:	BCD
Report Date:	08/15/2018

2. Summary of Test Results

Test	Test Condition	Lot# or Date Code	Test Results (S.S./Rej)	Comment
Temperature, Bias, and Operating Life	JESD22-A108, @+125°C for 1000 hours or equivalent	HP300301 HP317303 HP317304	80/0 80/0 80/0	
ESD: Human Body Model (HBM)	ANSI/ESDA/JEDEC JS-001	HP317303	3/0	>2000V
ESD: Device Charged Model (CDM)	ANSI/ESDA/JEDEC JS-002	HP317303	3/0	>750V
Latch-up	EIA/JESD78	HP317303	6/0	>+/-100mA & >1.5Vccmax
Moisture/Reflow Sensitivity	J-STD-020	1238 1244 1248	300/0 300/0 300/0	MSL = 3
High Temperature Storage Life	JESD22-A103, @150°C for 1000 hours	1244 1248 1305	50/0 50/0 50/0	
Temperature Cycling	JESD22-A104, from -65°C to 150°C for 1000 cycles or equivalent	1238 1244 1248	80/0 80/0 80/0	
Accelerated Moisture Resistance- Unbiased Autoclave	JESD22-A102, @121°C/100%RH for 168 hours or equivalent	1244 1248 1305	80/0 80/0 80/0	
Steady State Temperature Humidity Bias Life Test	JESD22-A101, @85°C/85%RH static bias at Vinmax for 1000 hours or equivalent	1248 1305 1315	80/0 80/0 80/0	

Mechanical Shock (MS)	JESD22-B104	1244 1248 1249	15/0 15/0 15/0	
Vibration Variable Frequency (VVF)	JESD22-B103 Sequence from MS	1244 1248 1249	15/0 15/0 15/0	
Constant Acceleration (CA)	M2001 Sequence from VVF	1244 1248 1249	15/0 15/0 15/0	

3. Failure Rate Calculation

Sample Size:	5350
Rejects:	0
Activation Energy (eV):	0.7
Equivalent Device Hours:	4.17×10^{8} Hours
Failure Rate (FIT@60%CL):	2.2 FIT
MTBF (years):	52,062 Year

Revision / Update History

Revision	Reason for Change	Date	Rel Engineer
1.0	Initial release	August 2013	Ramon Lei
2.0	Update	March 2014	Ramon Lei
3.0	Update	June 2016	Ramon Lei
4.0	Update	August 2018	Ramon Lei

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Appendix: Description of Reliability Test and Failure Rate Calculation

High Temperature Operating Life Test

Purpose: This test is a worst-case life test that checks the integrity of the product. The high temperature testing is use for acceleration of any potential failures over time. The calculation for failure rate (FIT) using the operating ambient temperature is done using the Arrhenius equation.

Condition: 125°C @ Vinmax

Pass Criteria: All units must pass the min/max limits of the datasheet.

ESD Test

Purpose: The purpose of the ESD test is to guarantee that the device can withstand electrostatic voltages during handling.

Condition: Human Body Model and Charged Device Model

Pass Criteria: ESD Testing on every pin. The device must be fully functional after testing and pass the min/max limits in the datasheet.

IC Latch-Up Test

Purpose: The purpose of this specification is to establish a method for determining IC latch-up characteristics and to define latch-up failure criteria. Latch-up characteristics are extremely important in determining product reliability and minimizing No Trouble Found (NTF) and Electrical Overstress (EOS) failures due to latch-up.

Condition: Voltage and current injection

Pass criteria: All pins with the exception of “no connect” pins and timing related pins, shall be latch-up tested. The device must be fully functional after testing and pass the min/max limits in the datasheet.

Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices

Purpose: The purpose of this standard is to identify the classification level of nonhermetic solid state surface mount devices (SMDs) that are sensitive to moisture-induced stress so that they can be properly packaged, stored, and handled to avoid damage during assembly solder reflow attachment and/or repair operations.

Condition: Bake + moisture sock + 3X reflow at 260°C

Pass criteria: All units must pass the min/max limits of the datasheet

High Temperature Storage Life

Purpose: The test is typically used to determine the effects of time and temperature, under storage conditions, for thermally activated failure mechanisms and time-to-failure distributions of solid state electronic devices, including nonvolatile memory devices (data retention failure mechanisms).

Condition: Bake at 150°C

Pass Criteria: All units must pass min/max limits of the datasheet

Accelerated Moisture Resistance- Unbiased Autoclave

Purpose: To check the performance of the device in humid environments. This test checks the integrity of the passivation, poor metal to plastic seal and contamination level during assembly and material compatibility.

Condition: 121°C/15psig/100% RH (no bias)

Pass Criteria: All units must pass min/max limits of the datasheet

Temperature Cycle Test

Purpose: This test is used to evaluate the die attach integrity and bond integrity. This is similar to the Thermal Shock test, but can generate different failure modes due to the longer dwell time and gradual temperature change.

Condition: -65°C to 150°C

Pass Criteria: All units must pass min/max limits of the datasheet

Monolithic Power Systems, Inc.

Steady State Temperature Humidity Bias Life Test

Purpose: This is to check the performance of the device in humid environments. This test checks the integrity of the passivation, poor metal to plastic seal and contamination level during assembly and material compatibility.

Condition: 85%RH at 85°C with Vin=Vinmax

Pass Criteria: All units must pass min/max limits of the datasheet

Highly Accelerated Temperature and Humidity Stress Test

Purpose: This is an equivalent test to Steady State Temperature Humidity Bias Life test with different (higher) temperature stress condition.

Condition: 85%RH at 130°C with Vin=Vinmax

Pass Criteria: All units must pass min/max limits of the datasheet

Failure Rate Calculation

The failure rate is gauged by a Failures-In-Time (FIT) based upon accelerated stress data. The unit for FIT is failure per billion device hour.

$$FIT\ Rate = \frac{(\chi^2/2) \times 10^9}{EDH}$$

Where

$\chi 2$ (Chi-Squared) is the goodness-of-fit test statistic at a specified level of confidence;
EDH= Equivalent Device Hours = AF × (Life test sample size) × (test duration);
AF= Acceleration Factor.

High Temperature Operating Life (HTOL) test is usually done under acceleration of temperature and voltage. The total number of failures from the stress test determines the chi-squared factor.

$$AF = AF_T \times AF_V$$

The Temperature Acceleration Factor AF_T:

$$AF_T = \exp\left(\frac{E_a}{K}\left(\frac{1}{T_{J(use)}} - \frac{1}{T_{J(stress)}}\right)\right)$$

T_{Juse} = Junction temp under typical operating conditions;
$T_{Jstress}$ =Junction temp under accelerated test conditions;
Ea is Activation energy=0.7eV;
K=Boltzmann's constant=8.62×10^{-5} eV/K.

The voltage Acceleration Factor AF_V:

$$AF_V = e^{\beta \times [V_{stress} - V_{use}]}$$

V_{use} = Gate voltage under typical operating conditions;
V_{stress} = Gate voltage under accelerated test conditions;
β = Voltage acceleration factor (in 1/Volts) and specified by technology.
Note: For calculation in the report, AF_V = 1 for simplicity.

MTBF (Mean Time Between Failure) equals to 10^9/FIT (in hours).