

TPS56C230EVM 12-A, Regulator Evaluation Module

This user's guide contains information for the TPS56C230EVM evaluation module as well as for the TPS56C230 dc/dc converter. Also included are the performance specifications, schematic, layout and the list of materials for the TPS56C230EVM.

Contents

1	Introduction	3
2	Performance Specification Summary	4
3	Modifications.....	5
	3.1 Output Voltage Setpoint.....	5
	3.2 Mode Selection.....	5
4	Test Setup and Results	6
	4.1 Input/Output Connections.....	6
	4.2 Efficiency.....	7
	4.3 Output Voltage Load Regulation.....	8
	4.4 Output Voltage Line Regulation.....	8
	4.5 Load Transient Response	9
	4.6 Output Voltage Ripple	10
	4.7 Input Voltage Ripple	11
	4.8 Loop Characteristics	12
	4.9 Start-Up.....	13
	4.10 Shut-Down	14
5	Board Layout.....	15
	5.1 Layout.....	15
6	Schematic, List of Materials, and Reference	18
	6.1 Schematic	18
	6.2 List of Materials.....	19

List of Figures

1	TPS56C230EVM Efficiency at 500-kHz/Eco mode	7
2	TPS56C230EVM Light Load Efficiency at 500-kHz/Eco Mode.....	7
3	TPS56C230EVM Load Regulation, $V_{IN} = 12\text{ V}$	8
4	TPS56C230EVM Line Regulation	8
5	TPS56C230EVM Load Transient Response	9
6	TPS56C230EVM Output Ripple, 10-mA Load	10
7	TPS56C230EVM Output Ripple, 800-mA Load	10
8	TPS56C230EVM Output Ripple, 12-A Load.....	10
9	TPS56C230EVM Input Ripple, 10-mA Load.....	11
10	TPS56C230EVM Input Ripple, 800-mA Load	11
11	TPS56C230EVM Input Ripple, 12-A Load.....	11
12	TPS56C230EVM Loop Response	12
13	TPS56C230EVM Start-Up Relative to V_{IN}	13
14	TPS56C230EVM Start-Up Relative to Enable	13
15	Shutdown Relative to V_{IN}	14
16	Shutdown Relative to Enable	14

17	TPS56C230EVM Top-Side Assembly	15
18	TPS56C230EVM Top-Side Layout	16
19	TPS56C230EVM Internal Layer-1 Layout	16
20	TPS56C230EVM Internal Layer-2 Layout	17
21	TPS56C230EVM Bottom Side Layout.....	17
22	TPS56C230EVM Schematic.....	18

List of Tables

1	Input Voltage and Output Current Summary	3
2	TPS56C230EVM Performance Specifications Summary.....	4
3	Mode Pin Resistor Settings	5
4	Connection and Test Points	6
5	TPS56C230EVM List of Materials	19

Trademarks

D-CAP3 is a trademark of Texas Instruments.

1 Introduction

The TPS56C230 is a synchronous buck converter designed to provide up to a 12-A output. The input voltage is rated for 4.5 V to 18 V. The TPS56C230 uses a proprietary D-CAP3™ control mode. It provides a fast transient response with no external compensation, and supports low ESR output capacitors. A MODE pin is used to set Forced Continuous Conduction Mode (FCCM) or Advanced Eco-mode operation. Rated input voltage and output current range for the evaluation module are given in [Table 1](#). The high-side and low-side switching MOSFETs are integrated inside the TPS56C230 package along with the gate-driver circuitry. The low drain-to-source on resistance of the MOSFET allows the TPS56C230 to achieve high efficiencies and helps keep the junction temperature low at high output currents. An external divider allows for an adjustable output voltage. Additionally, the TPS56C230 provides adjustable soft start and undervoltage lockout inputs and an open drain power good output.

The TPS56C230EVM evaluation module (EVM) is a single, synchronous buck converter providing 1.2 V at 12 A from 4.5 V to 18 V input. This user's guide describes the TPS56C230EVM performance.

Table 1. Input Voltage and Output Current Summary

EVM	INPUT VOLTAGE (V_{IN}) Range	OUTPUT CURRENT (I_{OUT}) Range
TPS56C230EVM	4.5 V to 18 V	0 A to 12 A

2 Performance Specification Summary

A summary of the TPS56C230EVM performance specifications is provided in [Table 2](#). Specifications are given for an input voltage of 12 V and an output voltage of 1.2 V, unless otherwise specified. The ambient temperature is 25°C for all measurement, unless otherwise noted.

Table 2. TPS56C230EVM Performance Specifications Summary

SPECIFICATIONS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN} Input voltage		4.5	12	18	V
V_{IN} start voltage		Internal UVLO			V
V_{IN} stop voltage		Internal UVLO			V
Output voltage setpoint		1.2			V
Output current range	$V_{IN} = 4.5\text{ V to }18\text{ V}$	0	12		A
Line regulation	$I_{OUT} = 6\text{ A}, V_{IN} = 4.5\text{ V to }17\text{ V}$	± 0.05%			
Load regulation	$V_{IN} = 12\text{ V}, I_{OUT} = 0\text{ to }12\text{ A}$	-0.02%, +0.25%			
Load transient response	$I_{OUT} = 1.2\text{ A to }10.8\text{ A}$	Voltage change	-38		mV
		Recovery time	75		µs
	$I_{OUT} = 10.8\text{ A to }1.2\text{ A}$	Voltage change	48		mV
		Recovery time	50		µs
Loop bandwidth	$V_{IN} = 12\text{ V}, I_{OUT} = 6\text{ A}$	126.5			kHz
Phase margin	$V_{IN} = 12\text{ V}, I_{OUT} = 6\text{ A}$	72.5			degree
Input ripple voltage	$V_{IN} = 12\text{ V}, I_{OUT} = 12\text{ A}$	290			mVPP
Output ripple voltage	$V_{IN} = 12\text{ V}, I_{OUT} = 12\text{ A}$	16			mVPP
Output rise time	Soft start pin floating	1.5			ms
Maximum efficiency	TPS56C230EVM, $V_{IN} = 12\text{ V}, I_{OUT} = 4\text{ A}$	89.75%			

3 Modifications

The evaluation module is designed to provide access to the features of the TPS56C230. Some modifications can be made to this module.

3.1 Output Voltage Setpoint

The output voltage is set by the resistor divider network of R4 (R_{TOP}) and R6 (R_{BOT}). R6 is fixed at 10.0 k Ω . To change the output voltage of the EVM, it is necessary to change the value of resistor R4. Changing the value of R4 can change the output voltage above the 0.6 V reference voltage V_{REF} . The value of R4 for a specific output voltage can be calculated using [Equation 1](#).

$$R_{(TOP)} = \frac{R_{(BOT)} \cdot (V_{OUT} - V_{REF})}{V_{REF}} \quad (1)$$

3.2 Mode Selection

TPS56C230 has a MODE pin to select the operation mode. The device reads the voltage on MODE pin during start-up and latches onto one of the MODE options listed below in [Table 3](#).

Table 3. Mode Pin Resistor Settings

VOLTAGE ON MODE	R9/10/11/12 (k Ω)	R13/14/15/16 (k Ω)	OPERATION	FREQUENCY (kHz)
(0~10%)*VCC	330	15	Eco-mode	500
(10~20%)*VCC	180	33	FCCM	500

Change the position of the jumper on J4 to modify the MODE configuration before start up.

4 Test Setup and Results

This section describes how to properly connect, set up, and use the TPS56C230EVM evaluation module. The section also includes test results typical for the evaluation module and covers efficiency, output voltage regulation, line regulation, load transient response, output voltage ripple, input voltage ripple, start-up and power-off.

4.1 Input/Output Connections

The TPS56C230EVM is provided with input/output connectors and test points as shown in [Table 4](#). A power supply capable of supplying greater than 5 A must be connected to J1 through a pair of 20-AWG wires or better. The load must be connected to J2 through a pair of 20-AWG wires. The maximum load current capability is 12 A. Wire lengths must be minimized to reduce losses in the wires. Test point TP3 provides a place to monitor the V_{IN} input voltages with TP8 providing a convenient ground reference. TP5 is used to monitor the output voltage with TP11 as the ground reference.

Table 4. Connection and Test Points

REFERENCE DESIGNATOR	FUNCTION
J1	V_{IN} input connector. (see Table 1 for V_{IN} range)
J2	V_{OUT} output connector. 1.2 V at 12 A maximum.
J3	Soft start selection. Remove the shunt to set the soft start time as internal default value.
J4	MODE selection. Refer to Section 3.2 .
J5	EN control. Shunt EN to GND to disable. Shunt EN to the other side to enable.
TP1	VCC
TP2	V_{IN} terminal
TP3	V_{IN} test point
TP4	V_{OUT} terminal
TP5	V_{OUT} test point
TP6	SW node test point
TP7	Test point between voltage divider network and output. Used for loop response measurements.
TP8~11	GND test point
TP12	PGOOD test point
TP13~15	GND test point
TP16	EN test point

4.2 Efficiency

Figure 1 shows the efficiency for the TPS56C230EVM in 500kHz/Eco mode. The ambient temperature is 25 °C.

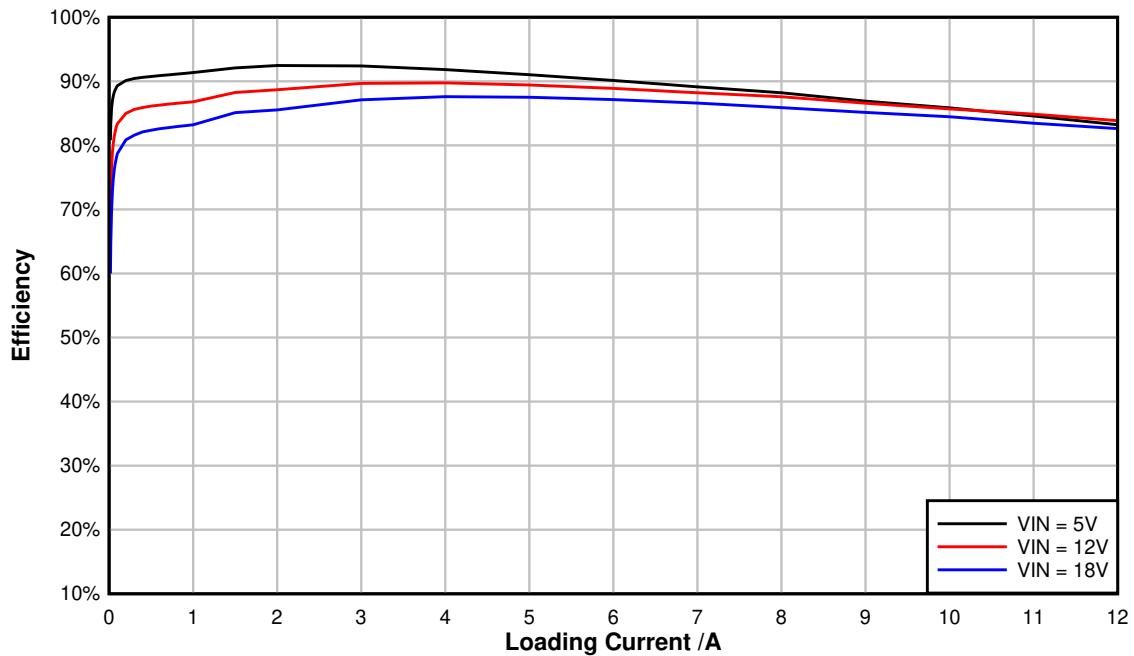


Figure 1. TPS56C230EVM Efficiency at 500-kHz/Eco mode

Figure 2 shows the efficiency at light loads for the TPS56C230EVM using a semi-log scale. The ambient temperature is 25 °C.

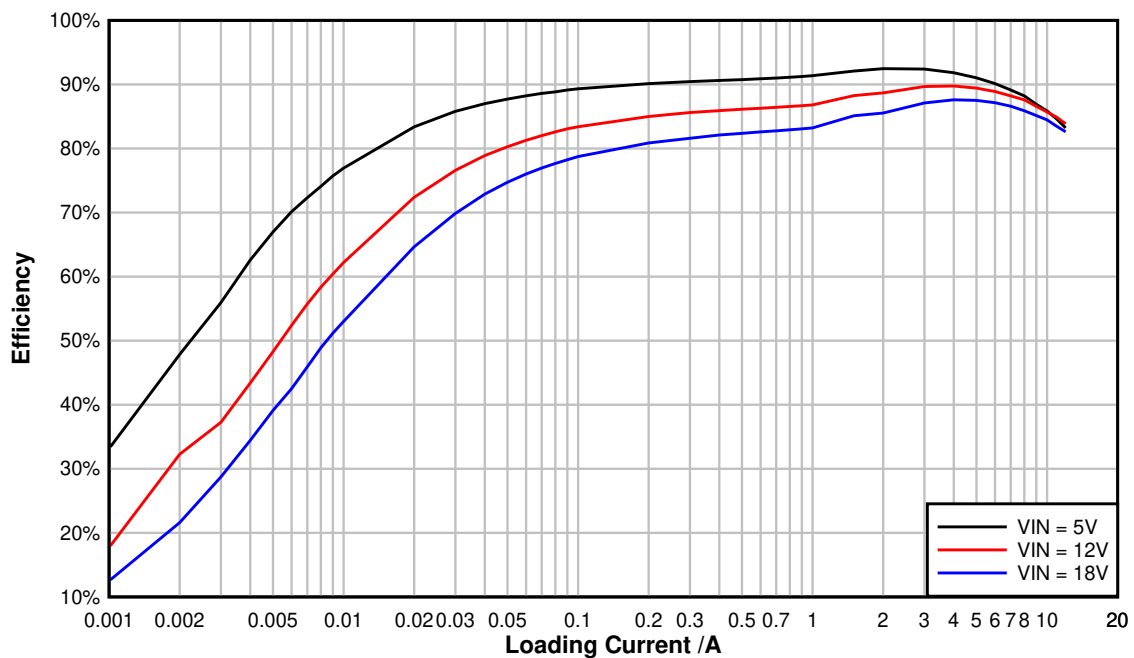


Figure 2. TPS56C230EVM Light Load Efficiency at 500-kHz/Eco Mode

The efficiency may be lower at higher ambient temperature, due to temperature variation in the drain-to-source resistance of the internal MOSFET.

4.3 Output Voltage Load Regulation

Figure 3 shows the load regulation for the TPS56C230EVM. Measurement is given for an ambient temperature of 25 °C.

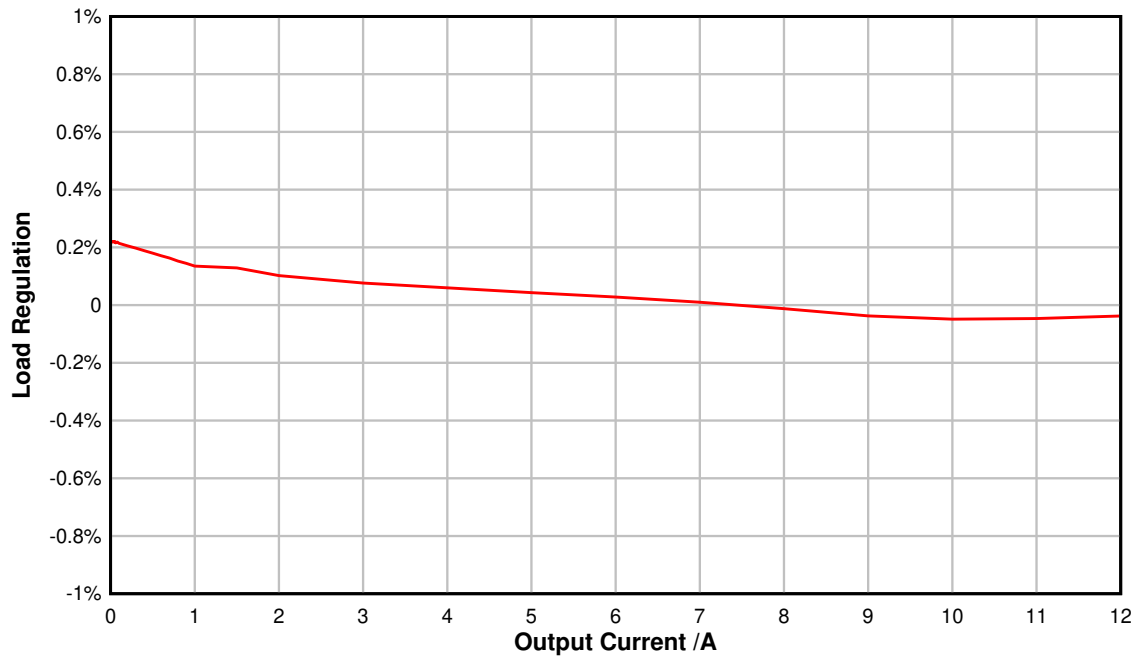


Figure 3. TPS56C230EVM Load Regulation, $V_{IN} = 12\text{ V}$

4.4 Output Voltage Line Regulation

Figure 4 shows the line regulation for the TPS56C230EVM. Measurement is given for an ambient temperature of 25 °C.

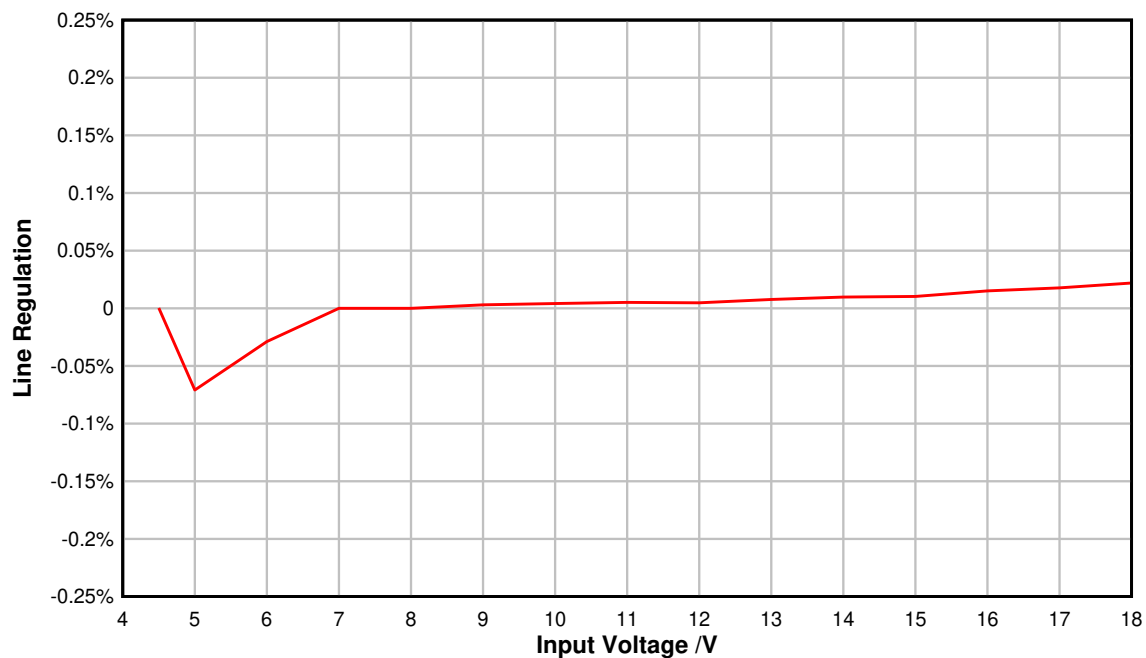


Figure 4. TPS56C230EVM Line Regulation

4.5 Load Transient Response

The TPS56C230EVM response to load transient is shown in Figure 5. The current steps and slew rates are indicated in the following figures. Total peak-to-peak voltage variation is as shown, including ripple and noise on the output.

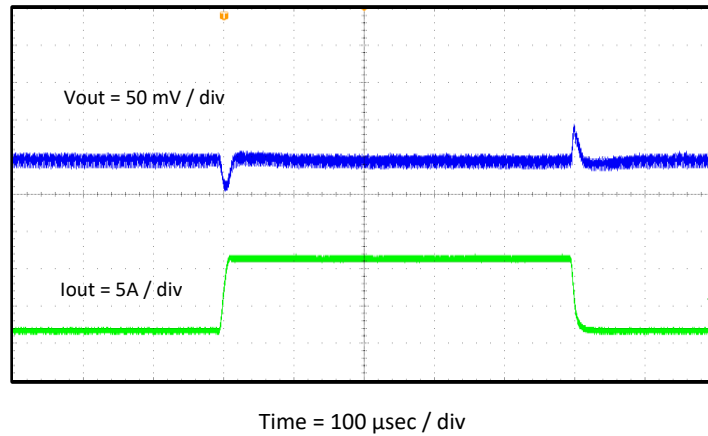


Figure 5. TPS56C230EVM Load Transient Response

4.6 Output Voltage Ripple

Figure 6, Figure 7, Figure 8 show the TPS56C230EVM output voltage ripple. The load currents are 10 mA, 800 mA, and 12 A. $V_{IN} = 12$ V. The ripple voltage is measured directly across TP5 and TP11.

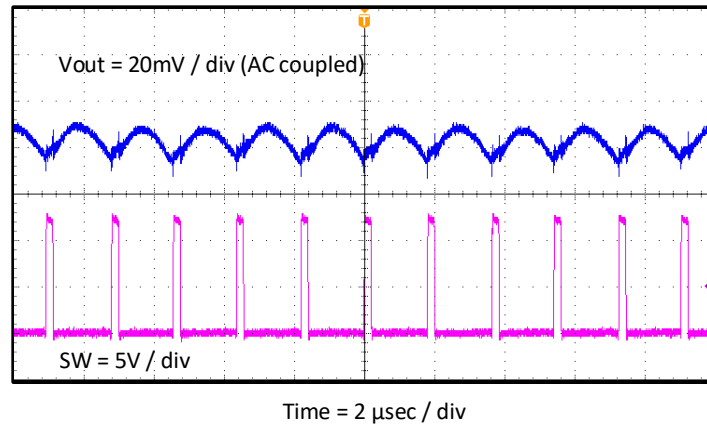


Figure 6. TPS56C230EVM Output Ripple, 10-mA Load

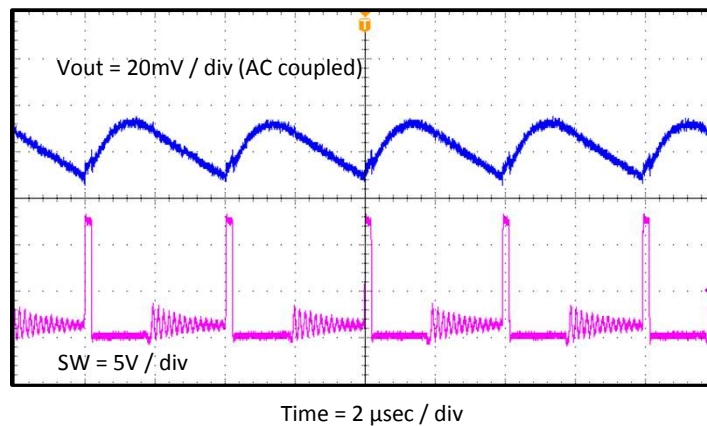


Figure 7. TPS56C230EVM Output Ripple, 800-mA Load

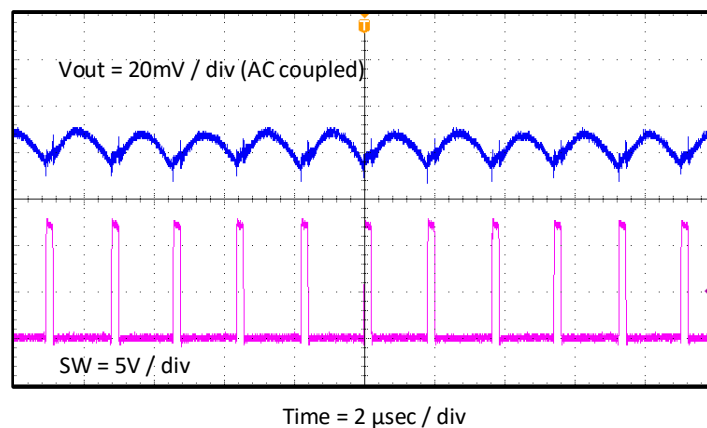
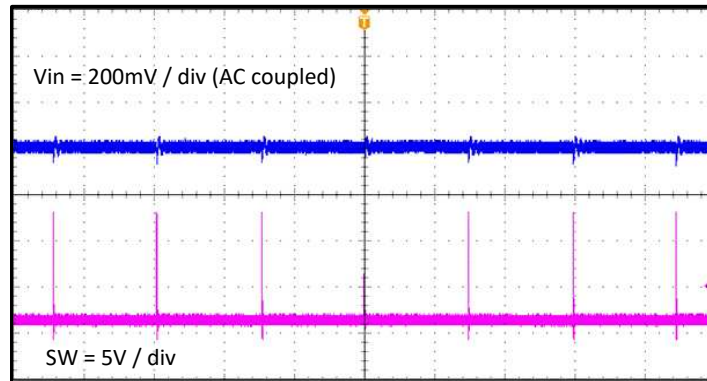


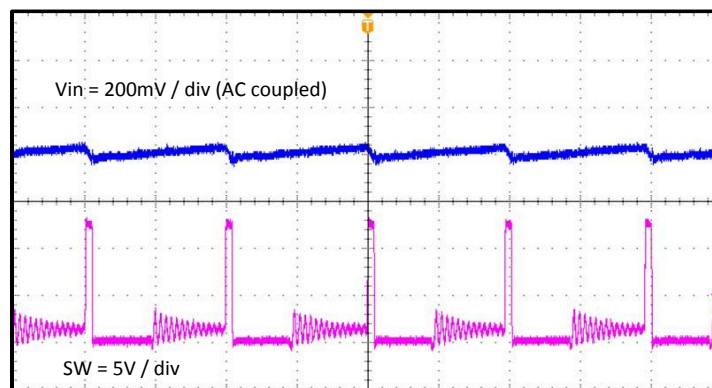
Figure 8. TPS56C230EVM Output Ripple, 12-A Load

4.7 Input Voltage Ripple

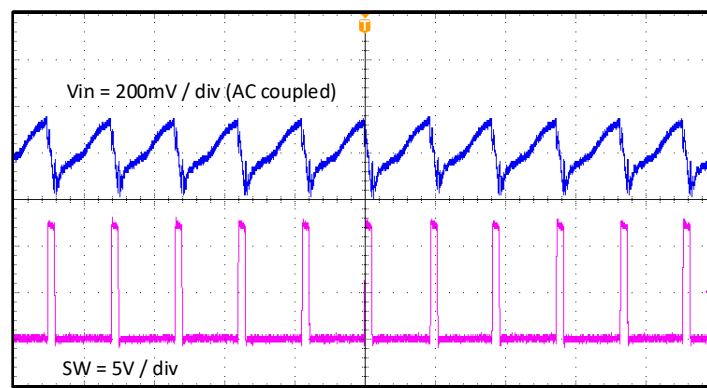
Figure 9, Figure 10 and Figure 11 show the TPS56C230EVM input voltage ripple at 500 kHz Eco-mode. The load currents are 10 mA, 800 mA and 12 A. The ripple voltage is measured directly across TP3 and TP8.



Time = 200 $\mu\text{sec} / \text{div}$
Figure 9. TPS56C230EVM Input Ripple, 10-mA Load



Time = 2 $\mu\text{sec} / \text{div}$
Figure 10. TPS56C230EVM Input Ripple, 800-mA Load



Time = 2 $\mu\text{sec} / \text{div}$
Figure 11. TPS56C230EVM Input Ripple, 12-A Load

4.8 Loop Characteristics

Figure 12 shows the TPS56C230EVM loop-response characteristics. Gain and phase plots are shown for V_{IN} voltage of 12 V. Load current for the measurement is 12 A.

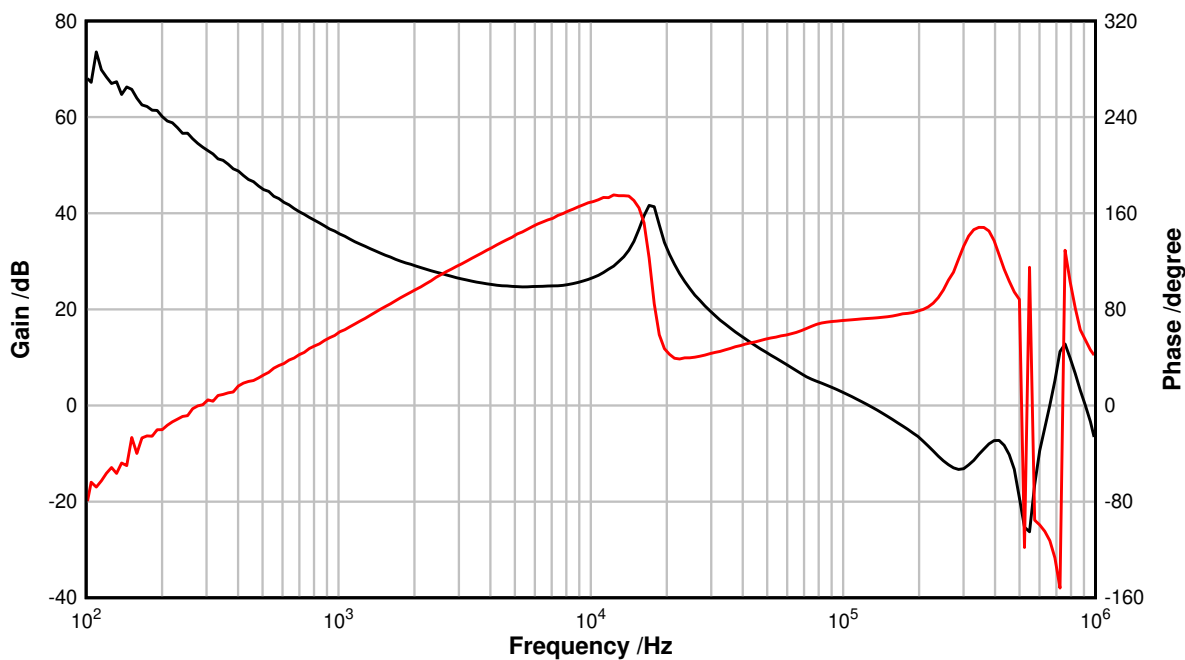


Figure 12. TPS56C230EVM Loop Response

4.9 Start-Up

Figure 13 and Figure 14 show the start-up waveforms for the TPS56C230EVM. In Figure 13, the output voltage ramps up as soon as the input voltage reaches the UVLO threshold. In Figure 14, the input voltage is initially applied and the output is inhibited by using a jumper at J5 to tie EN to GND. When the jumper is removed, EN is released. When the EN voltage reaches the enable-threshold voltage, the start-up sequence begins and the output voltage ramps up to the externally set value of 1.2 V. The input voltage for these plots is 12 V and the load is 1 Ω .

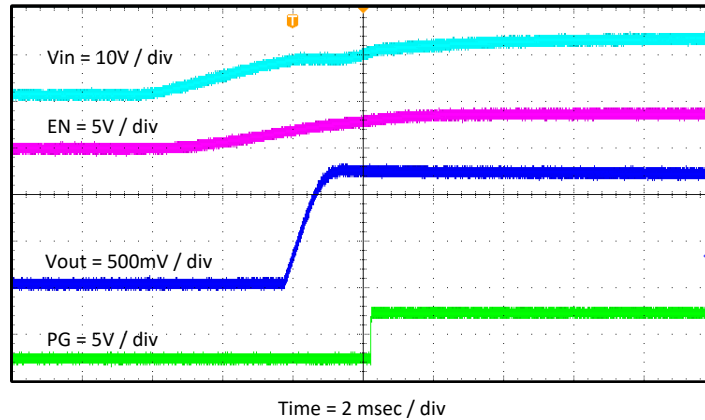


Figure 13. TPS56C230EVM Start-Up Relative to V_{IN}

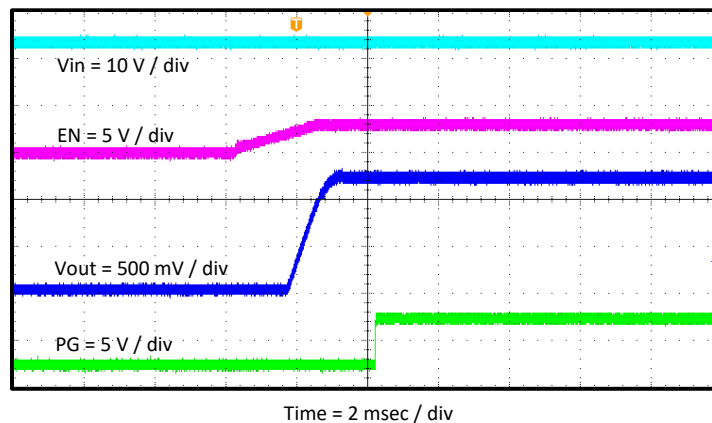


Figure 14. TPS56C230EVM Start-Up Relative to Enable

4.10 Shut-Down

Figure 15 and Figure 16 show the shutdown waveforms for the TPS56C230EVM. The input voltage for these plots is 12V and the load is 1Ω.

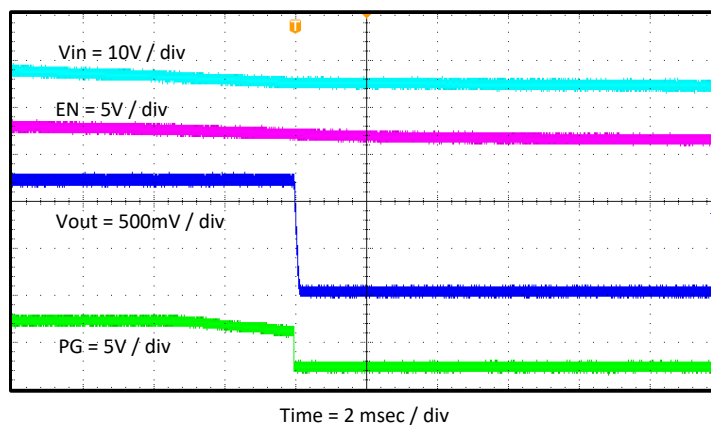


Figure 15. Shutdown Relative to V_{IN}

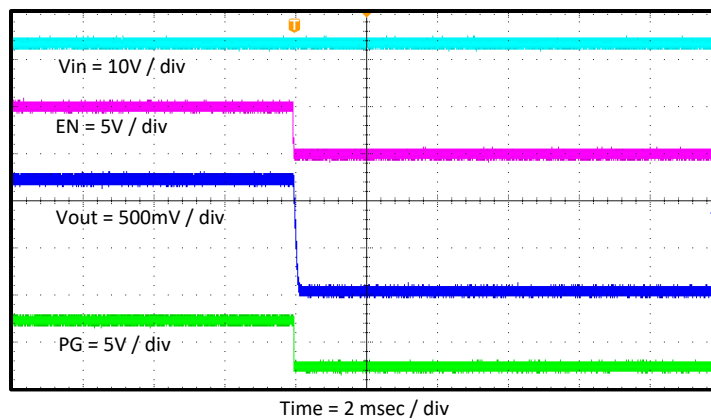


Figure 16. Shutdown Relative to Enable

5 Board Layout

This section provides a description of the TPS56C230EVM, board layout and layer illustrations.

5.1 Layout

The board layout for the TPS56C230EVM is shown in Figure 17 through Figure 21. The top and bottom layers are 2-oz copper thickness. Internal layers are 1-oz copper thickness.

The top layer contains the main power traces for VIN, VOUT and ground. Also on the top layer are connections for the pins of the TPS56C230 and a large area filled with ground. Most of the signal traces are located on the bottom left side, surrounding by a ground plane with an island for quiet analog ground that is connected to the main power ground at a single point. The internal layer-1 and internal layer-2 are dedicated ground planes. The bottom layer is another ground copper area with additional SW, VIN and VOUT copper fill. Ground traces on different layers are connected to each other with multiple vias placed on the board.

The input decoupling capacitors are located as close to the IC as possible. Critical analog circuits, such as the voltage set point divider, EN resistor, SS capacitor, Mode resistor, VCC and AGND pin are terminated to quiet analog ground island on the top layer. The input and output connectors, test points and all of the components are located on the top side. The bottom layer is a ground plane along with the switching node copper fill, VIN and VOUT copper fill and the feedback trace from the point of regulation to the top of the resistor divider network.

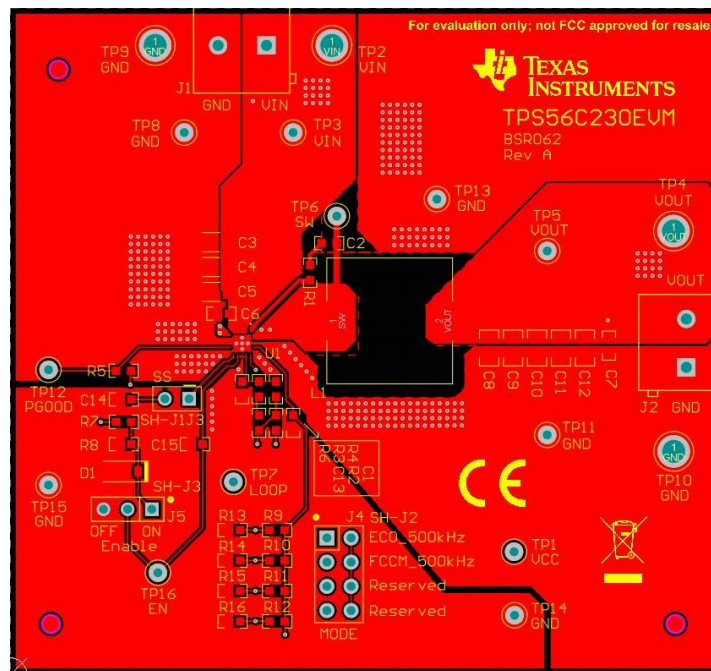


Figure 17. TPS56C230EVM Top-Side Assembly

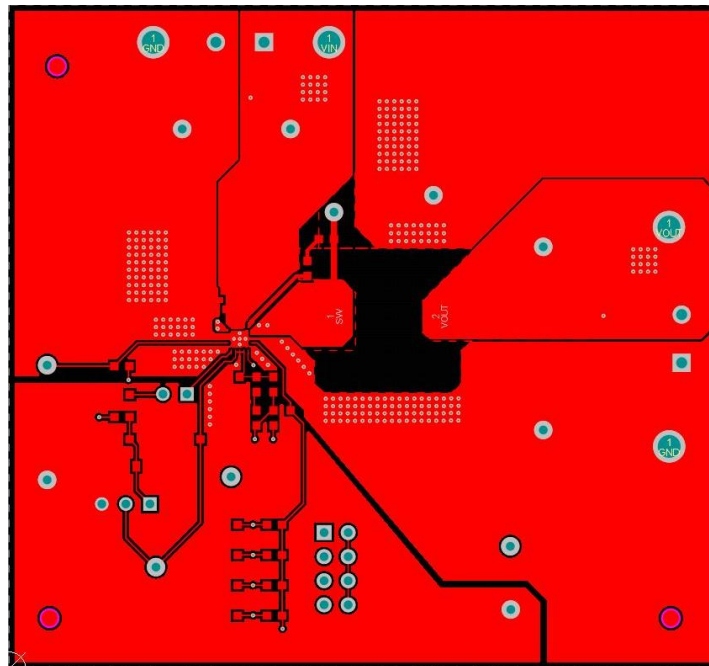


Figure 18. TPS56C230EVM Top-Side Layout

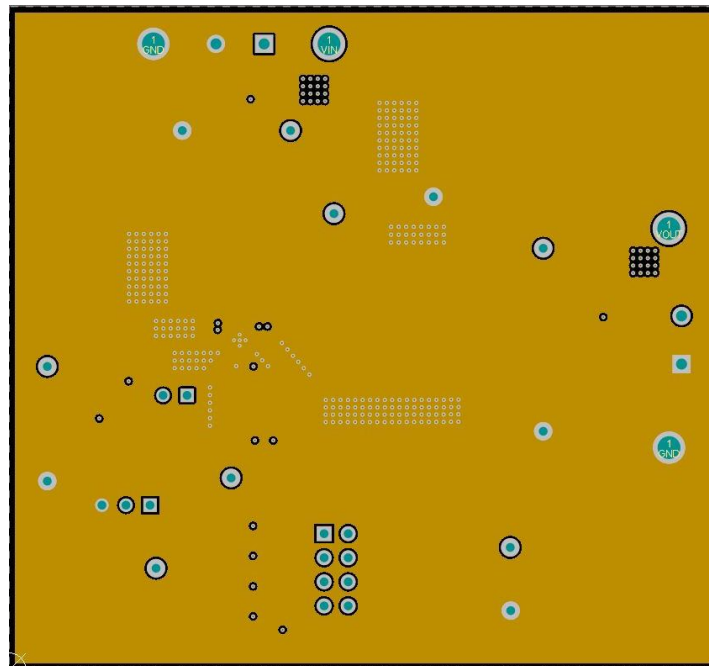


Figure 19. TPS56C230EVM Internal Layer-1 Layout

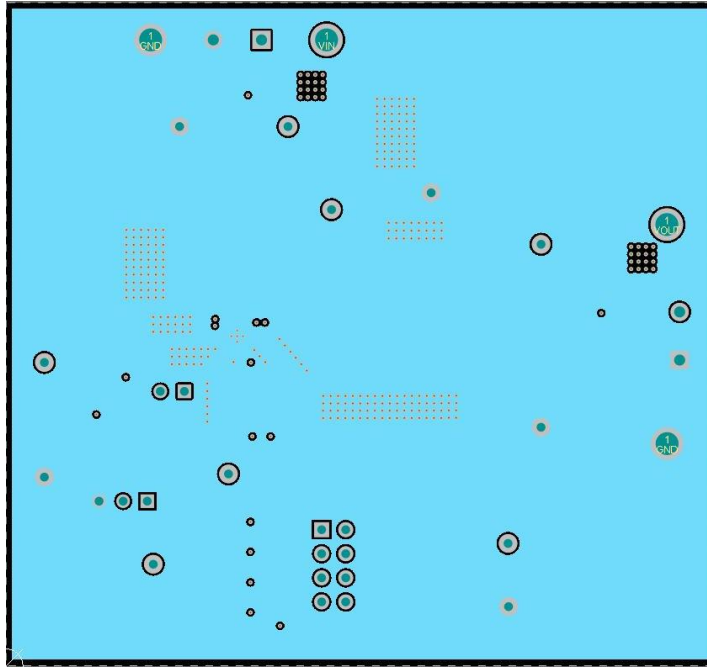


Figure 20. TPS56C230EVM Internal Layer-2 Layout

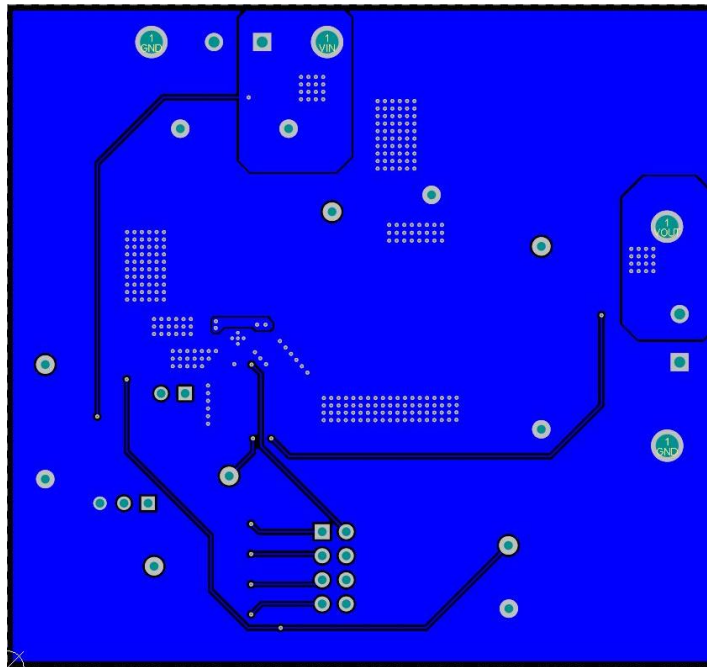


Figure 21. TPS56C230EVM Bottom Side Layout

6 Schematic, List of Materials, and Reference

6.1 Schematic

Figure 22 shows the schematic for TPS56C230EVM.

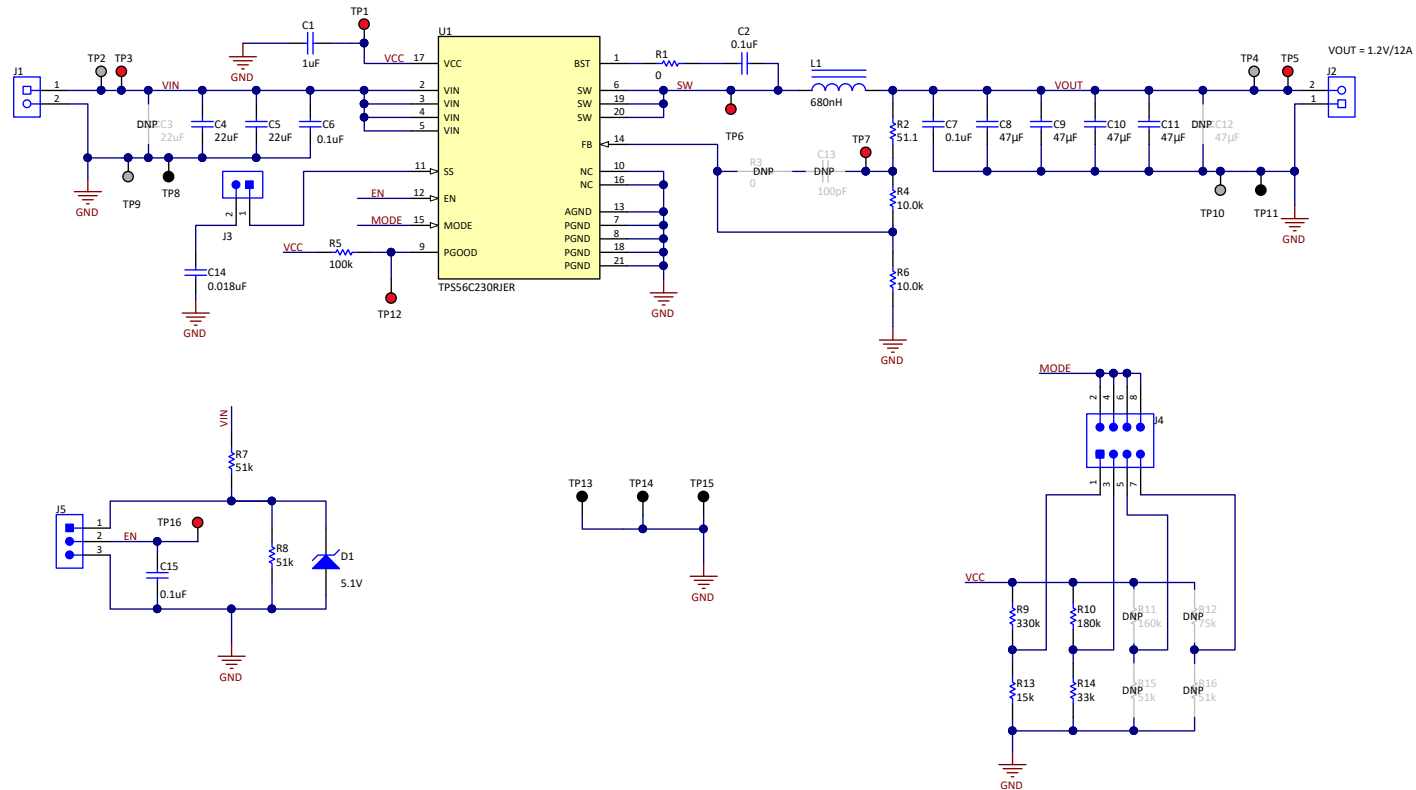


Figure 22. TPS56C230EVM Schematic

6.2 List of Materials

Table 5 presents the list of materials for the TPS56C230EVM.

Table 5. TPS56C230EVM List of Materials

DES	QTY	DESCRIPTION	PART NUMBER	MANUFACTURER
!PCB1	1	Printed circuit board	BSR062	Any
C1	1	Capacitor ceramic, 1 μ F, 25 V, \pm 10%, X5R, 0603	C1608X5R1E105K080A C	TDK
C2, C6, C7, C15	4	Capacitor ceramic, 0.1 μ F, 50 V, \pm 10%, X7R, 0603	C1608X7R1H104K080A A	TDK
C4, C5	2	Capacitor ceramic, 22 μ F, 35 V, \pm 20%, X5R, 1206	C3216X5R1V226M160A C	TDK
C8, C9, C10, C11	4	Capacitor ceramic, 47 μ F, 10 V, \pm 20%, X5R, 0805	GRM21BR61A476ME15 L	MuRata
C14	1	Capacitor ceramic, 0.018 μ F, 16 V, \pm 10%, X7R, 0603	GRM188R71C183KA01 D	MuRata
D1	1	Diode, Zener, 5.1 V, 500 mW, SOD-123	MMSZ5231B-7-F	Diodes Inc.
H1, H2, H3, H4	4	Bumpon, hemisphere, 0.44 X 0.20, clear	SJ-5303 (CLEAR)	3M
J1, J2	2	Terminal block, 5.08 mm, 2x1, brass, TH	ED120/2DS	On-Shore Technology
J3	1	Header, 100 mil, 2x1, tin, TH	PEC02SAAN	Sullins Connector Solutions
J4	1	Header, 100 mil, 4x2, tin, TH	PEC04DAAN	Sullins Connector Solutions
J5	1	Header, 100 mil, 3x1, tin, TH	PEC03SAAN	Sullins Connector Solutions
L1	1	Inductor, shielded drum core, powdered iron, 680 nH, 17.5 A, 0.0018 ohm, SMD	744373770068	Würth Elektronik
R1	1	Resistor, 0 Ω , 5%, 0.1 W, AEC-Q200 grade 0, 0603	CRCW06030000Z0EA	Vishay-Dale
R2	1	Resistor, 51.1 Ω , 1%, 0.1 W, AEC-Q200 grade 0, 0603	CRCW060351R1FKFA	Vishay-Dale
R4, R6	2	Resistor, 10.0 k Ω , 1%, 0.1 W, AEC-Q200 grade 0, 0603	CRCW060310K0FKFA	Vishay-Dale
R5	1	Resistor, 100 k Ω , 1%, 0.1 W, AEC-Q200 grade 0, 0603	CRCW0603100KFKFA	Vishay-Dale
R7, R8	2	Resistor, 51 k Ω , 5%, 0.1 W, AEC-Q200 grade 0, 0603	CRCW060351K0JNEA	Vishay-Dale
R9	1	Resistor, 330 k Ω , 5%, 0.1 W, AEC-Q200 grade 0, 0603	CRCW0603330KJNEA	Vishay-Dale
R10	1	Resistor, 180 k Ω , 1%, 0.1 W, AEC-Q200 grade 0, 0603	CRCW0603180KJNEA	Vishay-Dale
R13	1	Resistor, 15 k Ω , 5%, 0.1 W, AEC-Q200 grade 0, 0603	CRCW060315K0JNEA	Vishay-Dale
R14	1	Resistor, 33 k Ω , 5%, 0.1 W, AEC-Q200 grade 0, 0603	CRCW060333K0JNEA	Vishay-Dale
SH-J1, SH-J2, SH-J3	3	Shunt, 100 mil, gold plated, black	SNT-100-BK-G	Samtec
TP1, TP3, TP5, TP6, TP7, TP12, TP16	7	Test point, miniature, red, TH	5000	Keystone
TP2, TP4, TP9, TP10	4	Terminal, turret, TH, triple	1598-2	Keystone
TP8, TP11, TP13, TP14, TP15	5	Test point, miniature, black, TH	5001	Keystone
U1	1	4.5-V to 18-V Input, 12-A Synchronous Step-Down Voltage Regulator, RJE0020B (VQFN-20)	TPS56C230RJER	Texas Instruments
C3	0	Capacitor ceramic, 22 μ F, 35 V, \pm 20%, X5R, 1206	C3216X5R1V226M160A C	TDK
C12	0	Capacitor ceramic, 47 μ F, 10 V, \pm 20%, X5R, 0805	GRM21BR61A476ME15 L	MuRata
C13	0	Capacitor ceramic, 100 pF, 25 V, \pm 10%, X7R, 0603	06033C101KAT2A	AVX
FID1, FID2, FID3	0	Fiducial mark. There is nothing to buy or mount.	N/A	N/A

Table 5. TPS56C230EVM List of Materials (continued)

DES	QTY	DESCRIPTION	PART NUMBER	MANUFACTURER
R3	0	Resistor, 0 Ω , 5%, 0.1 W, AEC-Q200 grade 0, 0603	CRCW06030000Z0EA	Vishay-Dale
R11	0	Resistor, 160 k Ω , 5%, 0.1 W, AEC-Q200 grade 0, 0603	CRCW0603160KJNEA	Vishay-Dale
R12	0	Resistor, 75 k Ω , 5%, 0.1 W, AEC-Q200 grade 0, 0603	CRCW060375K0JNEA	Vishay-Dale
R15, R16	0	Resistor, 51 k Ω , 5%, 0.1 W, AEC-Q200 grade 0, 0603	CRCW060351K0JNEA	Vishay-Dale

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (January 2019) to A Revision
Page

-
- Added updated List of Materials. 19
-

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2019, Texas Instruments Incorporated