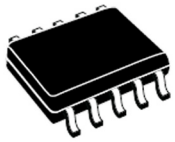
SRK2001A

Adaptive synchronous rectification controller for LLC resonant converter

Datasheet - production data



SSOP10

Features

- Secondary side synchronous rectification controller optimized for LLC resonant converter
- Dual gate driver for N-channel MOSFETs
- Adaptive turn-off logic
- Turn-on logic with adaptive masking time
- Auto-compensation of parasitic inductance
- Low consumption mode: 50 µA quiescent current
- V_{CC} operating voltage range 4.5 V to 32 V
- High voltage drain-to-source Kelvin sensing for each SR MOSFET
- Operating frequency up to 500 kHz
- Programmable exit load levels from burst-mode
- SSOP10 package

Applications

- AC-DC adapters
- All-in-one PC
- High-end flat panel TV
- 80+/85+ compliant ATX SMPS
- 90+/92+ compliant SERVER SMPS
- Industrial SMPS

Description

The SRK2001A controller implements a control scheme specific for secondary side synchronous rectification in LLC resonant converters that use a transformer with center tap secondary winding for full wave rectification.

It provides two high current gate drive outputs, each capable of directly driving N-channel power MOSFETs. Each gate driver is controlled separately and an interlock logic circuit prevents the two synchronous rectifier MOSFETs from conducting simultaneously.

The driver high-level voltage is clamped to 11 V in order to avoid providing excessive gate charge to SR MOSFETs, in case the device is supplied at higher VCC voltages.

The control scheme in this IC provides for each synchronous rectifier being switched on as the corresponding half-winding starts conducting and switched off as its current goes to zero.

The turn-on logic with adaptive masking time (up to 10% of clock cycle) and innovative adaptive turn-off logic allow maximizing the conduction time of the SR MOSFETs, eliminating the need of the parasitic inductance compensation circuit.

The low consumption mode of the device allows to meet the most stringent requirement for converter power consumption in light-load and no load conditions.

A noticeable feature is the very low external component count required.

Table 1. Device summary

Order code	Package	Packing
SRK2001A	SSOP10	Tube
SRK2001ATR		Tape and reel

This is information on a product in full production. www.st.com

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1 Block diagrams

Figure 1. Internal block diagram

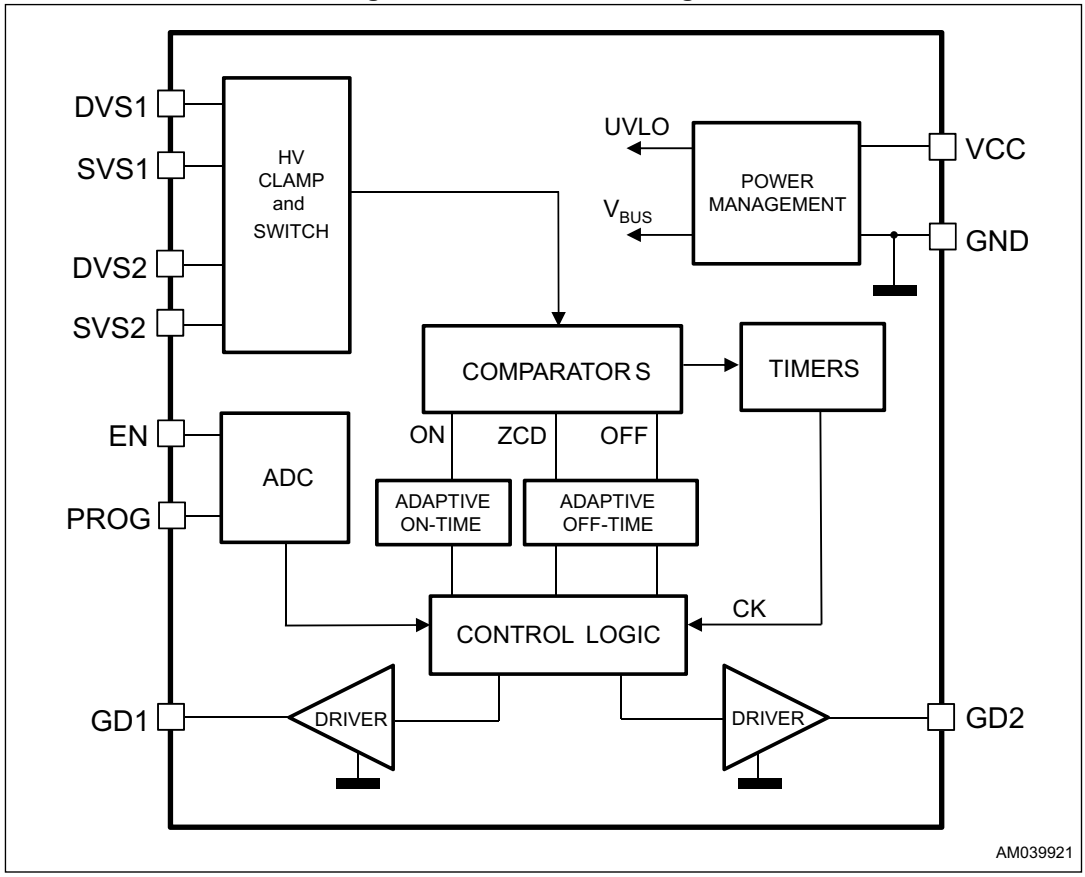
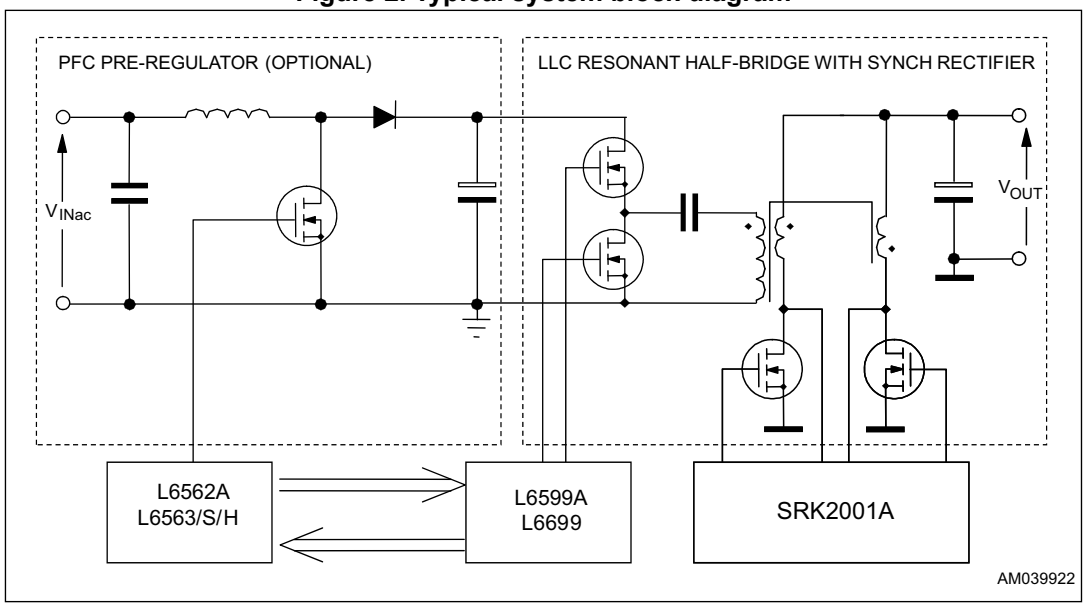


Figure 2. Typical system block diagram



2 Pin connections and functions

Figure 3. Pin connections (top view)

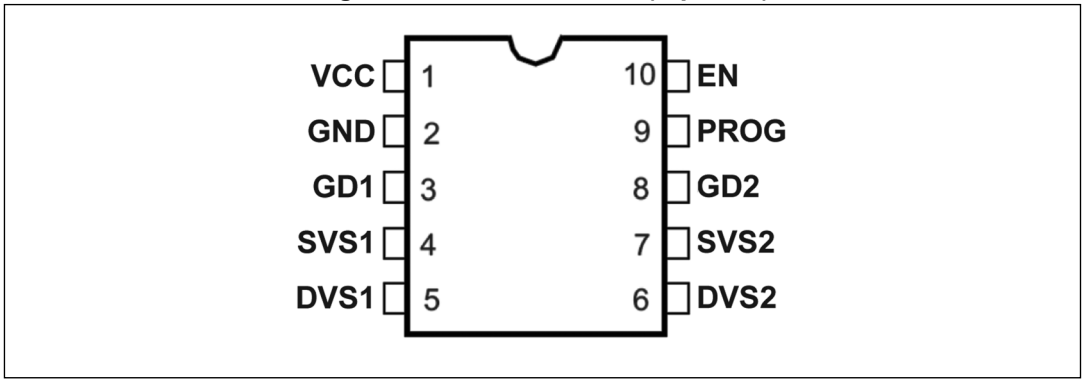


Table 2. Pin functions

No.	Name	Function
1	VCC	Supply voltage of the device. A bypass capacitor to GND, located as close to IC's pins as possible, helps to get a clean supply voltage for the internal control circuitry and acts as an effective energy buffer for the pulsed gate drive currents.
2	GND	Return of the device bias current and return of the gate drive currents. Route this pin to the common point where the source terminals of both synchronous rectifier MOSFETs are connected.
3 (8)	GD1 (GD2)	Gate driver output for section 1 (2). Each totem pole output stage is able to drive power MOSFETs with high peak current levels. To avoid excessive gate voltages in case the device is supplied with a high V_{CC}, the high-level voltage of these pins is clamped to about 11 V. The pin has to be connected directly to the SR MOSFET gate terminal.
4 (7)	SVS1 (SVS2)	Source voltage sensing for section 1 (2): it is the reference voltage of the corresponding drain sensing signal on the DVS1,2 pin. These pins have to be connected directly to the respective source terminals of the corresponding synchronous rectifier MOSFET.
5 (6)	DVS1 (DVS2)	Drain voltage sensing for section 1 (2). These pins have to be connected to the respective drain terminals of the corresponding synchronous rectifier MOSFET using a series resistor of 100 Ω.
9	PROG	Programming pin for conduction duty-cycle at burst-mode exiting. A resistor connected from this pin to GND, supplied by an internal precise current source, sets a voltage V_{PROG}; depending on this voltage level, during the start-up phase, the user can choose, according to the application requirements, the proper burst-mode exiting conduction duty-cycle among the ones contained in an internal lookup table which values are reported in *Table 6* (the values are predefined inside the table). For the proper choice of the resistor value see *Table 5*.
10	EN	Enable pin function with internal pull-up (remote ON/OFF): during the run mode, when the pin voltage is sensed below the internal threshold V_{EN_OFF}, the controller stops operating and enters a low consumption state; it resumes the operation if the pin voltage surpasses the threshold V_{EN_ON}.

3 Absolute maximum ratings

Table 3. Absolute maximum ratings

Symbol	Pin	Parameter	Value	Unit
V_{CC}	1	DC supply voltage	-0.3 to V_{CCZ}	V
I_{CCZ}	1	Internal Zener maximum current (V_{CC} = V_{CCZ})	25	mA
V_{PROG}	10	PROG pin voltage rating	-0.3 to 3.3	V
V_{EN}	9	EN pin voltage rating	-0.3 to 3.3	V
DVS1,2	5, 6	Drain sense voltage referred to source SVS1,2	-3 to 90	V
SVS1,2	4, 7	Source sense voltage referred to GND	-3 to 3	V

4 Thermal data

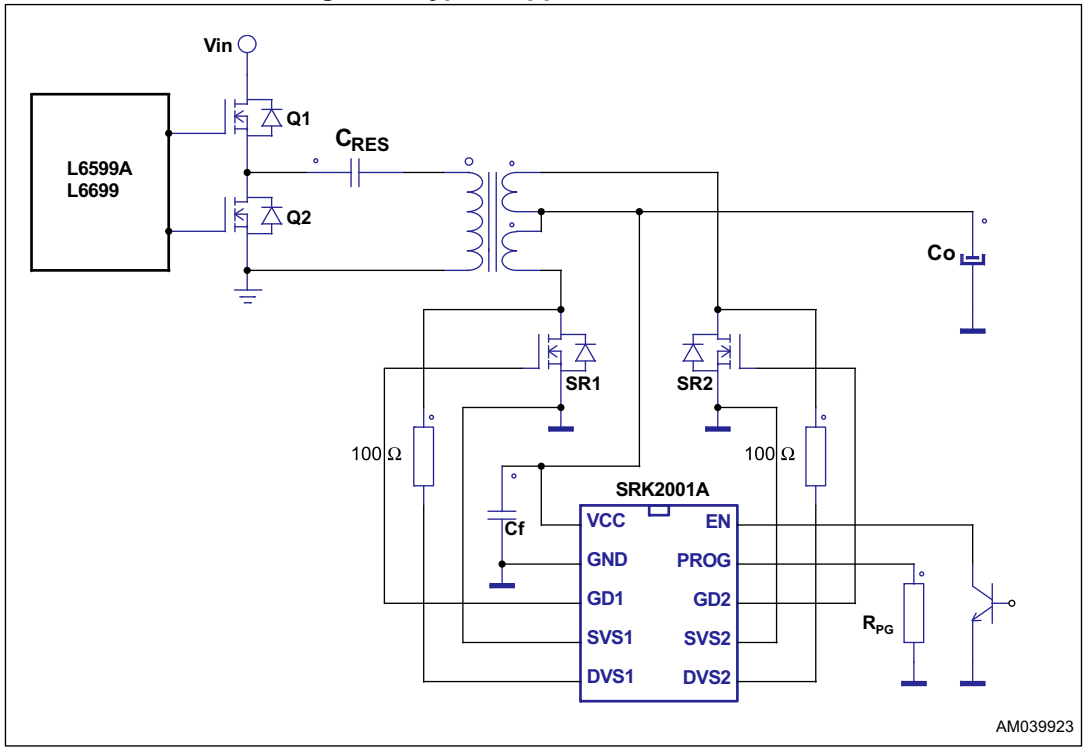
Table 4. Thermal data

Symbol	Parameter	Value	Unit
$R_{th\ j\text{-}amb}$	Max. thermal resistance, junction to ambient(1)	130	°C/W
$R_{th\ j\text{-}case}$	Max. thermal resistance, junction to case top(1)	10	°C/W
P_{tot}	Power dissipation at T_{amb} = 50 °C	0.75	W
T_j	Junction temperature operating range	-40 to 150	°C
T_{stg}	Storage temperature	-55 to 150	°C

1. With the pin 2 soldered to a dissipating copper area of 25 mm2, 35 µm thickness (PCB material FR4 1.6 mm thickness).

5 Typical application schematic

Figure 4. Typical application schematic



6 Electrical characteristics

(T_j = -25 to 125 °C, V_{CC} = 12 V, C_{GD1} = C_{GD2} = 4.7 nF, R_{PG} = 0 Ω; unless otherwise specified, typical values refer to T_j = 25 °C).

Table 5. Electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
SUPPLY SECTION						
V_{CC}	Operating range	After turn-on	4.5		32	V
V_{CC_On}	Turn-on supply voltage	(1)	4.25	4.5	4.75	V
V_{CC_Off}	Turn-off supply voltage	(1)	4	4.25	4.5	V
Hys	Hysteresis			0.25		V
V_{CCZ}	Clamp voltage	I_{CCZ} = 20 mA	33	36	39	V
I_{q_run}	Current consumption in run mode	After turn-on (excluding SR MOS gate capacitance charging/discharging) at 100 kHz		700		µA
I_{CC}	Operating supply current	At 300 kHz		35		mA
I_q	Quiescent current	Low-consumption mode operation, with DVS1,2 pins not switching(2), T_j = -25 °C to 85 °C		50	65	µA
DRAIN-SOURCE SENSING INPUTS AND SYNCH FUNCTIONS						
$V_{DS1,2_H}$	Drain-to-source sensing operating voltage				90	V
V_{TH_A}	Arming voltage	Positive-going edge		1.4		V
V_{TH_PT}	Pre-triggering voltage	Negative-going edge		0.7		V
V_{TH_ON}	Turn-on threshold	Negative-going edge	-130	-100	-70	mV
T_{diode_off}	Body diode residual conduction time after turn-off			75		ns
$T_{D_On_min}$	Minimum turn-on delay			100		ns
$T_{D_On_max}$	Maximum turn-on delay	At 100 kHz		0.5		µs
ENABLE PIN REMOTE ON/OFF FUNCTION						
V_{EN_OFF}	Disable threshold	(1)Negative-going edge during run mode	0.25	0.3	0.35	V
V_{EN_ON}	Enable threshold	(1)Positive-going edge during run mode	0.45	0.62	0.82	V
I_{EN_run}	Sourced current	During run mode	4	6	8	µA

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
BURST-MODE EXITING PROGRAMMING						
D_{ON}	Restart duty-cycle during primary controller burst-mode operation	R_{PG} = 0 Ω		80		%
		R_{PG} = 100 kΩ 1%		75		
		R_{PG} = 180 kΩ 1%		65		
		R_{PG} open		0		
I_{PROG}	Sourced current	(1)At V_{CC} startup	9	10	11	µA
GATE DRIVERS						
I_{source_pk}	Output source peak current	(3)		-0.35		A
$I_{sink_pk_ZCD}$	Max. output sink peak current	ZCD comparator triggered turn-off (3)		4		A
t_r	Rise time			140		ns
t_f	Fall time (adaptive turn-off comparator)	Adaptive turn-off triggered turn-off		80		ns
t_{f_ZCD}	Fall time (ZCD_OFF comparator)	ZCD_OFF comparator triggered turn-off		30		ns
$V_{GDclamp}$	Output clamp voltage	I_{GD} = -5 mA; V_{CC} = 20 V	9	11	13	V
V_{GDL_UVLO}	UVLO saturation	V_{CC} = 0 to V_{CC_On}, I_{sink} = 5 mA		1	1.3	V

1. Parameters tracking each other.
2. Low consumption mode is one of the following: primary converter burst-mode detect or the EN pin pulled low.
3. Parameter guaranteed by design.

7 Operation description

The device block diagram is shown in *Figure 1*. The SRK2001A can be supplied through the VCC pin by the same converter output voltage, within a wide voltage range (from 4.5 V to 32 V), internally clamped to V_{CCZ} (36 V typical). An internal UVLO (undervoltage lockout) circuit with hysteresis keeps the device switched off at supply voltage lower than the turn-on level V_{CC_On}, with reduced consumption.

After the startup, the operation with V_{CC} floating (or disconnected by supply voltage) while pins DVS1,2 are switching is not allowed: this in order to avoid that a dV/dt on the DVS pin may cause a high flowing current with possible damage of the IC.

The core of the device is the control logic block, implemented by asynchronous logic: this digital circuit generates the logic signals to the output drivers, so that the two external power MOSFETs are switched on and off, depending on the evolution of their drain-source voltages, sensed on the DVS-SVS pin pairs through the comparators block.

The logic that controls the driving of the two SR MOSFETs is based on two gate-driver state machines working in parallel in an interlocked way to avoid switching on both gate drivers at the same time. A third state machine manages the transitions from the normal operation to the low consumption mode and vice versa.

7.1 Drain voltage sensing

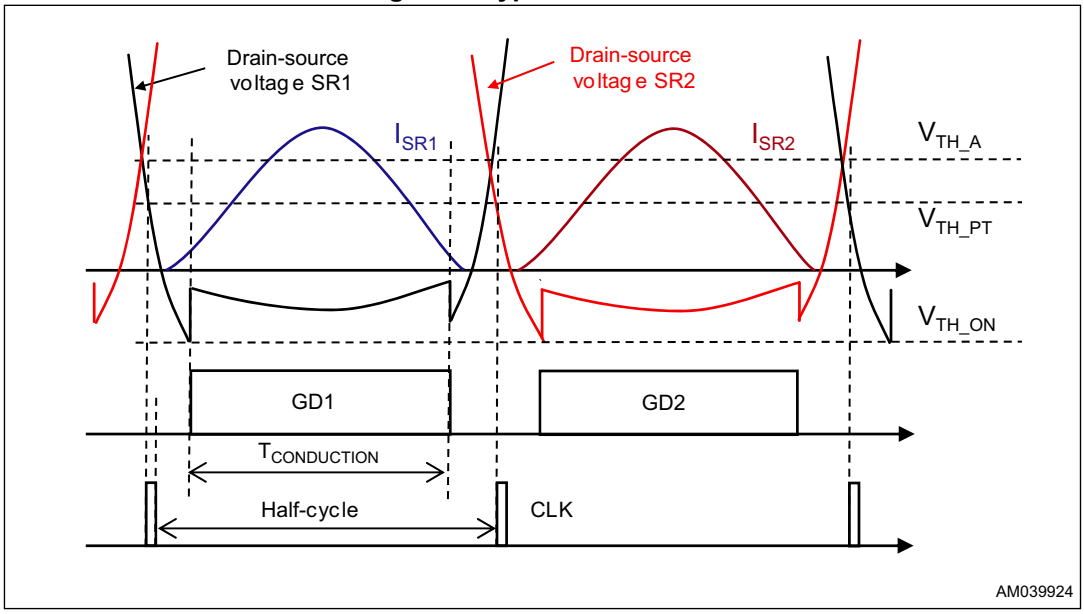
The SRK2001A basic operation is such that each synchronous rectifier MOSFET is switched on whenever the corresponding transformer half-winding starts conducting (i.e. when the MOSFET body diode, or an external diode in parallel, starts conducting) and it is then switched off when the flowing current approaches zero. To understand the polarity and the level of this current, the IC is provided with two pairs of pins (DVS1-SVS1 and DVS2-SVS2) that sense the drain-source voltage of either MOSFET (Kelvin sensing). In order to limit dynamic current injection in any condition, at least 100 Ω resistors in series to DVS1,2 pins must be used.

Referring to the typical waveforms in *Figure 5*, there are three significant voltage thresholds: the first one, V_{TH_A} (= 1.4 V), sensitive to positive-going edges, arms the opposite gate driver (interlock function). The second one, V_{TH_PT} (= 0.7 V), sensitive to negative-going edges provides a pre-trigger of the gate driver and sets the internal clock; the third one $V_{TH\text{-}ON}$ is the (negative) threshold that triggers the gate driver as the body diode of the SR MOSFET starts conducting.

7.2 Turn-on

The turn-on logic is such that each SR MOSFET is switched on when the sensed drain-source voltage goes below the V_{TH_ON} threshold: to avoid false triggering of the gate driver, an adaptive masking delay T_{D_On} is introduced. This delay assumes a minimum value at the high load ($T_{D_On.min}$) and increases with decreasing load levels (up to $T_{D_On.max}$ equal to 10% of the clock cycle).

Figure 5. Typical waveforms



The aim of T_{D_On} is to avoid a premature turn-on at lower load conditions, triggered by capacitive currents (due to secondary side parasitic capacitance and not really related to the current flowing through the MOSFET body diode. *Figure 6* shows the effect of this parasitic: in case at the reduced load a capacitive current spike should trigger the turn-on, there would be a current inversion (flowing from the output capacitor toward the SR MOSFET). This current inversion would cause a discharge of the output capacitor and consequently an increase of the rectified current rms value, in order to balance that dis-charge; this, in turn, would affect a bit the converter efficiency.

In case of SR MOSFETs with low parasitic capacitance, capacitive currents lasting less than 10% of the clock cycle are filtered: the gate drive of course will go high when the current really flows through the body diode (i.e. the comparator sensing DVS1,2 signal and referenced to the V_{TH_ON} threshold is triggered). In case of SR MOSFETs with higher parasitic capacitance, capacitive currents lasting more than 10% of the clock cycle cannot be filtered by the turn-on delay and premature turn-on will be present.

Figure 6. Capacitive current spike effect at turn-on

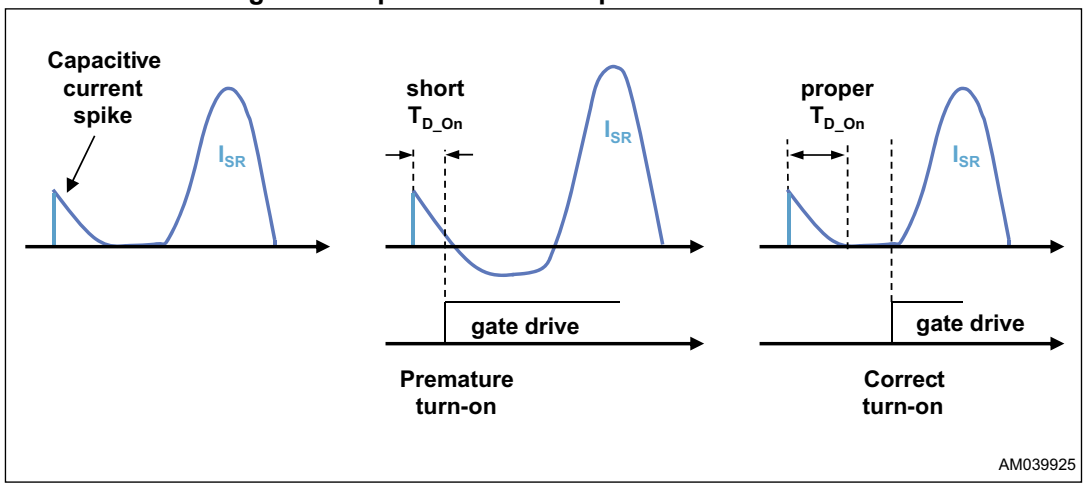
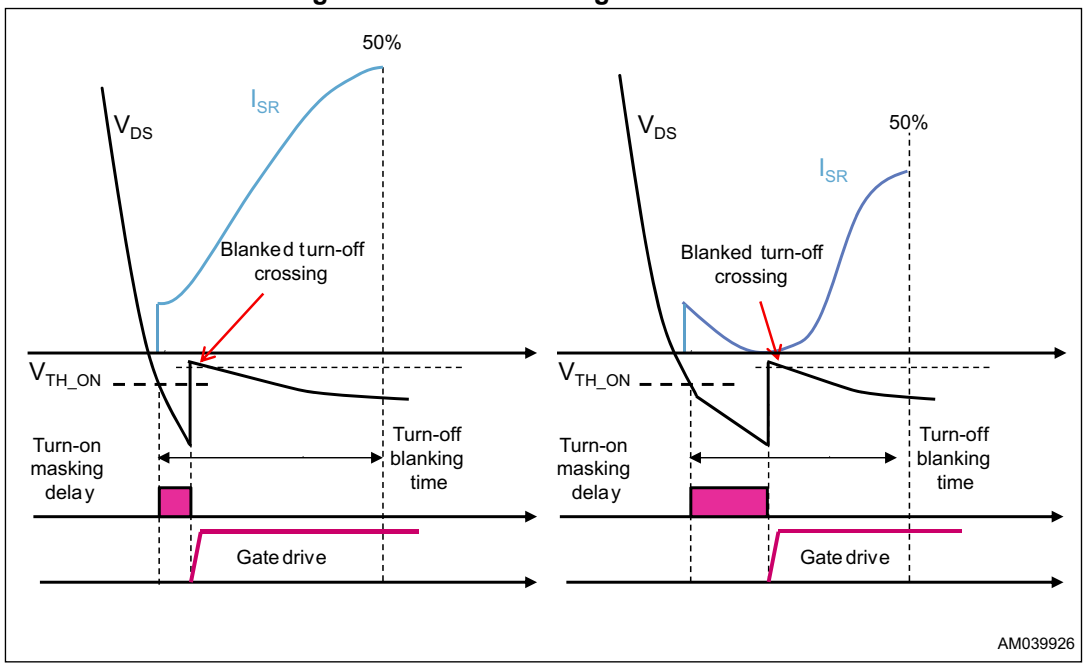


Figure 7 shows the turn-on at the full load with a minimum delay ($T_{D_On_min}$) and at the reduced load with an increased delay (up to $T_{D_On.max}$ equal to 10% of the clock cycle).

At the startup and on the low consumption mode exiting, the control circuit starts with a turn-on delay set to 7% of the clock cycle and progressively adapts it to the proper value.

Figure 7. Full load and light load turn-on



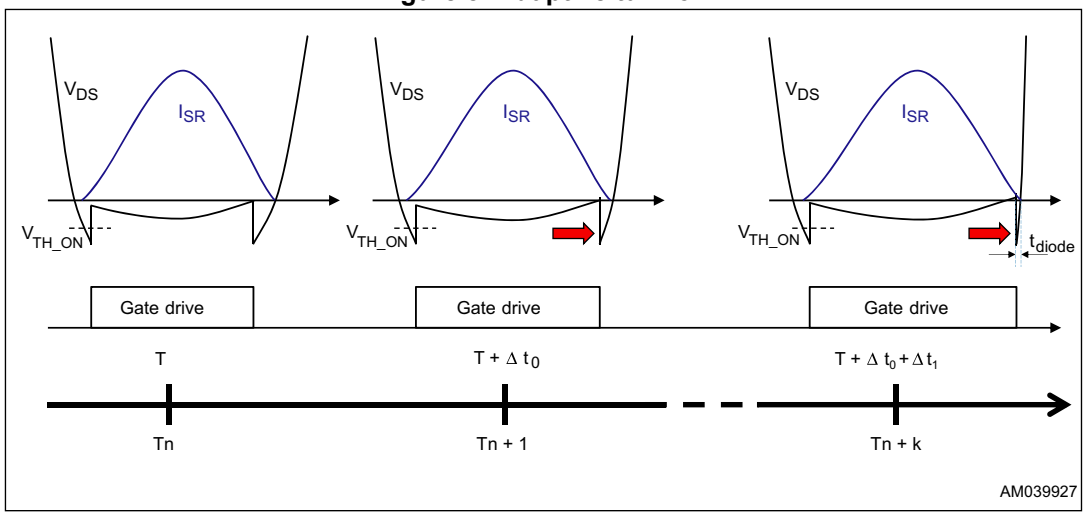
7.3 Adaptive turn-off

The SR MOSFET turn-off may be triggered by two different mechanisms: by the adaptive turn-off mechanism (two-slope turn-off) or by the ZCD_OFF comparator (fast turn-off, see *Section 7.4*).

Due to the stray inductance in series with the SR MOSFET $R_{DS(on)}$ (mainly the package stray inductance), the sensed drain-source signal is not really equal to the voltage drop across the MOSFET $R_{DS(on)}$, but it anticipates the time instant where the current reaches zero, causing a premature MOSFET turn-off.

To overcome this problem (without adding any stray inductance compensation circuit), the device uses a turn-off mechanism based on an adaptive algorithm. This consists in turning off the SR MOSFET with a certain delay after the sensed drain-source voltage has reached zero and adapting progressively this delay in order to maximize the conduction period and get the target residual conduction (T_{diode}) of the MOSFET body diode after the turn-off. *Figure 8* shows this adaptive algorithm: cycle-by-cycle the conduction time is maximized allowing in a steady-state the maximum converter efficiency.

Figure 8. Adaptive turn-off



After the turn-on, a blanking time (equal to 50% of the clock period - refer to *Figure 6*) masks the adaptive turn-off mechanism in order to avoid an undesired turn-off due to the drain-source voltage drop, consequent to the MOSFET switch-on (the flowing current passes from the body diode to MOSFET channel resistance) or due to the ringing generated at the MOSFET turn-on.

During the startup and on the low consumption mode exiting, the control circuit turns off the SR MOSFET at 50% of the clock cycle and progressively adapts this delay in order to maximize the SR MOSFET conduction time. This helps reducing system perturbations.

7.4 ZCD_OFF comparator turn-off

The IC is equipped with a ZCD_OFF comparator that is always ready to quickly turn-off the SR MOSFETs, avoiding in this way current inversions, that would cause SR MOSFETs failure and even half-bridge destruction, in case of the primary controller not equipped with proper protections.

The ZCD_OFF comparator acts during fast transient conditions, where a sudden slope variation of the rectified current presents or when (after a quick frequency change) the above resonance operation occurs. It senses that the current has reached the zero level and triggers the gate drive circuit for a very fast MOSFET turn-off. The ZCD_OFF comparator threshold is not fixed but self-adaptive. In fact, after a turn-off by the ZCD_OFF comparator, the circuit senses the body diode residual conduction: if it is longer than the target value T_{diode}, the comparator threshold is increased (by an amount proportional to the difference between the residual diode conduction and the target value), so that in the next cycle the residual body diode conduction is decreased. At the end, the comparator threshold sets to such a level that the turn-off is accomplished by the adaptive turn-off mechanism, while the ZCD_OFF comparator is ready to protect in case of a transient condition. Therefore, in the steady state load operation and in case of slow load transitions, the turn-off is prevalently managed by the adaptive mechanism (characterized by the two-slope turn-off driving). Instead, during fast transitions or during sudden above resonance operation, the ZCD_OFF comparator will take over, driving a fast MOSFET switch-off that prevents undesired current inversions.

The ZCD_OFF comparator is blanked for 300 ns after the turn-on time instant in order to avoid a premature turn-off: in fact, soon after the turn-on, the sensed drain-source voltage may cross the turn-off threshold due to switching noise on parasitic stray inductance, which may trigger the ZCD_OFF comparator.

Depending on SR MOSFET choice, some premature turn-off triggered by the ZCD_OFF comparator may be found at the low-load, due to the noise present on the drain-source sensed signal: this is worse with lower R_{DS_ON} (due to worse signal to noise ratio) and lower stray inductance of the MOSFET package. Normally the load level where this may happen is such that the circuit has already entered a low consumption state (for example in burst-mode from primary controller); if this is not the case, some noise reduction may be helpful, for example by using RC snubbers across the SR MOSFETs drain-source.

7.5 Gate drive

The IC is provided with two high current gate-drive outputs, each capable of driving one or more N-channel power MOSFETs in parallel.

The high-level voltage provided by the driver is clamped at $V_{GDclamp}$ in order to avoid excessive voltage levels on the gate in case the device is supplied with a high V_{CC}, thus minimizing the gate charge provided in each switching cycle.

The two gate drivers have a pull-down capability that ensures the SR MOSFETs cannot be spuriously turned on even at low V_{CC}: in fact, the drivers have a 1 V (typ.) saturation level at V_{CC} below the turn-on threshold.

As described in the previous paragraphs, either the SR MOSFET is switched on after the current starts flowing through the body diode, when the drain-source voltage is already low (equal to V_F); therefore there is no Miller effect nor switching losses at the MOSFET turn-on, in which case the drive doesn't need to provide a fast turn-on.

Also at the turn-off, during steady-state load conditions, when the decision depends on the adaptive control circuitry, there is no need to have a very fast drive with hard pull-down, because the current has not yet reached zero and the operation is far from the current inversion occurrence. Moreover, slow transitions also help reducing the perturbation introduced into the system that arise due to the MOSFET turn-on and turn-off, contributing to improve the overall behavior of the LLC resonant converter.

The gate-drive circuit is specifically designed to reduce the switching noise at the turn-off, due to parasitic inductance in the driving current path. In fact, during the adaptive turn-off, it provides a controlled turn-off time (with the characteristic two-slope falling edge) in order to limit the current peak during gate drive transition, and does not require any resistor in series to the SR MOSFET gates.

On the other side, during very fast load transitions or on a sudden occurrence of the above resonance operation, when the turn-off decision is taken by ZCD_OFF logic, the MOSFET turn-off needs to be very fast to avoid current inversion: therefore, the two gate drivers are designed to guarantee for a very short turn-off total delay.

In order to avoid current inversions, the SRK2001A stops driving SR MOSFETs during any operating condition where the converter enters deeply into the below resonance region (i.e. switching frequency gets lower than 60% of resonance frequency).

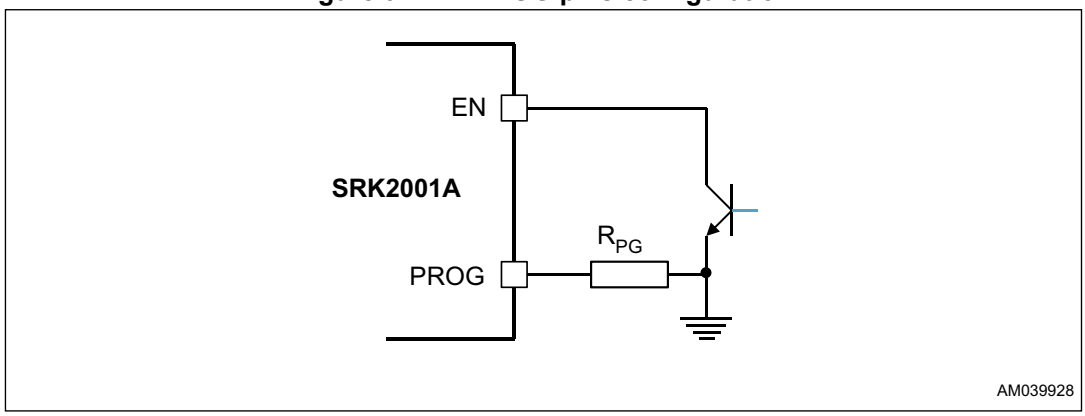
7.6 EN and PROG pins: function and usage

The SRK2001A can enter the low consumption mode in one of the following ways:

- By EN pin remote on-off (through a small signal NPN transistor)
- By detecting the primary controller burst-mode operation

The PROG pin allows the user to program the conduction duty-cycle of the SR MOSFET body diode to exit the low consumption mode: the configuration choice is done during the start-up phase (when the supply voltage reaches the turn-on level V_{CC_On}) and internally stored as long as V_{CC} is within the supply range. Referring to *Figure 9*: a precise current generator I_{PROG}, sourcing current to the PROG pin, fixes the voltage across the external resistor R_{PG}; depending on this voltage level, the conduction duty-cycle to exit the low consumption state is set, among those contained in the internal lookup table (see *Table 6*). After internal storing (pinstrap phase), the current generator I_{PROG} is disabled. In case during the startup the EN pin is kept low, the pinstrap phase will happen only after the EN pin is pulled high.

Figure 9. EN - PROG pins configuration



7.6.1 EN pin remote on-off

During the run mode, the EN pin can be used as remote on-off input, using a small signal transistor connected to the pin. When the switch is closed, the pin voltage goes below the V_{EN_OFF} threshold; the controller stops operating and enters a low consumption state. Then it resumes operation when the switch is opened and the pin voltage surpasses the V_{EN_ON} threshold (thanks to an internal pull-up of 20 µA, reduced to 6 µA in run mode, I_{EN_run}).

7.6.2 Burst-mode detection

Normally, at reduced loads, resonant converters enter burst mode operation in order to increase converter efficiency. The SRK2001A detects that the primary controller has stopped switching and enters its low consumption state. The condition to detect the burst-mode operation is that both DVS1,2 pins are above the arming voltage V_{TH_A} for at least 20 µs (typ). For the correct operation of the SRK2001A, the resonant converter has to be designed in such a way that, when it enters burst mode operation, the minimum idle time (the period during which the half-bridge is not switching) is longer than 20 µs (necessary to the SRK2001A to detect that operating condition). In case the converter may stop switching for a time shorter than 20 µs, for any reason (e.g. tripping of a protection), it is recommended to keep the PROG pin open.

Table 6. Burst-mode exiting lookup table

D_{ON}	R_{PG}
80%	R_{PG} = 0 Ω
75%	R_{PG} = 100 kΩ
65%	R_{PG} = 180 kΩ
0%	R_{PG} open

7.6.3 Low consumption state exit

After the primary controller restarts switching or the EN pin goes back high, the controller resumes the operation when it detects that the conduction duty cycle has increased above the value D_{ON} programmed by the user through a proper choice of the R_{PG} resistor. The number of clock cycles needed to exit the burst mode is proportional to the difference between the body diode conduction duty cycle and the programmed D_{ON} threshold: this allows a faster sleep-out in case of the heavy load transient low-to-high. After recognizing that the conduction duty cycle is longer than the programmed D_{ON}, 12 switching cycles (i.e. 24 clock cycles) are still needed before the SRK2001A restarts driving the SR MOSFETs (in order to allow the settlement of the internal timers, lost during the low consumption state, where most of the internal circuitry was not supplied or turned off).

7.7 Layout guidelines

The GND pin is the return of the bias current of the device and return for gate drive currents: it should be routed to the common point where the source terminals of both synchronous rectifier MOSFETs are connected. When laying out the PCB, care must be taken in keeping the source terminals of both SR MOSFETs as close to one another as possible and routing the trace that goes to the GND separately from the load current return path. This trace should be as short as possible and be as close to the physical source terminals as possible. Doing the layout as more geometrically symmetrical as possible will help make the circuit operation as much electrically symmetrical as possible.

Also drain-source voltage sensing should be done as physically close to the drain and source terminals as possible in order to minimize the stray inductance involved by the load current path that is in the drain-to-source voltage sensing circuit.

The usage of bypass capacitors between the V_{CC} and GND is recommended. They should be the low-ESR, low-ESL type and located as close to the IC pins as possible. Sometimes, a series resistor (in the tens Ω) between the converter's output voltage and the V_{CC} pin, forming an RC filter along with the by-pass capacitor, is useful to get a cleaner V_{CC} voltage.

8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

8.1 SSOP10 package information

Figure 10. SSOP10 package outline

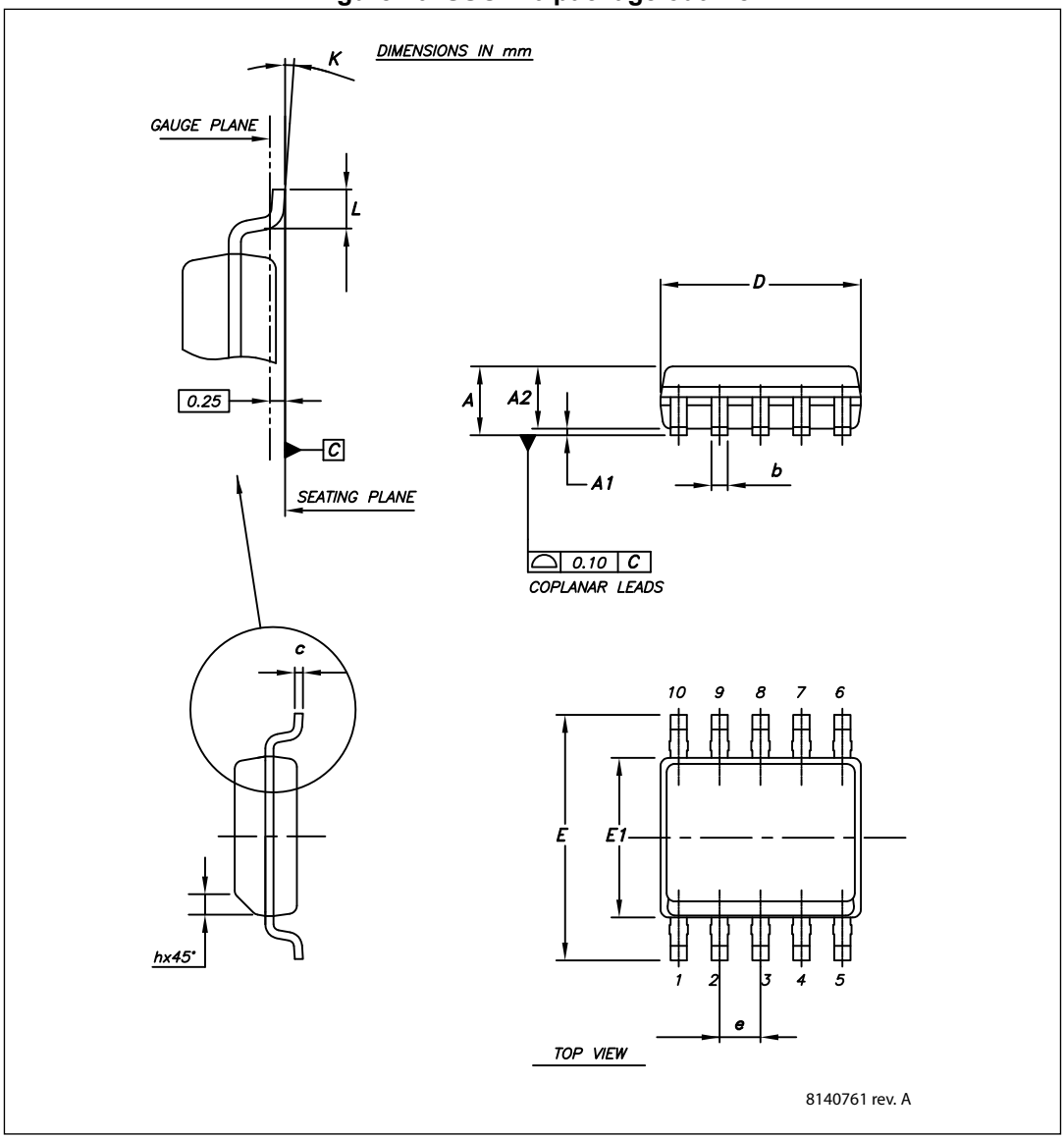


Table 7. SSOP10 package mechanical data

Symbol	Dimensions (mm)		
	Min.	Typ.	Max.
A			1.75
A1	0.10		0.25
A2	1.25		
b	0.31		0.51
c	0.17		0.25
D	4.80	4.90	5
E	5.80	6	6.20
E1	3.80	3.90	4
e		1	
h	0.25		0.50
L	0.40		0.90
K	0°		8°

9 Revision history

Table 8. Document revision history

Date	Revision	Changes
28-Jun-2016	1	Initial release.
6-Sept-2018	2	Updated *Section 7.6.2: Burst-mode detection* Updated *Section 7.6.3: Low consumption state exit*

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