16-Channel, Low Harmonic Distortion, High Voltage Analog Switch with Bleed Resistors

Features

- Low harmonic distortion
- Integrated bleed resistors on the outputs
- 3.3 or 5.5V CMOS input logic level
- 20MHz data shift clock frequency
- HVCMOS technology for high performance
- Very low quiescent power dissipation (-10µA)
- Low parasitic capacitance
- DC to 50MHz small signal frequency response
- CMOS logic circuitry for low power
- Excellent noise immunity
- Cascadable serial data register with latches
- Flexible operating supply voltages

Applications

- Medical ultrasound imaging
- NDT metal flaw detection
- Piezoelectric transducer drivers
- Optical MEMS modules

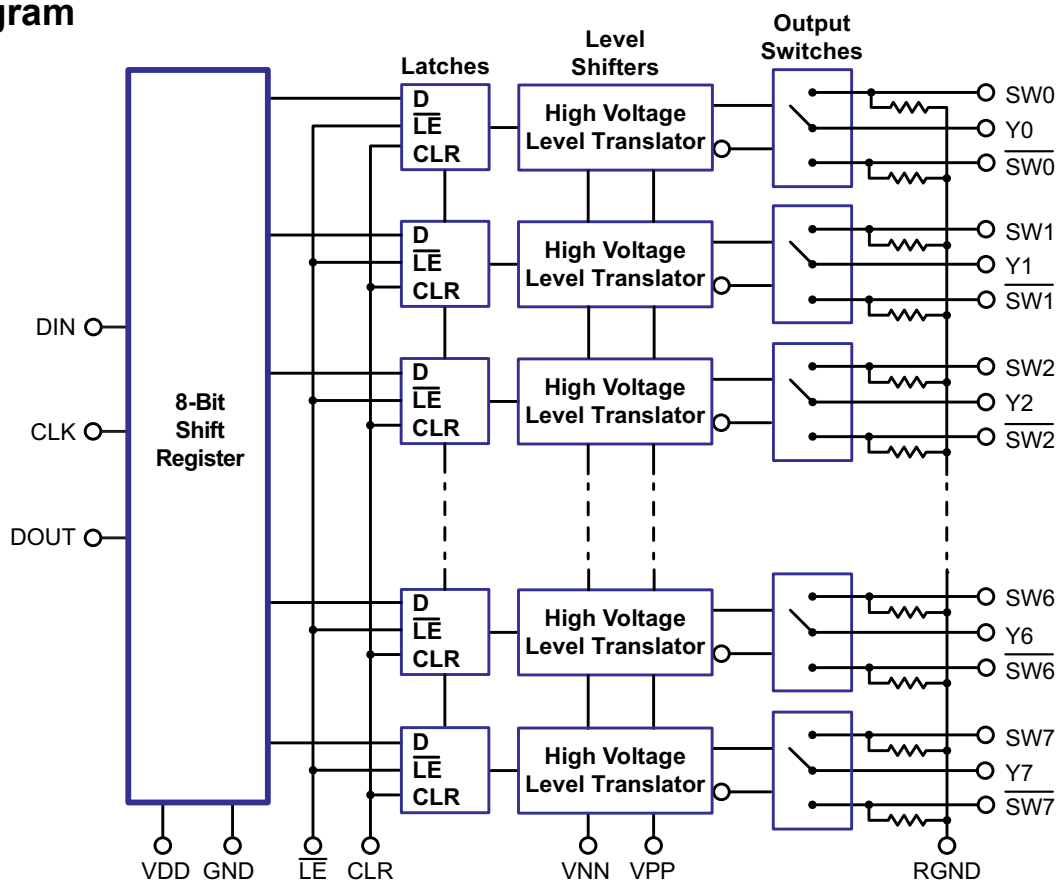
General Description

The Supertex HV2733 is a low charge injection, 16-channel, low harmonic distortion, high voltage analog switch integrated circuit (IC) intended for use in applications requiring high voltage switching, controlled by low voltage control signals, such as medical ultrasound imaging, piezoelectric transducer drivers, and printers. The bleed resistors eliminate voltage built up on capacitive loads such as piezoelectric transducers.

The outputs are configured as single-pole double-throw analog switches. Data are shifted into a 8-bit shift register using an external clock. The $\overline{LE}$ latches the shift register data into the individual switch latches. A logic high connects a switch common YX to SWX. A logic low connects YX to $\overline{SWX}$. A logic high in CLR resets all switches to $\overline{SWX}$ simultaneously.

To reduce any possible clock feed-through noise, the latch enable bar ($\overline{LE}$) should be left high until all bits are clocked in. Data are clocked in during the rising edge of the clock. Using HVCMOS technology, this device combines high voltage bilateral DMOS switches and low power CMOS logic to provide efficient control of high voltage analog signals.

Block Diagram

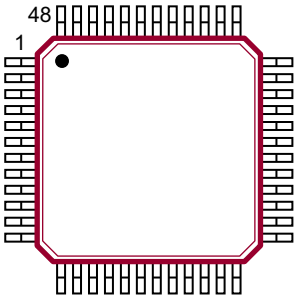


Ordering Information

Device	Package Option
	48-Lead LQFP *7.00x7.00mm body 1.60mm height (max) 0.50mm pitch*
HV2733	HV2733FG-G

-G indicates package is RoHS compliant ('Green')

Pin Configuration



48-Lead LQFP (FG)
(top view)

Absolute Maximum Ratings

Parameter	Value
V_{DD} logic supply	-0.5V to +7.0V
V_{PP} - V_{NN} differential supply	220V
V_{PP} positive supply	-0.5V to +200V
V_{NN} negative supply	+0.5V to -200V
Logic input voltage	-0.5V to V_{DD} +0.3V
V_{SIG} analog signal range	V_{NN} to V_{PP}
Peak analog signal current/channel	2.5A
Storage temperature	-65°C to 150°C
Power dissipation, 48-Lead LQFP	1.0W

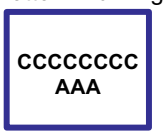
Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

Product Marking

Top Marking



Bottom Marking



YY = Year Sealed
WW = Week Sealed
L = Lot Number
C = Country of Origin*
A = Assembler ID*
_____ = "Green" Packaging

**May be part of top marking*

48-Lead LQFP (FG)

Packages may or may not include the following marks: Si or

Recommended Operating Conditions

Sym	Parameter	Value
V_{DD}	Logic power supply voltage	3.0V to 5.5V
V_{PP}	Positive high voltage supply	+40V to V_{NN} +200V
V_{NN}	Negative high voltage supply	-40V to -160V
V_{IH}	High level input voltage	0.9V_{DD} to V_{DD}
V_{IL}	Low level input voltage	0V to 0.1V_{DD}
V_{SIG}	Analog signal voltage peak-to-peak	V_{NN}+10V to V_{PP}-10V
T_A	Operating free air temperature	0°C to 70°C

Notes:

1. *Power up/down sequence is arbitrary except GND must be powered-up first and powered-down last.*
2. *V_{SIG} must be within V_{NN} and V_{PP} or floating during power up/down transition.*
3. *Rise and fall times of power supplies V_{DD}, V_{PP}, and V_{NN} should not be less than 1.0msec.*

DC Electrical Characteristics

(over recommended operating conditions unless otherwise noted)

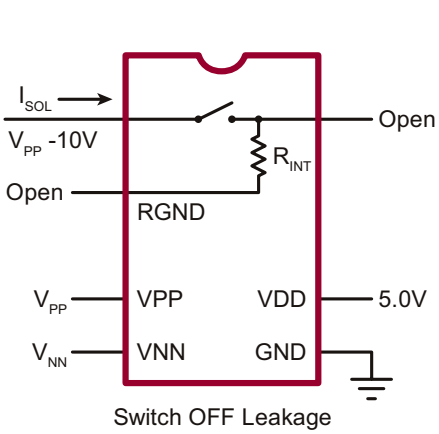
Sym	Parameter	0°C		+25°C			+70°C		Units	Conditions	
		Min	Max	Min	Typ	Max	Min	Max			
R_{ONS}	Small signal switch ON-resistance	-	30	-	26	38	-	48	Ω	I_{SIG} = 5.0mA	V_{PP} = +40V, V_{NN} = -160V
		-	25	-	22	27	-	32		I_{SIG} = 200mA	
		-	25	-	22	27	-	30		I_{SIG} = 5.0mA	V_{PP} = +100V, V_{NN} = -100V
		-	18	-	18	24	-	27		I_{SIG} = 200mA	
		-	23	-	20	25	-	30		I_{SIG} = 5.0mA	V_{PP} = +160V, V_{NN} = -40V
		-	22	-	16	25	-	27		I_{SIG} = 200mA	
ΔR_{ONS}	Small signal switch ON-resistance matching	-	20	-	5.0	20	-	20	%	I_{SIG} = 5.0mA, V_{PP} = +100V, V_{NN} = -100V	
R_{ONL}	Large signal switch ON-resistance	-	-	-	15	-	-	-	Ω	V_{SIG}= V_{PP} -10V, I_{SIG} = 1.0A	
R_{INT}	Value of output bleed resistor	-	-	35	50	65	-	-	KΩ	Output Switch to RGND I_{RINT} = 0.5mA	
I_{SOL}	Switch off leakage per switch	-	5.0	-	1.0	10	-	15	µA	V_{SIG} = V_{PP} -10V and V_{NN} +10V	
V_{OS}	DC offset switch off	-	50	-	-	50	-	50	mV	No Load, RGND = 0V	
	DC offset switch on	-	50	-	-	50	-	50	mV		
I_{PPQ}	Quiescent V_{PP} supply current	-	-	-	10	50	-	-	µA	All switches off	
I_{NNQ}	Quiescent V_{NN} supply current	-	-	-	-10	-50	-	-	µA	All switches off	
I_{PPQ}	Quiescent V_{PP} supply current	-	-	-	10	50	-	-	µA	All switches on, I_{SW} = 5.0mA	
I_{NNQ}	Quiescent V_{NN} supply current	-	-	-	-10	-50	-	-	µA	All switches on, I_{SW} = 5.0mA	
I_{SW}	Switch output peak current	-	2.0	-	-	2.0	-	2.0	A	V_{SIG} duty cycle < 0.1% pulse width ≤1.0µs	
f_{SW}	Output switching frequency	-	-	-	-	50	-	-	kHz	Duty cycle = 50%	
I_{PP}	Average V_{PP} supply current	-	5.2	-	-	5.6	-	6.4	mA	V_{PP} = +40V, V_{NN} = -160V	All output switches are turning on and off at 50kHz with no load.
		-	3.2	-	-	4.5	-	4.5		V_{PP} = +100V, V_{NN} = -100V	
		-	3.2	-	-	4.0	-	4.5		V_{PP} = +160V, V_{NN} = -40V	
I_{NN}	Average V_{NN} supply current	-	5.2	-	-	5.6	-	6.4	mA	V_{PP} = +40V, V_{NN} = -160V	All output switches are turning on and off at 50kHz with no load.
		-	3.2	-	-	4.0	-	4.5		V_{PP} = +100V, V_{NN} = -100V	
		-	3.2	-	-	4.0	-	4.5		V_{PP} = +160V, V_{NN} = -40V	
I_{DD}	Average V_{DD} supply current	-	2.0	-	-	2.0	-	2.0	mA	f_{CLK} = 5.0MHz, V_{DD} = 5.0V	
I_{DDQ}	Quiescent V_{DD} supply current	-	10	-	-	10	-	10	µA	All logic inputs are static	
I_{SOR}	Data out source current	0.45	-	0.45	0.70	-	0.40	-	mA	V_{OUT} = V_{DD} - 0.7V	
I_{SINK}	Data out sink current	0.45	-	0.45	0.70	-	0.40	-	mA	V_{OUT} = 0.7V	
C_{IN}	Logic input capacitance	-	10	-	-	10	-	10	pF	---	

AC Electrical Characteristics

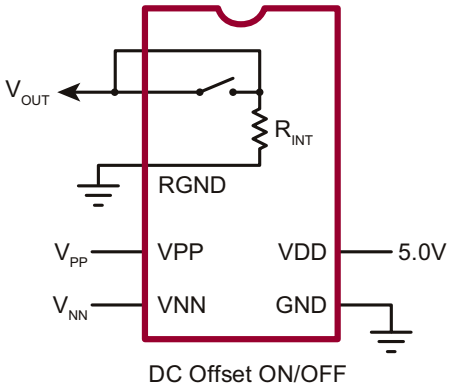
(over recommended operating conditions, V_{DD}= 5.0V, $t_R = t_F \leq$ 5.0ns, 50% duty cycle, C_{LOAD} = 20pF, unless otherwise noted)

Sym	Parameter	0°C		+25°C			+70°C		Units	Conditions
		Min	Max	Min	Typ	Max	Min	Max		
t_{SD}	Set up time before $\overline{LE}$ rises	25	-	25	-	-	25	-	ns	---
t_{WLE}	Time width of $\overline{LE}$	12	-	-	12	-	12	-	ns	V_{DD} = 5.0V
t_{DO}	Clock delay time to data out	15	40	15	30	40	15	40	ns	V_{DD}= 5.0V
t_{WCLR}	Time width of CLR	55	-	55	-	-	55	-	ns	---
t_{SU}	Set up time data to clock	7.0	-	-	7.0	-	7.0	-	ns	V_{DD}= 5.0V
t_H	Hold time data from clock	2.0	-	2.0	-	-	2.0	-	ns	---
f_{CLK}	Clock frequency	-	20	-	-	20	-	20	MHz	50% duty cycle, $f_{DATA} = f_{CLK}/2$
t_R,t_F	Clock rise and fall times	-	50	-	-	50	-	50	ns	----
T_{ON}	Turn on time	-	5.0	-	-	5.0	-	5.0	µs	$V_{SIG} = V_{PP}$ -10V, R_{LOAD} = 10kΩ
T_{OFF}	Turn off time	-	5.0	-	-	5.0	-	5.0	µs	$V_{SIG} = V_{PP}$ -10V, R_{LOAD} = 10kΩ
dv/dt	Maximum V_{SIG} slew rate	-	20	-	-	20	-	20	v/ns	V_{PP} = +40V, V_{NN} = -160V
		-	20	-	-	20	-	20		V_{PP} = +100V, V_{NN} = -100V
		-	20	-	-	20	-	20		V_{PP} = +160V, V_{NN} = -40V
K_O	Off isolation	-30	-	-30	-33	-	-30	-	dB	f = 5.0MHz, 1.0kΩ//15pF load
		-58	-	-58	-	-	-58	-		f = 5.0MHz, 50Ω load
K_{CR}	Switch crosstalk	-60	-	-60	-70	-	-60	-	dB	f = 5.0MHz, 50Ω load
I_{ID}	Output switch isolation diode current	-	300	-	-	300	-	300	mA	300ns pulse width, 2.0% duty cycle
$C_{SG(OFF)}$	Off capacitance SW to GND	5.0	17	5.0	12	17	5.0	17	pF	0V, f = 1.0MHz
$C_{SG(ON)}$	On capacitance SW to GND	25	50	25	38	50	25	50	pF	0V, f = 1.0MHz
$+V_{SPK}$	Output voltage spike	-	-	-	-	150	-	-	mV	V_{PP} = +40V, V_{NN} = -160V, R_{LOAD} = 50Ω
$-V_{SPK}$		-	-	-	-	150	-	-		
$+V_{SPK}$		-	-	-	-	150	-	-		V_{PP} = +100V, V_{NN} = -100V, R_{LOAD} = 50Ω
$-V_{SPK}$		-	-	-	-	150	-	-		
$+V_{SPK}$		-	-	-	-	150	-	-		V_{PP} = +160V, V_{NN} = -40V, R_{LOAD} = 50Ω
$-V_{SPK}$		-	-	-	-	150	-	-		

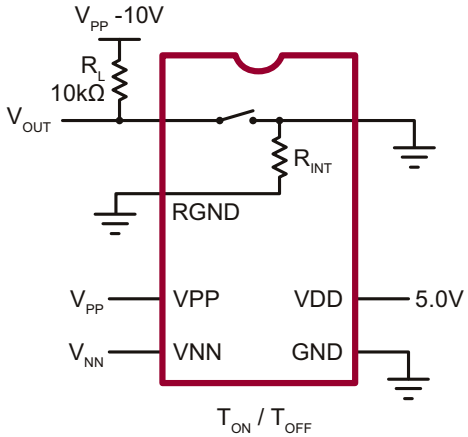
HV2733 Test Circuits



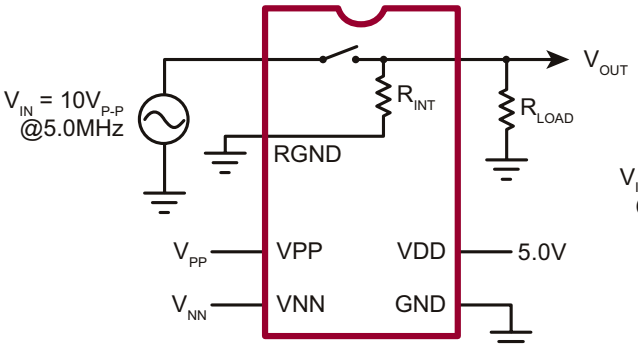
Switch OFF Leakage



DC Offset ON/OFF

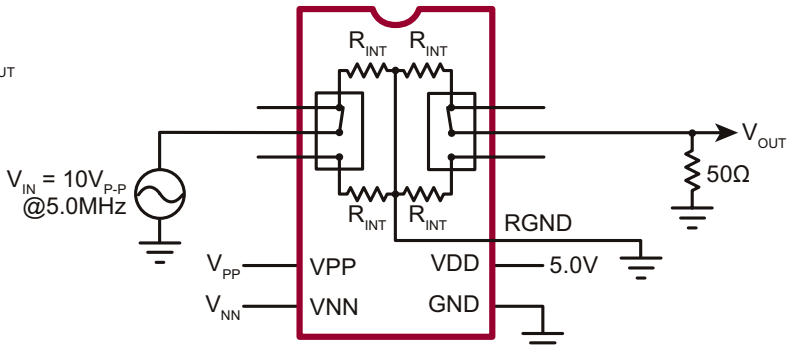


T_{ON} / T_{OFF}



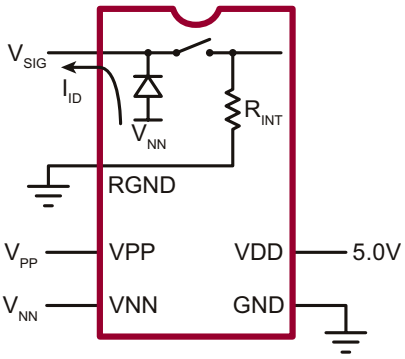
$K_O = 20\text{Log}\ \frac{V_{OUT}}{V_{IN}}$

Off Isolation

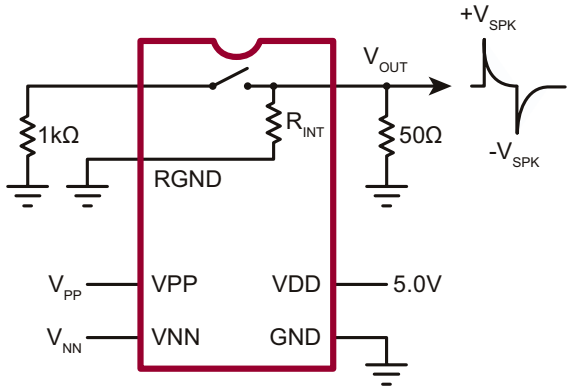


$K_{CR} = 20\text{Log}\ \frac{V_{OUT}}{V_{IN}}$

Crosstalk



Isolation Diode Current



Output Voltage Spike

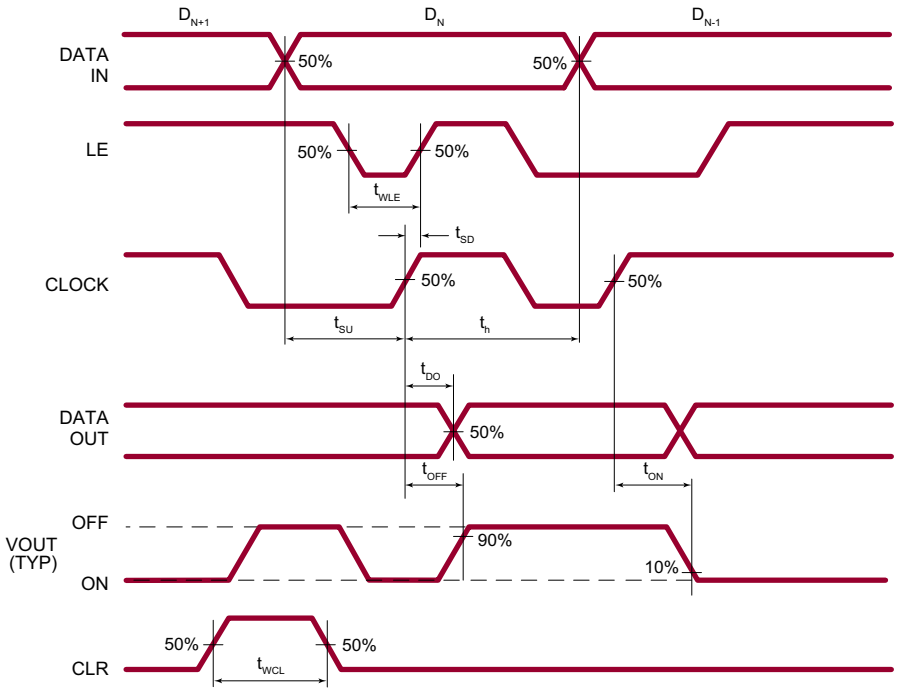
Truth Table

D0	D1	D2	D3	D4	D5	D6	D7	$\overline{LE}$	CLR	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
L	-	-	-	-	-	-	-	L	L	$\overline{SW0}$	-	-	-	-	-	-	-
H	-	-	-	-	-	-	-	L	L	SW0	-	-	-	-	-	-	-
-	L	-	-	-	-	-	-	L	L	-	$\overline{SW1}$	-	-	-	-	-	-
-	H	-	-	-	-	-	-	L	L	-	SW1	-	-	-	-	-	-
-	-	L	-	-	-	-	-	L	L	-	-	$\overline{SW2}$	-	-	-	-	-
-	-	H	-	-	-	-	-	L	L	-	-	SW2	-	-	-	-	-
-	-	-	L	-	-	-	-	L	L	-	-	-	$\overline{SW3}$	-	-	-	-
-	-	-	H	-	-	-	-	L	L	-	-	-	SW3	-	-	-	-
-	-	-	-	L	-	-	-	L	L	-	-	-	-	$\overline{SW4}$	-	-	-
-	-	-	-	H	-	-	-	L	L	-	-	-	-	SW4	-	-	-
-	-	-	-	-	L	-	-	L	L	-	-	-	-	-	$\overline{SW5}$	-	-
-	-	-	-	-	H	-	-	L	L	-	-	-	-	-	SW5	-	-
-	-	-	-	-	-	L	-	L	L	-	-	-	-	-	-	$\overline{SW6}$	-
-	-	-	-	-	-	H	-	L	L	-	-	-	-	-	-	SW6	-
-	-	-	-	-	-	-	L	L	L	-	-	-	-	-	-	-	$\overline{SW7}$
-	-	-	-	-	-	-	H	L	L	-	-	-	-	-	-	-	SW7
X	X	X	X	X	X	X	X	H	L	HOLD PREVIOUS STATE							
X	X	X	X	X	X	X	X	X	H	$\overline{SW0}$	$\overline{SW1}$	$\overline{SW2}$	$\overline{SW3}$	$\overline{SW4}$	$\overline{SW5}$	$\overline{SW6}$	$\overline{SW7}$

Notes:

1. *Serial data is clocked in on the L to H transition of the CLK.*
2. *All switches go to a state retaining their latched condition at the rising edge of $\overline{LE}$. When $\overline{LE}$ is low the shift registers data flow through the latch.*
3. *D_{OUT} is high when data in the shift register 7 is high.*
4. *Shift registers clocking has no effect on the switch states if $\overline{LE}$ is high.*
5. *The CLR clear input overrides all other inputs.*

Logic Timing Waveforms

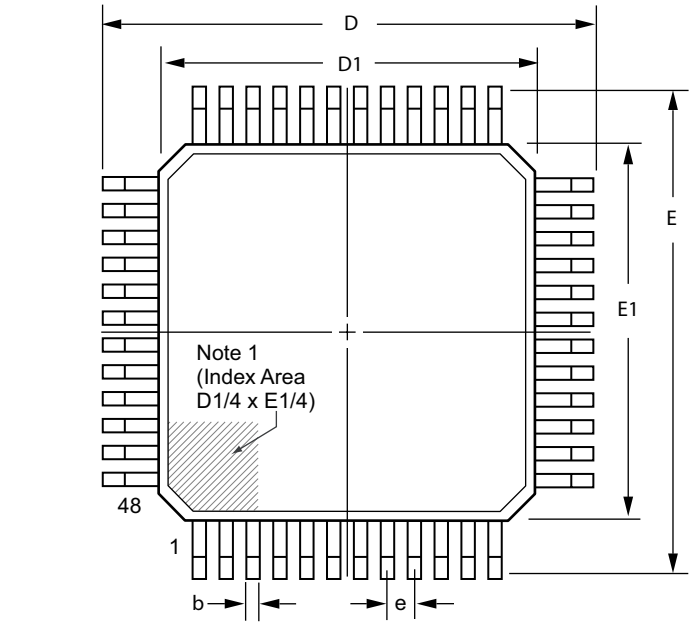


Pin Configuration
48-Lead LQFP (FG)

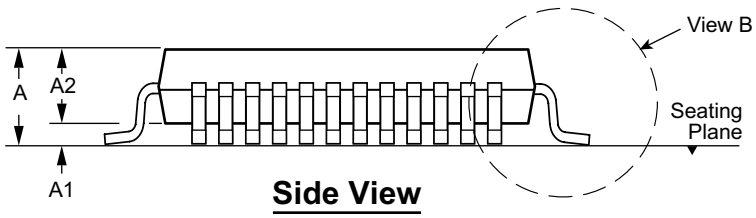
Pin #	Function	Pin #	Function	Pin #	Function	Pin #	Function
1	SW0	13	SW3	25	NC	37	RGND
2	Y0	14	Y3	26	$\overline{SW5}$	38	GND
3	$\overline{SW0}$	15	$\overline{SW3}$	27	Y5	39	VDD
4	NC	16	NC	28	SW5	40	DOUT
5	SW1	17	VNN	29	NC	41	NC
6	Y1	18	NC	30	$\overline{SW6}$	42	NC
7	$\overline{SW1}$	19	NC	31	Y6	43	NC
8	NC	20	VPP	32	SW6	44	CLR
9	SW2	21	NC	33	NC	45	$\overline{LE}$
10	Y2	22	$\overline{SW4}$	34	$\overline{SW7}$	46	CLK
11	$\overline{SW2}$	23	Y4	35	Y7	47	DIN
12	NC	24	SW4	36	SW7	48	RGND

48-Lead LQFP Package Outline (FG)

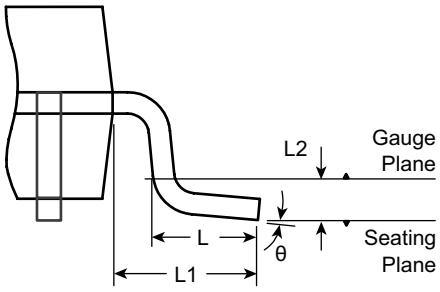
7.00x7.00mm body, 1.60mm height (max), 0.50mm pitch



Top View



Side View



View B

Note:

1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*

Symbol		A	A1	A2	b	D	D1	E	E1	e	L	L1	L2	θ
Dimension (mm)	MIN	1.40*	0.05	1.35	0.17	8.80*	6.80*	8.80*	6.80*	0.50 BSC	0.45	1.00 REF	0.25 BSC	0°
	NOM	-	-	1.40	0.22	9.00	7.00	9.00	7.00		0.60			3.5°
	MAX	1.60	0.15	1.45	0.27	9.20*	7.20*	9.20*	7.20*		0.75			7°

JEDEC Registration MS-026, Variation BBC, Issue D, Jan. 2001.

** This dimension is not specified in the JEDEC drawing.*

Drawings are not to scale.

Supertex Doc. #: *DSPD-48LQFPFG Version, D041309.*

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)

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