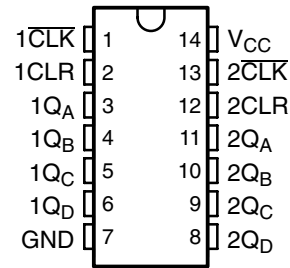


SN74LV393A-Q1 DUAL 4-BIT BINARY COUNTER

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- Qualified for Automotive Applications
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- 2-V to 5.5-V V_{CC} Operation
- Max t_{pd} of 9.5 ns at 5 V
- Typical V_{OLP} (Output Ground Bounce) <0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) >2.3 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- I_{off} Supports Partial-Power-Down-Mode Operation
- Dual 4-Bit Binary Counters With Individual Clocks
- Direct Clear for Each 4-Bit Counter
- Can Significantly Improve System Densities by Reducing Counter Package Count by 50 Percent

PW PACKAGE
(TOP VIEW)



description/ordering information

The SN74LV393A contains eight flip-flops and additional gating to implement two individual 4-bit counters in a single package. This device is designed for 2-V to 5.5-V V_{CC} operation.

This device comprises two independent 4-bit binary counters, each having a clear (CLR) and a clock ($\overline{\text{CLK}}$) input. The device changes state on the negative-going transition of the $\overline{\text{CLK}}$ pulse. N-bit binary counters can be implemented with each package, providing the capability of divide by 256. The SN74LV393A has parallel outputs from each counter stage so that any submultiple of the input count frequency is available for system timing signals.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

ORDERING INFORMATION†

T_A	PACKAGE‡		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 105°C	TSSOP – PW	Tape and reel	SN74LV393ATPWRQ1	LV393AT

† For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at <http://www.ti.com>.

‡ Package drawings, thermal data, and symbolization are available at <http://www.ti.com/packaging>.

FUNCTION TABLE

INPUTS		FUNCTION
CLK	CLR	
↑	L	No change
↓	L	Advance to next stage
X	H	All outputs L



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

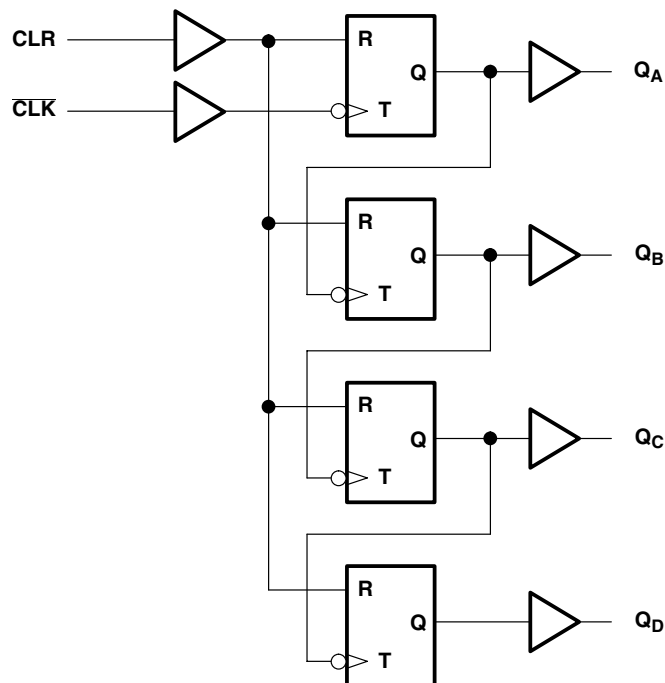
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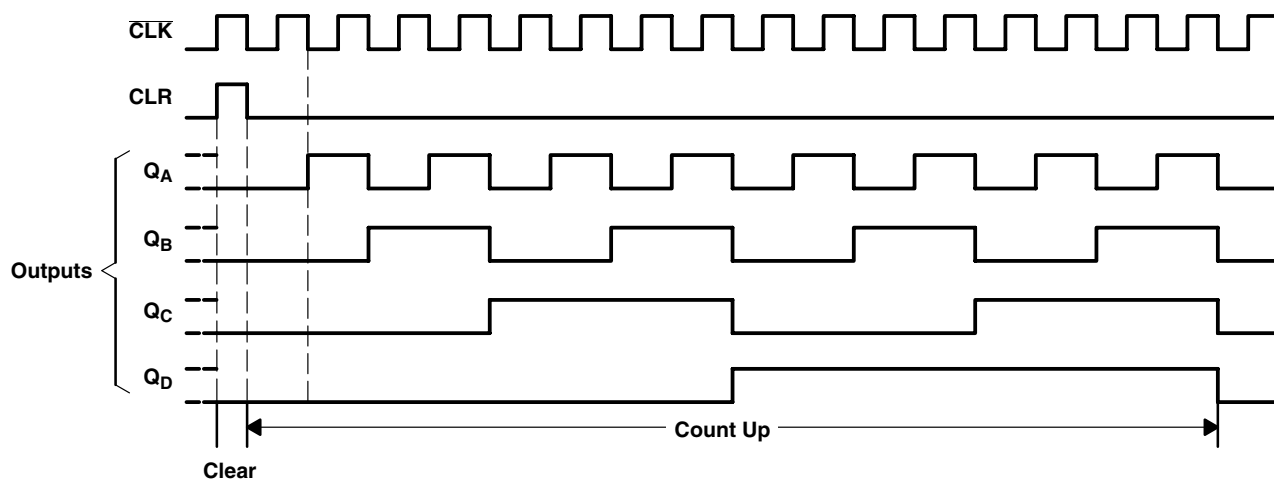
SN74LV393A-Q1 DUAL 4-BIT BINARY COUNTER

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logic diagram, each counter (positive logic)



timing diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Output voltage range applied in high or low state, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Output voltage range applied in power-off state, V_O (see Note 1)	–0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$)	–20 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±25 mA
Continuous current through V_{CC} or GND	±50 mA
Package thermal impedance, θ_{JA} (see Note 3)	113°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
2. This value is limited to 7 V maximum.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 4)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	2	5.5	V
V_{IH}	High-level input voltage	$V_{CC} = 2$ V	1.5	V
		$V_{CC} = 2.3$ V to 2.7 V	$V_{CC} \times 0.7$	
		$V_{CC} = 3$ V to 3.6 V	$V_{CC} \times 0.7$	
		$V_{CC} = 4.5$ V to 5.5 V	$V_{CC} \times 0.7$	
V_{IL}	Low-level input voltage	$V_{CC} = 2$ V	0.5	V
		$V_{CC} = 2.3$ V to 2.7 V	$V_{CC} \times 0.3$	
		$V_{CC} = 3$ V to 3.6 V	$V_{CC} \times 0.3$	
		$V_{CC} = 4.5$ V to 5.5 V	$V_{CC} \times 0.3$	
V_I	Input voltage	0	5.5	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 2$ V	–50	μA
		$V_{CC} = 2.3$ V to 2.7 V	–2	mA
		$V_{CC} = 3$ V to 3.6 V	–6	
		$V_{CC} = 4.5$ V to 5.5 V	–12	
I_{OL}	Low-level output current	$V_{CC} = 2$ V	50	μA
		$V_{CC} = 2.3$ V to 2.7 V	2	mA
		$V_{CC} = 3$ V to 3.6 V	6	
		$V_{CC} = 4.5$ V to 5.5 V	12	
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 2.3$ V to 2.7 V	200	ns/V
		$V_{CC} = 3$ V to 3.6 V	100	
		$V_{CC} = 4.5$ V to 5.5 V	20	
T_A	Operating free-air temperature	–40	105	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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DUAL 4-BIT BINARY COUNTER

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
V _{OH}	I _{OH} = –50 µA	2 V to 5.5 V	V _{CC} –0.1			V
	I _{OH} = –2 mA	2.3 V	2			
	I _{OH} = –6 mA	3 V	2.48			
	I _{OH} = –12 mA	4.5 V	3.8			
V _{OL}	I _{OL} = 50 µA	2 V to 5.5 V			0.1	V
	I _{OL} = 2 mA	2.3 V			0.4	
	I _{OL} = 6 mA	3 V			0.44	
	I _{OL} = 12 mA	4.5 V			0.55	
I _I	V _I = 5.5 V or GND	0 to 5.5 V			±1	µA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V			20	µA
I _{off}	V _I or V _O = 0 to 5.5 V	0			5	µA
C _i	V _I = V _{CC} or GND	3.3 V		1.8		pF

timing requirements over recommended operating free-air temperature range, V_{CC} = 2.5 V ± 0.2 V (unless otherwise noted) (see Figure 1)

		T _A = 25°C		MIN	MAX	UNIT
		MIN	MAX			
t _w	Pulse duration	CLK high or low		5	5	ns
		CLR high		5	5	
t _{su}	Setup time	CLR inactive before CLK↓		6	6	ns

timing requirements over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

		T _A = 25°C		MIN	MAX	UNIT
		MIN	MAX			
t _w	Pulse duration	CLK high or low		5	5	ns
		CLR high		5	5	
t _{su}	Setup time	CLR inactive before CLK↓		5	5	ns

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

		T _A = 25°C		MIN	MAX	UNIT
		MIN	MAX			
t _w	Pulse duration	CLK high or low		5	5	ns
		CLR high		5	5	
t _{su}	Setup time	CLR inactive before CLK↓		4	4	ns



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SN74LV393A-Q1 DUAL 4-BIT BINARY COUNTER

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switching characteristics over recommended operating free-air temperature range, $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
				MIN	TYP	MAX			
$f_{\max}$			$C_L = 50\text{ pF}$	30	70		25		MHz
t_{pd}	$\overline{\text{CLK}}$	Q_A	$C_L = 50\text{ pF}$		9.3	21.3	1	24.5	ns
		Q_B			10.9	23.9	1	27.5	
		Q_C			12.3	26.1	1	30	
		Q_D			13.4	27.8	1	32	
t_{PHL}	CLR	Q_n			9.1	17.4	1	20	

switching characteristics over recommended operation free-air temperature range, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
				MIN	TYP	MAX			
$f_{\max}$			$C_L = 50\text{ pF}$	45	105		35		MHz
t_{pd}	$\overline{\text{CLK}}$	Q_A	$C_L = 50\text{ pF}$		6.7	16.7	1	19	ns
		Q_B			7.8	19.3	1	22	
		Q_C			8.7	21.5	1	24.5	
		Q_D			9.5	23.2	1	26.5	
t_{PHL}	CLR	Q_n			6.8	15.8	1	18	

switching characteristics over recommended operating free-air temperature range, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
				MIN	TYP	MAX			
$f_{\max}$			$C_L = 50\text{ pF}$	85	150		75		MHz
t_{pd}	$\overline{\text{CLK}}$	Q_A	$C_L = 50\text{ pF}$		4.9	10.5	1	12	ns
		Q_B			5.6	11.8	1	13.5	
		Q_C			6.2	13.2	1	15	
		Q_D			6.6	14.5	1	16.5	
t_{PHL}	CLR	Q_n			5.2	10.1	1	11.5	



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DUAL 4-BIT BINARY COUNTER

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noise characteristics, $V_{CC} = 3.3\text{ V}$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$ (see Note 5)

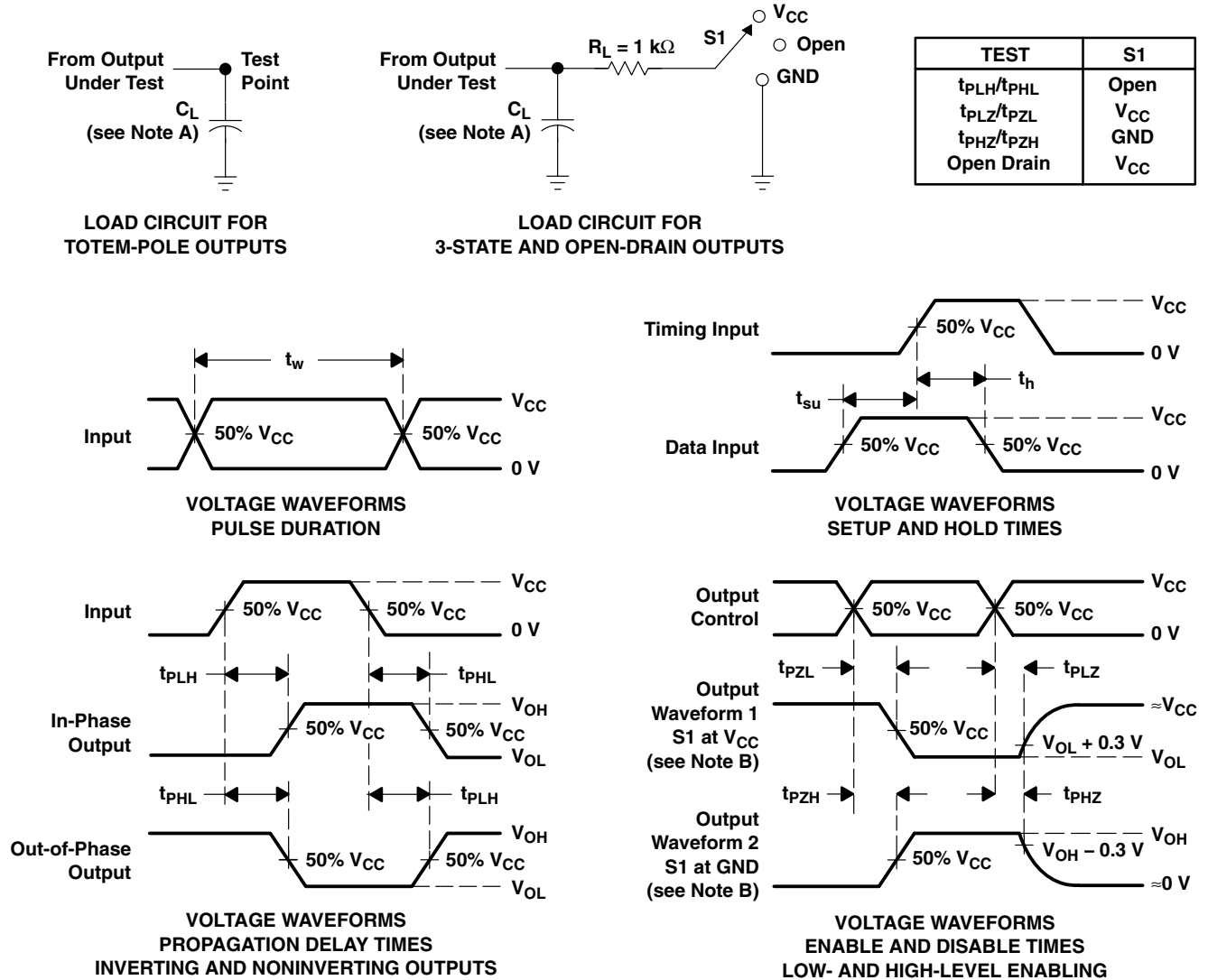
PARAMETER		MIN	TYP	MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.3	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		–0.2	–0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		2.8		V
$V_{IH(D)}$	High-level dynamic input voltage	2.31			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.99	V

NOTE 5: Characteristics are for surface-mount packages only.

operating characteristics, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	$C_L = 50\text{ pF}$, $f = 10\text{ MHz}$	3.3 V	15.2	pF
			5 V	17.3	

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.
- D. The outputs are measured one at a time, with one input transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. t_{PHL} and t_{PLH} are the same as t_{pd} .
- H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LV393ATPWRG4Q1	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 105	LV393AT	Samples
SN74LV393ATPWRQ1	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 105	LV393AT	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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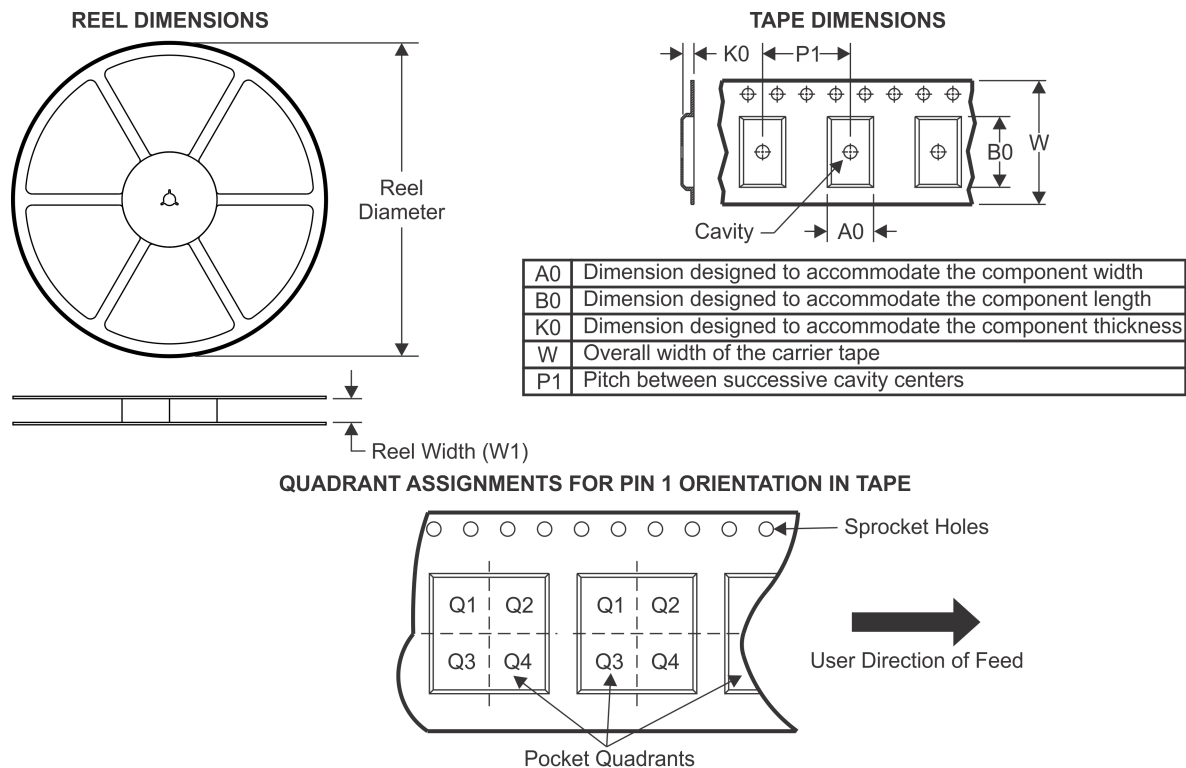
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OTHER QUALIFIED VERSIONS OF SN74LV393A-Q1 :

- Catalog: [SN74LV393A](#)
- Enhanced Product: [SN74LV393A-EP](#)

NOTE: Qualified Version Definitions:

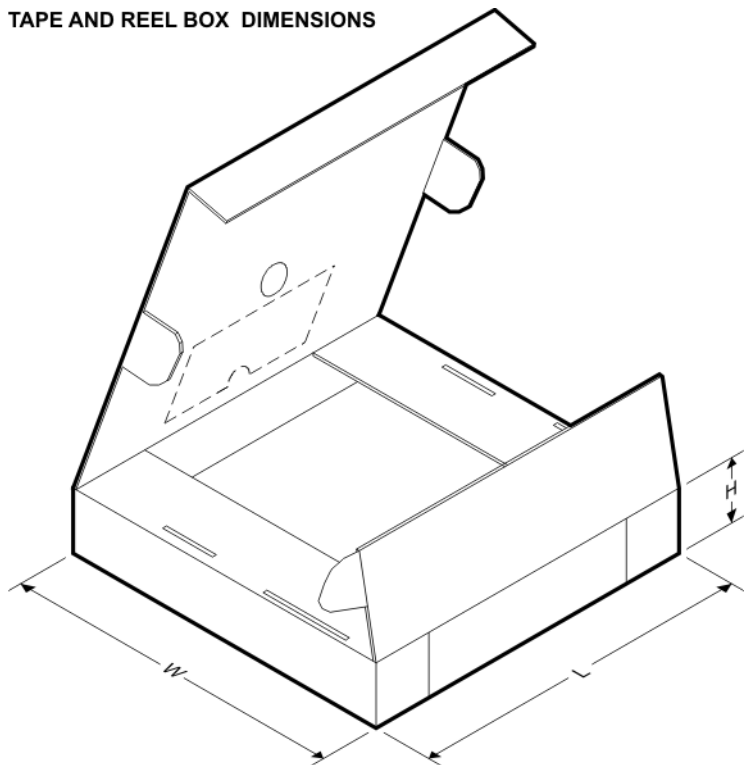
- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV393ATPWG4Q1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV393ATPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

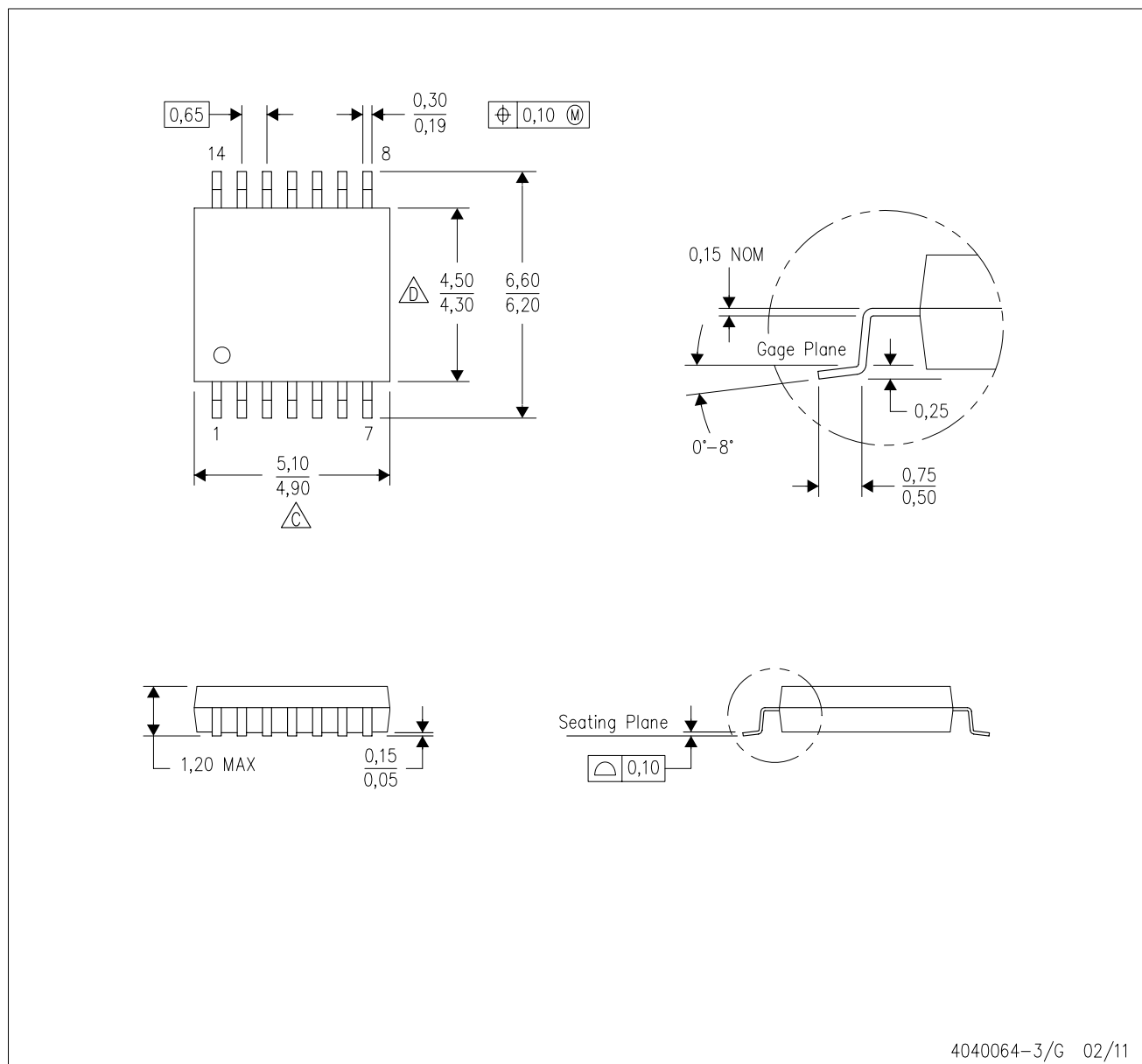


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV393ATPWRG4Q1	TSSOP	PW	14	2000	367.0	367.0	35.0
SN74LV393ATPWRQ1	TSSOP	PW	14	2000	367.0	367.0	35.0

PW (R-PDSO-G14)

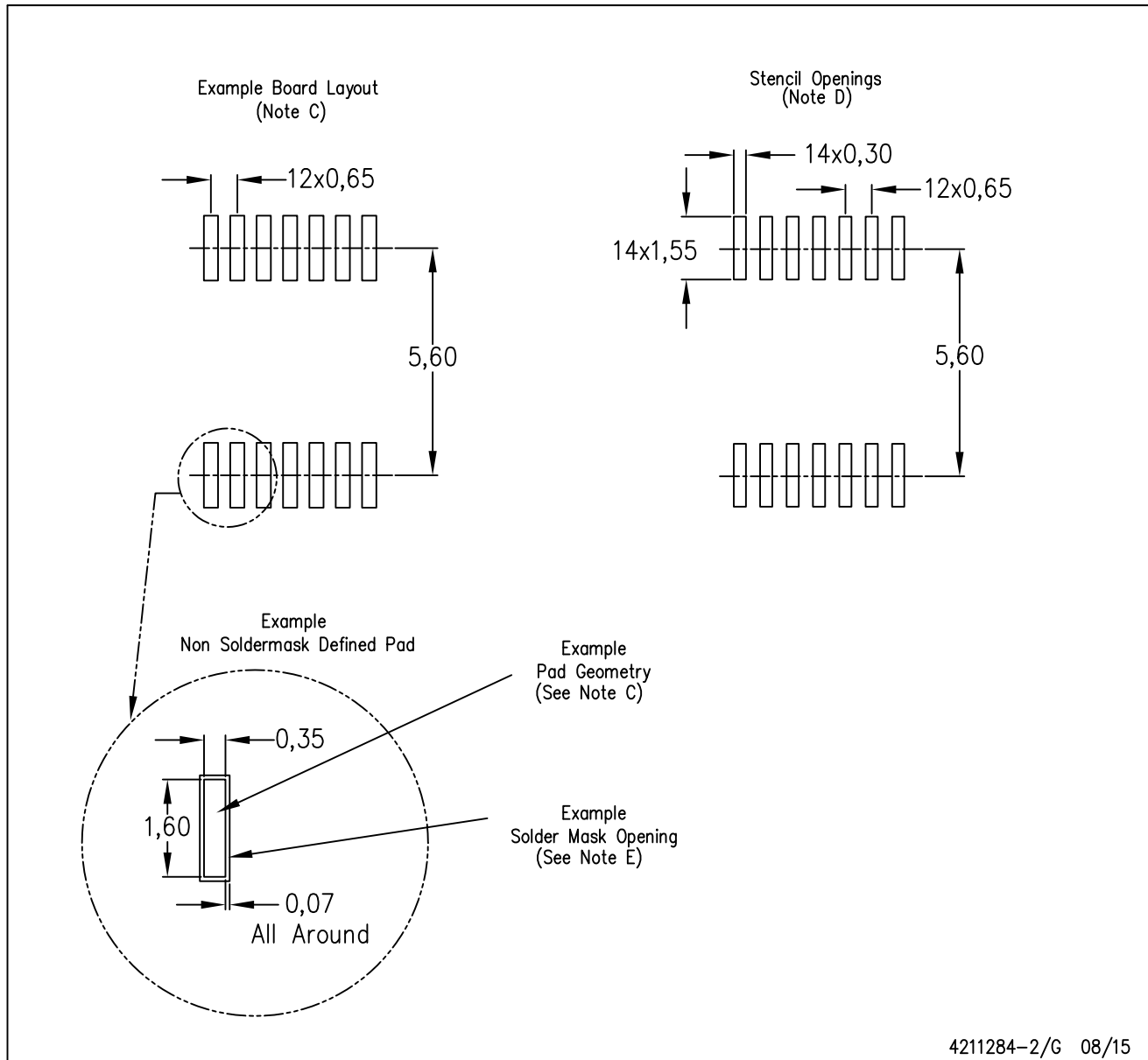
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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