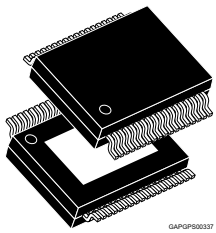
L9301

Automotive octal low side driver or quad low side plus quad high side driver

Datasheet - production data



PowerSSO36

Features



- AEC-Q100 qualified
- Eight integrated PowerMOS configurable as:
  - 8 low side ON-OFF with $R_{ON(max)}$ = 0.3 Ω @ T_j = 175 °C
  - High/low side PWM with $R_{ON(max)}$ = 0.6 Ω @ T_j = 175 °C and 4 Low side with $R_{ON(max)}$ = 0.3 Ω @ T_j = 175 °C
- Operating battery supply voltage 5 V to 18 V
- Operating V_{dd} supply voltage 4.75 V to 5.25 V
- Logic inputs TTL/CMOS-compatible
- Output voltage clamping 37 V typ. in low-side configuration
- SPI interface for outputs control and for diagnosis data communication
- Additional PWM inputs for 8 outputs
- Over temperature protection
- Open load, short to GND, short to VB
- Overcurrent diagnostics in latched or unlatched mode for each channel
- Controlled SR for improved EMC behavior

Description

The L9301 is a SPI (Serial Peripheral Interface) controlled octal channel with 4 high/low and 4 low side drivers with the possibility to use four integrated PowerMOS as recirculation diodes for PWM load driving.

L9301 contains 12 PowerMOS: 4 configurable High/Low side drivers with R_{onmax} = 0.6 Ω (DRN1-4, SRC1-4), 4 low side drivers with R_{onmax} = 0.6 Ω (OUT1-4) and 4 low side drivers with R_{onmax} = 0.3 Ω (OUT5-8).

The power DRN/SRC1-4 and OUT1-4 can be connected in parallel outside the device in order to get 4 low-side drivers with R_{onmax} = 0.3 Ω: DRN1//DRN2, DRN3//DRN4, OUT1//OUT2, OUT3//OUT4.

In this way there is a total of 8 LS channels for ON-OFF mode with R_{onmax} = 0.3 Ω.

There is also the possibility to connect the OUT1-4 and OUT5-8 in order to drive in PWM mode a load connected to VB or GND without the necessity of a freewheeling diode. In this case the R_{onmax} = 0.6 Ω.

The above configuration can be driven by parallel input or SPI command.

Through the SPI it is possible to configure the device parameters like configuration, Slew-rate, Overcurrent threshold, to send the drivers commands and to read back the diagnosis results.

Table 1. Device summary

Order code	Package	Packing
L9301-TR	PowerSSO36 (Exp. pad opt.B)	Tape & Reel

This is information on a product in full production. www.st.com

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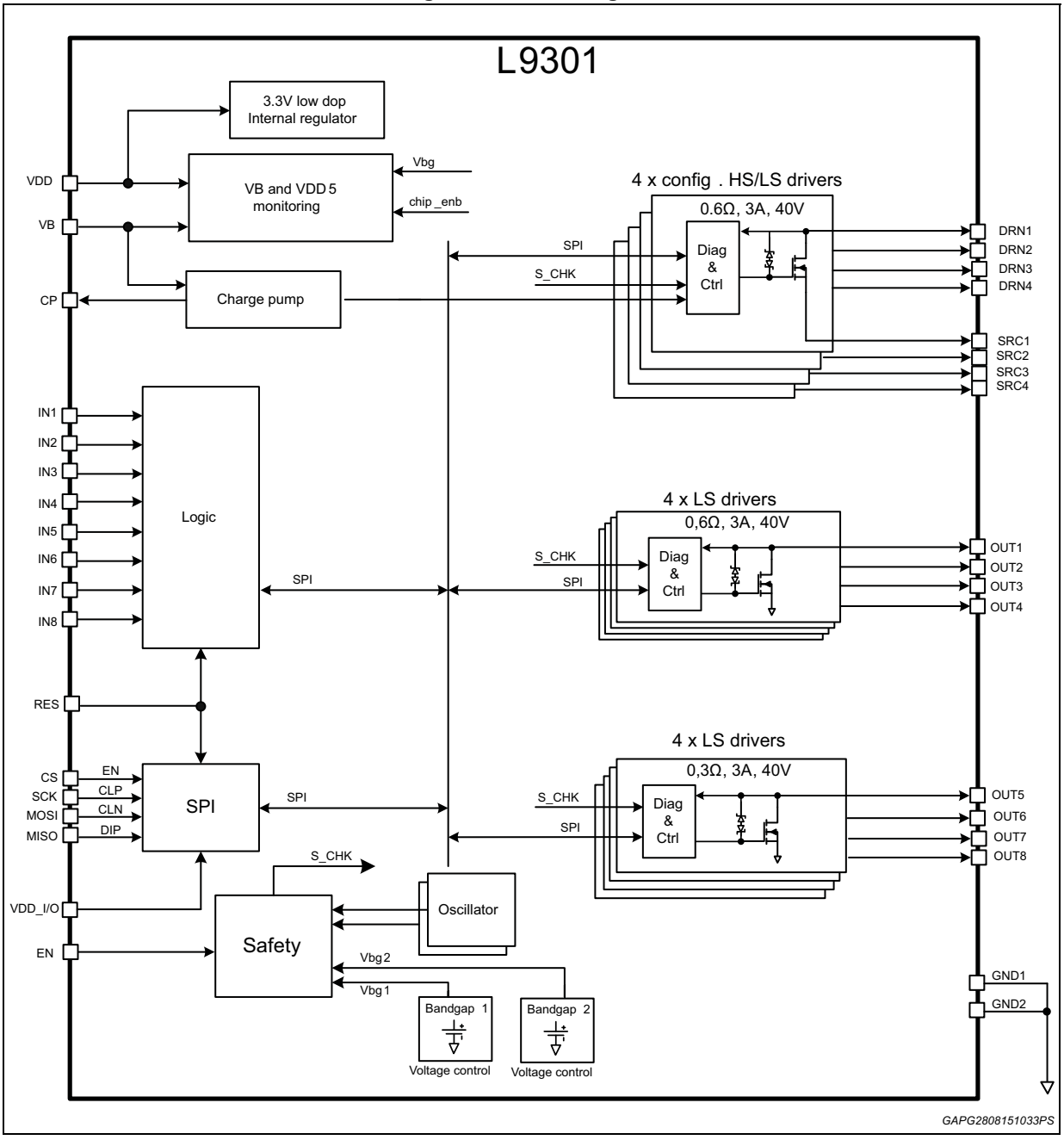
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1 Block diagram

Figure 1. Block diagram



2 Pin description

Figure 2. Pin connection diagram

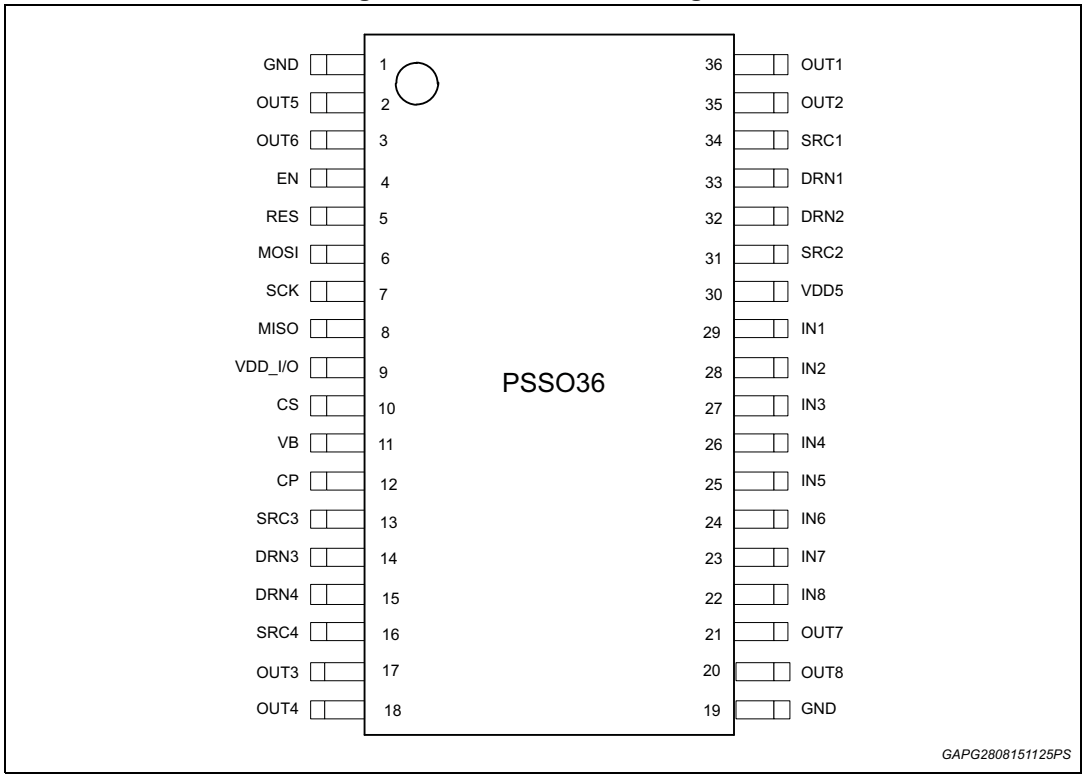


Table 2. Pin description

Pin	Symbol	Function
1	GND	Power ground of OUT1,2,5,6
2	OUT5	Output 5
3	OUT6	Output 6
4	EN	Enable
5	RES	Reset input (active low)
6	MOSI	SPI data in
7	SCK	SPI serial clock input
8	MISO	SPI data out
9	VDD_I/O	Microcontroller logic interface voltage
10	CS	SPI chip select (active low)
11	VB	Battery supply voltage
12	CP	Charge pump
13	SRC3	Source pin of configurable driver #3
14	DRN3	Drain pin of configurable driver #3

Table 2. Pin description (continued)

Pin	Symbol	Function
15	DRN4	Drain pin of configurable driver #4
16	SRC4	Source pin of configurable driver #4
17	OUT3	Output 3
18	OUT4	Output 4
19	GND	Power ground of OUT3,4,7,8
20	OUT8	Output 8
21	OUT7	Output 7
22	IN8	Discrete input used to PWM output driver #8
23	IN7	Discrete input used to PWM output driver #7
24	IN6	Discrete input used to PWM output driver #6
25	IN5	Discrete input used to PWM output driver #5
26	IN4	Discrete input used to PWM output driver #4
27	IN3	Discrete input used to PWM output driver #3
28	IN2	Discrete input used to PWM output driver #2
29	IN1	Discrete input used to PWM output driver #1
30	VDD5	5 Volt supply input
31	SRC2	Source pin of configurable driver #2
32	DRN2	Drain pin of configurable driver #2
33	DRN1	Drain pin of configurable driver #1
34	SRC1	Source pin of configurable driver #1
35	OUT2	Output 2
36	OUT1	Output 1
EP	GND	Exposed pad: connected to GND

3 Electrical specifications

3.1 Absolute maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Value [DC voltage]	Unit
VB	Supply voltage	-0.3 to 35	V
VDD, VDD_I/O	Stabilized supply voltage	-0.3 to 18(1)	V
V_{CS}, V_{SCK}, V_{MOSI}, V_{MISO}, V_{EN}, V_{IN1-8}, V_{RES}	Logic input/output voltage range	-0.3 to 18(1)	V
OUT1-8	-	-1 to VCL	V
SRC1-4	-	-1 to VB	V
DRN1-4	-	-1 to VCL	V
CP	-	-0.3 to (VB+CP_DELTA)	V
GND	-	-0.3 to +0.3	V

1. Short to 18 V for 100 h max.

Note: A suitable device to clamp the voltage during 'load dump' event to a value ≤35 V must be present at application level.

3.2 ESD protection

Table 4. ESD protection

Parameter	Value	Unit
ESD according to Human Body Model (HBM), Q100-002 for pins (1); (100 pF/1.5 kΩ)	±4000	V
ESD according to Human Body Model (HBM), Q100-002 for all other pins; (100 pF/1.5 kΩ)	±2000	V
ESD according to Charged Device Model (CDM), Q100- 011 Corner pins	±750	V
ESD according to Charged Device Model (CDM), Q100-011 Non-corner pins	±500	V

1. VB, DRN1-4, SRC1-4, OUT1-8.

3.3 Operating range

Table 5. Operating range

Symbol	Parameter	Min.	Max.	Unit
VB	Supply voltage	VB_UV	18	V
VDD	Stabilized supply voltage	VDD_UV	VDD_OV	V
VDD_IO	Logic output supply voltage	3.0	5.5	V

3.4 Thermal data

Table 6. Thermal data

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_{amb} (1)	Operating ambient temperature	-40	-	125	°C
T_{stg}	Storage temperature	-40	-	150	°C
T_j	Junction temperature	-40	-	175	°C
T_{sd}	Thermal shutdown temperature	180	-	195	°C
T_{sd-hys}	Thermal shutdown temperature hysteresis	-	10	-	°C

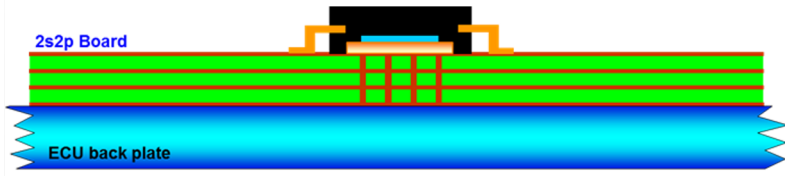
1. For information only, in any case T_j limits must not exceed.

Table 7. Thermal resistance

Symbol	Parameter	Working conditions	Value	Unit
$R_{th\ j\text{-}amb}$	Junction to ambient	2s2p (4L) board; Natural convection(1)	27	°C/W
		2s2p (4L) board on ECU metal plate(2)	8	°C/W
$R_{th\ j\text{-}bottom\ case}$	Junction to bottom case	Bottom cold plate(3)	1	°C/W
$R_{th\ j\text{-}top\ case}$	Junction to top case	Top cold plate(4)	21	°C/W
$Psi_{j\text{-}top\ case}$	Psi Junction to top case	2s2p (4L) board; Natural convection (1)	2	°C/W

1. Jedec STD. JESD51.
2. Package assembled on 2s2p (4L) board. The board bottom side is in contact with a metal plate as per typical automotive application (ECU system). See *Figure 3*.
3. Thermal resistance between the die and the bottom case surface in ideal contact and measured by cold plate as per Jedec best practice guidelines (JESD51).
4. Thermal resistance between the die and the top case surface in ideal contact and measured by cold plate as per Jedec best practice guidelines (JESD51).

Figure 3. Device assembled on 2s2p PCB with high density vias in contact with a metal plate



4 Supply pins

4.1 VDD

An external +5.0 ±0.25 VDC supply provided from an external source is the primary power source to the L9301. This supply is used as the power source for all of its internal logic circuitry and other miscellaneous functions.

The VDD is monitored for under and over voltage and a dedicated SPI flag of each event is set to report those conditions. Once the fault flag is asserted it will be latched until a clear operation, writing 0, is performed. The device behavior in case of VDD fault detection can be defined using the proper configuration bit (CR0: vdduv_conf, vddov_conf) that allows to choose if the OUT must be disabled or not.

5 V ≤ VB < 18 V; -40 °C ≤ Tj ≤ 175 °C unless otherwise specified.

Table 8. VDD

Pin	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
VDD	VDD_UV	VDD undervoltage detection threshold	VDD decreasing	4.5	-	4.7	V
	VDD_uv_filt	VDD undervoltage filter time for output disable	Tested by scan	90	-	145	µs
	VDD_OV	VDD overvoltage detection threshold	VDD increasing	5.25	-	5.5	V
	VDD_ov_filt	VDD overvoltage filter time for output disable	Tested by scan	90	-	145	µs
	VDD_Istby	VDD standby current consumption	VDD = 5.25 V EN = 0; RES = 0	-	-	7.5	mA
	VDD_Ibias	VDD current consumption	VDD = 5.25 V EN = 1; RES = 1	-	-	13.8	mA

4.2 VB

This input is the supply for the on board charge pump and it shall be connected to protect battery line. In case of high-side configuration, to get the specified Ron value this pin must be connected to the same VB where the loads are connected. If it is present an additional voltage drop between the two VB, the R_{dson} of that given output will be higher than the specified maximum.

The VB is monitored for under and over voltage and a dedicated SPI flag of each event is set to report those conditions. Once the fault flag is asserted it will be latched until a clear operation, writing 0, is performed. The device behavior in case of VB fault detection can be defined using the proper configuration bit that allows to choose if the OUT must be disabled or not.

5 V ≤ VB < 18 V; -40 °C ≤ Tj ≤ 175 °C unless otherwise specified.

Table 9. VB

Pin	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
VB	VB_UV	VB undervoltage detection threshold	VB decreasing	3.5	-	4	V
	VB_UV_on	VB undervoltage detection threshold	VB increasing	4	-	4.5	V
	VB_UV_hys	VB undervoltage hysteresis	-	0.1	-	1	V
	VB_UV_filt	VB undervoltage filtering time	Tested by scan	90	-	145	us
	VB_OV	VB overvoltage detection threshold	VB increasing	19	-	22	V
	VB_OV_on	VB overvoltage detection threshold	VB decreasing	19	-	21	V
	VB_UV_hys	VB overvoltage hysteresis	-	0.1	-	1	V
	VB_OV_filt	VB overvoltage filtering time	Tested by scan	90	-	145	µs
	VB_Istby	VB standby current consumption	VB = 18 V EN = 0; RES = 0	-	-	0.19	mA
	VB_Ibias	VB current consumption	VB = 18 V EN = 1; RES = 1	-	-	0.55	mA

4.3 VDD_IO

This pin is used to supply the discrete MISO output stage of L9301 and must be connected to the same voltage used to supply the peripherals of the processor interfaced to L9301.

Table 10. VDDIO

Pin	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
VDDIO	VDDIO_Istby	VDDIO standby current consumption	VDDIO = 5.25 V EN = 0; RES = 0	4.5	-	4.7	mA
	VDDIO_Ibias	VDDIO current consumption	VDDIO = 5.25 V EN = 1; RES = 1	90	-	145	mA

5 Discrete inputs

5.1 Output enable EN

The EN pin is the general output enable which allows the µC to immediately switch off the output in case of need. Output driving is allowed only if this pin is driven to high level. The device configuration can be changed only with EN pin is driven to low level.

An internal pull down is present on the pin.

5.2 Output enable input IN1 to IN8

These inputs allow the outputs, depending on the configuration selected, to be enabled without the use of the SPI. The SPI command and the IN1-8 input are logically OR'd together.

A logic ‘1’ on this input will enable the correspondent output no matter what the status of the SPI command register is. A logic ‘0’ on this input will disable this output if the SPI command register is not commanding this output on. These pins can be left ‘open’ if the internal power stages are controlled only via the SPI. This input has a nominal 100 kΩ pull down resistor to GND, which will pull this pin to ground if an open circuit condition occurs. This input is ideally suited for loads that are pulse width modulated (PWM'd). This allows PWM control without the use of the SPI inputs.

Table 11. Output enable input IN1 to IN8

EN	RESET	INx	OUTx/DRNx/SRCx
X	0	X	OFF
0	X	X	OFF
1	1	0	OFF
1	1	1	ON

5.3 Reset input

When this input goes low it resets all the internal registers and switches off all the output stages. This input has a nominal 100 kΩ resistor connected from this pin to the internal 3.3 V regulator, which will pull this pin to 3.3 V if an open circuit condition occurs. No filter is present on this input so spurious pulse must be avoided.

5 V ≤ VB < 18 V; -40 °C ≤ Tj ≤ 175 °C unless otherwise specified.

Table 12. Electrical characteristic of EN, IN1...8, RES pin

Pin	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
IN1...8, EN, RES	V_IH	Logic input high voltage	-	1.75		VDD+0.3	V
	V_IL	Logic input low voltage	-	-0.3		0.75	V
	V_Ihys	Logic input hysteresis	-	100		1000	mV
IN1...8, EN	Ri_pd	Pull down resistor	Tested at 1.5 V	50	100	150	kΩ
RES	Ri_pu	Pull up resistor	Tested at 1.5 V, R = (3.3-1.5)/$I_{measure}$	50	100	150	kΩ

6 Configuration

The selected configuration can be configured by SPI, there are 2 bits dedicated to configuration selection:

Table 13. Configuration

Bit1	Bit0	Configuration	Input → Output	Description
0	0	1	IN1-4 → DRN1-4, OUT1-4 (paralleled) IN5-8 → OUT5-8	8 low side channels with R_{dson} = 0.3 Ω
0	1	2	IN1-4 → OUT1-4 IN5-8 → OUT5-8	4 low side channels with R_{dson} = 0.6 Ω 4 low side channels with R_{dson} = 0.3 Ω
1	0	3	IN1-4 → SRC1-4, IN5-8 → OUT5-8	4 high side channels with R_{dson} = 0.6 Ω 4 low side channels with R_{dson} = 0.3 Ω
1	1	4	IN1-4 → OUT1-4, IN5-8 → OUT5-8, SPI → DRN/SRC1-4	4 low side channels with R_{dson} = 0.6 Ω 4 low side channels with R_{dson} = 0.3 Ω 4 low/high side ch. with R_{dson} = 0.6 Ω

The configuration is enabled only when EN pin is logic 0.

In configuration 4, the output DRN/SRC1-4 can be controlled by SPI only; for those outputs the selection between high side and low side configuration can be done through the dedicated bit (bit8 of Device general configuration register).

7 Configuration 1: 8 low side drivers

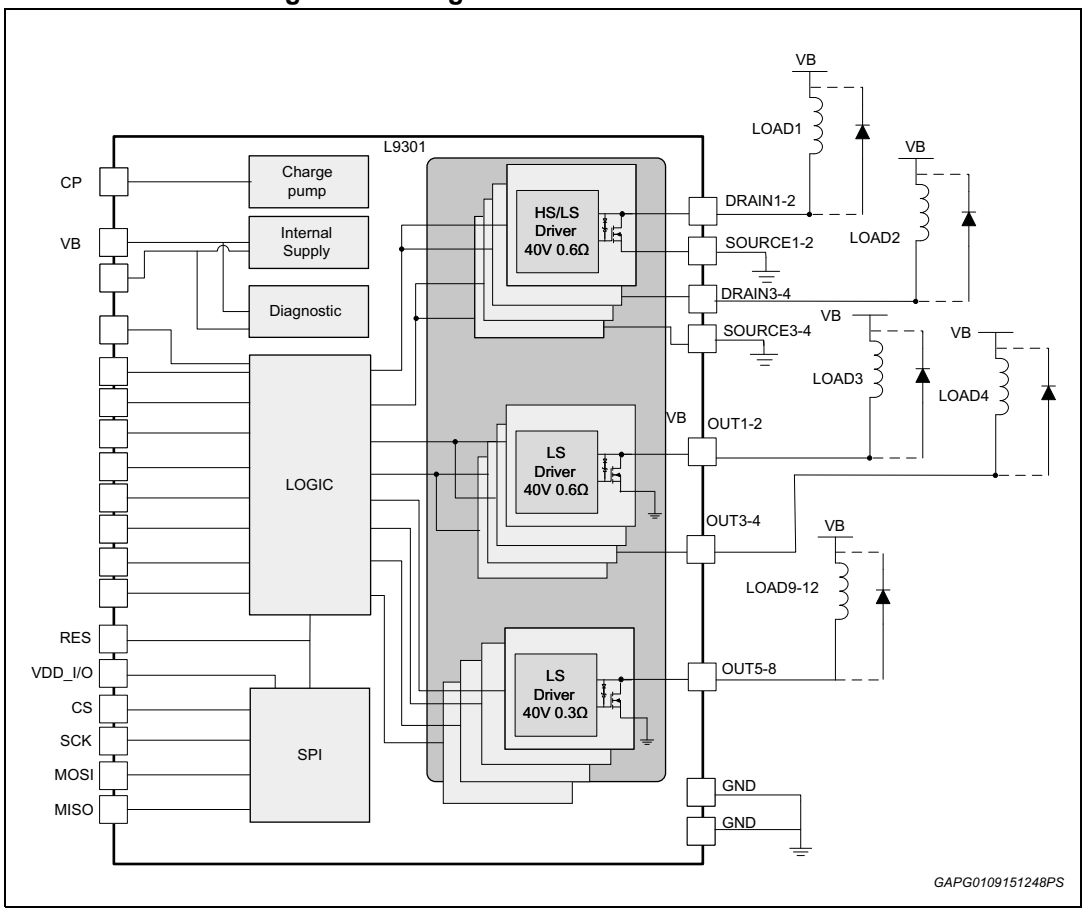
In this configuration there are 8 low side drivers available that can be driven by SPI or by the parallel input: IN1-4 control both DRAIN1-4 and OUT1-4 that must be turned on and off simultaneously while IN5-8 control OUT5-8. Parallelized output must be externally connected to each other to ensure correct functionality and diagnostic.

The corresponding relations are:

Table 14. Config 1

INx	SPI: CR13	Output
IN1	Cmd1	OUT1//OUT2
IN2	Cmd2	OUT3//OUT4
IN3	Cmd3	DRN1//DRN2
IN4	Cmd4	DRN3//DRN4
IN5	Cmd5	OUT5
IN6	Cmd6	OUT6
IN7	Cmd7	OUT7
IN8	Cmd8	OUT8

Figure 4. Configuration 1: 8 Low side drivers



Note: pwm_en bit has no effect in this configuration

7.1 Configuration 2: 4 low-side PWM mode and 4 low-side drivers

In this configuration there are 4 low side drivers with integrated free-wheeling diodes and 4 low side drivers available. All the channels can be driven by SPI or by the parallel input. To enable the OUT1-4 driving, the PWM enable SPI bit for OUT1-4 and SRC1-4 must be set.

The IN1-4 control the low side power OUT1-4 used to drive the LOAD1-4 and the device assures that when the low-side is switched off, the high-side, acting as a free-wheeling diode, must be turned on. To avoid cross conduction the LS VGS voltage is monitored.

When OUT1-4 are commanded ON either by INx or SPI, the L9301 switches off the HS first, then with 2 µs delay after detecting HS VGS low, it switches on LS.

When OUT1-4 are commanded OFF either by INx or SPI, the L9301 switches off the LS first, then with 2 µs delay after detecting LS VGS low, it switches on the HS.

IN5-8 control OUT5-8

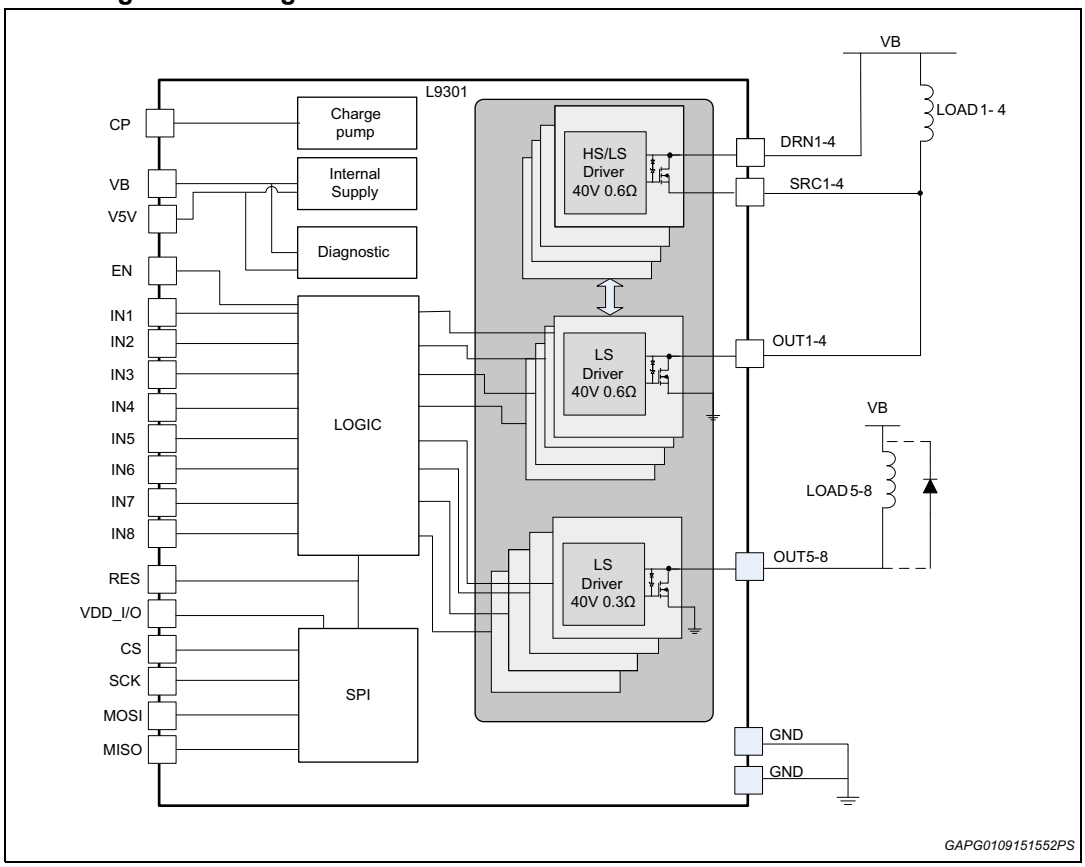
The selected configuration must be configured by SPI and the wanted channel must be enabled using pwm_en bit in the corresponding register.

The corresponding relations are:

Table 15. Config 2

INx	SPI: CR13	Output
IN1	Cmd1	OUT1 <-> SRC2
IN2	Cmd2	OUT2 <-> SRC1
IN3	Cmd3	OUT3 <-> SRC4
IN4	Cmd4	OUT4 <-> SRC3
IN5	Cmd5	OUT5
IN6	Cmd6	OUT6
IN7	Cmd7	OUT7
IN8	Cmd8	OUT8

Figure 5. Configuration 2: 4 low-side PWM mode and 4 low-side drivers



7.2 Configuration 3: 4 high-side PWM mode and 4 low-side drivers

In this configuration there are 4 high side drivers with integrated free-wheeling diodes and 4 low side drivers available. All the channels can be driven by SPI or by the parallel input. To enable the SRC1-4 driving, the PWM enable SPI bit for SRC1-4 and OUT1-4 must be set.

The IN1-4 control the high side power SRC1-4 used to drive the LOAD1-4 and the device assures that when the high-side is switched off, the low-side, acting as a free-wheeling diode, must be turned on. To avoid cross conduction the HS VGS voltage is monitored.

When SRC1-4 is commanded ON either by INx or SPI, the L9301 switches off the LS first, then with 2 µs delay after detecting LS VGS low, it switches on HS.

When SRC1-4 is commanded OFF either by INx or SPI, the L9301 switches off the HS first, then with 2 µs delay after detecting HS VGS low, it switches on the LS.

IN5-8 control OUT5-8

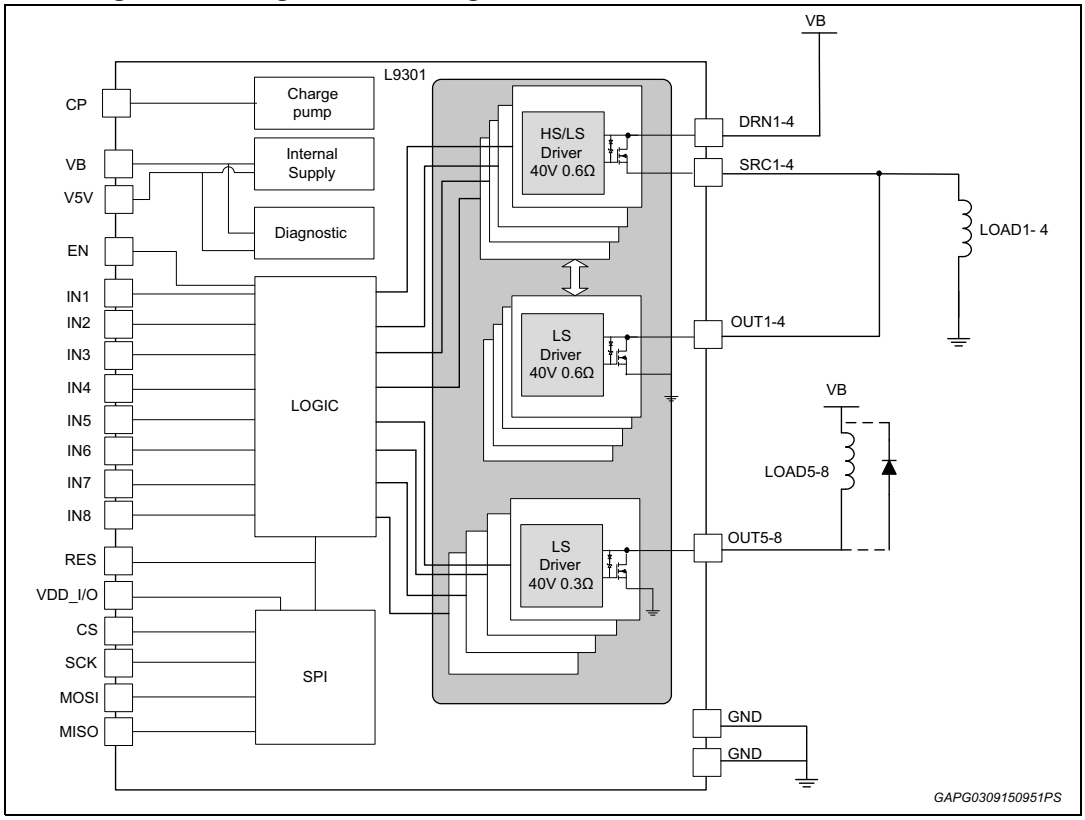
The selected configuration must be configured by SPI and the wanted channel must be enabled using pwm_en bit in the corresponding register.

The corresponding relations are:

Table 16. Config 3

INx	SPI: CR13	Output
IN1	Cmd1	SRC1 <-> OUT2
IN2	Cmd2	SRC2 <-> OUT1
IN3	Cmd3	SRC3 <-> OUT4
IN4	Cmd4	SRC4 <-> OUT3
IN5	Cmd5	OUT5
IN6	Cmd6	OUT6
IN7	Cmd7	OUT7
IN8	Cmd8	OUT8

Figure 6. Configuration 3: 4 high-side PWM mode and 4 low-side drivers



7.3 Configuration 4: 4 configurable drivers and 8 low-side drivers

In this configuration there are 4 HS/LS drivers and 8 low side drivers available. All the LS can be driven by SPI or by the parallel input.

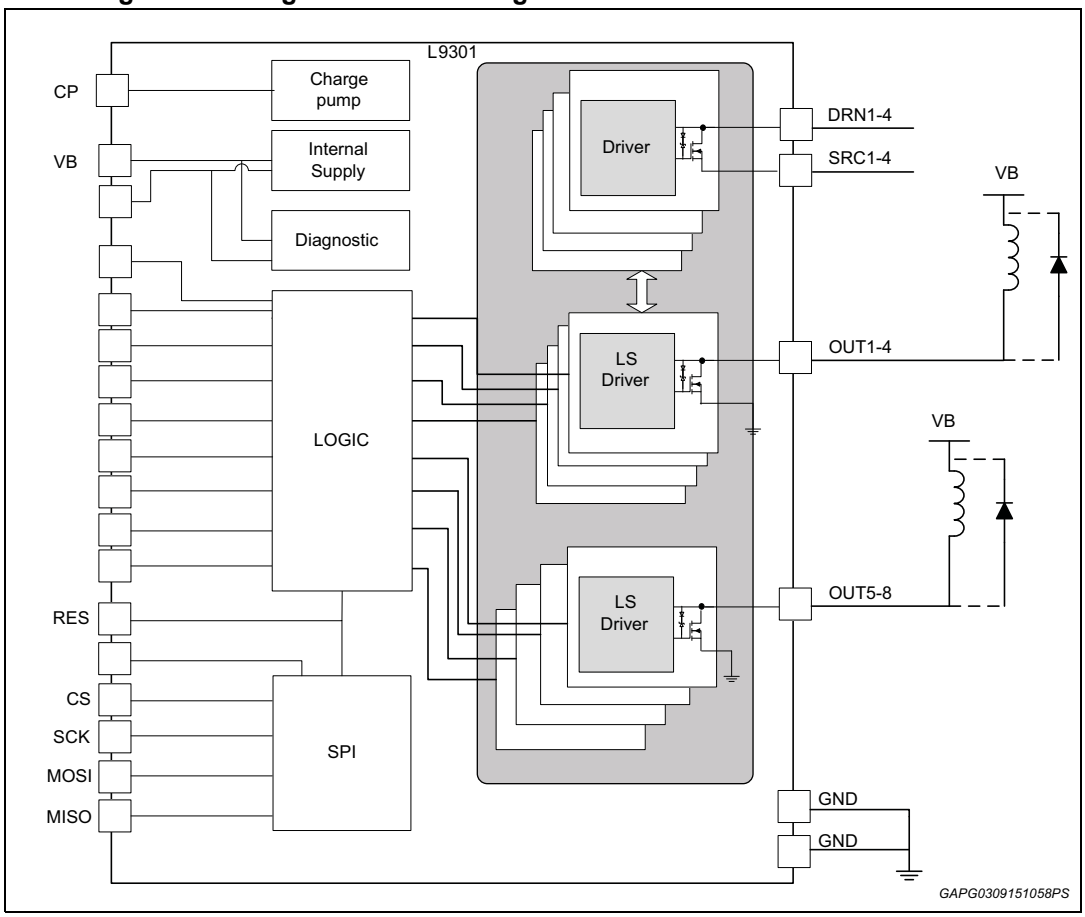
The IN1-8 control OUT1-8 while the configurable driver can only be controlled by SPI.

The four configurable drivers (DRN1-4, SRC1-4) can be configured separately as LS or HS using the dedicated SPI bit.

Table 17. Config 4

INx	SPI: CR13	Output
IN1	Cmd1	OUT1
IN2	Cmd2	OUT2
IN3	Cmd3	OUT3
IN4	Cmd4	OUT4
IN5	Cmd5	OUT5
IN6	Cmd6	OUT6
IN7	Cmd7	OUT7
IN8	Cmd8	OUT8
-	Cmd9	DRN1 - SRC1
-	Cmd10	DRN2 - SRC2
-	Cmd11	DRN3 - SRC3
-	Cmd12	DRN4 - SRC4

Figure 7. Configuration 4: 4 configurable drivers and 8 low-side drivers



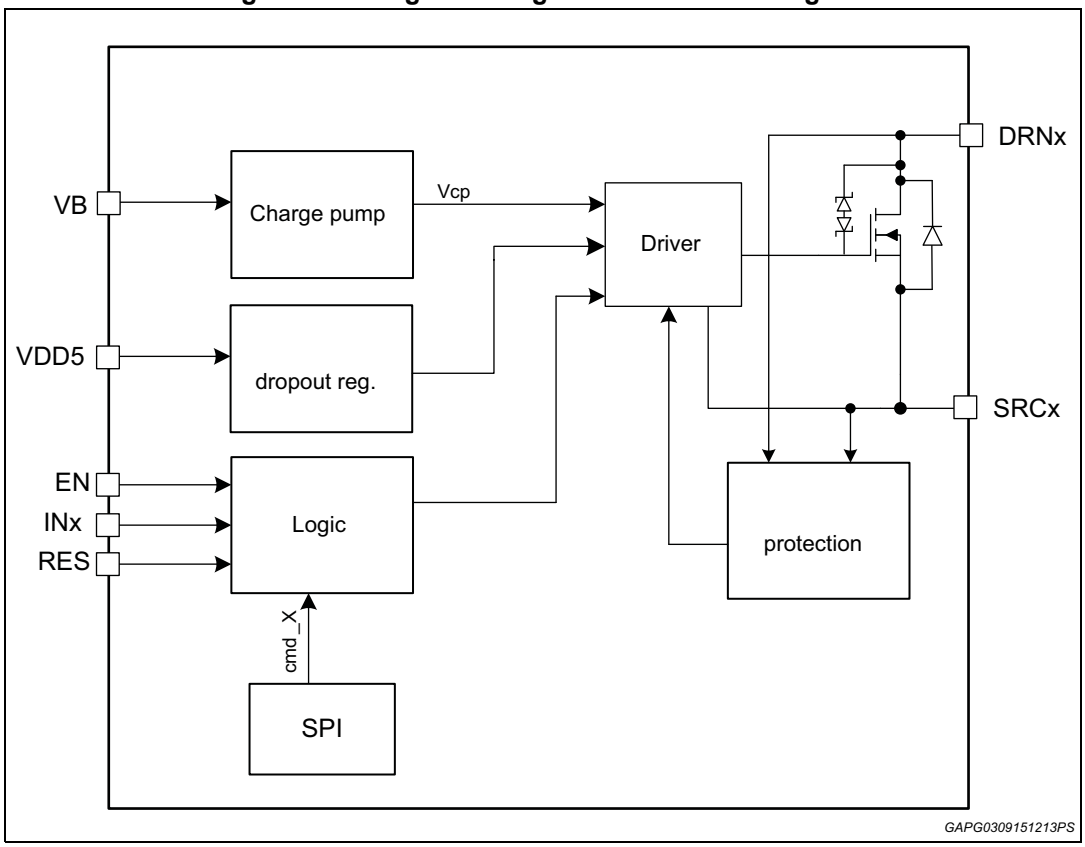
Note: pwm_en bit has no effect in this configuration

8 Configurable high/low side driver

The channels 1 to 4 can be configured as high or low side using SPI CR0: conf4_lshs. In the low side configuration an internal clamp is present.

In high side configuration, the DRNx are connected to VB pin on PCB. To guarantee the OC (over current) function, the DRNx voltage has to be within the range of (VB-1 V, VB+1 V).

Figure 8. Configurable high/low side driver diagram



8.1 Electrical characteristics DRN/SRC1-4

5 V ≤ VB < 18 V; -40°C ≤ T_j ≤ 175°C unless otherwise specified.

Table 18. Configurable high/low side drivers 1-4 electrical characteristics

Pin	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
DRN1-4 SRC1-4	$R_{DS\text{-}on_HLS}$	-	HS/LS configuration VB = 13.5 V; I_load = 1 A	-	-	0.6	Ω

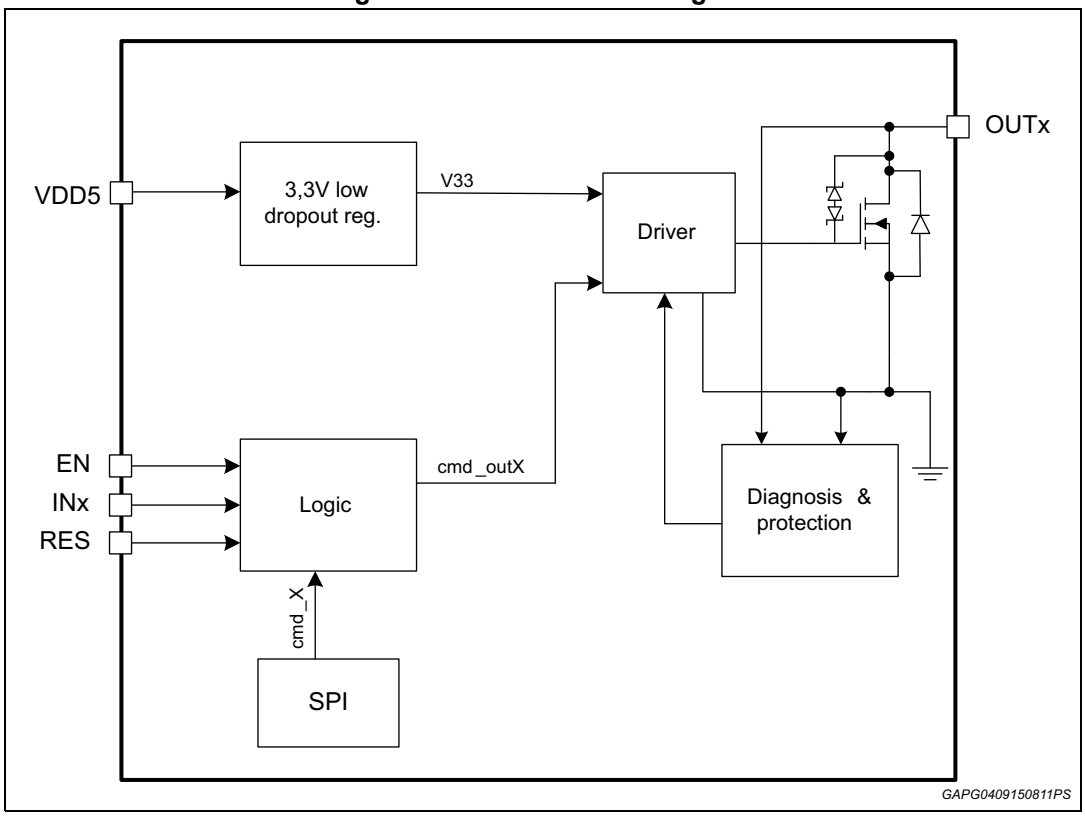
Table 18. Configurable high/low side drivers 1-4 electrical characteristics (continued)

Pin	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
DRN1-4 SRC1-4	$I_{OUT_LK_HLS}$	Output leakage current	HS configuration DRNx = 13.5 V; SRCx = 0 V	-	-	10	µA
			LS configuration DRNx = 13.5 V; SRCx = 0 V	-	-	10	µA
	V_S/RS	Voltage S/R on/off slow	HS/LS configuration VB 13.5 V Load: 8 Ω, 10 nF – From 80% to 30% of DRNx(SRCx)	2	4	6	V/µs
	V_S/Rf	Voltage S/R on/off fast	HS/LS configuration VB 13.5 V Load: 8 Ω, 10 nF – From 80% to 30% of DRNx(SRCx)	5	10	15	V/µs
	$T_{turn\text{-}on_HLS}$	Turn-on delay time	HS configuration VB 13.5 V From command to 10% SRCx Load: 8 Ω, 10 nF	-	-	3	µs
			LS configuration VB 13.5 V From command to 90% DRNx Load: 8 Ω, 1 0nF	-	-	3	µs
	$T_{turn\text{-}off_HLS}$	Turn-off delay time	HS configuration VB 13.5 V From command to 90% SRCx Load: 8 Ω, 10 nF	-	-	3	µs
			LS configuration VB 13.5 V From command to 10% DRNx Load: 8 Ω, 10 nF	-	-	3	µs
	Min_duty	Minimum ON/OFF time of INx or SPI CMDx	Note for application	-	-	28	µs
	V_{CL_LS}	Output clamping voltage	LS configuration I_load= 0.6 A T = 130 °C	34	37.5	41	V
			LS configuration I_load = 0.6 A, T = -40 °C and 25 °C	35	37.5	41	
	$E_{clampSP_LS}$	Energy repetitive pulse	LS configuration I_load = 0.7 A, T_j = 150 °C, 100 kpulses	-	-	5	mJ
	$E_{clampSP_LS}$	Single pulse energy	LS configuration I_load = 0.7 A, T_j = 150 °C	-	-	10	

9 Low side driver

The channels OUT1 to 8 are low side drivers with internal clamp.

Figure 9. Low side driver diagram



9.1 Electrical characteristics OUT1-4

5 V ≤ VB < 18 V; -40 °C ≤ T_j ≤ 175 °C unless otherwise specified.

Table 19. Low-side drivers OUT1-4 electrical characteristics

Pin	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
OUT1-4	$R_{DS\text{-}on_LS}$	Drain–source resistance	I_load = 1 A	-	-	0.6	Ω
	$I_{OUT_LK_LS}$	Output leakage current	OUTx = 13.5 V	-	-	10	µA
	V_{S/R_s_LS}	Voltage S/R on/off “slow”	VB = 13.5 V Load: 8 Ω, 10 nF – From 80% to 30% of OUTx	2	4	6	V/µs
	V_{S/R_f_LS}	Voltage S/R on/off “fast”	VB = 13.5 V Load: 8 Ω, 10 nF – From 80% to 30% of VOUT	5	10	15	V/µs

Table 19. Low-side drivers OUT1-4 electrical characteristics (continued)

Pin	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
OUT1-4	$T_{turn-on_LS}$	Turn-on delay time	From command to 80% OUTx, VB = 13.5 V Load: 8 Ω, 10 nF	-	-	3	µs
	$T_{turn-off_LS}$	Turn-off delay time	From command to 30% OUTx, VB = 13.5 V Load: 8 Ω, 10nF	-	-	3	µs
	Min_duty	Minimum ON/OFF time of INx or SPI CMDx	Note for application	-	-	28	µs
	V_{CL_LS}	Output clamping voltage	I_load = 0.6 A T = 130 °C	34	37.5	41	V
			I_load = 0.6A T= -40 °C and 25 °C	35	37.5	41	
	$E_{clampSP_LS}$	Energy repetitive pulse	LS configuration I_load = 0.7 A, T_j = 150 °C, 100 kpulses	-	-	5	mJ
	$E_{clampSP_LS}$	Single pulse energy	LS configuration I_load = 0.7 A, T_j = 150 °C	-	-	10	

9.2 Electrical characteristics OUT5-8

5 V ≤ VB < 18 V; -40 °C ≤ T_j ≤ 175 °C unless otherwise specified.

Table 20. Low-side drivers OUT5-8 electrical characteristics

Pin	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
OUT5-8	$R_{DS\text{-}on_LS}$	Drain–source resistance	I_load = 2 A	-	-	0,3	Ω
	$I_{OUT_LK_LS}$	Output leakage current	OUTx = 13.5 V	-	-	10	µA
	V_{S/R_s_LS}	Voltage S/R on/off “slow”	VB = 13.5 V Load: 8 Ω, 10 nF – From 80% to 30% of OUTx	2	4	6	V/µs
	V_{S/R_f_LS}	Voltage S/R on/off “fast”	VB = 13.5 V Load: 8 Ω, 10 nF – From 80% to 30% of VOUT	5	10	15	V/µs
	$T_{turn\text{-}on_LS}$	Turn-on delay time	From command to 80% OUTx Load: 8 Ω, 10 nF	-	-	3	µs
	$T_{turn\text{-}off_LS}$	Turn-off delay time	From command to 30% OUTx Load: 8 Ω, 10 nF	-	-	3	µs
	Min_duty	Minimum ON/OFF time of INx or SPI CMDx	Note for application	-	-	28	µs
	V_{CL_LS}	Output clamping voltage	I_load = 1.25 A T = 130 °C	34	37.5	41	V
			I_load = 1.25 A T= -40 °C and 25 °C	35	37.5	41	
	$E_{clampSP_LS}$	Energy repetitive pulse	LS configuration I_load = 2.2 A, T_j = 150 °C, 100 kpulses	-	-	15	mJ
	$E_{clampSP_LS}$	Single pulse energy	LS configuration I_load = 2.2 A, T_j = 150 °C	-		18.1	mJ

9.3 Driver diagnostic

9.3.1 Thermal protection

Each solenoid channel has a dedicated temperature sensor that continuously monitors the temperature of the PowerMOS.

In case the shutdown temperature T_{sd} is reached the related channel is turned off and the dedicated diagnostic bits are set. t_sdl_x is the bit that latches the thermal shut down and it is cleared after sending dedicated SPI to clear the bit, t_sd_x is the other thermal shut down bit and once it is set by thermal shut down condition it is cleared only when the T_j decreases below the thermal shut down threshold (hysteresis). If the microcontroller, when the device

is still in temperature shut down condition (t_sd_x = 1), clears the t_sdl_x and tries to turn on the output, the actuation is not performed and the t_sdl_x will be set again. To avoid these multiple interrupts the microcontroller can poll the t_sd_x bit and enable the next actuation only when the bit is zero.

To re-switch on the channel after thermal shut down, the SPI needed to switch off the channel is required.

9.3.2 Overcurrent protection

An overcurrent protection is present for each driver OUT1-8 and DRN/SRC1...4. The overcurrent threshold is selectable through oc_thres_x (where x indicates the channel). In case of overcurrent the output driver is turned off and a dedicated diagnostic bit is set oc_x where x indicates the channel where the fault occurred.

If bit oc_restart = 0, to restart the channel the microcontroller has to clear the fault bit (writing 0 in the corresponding SPI flag), and to write to 1 the SPI command bit or to provide a rising edge on the parallel input command.

If bit oc_restart = 1, the restart function is activated. The slew rate of the channel in fault condition is automatically set to the higher value to limit dissipation issue then to restart the channel the microcontroller has to write to 1 the SPI command bit or to provide a rising edge on the parallel input command.

The diagnostic bit oc_x can be cleared only by writing it to 0 in the corresponding driver status register by SPI however the channel can be restarted as described above.

9.3.3 Output status

During the ON phase, the output voltage is compared with the VTopen threshold voltage in order to verify if the output status is aligned with the ON command:

- in case of low side usage if the DRNx voltage is above the VTopen threshold a dedicated bit (SRx: bit 8 os) is set to indicate the anomaly
- in case of high side usage if the SRCx voltage is below the VTopen threshold a dedicated bit is (SRx: bit 8 os) set to indicate the anomaly
- if OUTx voltage is above VTopen threshold a dedicated bit (SRx: bit 8 os) is set to indicate the anomaly

9.3.4 Charge Pump (CP)

The charge pump is enabled when the selected configuration includes high side drivers (like configuration 2, 3, 4). In configuration 1 the charge pump is internally shorted to VB.

On the CP pin it's required to connect a 100 nF capacitor toward the VB line.

The charge pump is ON if VB > UV threshold & VDD > UV threshold

The charge pump is OFF if VB< UV threshold or VDD< UV threshold. The CP voltage is equal to VB-Vbe.

When the CP is ON, the low CP diagnosis is enabled. When any HS is switched on but CP voltage is not high enough to switch on HS, low CP fault is detected and stored in cpl SPI flag. In order to reset the flag a 0 has to be written by microcontroller. A SPI bit allows configuring the actions to be taken in case of low CP fault.

5 V ≤ VB < 18 V; -40 °C ≤ T_j ≤ 175 °C unless otherwise specified.

Table 21. Charge pump

Pin	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
CP	CP_DELTA	Delta voltage CP-VB	VB>5V	3	-	6	V

9.3.5 DLOSS

When the L9301 is configured with low side and external diodes are used for freewheeling, there is the possibility through a dedicated SPI bit to enable the ‘diode loss’ diagnosis that is used to detect if the external diode is no more connected checking if during the OFF phase the internal clamp is activated. In case of fault is stored in DLOSS SPI flag. In order to reset the flag a 0 has to be written by microcontroller. Another SPI bit allows configuring the actions to be taken in case of DLOSS fault.

When the L9301 is configured as high side and internal/external diodes are used for freewheeling, there is the possibility through a dedicated SPI bit to enable the ‘diode loss’ diagnosis that is used to detect if the diode is no more connected checking if during the OFF phase the HS is forced to switch on. In case of fault is stored in DLOSS SPI flag. In order to reset the flag a 0 has to be written by microcontroller. Another SPI bit allows configuring the actions to be taken in case of DLOSS fault.

In addition, diode loss on LS (including configurable channels configured as LS) is only detected when VBOV is not present.

9.3.6 OFF state diagnostic

The device provides the off-state diagnostic for each channel.

In low-side configuration the short to ground and open load faults can be detected. The fault is reported in a SPI register. The pull-up current on the single channel can be disabled using the dis_source bit in registers CR1-CR12. The OFF diagnostic can be disabled using the dis_diag_off bit in registers CR1-CR12.

Figure 10. LS configuration diagnostic

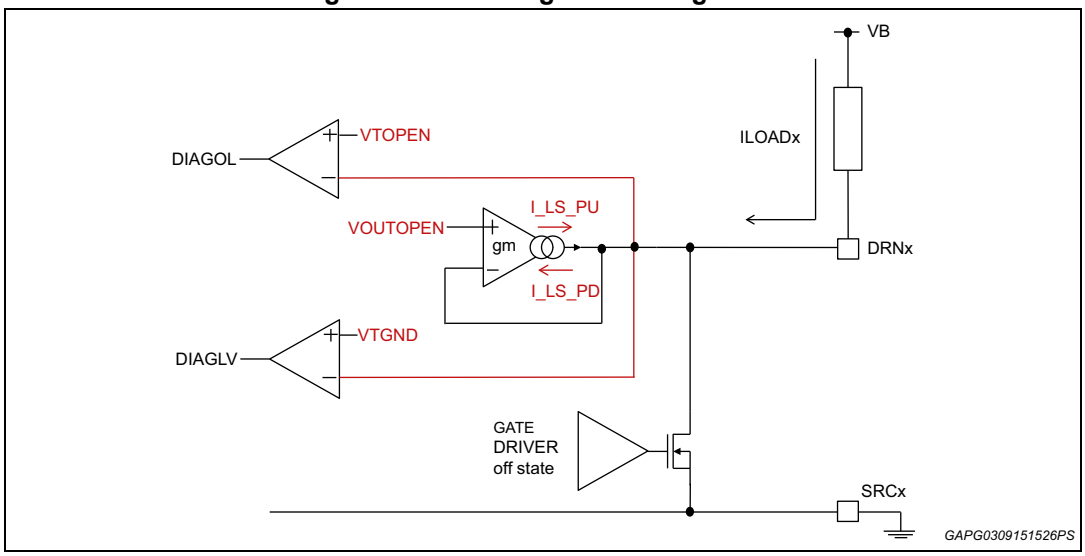


Table 22. LS diagnostic

DIAGOL	DIAGLV	FAULT DETECTION
0	0	no fault
0	1	not possible
1	0	open load
1	1	short to ground

In high-side configuration the short to battery and open load faults can be detected. The fault is reported in a SPI register.

Figure 11. HS configuration diagnostic

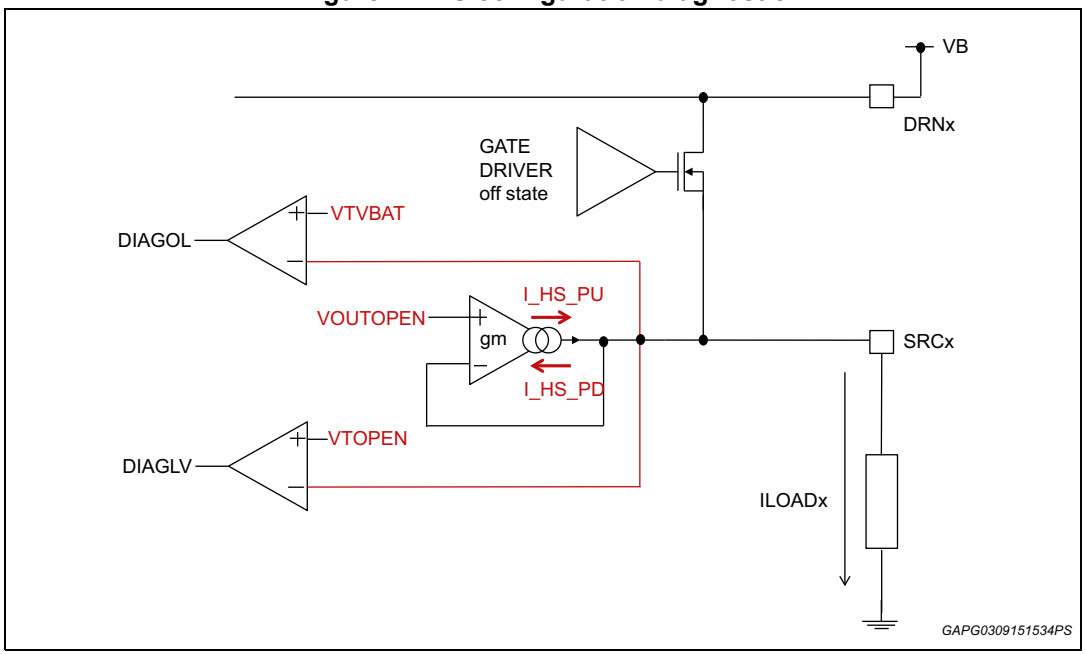


Table 23. HS diagnostic

DIAGOL	DIAGLV	FAULT DETECTION
0	0	short to battery
0	1	not possible
1	0	open load
1	1	no fault

The diagnostic blanking time is configurable through the dedicated diagoff_blank_sel bit.

The OFF diagnosis is triggered at driver OFF CMD and will not be refreshed after clearing the flags. To recover the OFF diagnosis in OFF stage, send SPI to disable OFF diagnosis and then enable it.

9.3.7 Over current (OC) comparator self-test

L9301 provides driver OC (over current) comparator self-test function. During OFF phase, the OC comparator still works and the expected result is '1' due to high drain-source voltage. If L9301 detects OC '0' during OFF phase, the SPI bit oc_comparator_f is set to '1'.

For DRN1-4, when they are configured as LS, a Short To Ground (STG) fault will not trigger OC '1', so L9301 will report both STG and OC comparator self-test fail, when they are configured as HS, a short-to-battery (STB) fault will not trigger OC '1', so L9301 will report both STB and OC comparator self-test fail. For OUT1-8, if a STG is present at OFF phase, the OC comparator inputs are still forced to have OC '1'.

9.3.8 Electrical characteristics related to diagnosis

5 V ≤ VB < 18 V; -40 °C ≤ T_j ≤ 175 °C unless otherwise specified.

Table 24. Electrical characteristics related to diagnosis

Pin	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
DRN1-4 SRC1-4	$T_{Over_temperature_blanking}$	Over temperature blanking time	Tested by scan	1	-	1.5	µs
	$T_{Over_temperature_filter}$	Over temperature filter time	Tested by scan	2	-	5	µs
	$T_{Charge_pump_low}$	Charge pump low filter time	Tested by scan	3	-	5	µs
	$T_{Charge_pump_low_blanking}$	Charge pump low blanking time	Tested by scan	25	-	40	µs
	$T_{diode_loss_filter_time}$	Diode loss filter time	Tested by scan	3	-	5	µs
	$R_{open_load_HLS}$	Min. resistor value open load detection	Not tested	10	-		kΩ
	I_{OC_HLS}	Over current threshold 1	-	1	2	3	A
	I_{OC_HLS}	Over current threshold 2	-	3	4	5	A
	$T_{FLT_OC_HLS}$	Over current filtering time	Tested by scan	3	-	5	µs
	$T_{FLT_diagoff_HLS}$	Filtering open load and short to GND diag. off	Tested by scan	55	-	80	µs
	$T_{d_blank0_HLS}$	Diagnosis blanking time after switch-off	Tested by scan	900	-	1300	µs
	$T_{d_blank1_HLS}$	Diagnosis blanking time after switch-off	Tested by scan	450	-	650	µs
	V_{TOPEN_HS}	Open load threshold voltage	HS configuration	1.9	2.1	2.3	V
	V_{TOPEN_LS}		LS configuration	2.7	2.9	3.1	V

Table 24. Electrical characteristics related to diagnosis (continued)

Pin	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
DRN1-4 SRC1-4	$V_{OUTOPEN_HLS}$	Open load output voltage	HS and LS configuration Open load condition	2,3	-	2,7	V
	V_{TVBAT_HS}	Output short-circuit to VB voltage threshold (HS configuration)	HS configuration	2.7	-	3.1	V
	V_{TGND_LS}	Output short-circuit to GND voltage threshold (LS configuration)	LS configuration	1.9	-	2.3	V
	$I_{OUT_PD_HLS}$	Output diagnostic pull- down current @ OFF STATE	HS configuration DRNx =13.5V SRCx =5V	210	245	300	µA
			LS configuration DRNx =5V SRCx =0V	40	70	100	µA
	$I_{OUT_PU_HLS}$	Output diagnostic pull-up current @ OFF STATE	HS configuration DRNx =13.5V SRCx =1.5V	40	70	100	µA
			LS configuration DRNx =1.5V SRCx =0V	50	75	100	µA
	-	Minimum OFF time for correct diagnostic (Blank time 0)	Application note NOT TESTED (ESD cap < 12nF, Bit_blank=0)	-	1380	-	µs
	-	Minimum OFF time for correct diagnostic (Blank time 1)	Application note NOT TESTED (ESD cap < 6nF, Bit_blank=1)	-	730	-	µs

Table 24. Electrical characteristics related to diagnosis (continued)

Pin	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
OUT1-8	$T_{Over_temperature_blanking}$	Over temperature blanking time	Tested by scan	1	-	1.5	µs
	$T_{Over_temperature_filter}$	Over temperature filter time	Tested by scan	2	-	5	µs
	$R_{open_load_LS}$	Min. resistor value open load detection	Not tested	50	-	-	kΩ
	I_{MAX_LS}	Output current	Not tested	-	2.2	-	A
	I_{OVC1_OUT1-4}	Over current threshold1 OUT1-4	-	1	2	3	A
	I_{OVC2_OUT1-4}	Over current threshold2 OUT1-4	-	3	4	5	A
	I_{OVC1_OUT5-8}	Over current threshold1 OUT5-8	-	2	4	6	A
	I_{OVC2_OUT5-8}	Over current threshold2 OUT5-8	-	6	8	10	A
	$T_{FLT_OVC_LS}$	Over current filtering time	Tested by scan	3	-	5	µs
	$T_{FLT_diagoff_LS}$	Filtering open load and short to GND diag. off	Tested by scan	55	-	80	µs
	$T_{d_blank0_LS}$	Diagnosis blanking time after switch-off	Tested by scan	600	-	900	µs
	$T_{d_blank1_LS}$	Diagnosis blanking time after switch-off	Tested by scan	300	-	450	µs
	V_{TOPEN_LS}	Open load threshold voltage	-	2.7	-	3.1	V

Table 24. Electrical characteristics related to diagnosis (continued)

Pin	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
OUT1-8	$V_{OUTOPEN_LS}$	Open load output voltage	Open load condition	2,3	2.5	2,7	V
	V_{TGND_LS}	Output short-circuit to GND voltage threshold	-	1.9	-	2.3	V
	$I_{OUT_PD_LS}$	Output diagnostic pull- down current @ OFF STATE	OUTx = 5 V	40	70	100	µA
	$I_{OUT_PU_LS}$	Output diagnostic pull-up current @ OFF STATE	OUTx=1.5 V	50	75	100	µA
	-	Minimum OFF time for correct diagnostic (Blank time 0)	Application note (ESD cap < 12 nF, Bit_blank = 0)	980	-	-	µs
	-	Minimum OFF time for correct diagnostic (Blank time 1)	Application note (ESD cap < 6 nF, Bit_blank = 1)	530	-	-	µs

9.4 Combined diagnosis (configuration 1, 2 & 3)

In configuration 1, there are four couples of drivers in parallel to get four channels with lower RdsON: OUT1 with OUT2, OUT3 with OUT4, DRN1 with DRN2, and DRN3 with DRN4. For each couple, only one driver off diagnosis is enabled (OUT1, OUT3, DRN1, DRN3) while the off diagnosis results are stored in both drivers registers. The other diagnosis of the two drivers in parallel, as over-current, over-temperature and DLOSS, are both enabled.
The correct effect of the diagnosis can be guaranteed only if the drivers are correctly parallelized externally.

In configuration 2 the off diagnosis is enabled for OUT1-4 only. Considering that the diagnosis blanking time can be longer than the off time of PWM, the diagnosis results can be affected. The short to GND fault can be detected by the HS OC fault when it is switched on. The Open Load Fault can be detected when PWM is disabled (PWM disable SPI bit = 1) only because in such a condition both HS and LS are OFF. In this condition the OUTx is pulled down by LS off diagnosis pull down current (typical 70 µA) and it's necessary to wait the time needed to discharge OUTx to get Open Load (OL) detection. The time to be considered starts from the PWM disable bit writing.

Table 25. Configuration 2

Parameter	Test condition	Min.	Typ.	Max.	Unit
Minimum OFF time for correct diagnostic (Blank time 0)	Application note NOT TESTED (ESD cap < 12 nF, Bit_blank = 0)	4140	-	-	µs
Minimum OFF time for correct diagnostic (Blank time 1)	Application note NOT TESTED (ESD cap < 6 nF, Bit_blank=1)	2190	-	-	µs

In configuration 3 the off diagnosis is enabled for HS1-4 only. Considering that the diagnosis blanking time can be longer than the off time of PWM, the diagnosis results can be affected. The short to VB fault can be detected by the OC fault when it is switched on. The Open Load Fault can be detected when PWM is disabled (PWM disable SPI bit = 1) only because in such a condition both HS and LS are OFF. In this condition the OUTx is pulled up by HS off diagnosis pull up current (typical 75 µA) and it's necessary to wait the time needed to discharge OUTx to get Open Load (OL) detection. The time to be considered starts from the PWM disable bit writing.

Table 26. Configuration 3

Parameter	Test condition	Min.	Typ.	Max.	Unit
Minimum OFF time for correct diagnostic (Blank time 0)	Application note NOT TESTED (ESD cap < 12 nF, Bit_blank = 0)	980	-	-	µs
Minimum OFF time for correct diagnostic (Blank time 1)	Application note NOT TESTED (ESD cap < 6 nF, Bit_blank=1)	530	-	-	µs

In configuration 2 and 3, unless the PWM enable SPI bit for OUT1-4 and DRN/SRC1-4 are set, the eight drivers are all switched off.

10 Logic BIST

After VDD power on with RES = Hi, SCK = Lo a digital logic BIST (built-in self-test) it's started and it takes max 11ms to be completed. In case of RES = Hi and SCK = Hi the BIST will be not executed. The BIST status register (0x1E) contains three bits to reflect the status of BIST.

The purpose of logic BIST is to test the control and diagnosis logic. If the BIST ends with an error, the device is no longer reliable.

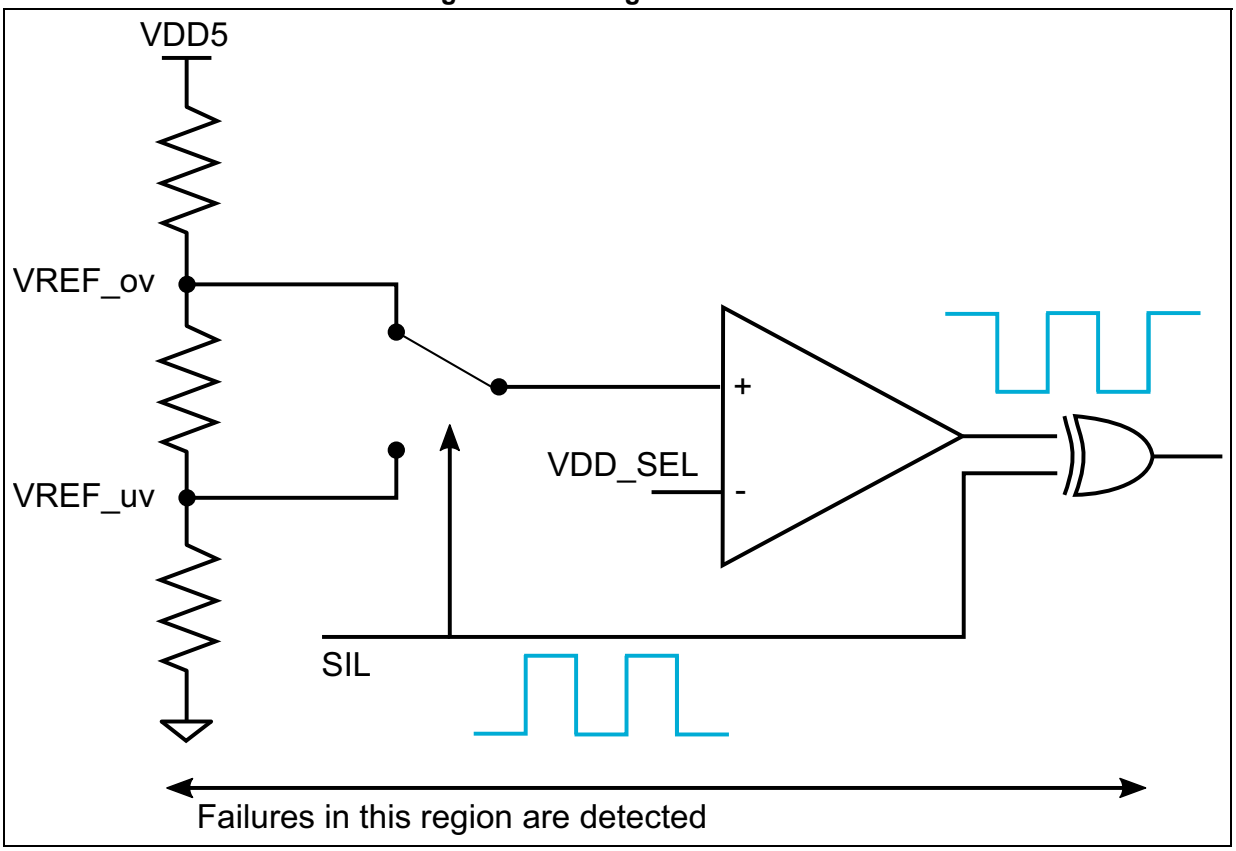
While the BIST is running, the device is not operative.

The oscillator FLL (Spread Spectrum) is enabled after BIST run (clkch_en bit).

11 Analog BIST

Over current, over/under voltage, open load circuitry is checked through analog BIST self-test implementation controlled by SPI command (CR14 dr_s_chk). The check can be implemented by microcontroller after POR by SPI command or also at run-time depending on the application requirement.

Figure 12. Analog BIST self-test



12 Clock monitor

For safety reasons the device has two clock signals: main clock and diagnosis clock.

The diagnosis clock is a redundant oscillator which has been introduced with the aim to perform a frequency check with the main clock. A dedicated digital block is present to accomplish this task.

If a clock signal is running out of range, a status bit is set (clkbad). In case the main clock stops working, a digital internal reset is asserted, until POR or RES clears it.

If the main clock is running 25% faster or slower than diagnosis clock, the bit clkbad is set.

If the main clock is running 85% slower than diagnosis clock, a digital internal reset is asserted, the device is put to reset state, all drivers are off and no response to any input signal is given, until power off or RES pin assert (RES pin set to '0') to clear it.

5 V ≤ VB < 18 V; -40 °C ≤ T_j ≤ 175 °C unless otherwise specified.

Table 27. Clock monitor

Parameter	Test condition	Min.	Typ.	Max.	Unit
Main clock frequency	FLL not active	4.5	5	5.5	MHz

13 SPI

The SPI interface is used to configure the device, control the output and read the diagnostic and output status registers.

Every time a bit in one of the SPI registers is set by the L9301 (for example when an error is detected) it will not be reset until the corresponding registers have been wrote to 0 by SPI. The bit will not be reset if an SPI error occurs during access to register by the µC or while L9301 sends the content of the register as an answer.

13.1 CS, SCK, MOSI

5 V ≤ VB < 18 V; -40 °C ≤ T_j ≤ 175 °C unless otherwise specified.

Table 28. CS, SCK, MOSI

Pin	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
CS, SCK, MOSI	V_IH	Logic input high voltage	-	1.75	-	VDD+0.3	V
	V_IL	Logic input low voltage	-	-0.3	-	0.75	V
	V_Ihys	Logic input hysteresis	-	100	-	1000	mV
	Iin	Input current	-	-	-	5	µA
	Ri_pu	Pull up resistor	Tested at 1.5 V, R = (3.3-1.5)/$I_{measure}$	50	-	250	kΩ

13.2 MISO

Back supply current into supply pin of MISO is not allowed.

Back to Back structure: in case of an over-voltage condition at the MISO output, the HS path (Back to Back) is switched off after tOFF_PROT by analog circuitry to avoid back supply current into supply pin of SDO.

5 V ≤ VB < 18 V; -40 °C ≤ T_j ≤ 175 °C unless otherwise specified.

Table 29. MISO

Pin	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
MISO	V_OH	Logic output high voltage	I_{sink} = 2 mA	VDD_I/O-0.4	-	-	V
	V_OL	Logic output low voltage	I_{source} = 2 mA		-	0.4	V
	VOV_MISO	Over voltage detection threshold at MISO output	-	VDDIO+0.05	-	VDDIO+0.2	V
	tOFF_PROT	Turn OFF delay for over voltage reverse supply protection	-	0	-	1.5	µs

13.3 SPI frame

MOSI

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
W/R	ADD							RES	DATA[19..13]						
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA[12..0]													CRC[2..0]		

W/R 1 = Write

0 = Read

ADD Address

RES Reserved

DATA Data

CRC CRC: Polynomial is x^3+x^2+x+1

MISO

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SPIErr[2..0]			CHExcp[5..0]						DATA[19..13]						
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA[12..0]													CRC[2..0]		

SPIErr[2] SPI Short Frame: a less-than-32bit SPI frame was received

SPIErr[1] SPI Long Frame: a more-than-32bit SPI frame was received

SPIErr[0] SPI CRC Error: SPI CRC checksum error

CHExcp[5] gf: bit 6 of General device diagnostic register

CHExcp[4] got: bit 4 of General device diagnostic register

CHExcp[3] vdduv: bit 3 of General device diagnostic register

CHExcp[2] vddov: bit 2 of General device diagnostic register

CHExcp[1] vbuv: bit 1 of General device diagnostic register

CHExcp[0] vbov: bit 0 of General device diagnostic register

DATA Data

CRC CRC: Polynomial is x^3+x^2+x+1

13.4 SPI registers

CR0(0x00) Device general configuration register

19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								conf4_lshs				dloss_conf	cpl_conf	vdduv_conf	vddov_conf	vbuv_conf	vbov_conf	output_conf[1:0]	
0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	

[19:12] RESERVED: Reserved

[11] conf4_lshs[3]
0 = HS is configured as high side driver during configuration4
1 = HS is configured as low side driver during configuration4

[10] conf4_lshs[2]
0 = HS is configured as high side driver during configuration4
1 = HS is configured as low side driver during configuration4

[9] conf4_lshs[1]
0 = HS is configured as high side driver during configuration4
1 = HS is configured as low side driver during configuration4

[8] conf4_lshs[0]
0 = HS is configured as high side driver during configuration4
1 = HS is configured as low side driver during configuration4

[7] dloss_conf
0 = no auto shut driver when freewheeling diode loss
1 = auto shut driver when freewheeling diode loss

[6] cpl_conf
0 = no auto shut driver when charge pump low
1 = auto shut driver when charge pump low

[5] vdduv_conf
0 = no auto shut driver when vdduv
1 = auto shut driver when vdduv

[4] vddov_conf
0 = no auto shut driver when vddov
1 = auto shut driver when vddov

[3] vbuv_conf
0 = no auto shut driver when vbuv
1 = auto shut driver when vbuv

[2] vbov_conf
0 = no auto shut driver when vbov
1 = auto shut driver when vbov

[1:0] output_conf (1)

output_conf[1]	output_conf[0]	Configuration
0	0	1
0	1	2
1	0	3
1	1	4

1. Output_conf bits can only be modified when EN pin is logic 0

CR1-CR12 (0x01-0x0C) Device configuration register

19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												pwm_en	dis_diagoff	dis_source	dloss_act	diagoff_blank_sel	oc_restart	oc_thres	slew_rate
0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)

[19:8] RESERVED: Reserved

[7] pwm_en
0 = driver is disabled
1 = driver is enabled
available only in LS4-1 and HS4-1

[6] dis_diagoff
0 = enable OFF diagnosis
1 = disable OFF diagnosis

[5] dis_source
0 = enable OFF diagnosis pull up current
1 = disable OFF diagnosis pull up current

[4] dloss_act
0 = disable the dloss signal diagnosis
1 = enable the dloss signal diagnosis

[3] diagoff_blank_sel
0 = long blanking time
1 = short blanking time

[2] oc_restart
0 = restart the channel only after clearing the fault bit
1 = restart the channel without clearing the fault bit

[1] oc_thres
0 = normal over current threshold
1 = enable double over current threshold

[0] slew_rate
0 = slew rate is low
1 = slew rate is high

Note: Address 0x01 is for LS1, 0x02 is for LS2… 0x09 is for HS1, 0x0A is for HS2 and so on. pwm_en is only available in 0x01-0x04, 0x09-0x0C.

CR13 (0x0D) Driver command register

19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								cmd12	cmd11	cmd10	cmd9	cmd8	cmd7	cmd6	cmd5	cmd4	cmd3	cmd2	cmd1
0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)

[19:12] RESERVED: Reserved

[11] cmd12
Command HS4 (no effect in Config 1)

[10] cmd11
Command HS3 (no effect in Config 1)

[9] cmd10
Command HS2 (no effect in Config 1)

[8] cmd9
Command HS1 (no effect in Config 1)

[7] cmd8
Command OUT8

[6] cmd7
Command OUT7

[5] cmd6
Command OUT6

[4] cmd5
Command OUT5

[3] cmd4
Command OUT4 (in Configuration1 controls DRN/SRC3 DRN/SRC4)

[2] cmd3
Command OUT3 (in Configuration1 controls DRN/SRC1 DRN/SRC2)

[1] cmd2
Command OUT2 (in Configuration1 controls OUT3/OUT4)

[0] cmd1
Command OUT1 (in Configuration1 controls OUT1/OUT2)

CR14 (0x0E) MCU controlled comparator test and clock check register

19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																		dr_s_chk	clkch_en
0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	1 (R/W)

[19:2] RESERVED: Reserved

[1] dr_s_chk
0 = normal
1 = invert hv/lv and OC comparator input
used in MCU controlled comparator test

[0] clkch_en
0 = disable clock check block
1 = enable clock check block

SR0 (0x10) General device status register

19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											clkbad	RESERVE	gf	cpl	got	vdduv	vddov	vbuv	vbov
0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)

[19:9] RESERVED: Reserved

[8] clkbad
0 = main clock and diagnosis clock frequency deviation within 25%
1 = main clock and diagnosis clock frequency deviation over 25%

[7] RESERVE: Reserve

[6] gf
0 = no fault in all the channels
1 = logic OR combination of bit 1/2/3/4/5/6/8 of all the Driver status register

[5] cpl
0 = no charge pump low
1 = charge pump low

[4] got
0 = no over temperature
1 = logic OR combination of bit 0 of all the Driver status register

[3] vdduv
0 = no VDD under voltage
1 = VDD under voltage

[2] vddov
0 = no VDD over voltage
1 = VDD over voltage

[1] vbuv
0 = no VB under voltage
1 = VB under voltage

[0] vbov
0 = no VB over voltage
1 = VB over voltage

Note: bit4 and bit6 cannot be directly written '0'. They are only cleared when the relating bits get cleared

SR1-SR12 (0x11-0x1C) Driver status register

19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED										oc_comp_f	os	cs	ol	shvb	shgnd	dloss	oc	t_sdl	t_sd
0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)

[19:10] RESERVED: Reserved

[9] oc_comp_f
0 = no comparator self test fail
1 = over current comparator self test fail

[8] os: output status
0 = driver status is aligned to the command in on state
1 = driver output is not aligned to the command in on state

[7] cs: command status
0 = CR13 or pin IN1-8 put driver to off status
1 = CR13 or pin IN1-8 put driver to on status

[6] ol: open load
0 = no open load
1 = open load

[5] shvb: short to VB
0 = no short to VB
1 = short to VB
available only in SR9-SR12

[4] shgnd: short to GND
0 = no short to GND
1 = short to GND

[3] dloss: diode loss
0 = no diode loss
1 = diode loss

[2] oc: over current
0 = no over current
1 = over current

[1] t_sdl
0 = no over temperature
1 = over temperature

[0] t_sd
0 = no over temperature occurring
1 = over temperature occurring (live bit)

Note: address 0x11 is for LS1, 0x12 is for LS2… 0x19 is for HS1, 0x1A is for HS2 and so on.

SR13 (0x1D) IC version register

19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVE														silicon version					
0 (R)	0 (R)	0 (R)	0 (R)	0 (R)	0 (R)	0 (R)	0 (R)	0 (R)	0 (R)	0 (R)	0 (R)	0 (R)	0 (R)	0 (R)	0 (R)	0 (R)	0 (R)	0 (R)	0 (R)

[19:6] RESERVE: Reserve

[5:0] silicon version: silicon version (AB=100010)

SR14 (0x1E) Bist status register

19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVE																	lbist run	lbist end	lbist pass
0 (R)	0 (R)	0 (R)	0 (R)	0 (R)	0 (R)	0 (R)	0 (R)	0 (R)	0 (R)	0 (R)	0 (R)	0 (R)	0 (R)	0 (R)	0 (R)	0 (R)	0 (R)	0 (R)	0 (R)

[19:3] RESERVE: Reserve

[2] lbist run
0 = bist is not currently running
1 = bist is currently running

[1] lbist end
0 = bist unfinished yet
1 = bist finished

[0] lbist pass
0 = bist is not finished yet or finished with error
1 = bist finished without error

13.5 SPI timings

Figure 13. SPI timing diagram

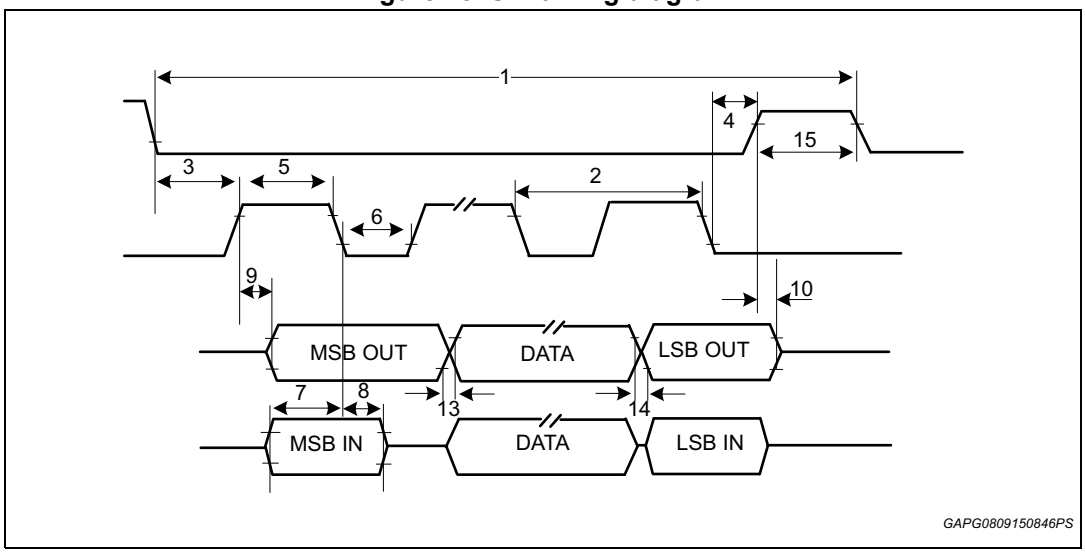


Table 30. SPI timing characteristics

No	Symbol	Parameter	Conditions	Min	Max	Units
1	f_{op}	Transfer frequency	Design Information	-	6	MHz
2	t_{sclk}	SCLK period	Design Information	167	-	ns
3	t_{lead}	Enable lead time	Design Information	750	-	ns
4	t_{lag}	Enable lag time	Design Information	100	-	ns
5	t_{sclkhs}	SCLK high time	Design Information	75	-	ns
6	t_{sclkls}	SCLK low time	Design Information	75	-	ns
7	t_{sus}	MOSI input setup time	Design Information	30	-	ns
8	t_{hs}	MOSI input hold time	Design Information	30	-	ns
9	t_{a}	MISO access time	50 pF load	-	100	ns
10	t_{dis}	MISO disable time	50 pF load	-	100	ns
11	t_{vs}	MISO output valid time	50 pF load	-	70	ns
12	t_{ho}	MISO output hold time	50 pF load	10	-	ns
13	t_{r}	MISO rise time	50 pF load	-	50	ns
14	t_{f}	MISO fall time	50 pF load	-	50	ns
15	t_{csn}	CS negated time	Design Information	750	-	ns
16	t_{sh}	SCLK $_{\text{Hold Ti}}$me	Design Information	100	-	ns

14 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK is an ST trademark.

14.1 PowerSSO-36 (exposed pad) package information

Figure 14. PowerSSO-36 (exposed pad) package outline

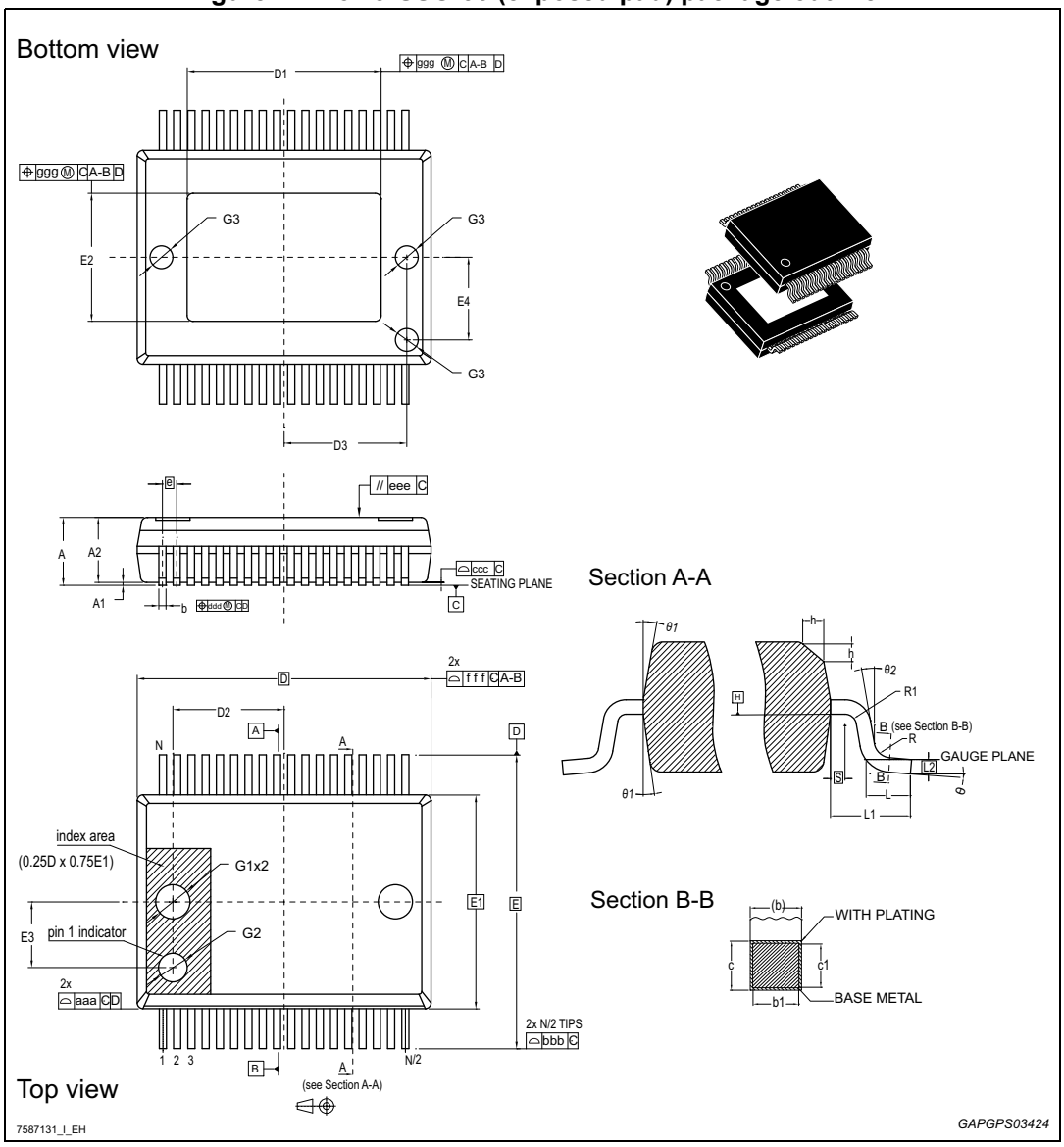


Table 31. PowerSSO-36 (exposed pad) package mechanical data

Ref	Dimensions					
	Millimeters			Inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
Θ	0°	-	8°	0°	-	8°
Θ1	5°	-	10°	5°	-	10°
Θ2	0°	-	-	0°	-	-
A	2.15	-	2.45	0.0846	-	0.0965
A1	0.0	-	0.1	0.0	-	0.0039
A2	2.15	-	2.35	0.0846	-	0.0925
b	0.18	-	0.32	0.0071	-	0.0126
b1	0.13	0.25	0.3	0.0051	0.0098	0.0118
c	0.23	-	0.32	0.0091	-	0.0126
c1	0.2	0.2	0.3	0.0079	0.0079	0.0118
D[2]	10.30 BSC			0.4055 BSC		
D1	VARIATION					
D2	-	3.65	-	-	0.1437	-
D3	-	4.3	-	-	0.1693	-
e	0.50 BSC			0.0197 BSC		
E	10.30 BSC			0.4055 BSC		
E1[2]	7.50 BSC			0.2953 BSC		
E2	VARIATION					
E3	-	2.3	-	-	0.0906	-
E4	-	2.9	-	-	0.1142	-
G1	-	1.2	-	-	0.0472	-
G2	-	1	-	-	0.0394	-
G3	-	0.8	-	-	0.0315	-
h	0.3	-	0.4	0.0118	-	0.0157
L	0.55	0.7	0.85	0.0217	-	0.0335
L1	1.40 REF			0.0551 REF		
L2	0.25 BSC			0.0098 BSC		
N	36			1.4173		
R	0.3	-	-	0.0118	-	-
R1	0.2	-	-	0.0079	-	-
S	0.25	-	-	0.0098	-	-

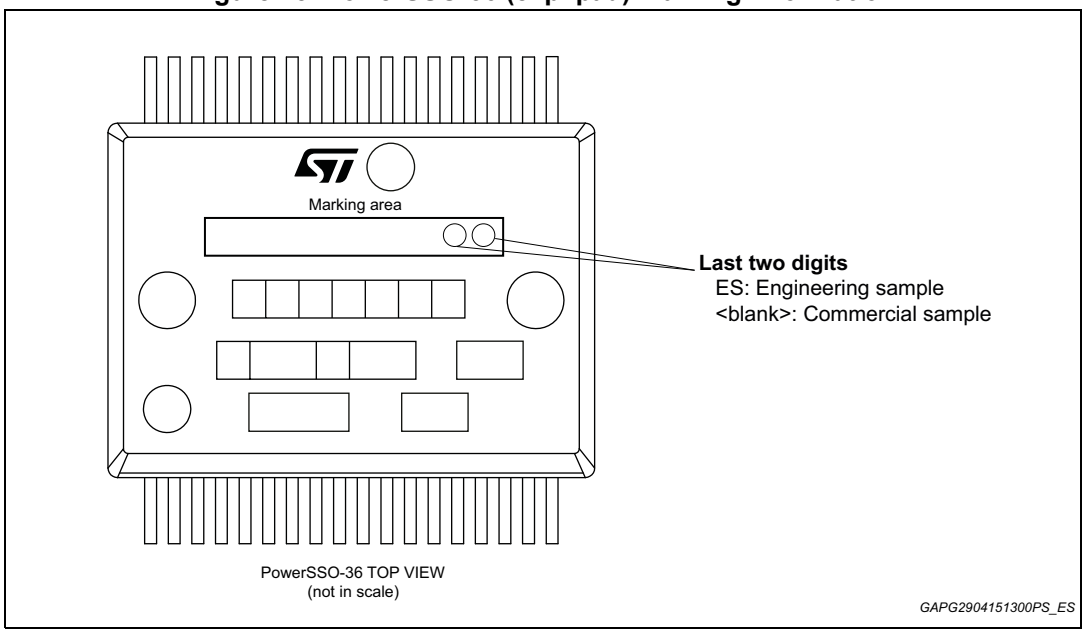
Table 31. PowerSSO-36 (exposed pad) package mechanical data (continued)

Ref	Dimensions					
	Millimeters			Inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
Tolerance of form and position						
aaa		0.2			0.0079	
bbb		0.2			0.0079	
ccc		0.1			0.0039	
ddd		0.2			0.0079	
eee		0.1			0.0039	
ffff		0.2			0.0079	
ggg		0.15			0.0059	
VARIATIONS						
Option A						
D1	6.5	-	7.1	0.2559	-	0.2795
E2	4.1	-	4.7	0.1614	-	0.1850
Option B						
D1	4.9	-	5.5	0.1929	-	0.2165
E2	4.1	-	4.7	0.1614	-	0.1850
Option C						
D1	6.9	-	7.5	0.2717	-	0.2953
E2	4.3	-	5.2	0.1693	-	0.2047

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. Dimensions D and E1 do not include mold flash or protrusions. Allowable mold flash or protrusions is ‘0.25 mm’ per side D and ‘0.15 mm’ per side E1. D and E1 are maximum plastic body size dimensions including mold mismatch.

14.2 PowerSSO-36 (exp. pad) marking information

Figure 15. PowerSSO-36 (exp. pad) marking information



Note: Engineering Samples: these samples are clearly identified by the last two digits 'ES' in the marking of each unit. These samples are intended to be used for electrical compatibility evaluation only; usage for any other purpose may be agreed only upon written authorization by ST. ST is not liable for any customer usage in production and/or in reliability qualification trials.

Commercial Samples: Fully qualified parts from ST standard production with no usage restrictions.

15 Revision history

Table 32. Document revision history

Date	Revision	Changes
30-Nov-2015	1	Initial release.
14-Dec-2015	2	Corrected: – *Section 9.3: Driver diagnostic on page 27*; – *Section 9.4: Combined diagnosis (configuration 1, 2 & 3) on page 34*; – *Section 13: SPI on page 39*; – *CR0(0x00) on page 42* ([2] and [1:0]); – *SR13 (0x1D) on page 47*.
21-Jan-2016	3	Updated *Section 9.3.4: Charge Pump (CP) on page 28*.
04-Mar-2016	4	Updated *Section 3.4: Thermal data on page 10*.
11-Apr-2016	5	Modified in cover page: Title and Features bullet. Updated *Table 8: VDD on page 11*.
18-Apr-2016	6	ST Restricted watermark removal for ST web site publication.
14-Oct-2019	7	Added: – *Chapter 11: Analog BIST*. Minor text changes.

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