NCP434, NCP435

2A Ultra-Small Controlled Load Switch with Auto-Discharge Path

The NCP434 and NCP435 are a low Ron MOSFET controlled by external logic pin, allowing optimization of battery life, and portable device autonomy.

Indeed, due to a current consumption optimization with PMOS structure, leakage currents are eliminated by isolating connected IC's on the battery when not used.

Output discharge path is also embedded to eliminate residual voltages on the output (NCP435 only).

Available in wide input voltage range from 1.0 V to 4.0 V, and a very small 0.96 x 0.96 mm WLCSP4, 0.5 mm pitch.

Features

- 1 V − 3.6 V Operating Range
- 29 mΩ P MOSFET at 3.3 V
- DC current up to 2 A
- Output Auto−discharge (NCP435)
- Active high EN pin
- WLCSP4 0.96 x 0.96 mm
- These are Pb−Free Devices

Typical Applications

- Mobile Phones
- Tablets
- Digital Cameras
- GPS
- Portable Devices

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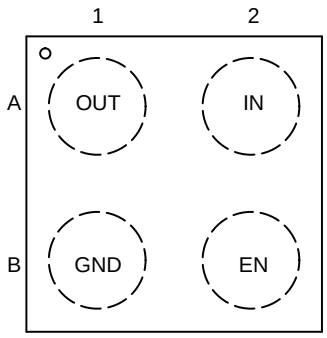
WLCSP4
CASE 567FG

MARKING DIAGRAM



XX = Specific Device Code
A = Assembly Location
Y = Year
W = Wafer Lot

PIN DIAGRAM



(Top View)

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 9 of this data sheet.

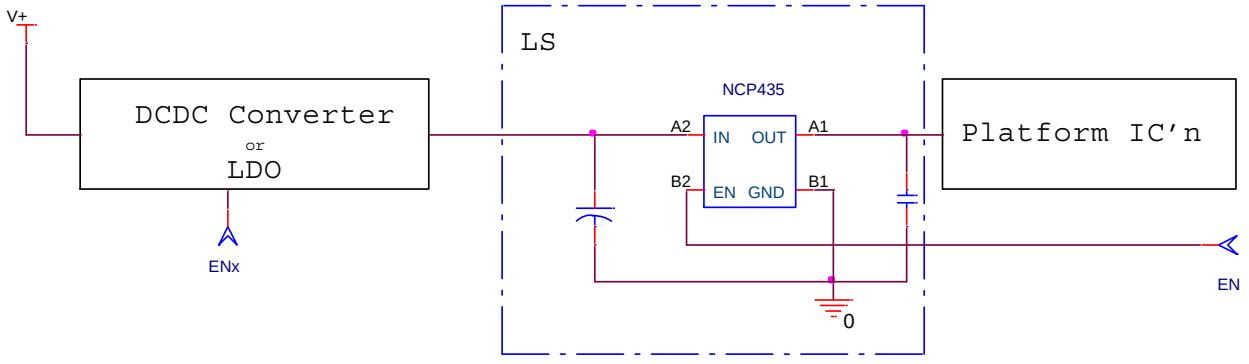


Figure 1. Typical Application Circuit

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PIN FUNCTION DESCRIPTION

Pin Name	Pin Number	Type	Description
IN	A2	POWER	Load−switch input voltage; connect a 1 μF or greater ceramic capacitor from IN to GND as close as possible to the IC.
GND	B1	POWER	Ground connection.
EN	B2	INPUT	Enable input, logic high turns on power switch.
OUT	A1	OUTPUT	Load−switch output; connect a 1 μF ceramic capacitor from OUT to GND as close as possible to the IC is recommended.

BLOCK DIAGRAM

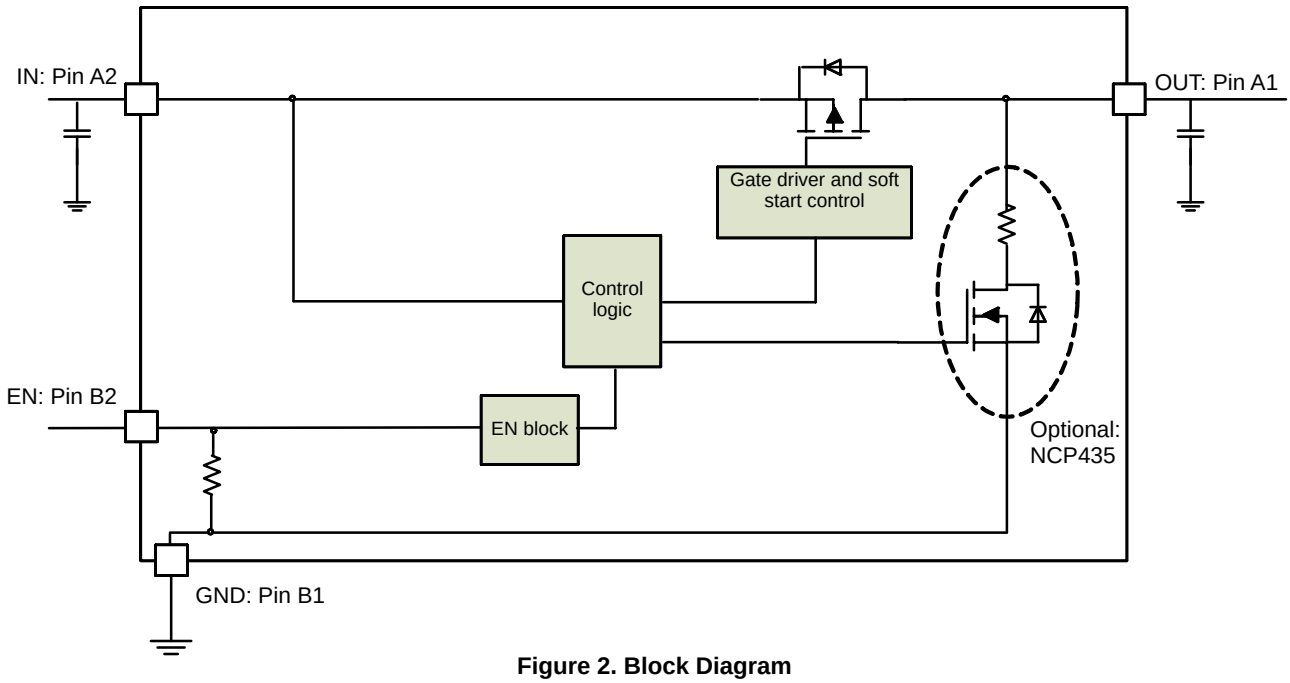


Figure 2. Block Diagram

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
IN, OUT, EN, Pins	V_{EN} , V_{IN} , V_{OUT}	−0.3 to + 4.0	V
From IN to OUT Pins: Input/Output	V_{IN} , V_{OUT}	0 to + 4.0	V
Maximum Junction Temperature	T_J	−40 to + 125	°C
Storage Temperature Range	T_{STG}	−40 to + 150	°C
Moisture Sensitivity (Note 1)	MSL	Level 1	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Moisture Sensitivity Level (MSL): 1 per IPC/JEDEC standard: J−STD−020.

OPERATING CONDITIONS

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IN}	Operational Power Supply			1.0		3.6	V
V_{EN}	Enable Voltage			0		3.6	
T_A	Ambient Temperature Range			−40	25	+85	°C
C_{IN}	Decoupling input capacitor			1			μF
C_{OUT}	Decoupling output capacitor			1			μF
$R_{\theta JA}$	Thermal Resistance Junction−to−Air	WLCSP package (Note 6)			100		°C/W
I_{OUT}	Maximum DC current					2	A
P_D	Power Dissipation Rating (Note 7)	$T_A \le 25°C$	WLCSP package		0.5		W
		$T_A = 85°C$	WLCSP package		0.2		W

2. According to JEDEC standard JESD22−A108.
3. This device series contains ESD protection and passes the following tests:
4. Human Body Model (HBM) ±4.0 kV per JEDEC standard: JESD22−A114 for all pins.
   Machine Model (MM) ±250 V per JEDEC standard: JESD22−A115 for all pins.
   Charge Device Model (CDM) ±2.0 kV per JEDEC standard: JESD22−C101 for all pins.
5. Latch up Current Maximum Rating: ±100 mA per JEDEC standard: JESD78 class II.
6. The $R_{\theta JA}$ is dependent of the PCB heat dissipation and thermal via.
7. The maximum power dissipation ($_{PD}$) is given by the following formula:

$$P_D = \frac{T_{JMAX} - T_A}{R_{\theta JA}}$$

ELECTRICAL CHARACTERISTICS Min and Max Limits apply for T_A between −40°C to +85°C for V_{IN} between 1.0 V to 3.6 V (Unless otherwise noted). Typical values are referenced to T_A = +25°C and V_{IN} = 3.3 V (Unless otherwise noted).

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
POWER SWITCH							
$R_{DS(on)}$	Static drain−source on−state resistance	V_{IN} = 4 V	T_A = 25°C, I = 200 mA (Note 9)		27	30	mΩ
		V_{IN} = 3.3 V	T_A = 25°C, I = 200 mA		29	34	
		V_{IN} = 3.3 V	T_A = 85°C			38	
		V_{IN} = 1.8 V	T_A = 25°C, I = 200 mA		43	52	
		V_{IN} = 1.2 V	T_A = 25°C, I = 200 mA		80	120	
		V_{IN} = 1.1 V	T_A = 25°C, I = 100 mA		110		
R_{DIS}	Output discharge path	EN = low	V_{IN} = 3.3 V, NCP435 only		65	90	Ω
T_R	Output rise time	V_{IN} = 3.3 V	C_{LOAD} = 1 μF, R_{LOAD} = 25 Ω (Note 8)	35	61	90	μs
T_F	Output fall time	V_{IN} = 3.3 V	C_{LOAD} = 1 μF, R_{LOAD} = 25 Ω (Note 8)	20	42	70	μs
T_{on}	Gate turn on	V_{IN} = 3.3 V	Gate turn on + Output rise time	65	126	190	μs
T_{en}	Enable time	V_{IN} = 3.3 V	From EN low to high to V_{OUT} = 10% of fully on	30	66	100	μs
V_{IH}	High−level input voltage			0.9			V
V_{IL}	Low−level input voltage					0.5	V
R_{EN}	Pull down resistor				5.1	7	MΩ
QUIESCENT CURRENT							
I_Q	Current consumption	V_{IN} = 3.3 V, EN = low, No load			0.15	0.6	μA
		V_{IN} = 3.3 V, EN = high, No load			0.3	0.6	μA

8. Parameters are guaranteed for C_{LOAD} and R_{LOAD} connected to the OUT pin with respect to the ground
9. Guaranteed by design and characterization, not production tested.

TIMINGS

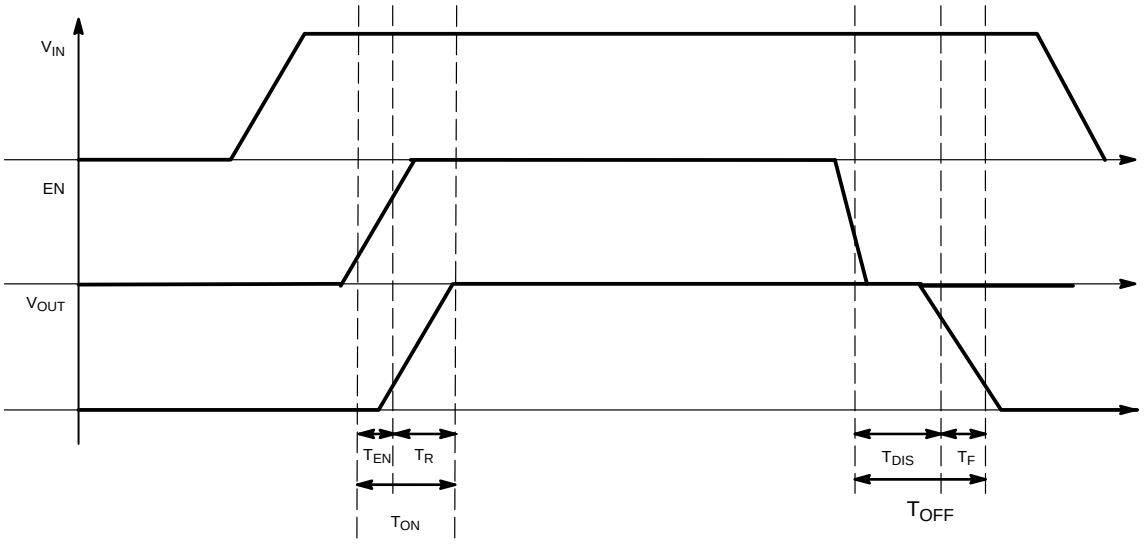


Figure 3. Enable, Rise and fall time

TYPICAL CHARACTERISTICS

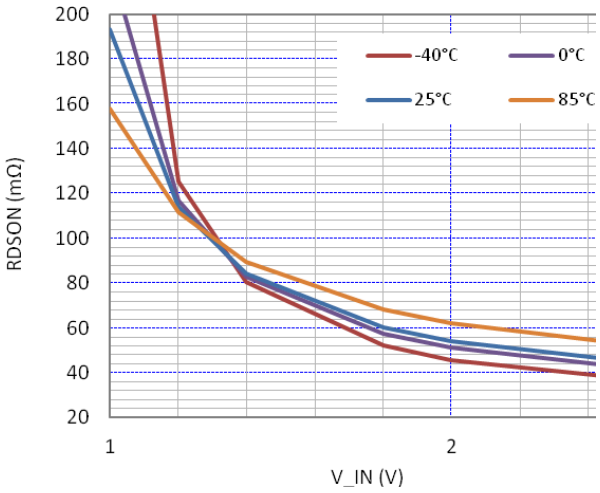


Figure 4. $R_{DS(on)}$ (mΩ) vs. V_{IN} (V) from 1 V to 2. 6 V

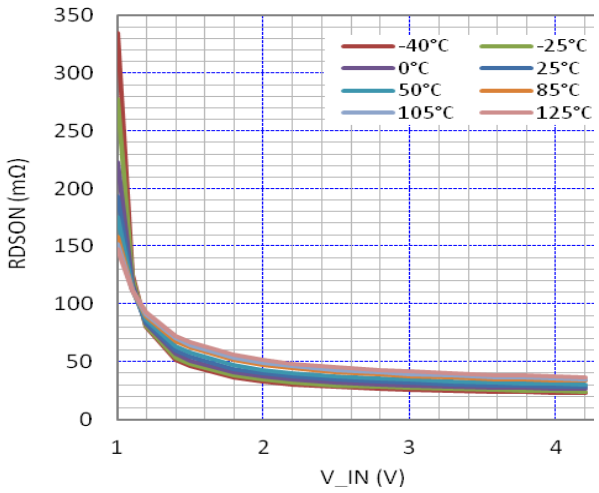


Figure 5. $R_{DS(on)}$ (mΩ) vs. V_{IN} (V) from 1 V to 4 V

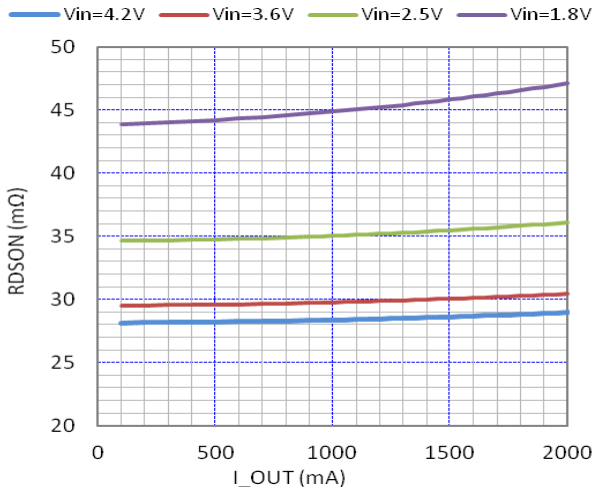


Figure 6. $R_{DS(on)}$ (mΩ) vs. I_{load} (mA)

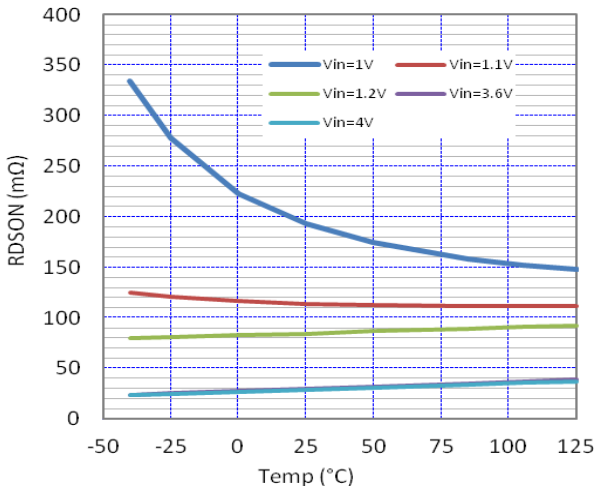


Figure 7. $R_{DS(on)}$ (mΩ) vs. Temperature (°C)

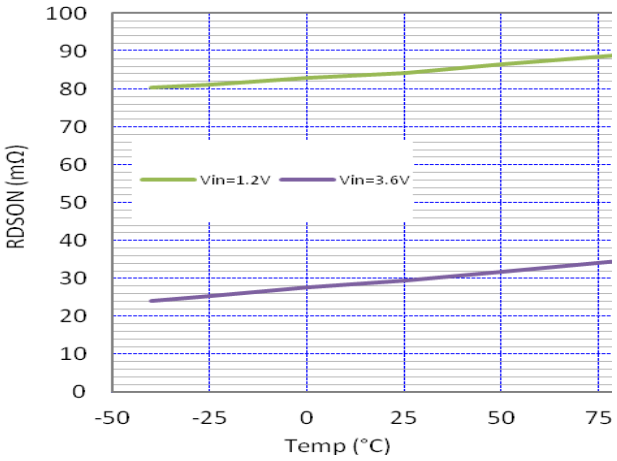


Figure 8. $R_{DS(on)}$ (mΩ) vs. Temperature (°C) at 1.2 V and 3.6 V

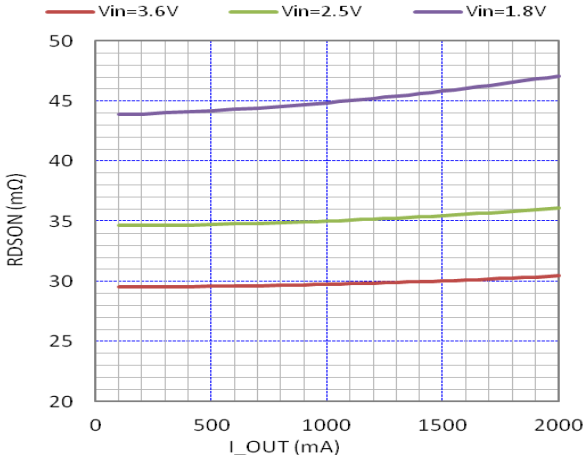


Figure 9. $R_{DS(on)}$ (mΩ) vs. Current (mA)

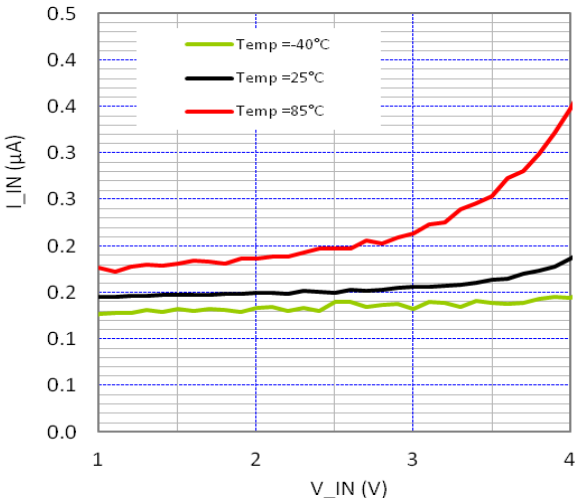


Figure 10. Standby Current (µA) versus V_{IN} (V), No Load

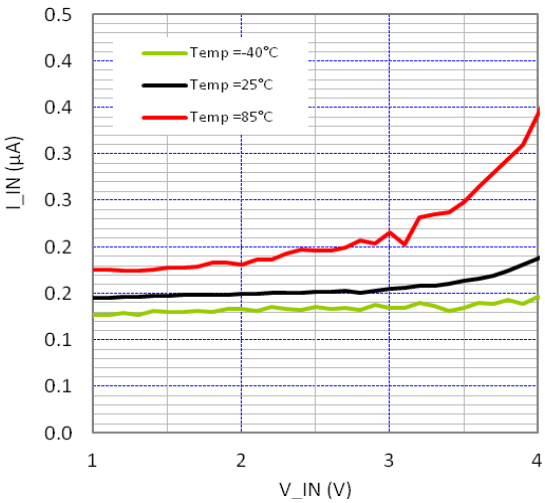


Figure 11. Standby Current (µA) versus V_{IN} (V), V_{OUT} Short to GND

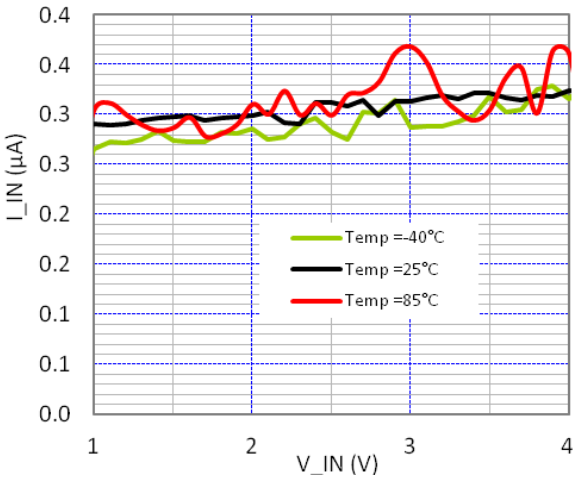


Figure 12. Quiescent Current (µA) versus V_{IN} (V), No Load

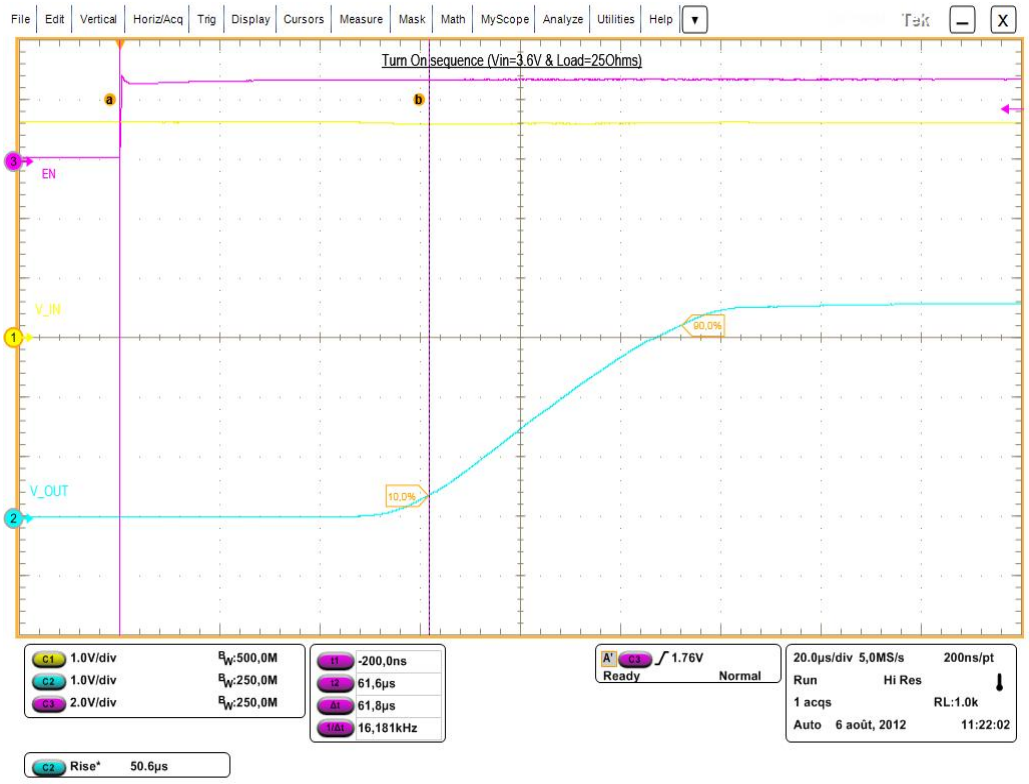


Figure 13. Enable Time, Rise Time, and Ton Time

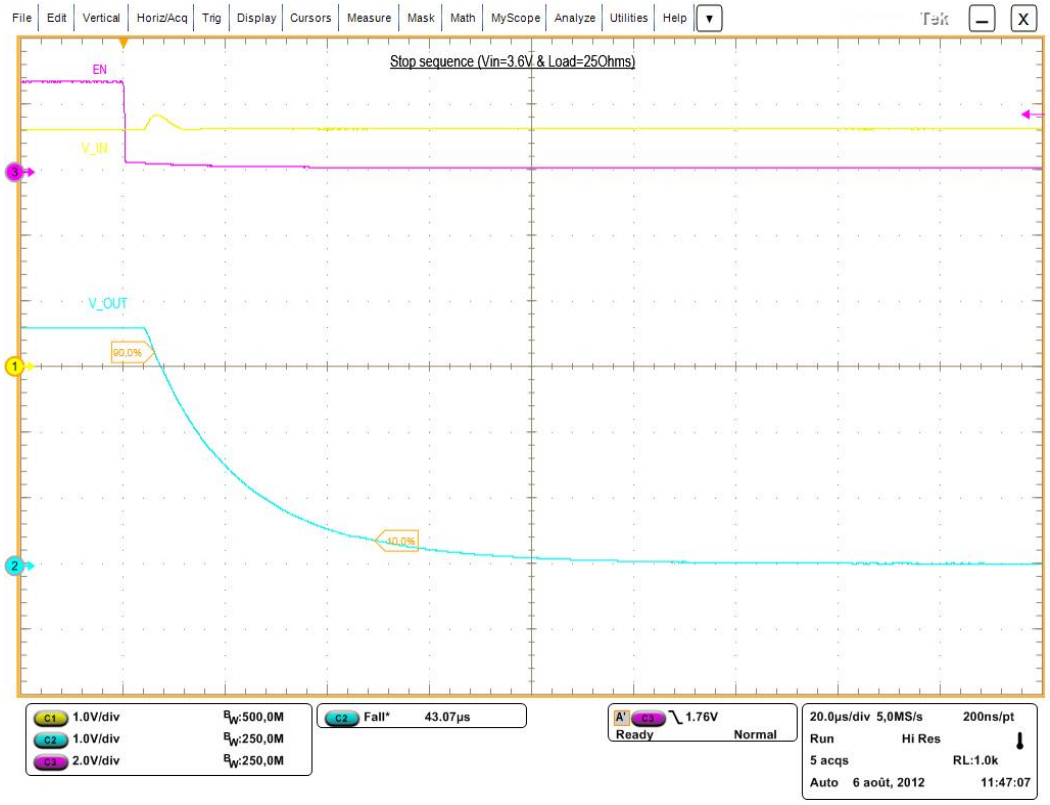


Figure 14. Disable Time, Fall Time and Toff Time

FUNCTIONAL DESCRIPTION

Overview

The NCP434 − NCP435 are high side P channel MOSFET power distribution switch designed to isolate ICs connected on the battery in order to save energy. The part can be turned on, with a range of battery from 1.0 V to 4 V.

Enable Input

Enable pin is an active high. The path is opened when EN pin is tied low (disable), forcing P MOS switch off.

The IN/OUT path is activated with a minimum of V_{IN} of 1.0 V and EN forced to high level.

Auto Discharge (NCP435 Only)

NMOS FET is placed between the output pin and GND, in order to discharge the application capacitor connected on OUT pin.

The auto−discharge is activated when EN pin is set to low level (disable state).

The discharge path (Pull down NMOS) stays activated as long as EN pin is set at low level and V_{IN} > 1.0 V.

In order to limit the current across the internal discharge NMOSFET, the typical value is set at 65 Ω.

C_{IN} and C_{OUT} Capacitors

IN and OUT, 1 μF, at least, capacitors must be placed as close as possible the part for stability improvement.

APPLICATION INFORMATION

Power Dissipation

Main contributor in term of junction temperature is the power dissipation of the power MOSFET. Assuming this, the power dissipation and the junction temperature in normal mode can be calculated with the following equations:

$$P_D = R_{DS(on)} \times \left(I_{OUT}\right)^2$$

P_D = Power dissipation (W)
$R_{DS(on)}$ = Power MOSFET on resistance (Ω)
I_{OUT} = Output current (A)

$$T_J = R_D \times R_{\theta JA} + T_A$$

T_J = Junction temperature (°C)
$R_{\theta JA}$ = Package thermal resistance (°C/W)
T_A = Ambient temperature (°C)

PCB Recommendations

The NCP434 − NCP435 integrate an up to 2 A rated PMOS FET, and the PCB design rules must be respected to properly evacuate the heat out of the silicon. By increasing PCB area, especially around IN and OUT pins, the $R_{\theta JA}$ of the package can be decreased, allowing higher power dissipation.

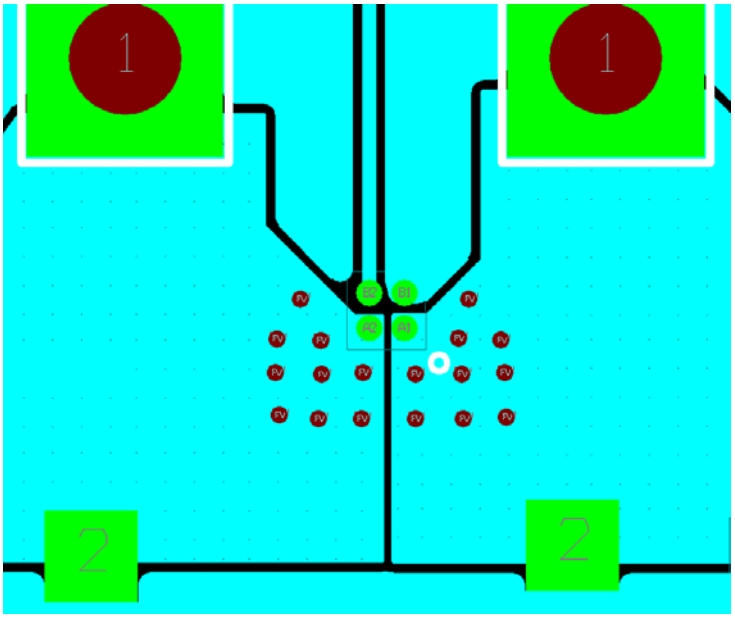


Figure 15. Routing Example 1 oz, 2 Layers, 100°C/W

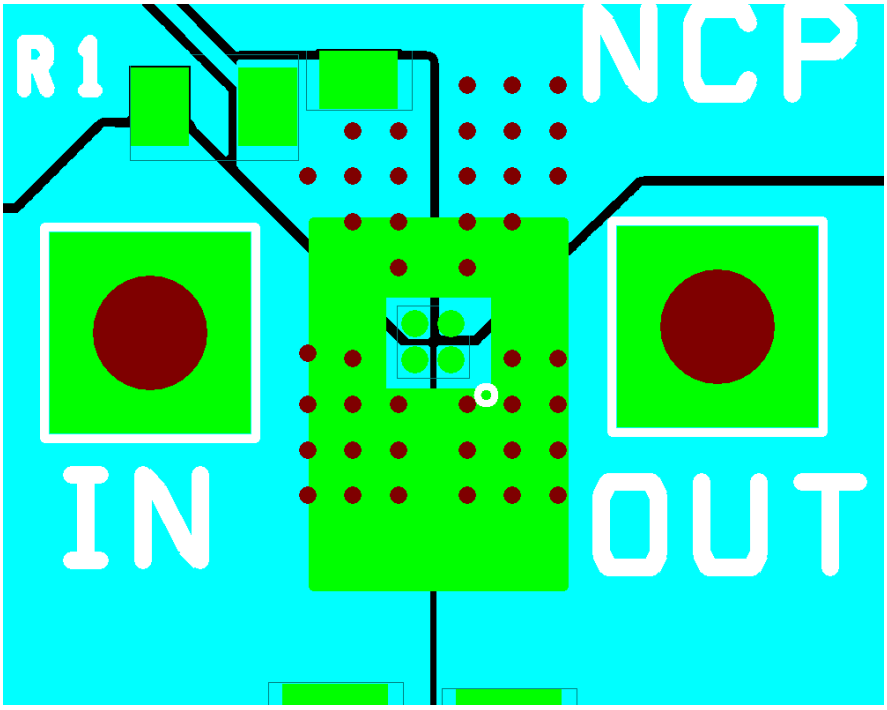


Figure 16. Routing Example 2 oz, 4 Layers, 60°C/W

Example of Application Definition

$$T_J - T_A = R_{\theta JA} \times P_D = R_{\theta JA} \times R_{DS(on)} \times I^2$$

T_J: Junction Temperature.
T_A: Ambient Temperature.
R_θ = Thermal resistance between IC and air, through PCB.
$R_{DS(on)}$: intrinsic resistance of the IC MOSFET.
I: load DC current.

Taking into account of R_θ obtain with:

- 1 oz, 2 layers: 100°C/W.

At 2 A, 25°C ambient temperature, $R_{DS(on)}$ 44 mΩ @ V_{IN} 1.8 V, the junction temperature will be:

$$T_J = R_{\theta JA} \times P_D = 25 + \left(0.044 \times 2^2\right) \times 100 = 46°C$$

Taking into account of Rt_θ obtain with:

- 2 oz, 4 layers: 60°C/W.

At 2 A, 25°C ambient temperature, $R_{DS(on)}$ 44 mΩ @ V_{IN} 1.8 V, the junction temperature will be:

$$T_J = T_A + R_\theta \times P_D = 25 + \left(0.044 \times 2^2\right) \times 60 = 35.5°C$$

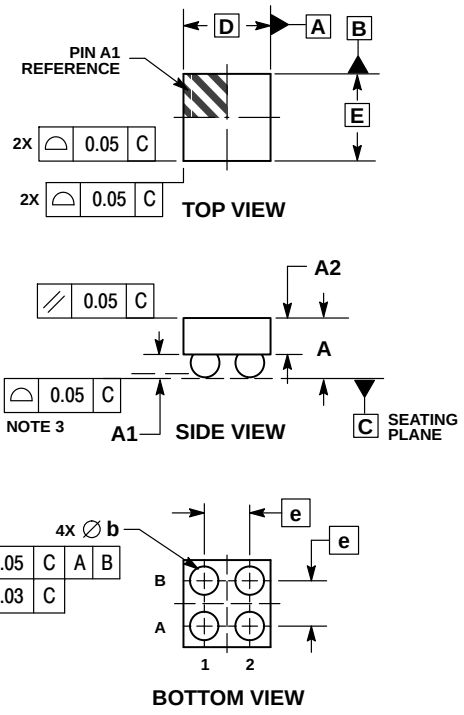
ORDERING INFORMATION

Device	Marking	Package	Shipping†
NCP434FCT2G	AJ	WLCSP 0.96 x 0.96 mm (Pb−Free)	3000 / Tape & Reel
NCP435FCT2G	AH	WLCSP 0.96 x 0.96 mm (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

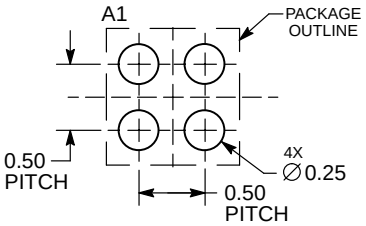
WLCSP4, 0.96x0.96
CASE 567FG
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.

DIM	MILLIMETERS MIN	MAX
A	0.54	0.63
A1	0.22	0.28
A2	0.33 REF	
b	0.29	0.34
D	0.96 BSC	
E	0.96 BSC	
e	0.50 BSC	

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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NCP435/D