

QUICK START GUIDE FOR DEMONSTRATION CIRCUIT 1231A

DUAL OUTPUT, DUAL PHASE 5A SYNCHRONOUS BUCK CONVERTER

LTC3850EGN

DESCRIPTION

Demonstration circuit 1231A is a Dual Output, Dual Phase 5A Synchronous Buck Converter featuring the LTC3850EGN. The entire circuit, including the bulk output capacitors, fit within a 1.04" X 0.94" area on all layers. The package style for the LTC3850EGN is a 28-lead narrow plastic SSOP.

The main features of the board include rail tracking, an internal 5V linear regulator for bias, RUN pins for each output and a PGOOD signal and a Mode selector that allow the converter to run in CCM, pulse skip or Burst Mode operation. Synchronization to an external clock is also possible through some minor component changes.

Two versions of the board are available. DC-1231A-A has an on-board sense resistor for current feedback, while the DC1231A-B is configured with a DCR sense circuit that allows the converter to use the inductor's DCR as the sense element instead of the on-board sense resis-

tors to save cost and board space and improves efficiency.

The input voltage range is 6.5V to 24V. For applications with narrow, $5V \pm 0.5V$, input range, the board has an optional resistor to tie the INTVCC pin to the VIN pin.

The LTC3850 datasheet gives a complete description of the part, operation and application information. The datasheet must be read in conjunction with this quick start guide for demo circuit 1231A.

Design files for this circuit board are available. Call the LTC factory.

Burst Mode is a trademark of Linear Technology Corporation

Table 1. Performance Summary ($T_A = 25^\circ\text{C}$)

PARAMETER	CONDITION	VALUE	
Minimum Input Voltage		6.5V	
Maximum Input Voltage		24V	
Output Voltage V_{OUT1}	$V_{IN} = 6.5V \text{ to } 24V, I_{OUT1} = 0A \text{ to } 5A$	$3.3V \pm 2\%$	
Output Voltage V_{OUT2}	$V_{IN} = 6.5V \text{ to } 24V, I_{OUT2} = 0A \text{ to } 5A$	$2.5V \pm 2\%$	
Typical Output Ripple V_{OUT}	$V_{IN} = 24V, I_{OUT1} = 5A \text{ (20MHz BW)}$	$<30mV_{P-P}^*$	
	$V_{IN} = 24V, I_{OUT2} = 5A \text{ (20MHz BW)}$	$<30mV_{P-P}^*$	
Output Regulation	Line	$\pm 0.05\%$	
	Load	$\pm 0.1\%$	
Nominal Switching Frequency		400kHz	
Efficiency See Figures 3 and 4 for efficiency curves		DC1231A-A	DC1231A-B
	$V_{OUT1} = 3.3V, I_{OUT1} = 5A; V_{IN} = 24V$	90.3% * Typical	91.2% * Typical
	$V_{OUT2} = 2.5V, I_{OUT1} = 5A; V_{IN} = 24V$	88.6% * Typical	89.5% * Typical

* Optional Mosfet (Si4816BDY) will result in up to 0.4% improvement in efficiency at full load

* Measured at bulk output capacitor

QUICK START PROCEDURE

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Demonstration circuit 1231A is easy to set up to evaluate the performance of the LTC3850EGN. Refer to Figure 1 for proper measurement equipment setup and follow the procedure below:

NOTE: When measuring the input or output voltage ripple, care must be taken to avoid a long ground lead on the oscilloscope probe. Measure the input or output voltage ripple by touching the probe tip directly across the Vin or Vout and GND terminals. See Figure 2 for proper scope probe technique.

1. Place jumpers in the following positions:

JP1 On
JP2 On
JP3 CCM

2. With power off, connect the input power supply to Vin and GND.

3. Turn on the power at the input.

NOTE: Make sure that the input voltage does not exceed 26V.

4. Check for the proper output voltages.

Vout1 = 3.234V to 3.366V,
Vout2 = 2.450V to 2.550V

NOTE: If there is no output, temporarily disconnect the load to make sure that the load is not set too high.

5. Once the proper output voltages are established, adjust the loads within the operating range and observe the output voltage regulation, ripple voltage, efficiency and other parameters.

6. Different operating modes can be evaluated by changing position of jumper JP3.

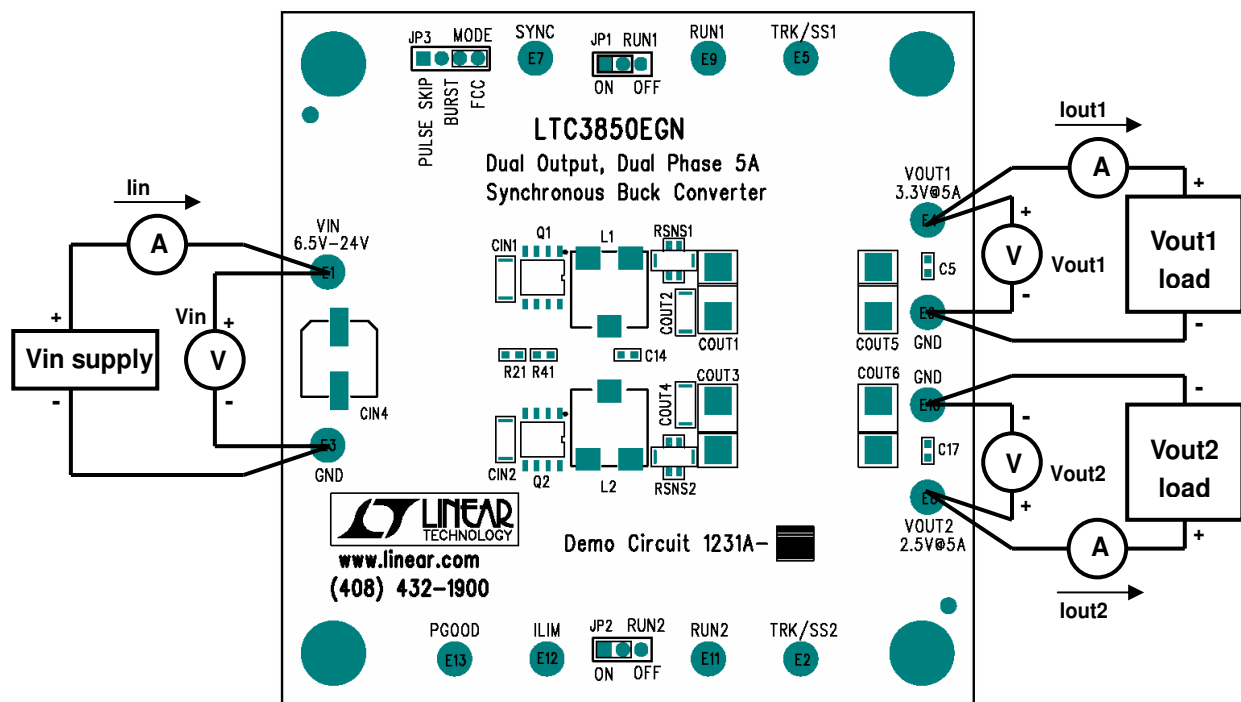


Figure 1. Proper Measurement Equipment Setup

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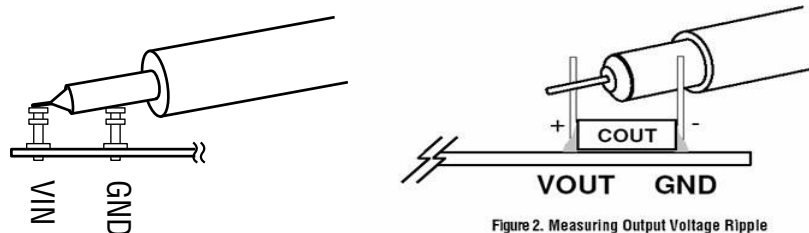


Figure 2. Measuring Input or Output Ripple Across Terminals or Directly Across Bulk Capacitor

RAIL TRACKING

Demonstration circuit 1231 is setup for coincident rail tracking where VOUT2 tracks VOUT1 and the ramp-rate for VOUT1 is determined by the value of the TRK/SS1 capacitor at C6.

This board can be modified on the bench for external rail tracking or for independent turn-on of the rails. For

the latter case, the ramp-rate for VOUT1 and VOUT2 will be determined by their respective TRK/SS capacitors. Refer to Table 2 for tracking options and to the data sheet for more details.

Table 2. Output Tracking Options

CONFIGURATION	TRACK1 DIVIDER		TRK/SS1 CAP	TRACK2 DIVIDER		TRK/SS2 CAP
	R10	R12	C	R1	R4	C
Soft Start Without Tracking						
Vout1	0Ω	open	10nF			
Vout2				open	open	10nF
Coincident Tracking:						
Vout1 tracking External Ramp	63.4kΩ	20.0kΩ	open			
Vout2 tracking Vout1				43.2kΩ	20.0kΩ	Open
Ratiometric Tracking:						
Vout2 tracking Vout1				63.4kΩ	20.0kΩ	open

FREQUENCY SYNCHRONIZATION

Demonstration circuit 1231's Mode selector allows the converter to run in CCM, pulse skip or Burst Mode operation by changing position of jumper JP3. For

synchronizing to an external clock source, however, some bench modification is needed. Refer to Table 3 and to the data sheet for more details.

Table 3. Free Running and Synchronized Operation Options

CONFIGURATION	FREQ PIN COMPONENTS			MODE SELECTOR
	R2	R3	R7	JP3
Free Running	10k Ω	0 Ω	2.49k Ω	FCC, Pulse Skip or Burst Mode
Synchronized to External Clock	open	10k Ω	0.01 μ F	Burst Mode or Open

INDUCTOR DCR SENSING AND RESISTOR SENSING

The two different versions of the board offer either an on-board sense resistor or an inductor DCR sense circuit for current feedback. The DCR sense circuit uses the resistive voltage drop across the inductor to estimate the current. In contrast to the traditional sense resistor current feedback, the DCR sensing circuit offers lower cost and higher efficiency, but results in less accurate current limit due to the large variation in the inductor resistance.

Furthermore, this indirect current sensing method cannot detect inductor saturation and requires the use of 'soft' saturating inductors (such as powder iron) resulting in increased core losses or 'hard' saturating inductors (such as ferrite) with sufficiently high current ratings resulting in increased inductor size.

The demonstration circuit 1231A-B is intended to demonstrate the feasibility of a high performance, high efficiency synchronous buck converter using a 'hard' saturating ferrite inductor with DCR sensing.

The typical efficiency versus load current for each of the outputs is given in Figure 3 and Figure 4 respectively. The efficiency is measured at both the minimum and maximum input voltage. The typical efficiency curves for both the sense resistor (A-A) and DCR sensing (A-B) boards are shown. An efficiency improvement of up to 1% is possible for the DCR sensing version.

If further improvement in efficiency is required, the switching devices can be replaced by the optional mosfets Q3 and Q4.

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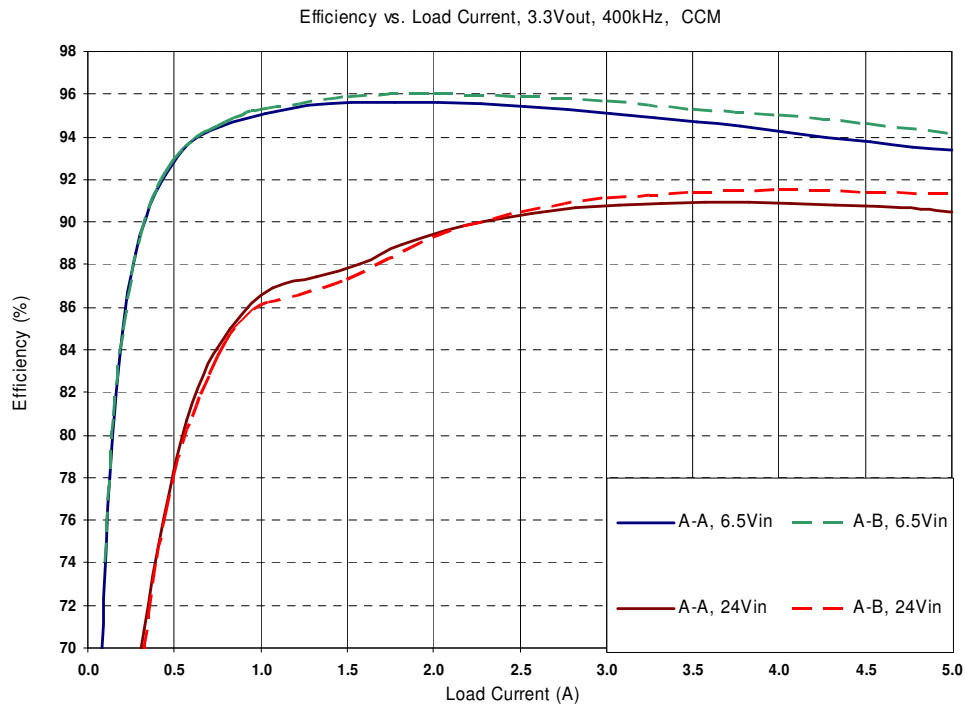


Figure 3. Typical Efficiency vs. Load Current for A-A and A-B boards – 3.3Vout

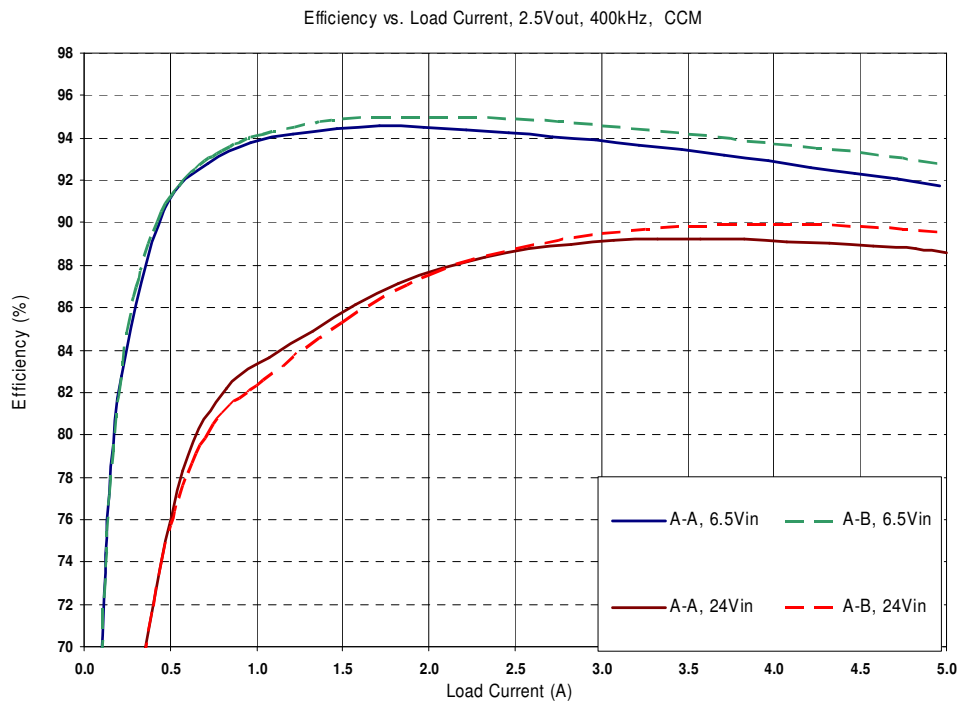


Figure 4. Typical Efficiency vs. Load Current for A-A and A-B boards – 2.5Vout

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