MP4050

Non-Isolated, High Brightness, LED Driver

The Future of Analog IC Technology

DESCRIPTION

The MP4050 is a constant current LED driver integrated with an internal 500V MOSFET. It is specifically designed for energy efficient and low cost LED bulk replacement applications.

MP4050 is designed to drive high-brightness LEDs from an $85V_{AC}$ to $265V_{AC}$ line. It is also useable under DC input voltage. The accurate output LED current is achieved by an averaging internal current feedback loop. Constant LED current is delivered quietly by switching the internal MOSFET at a frequency regulated above 22kHz.

MP4050 can be directly powered by the high input voltage. An internal high voltage current source regulates supply voltage without external circuitry. MP4050 features various protections like Thermal Shutdown (TSD), VCC Under Voltage Lockout (UVLO), Open Lamp Protection and Short Lamp Protection. All of there features make MP4050 an ideal solution for simple, off-line and non-isolated LED applications.

MP4050 is available in the TSOT23-5 and SOIC8 packages.

FEATURES

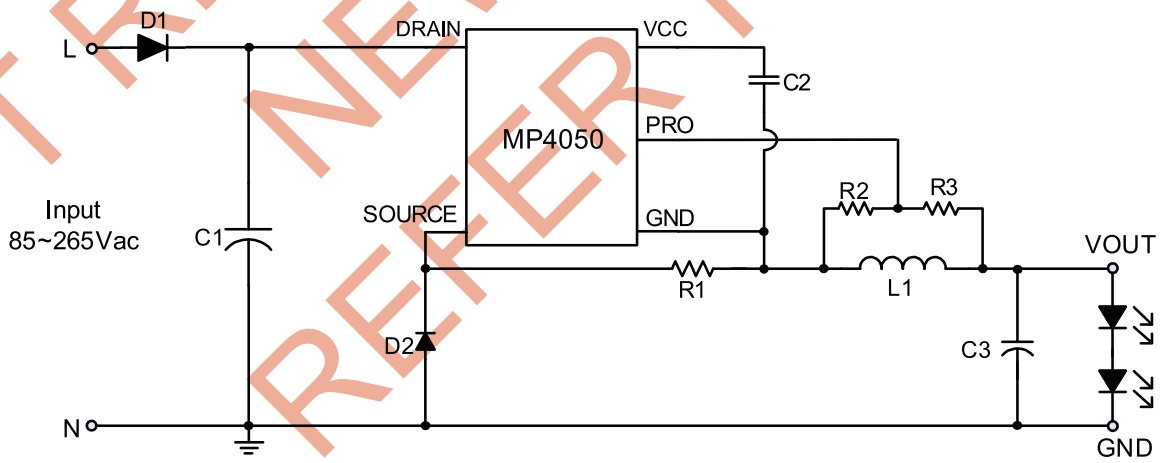
- Constant Current LED Driver
- 500V/7.2Ω MOSFET integrated
- Low Vcc Operating Current
- Maximum frequency limit
- Audible noise restrain
- Internal High Voltage Current Source
- Internal 200ns Leading Edge Blanking
- Thermal Shutdown (auto restart with Hysteresis)
- VCC Under Voltage Lockout with Hysteresis (UVLO)
- Open Lamp Protection
- Short Lamp Protection

APPLICATIONS

- AC/DC or DC/DC LED driver application
- General Illumination
- Industrial Lighting
- Automotive/Decorative LED Lighting

All MPS parts are lead-free, halogen free, and adhere to the RoHS directive. For MPS green status, please visit MPS website under Quality Assurance.
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TYPICAL APPLICATION



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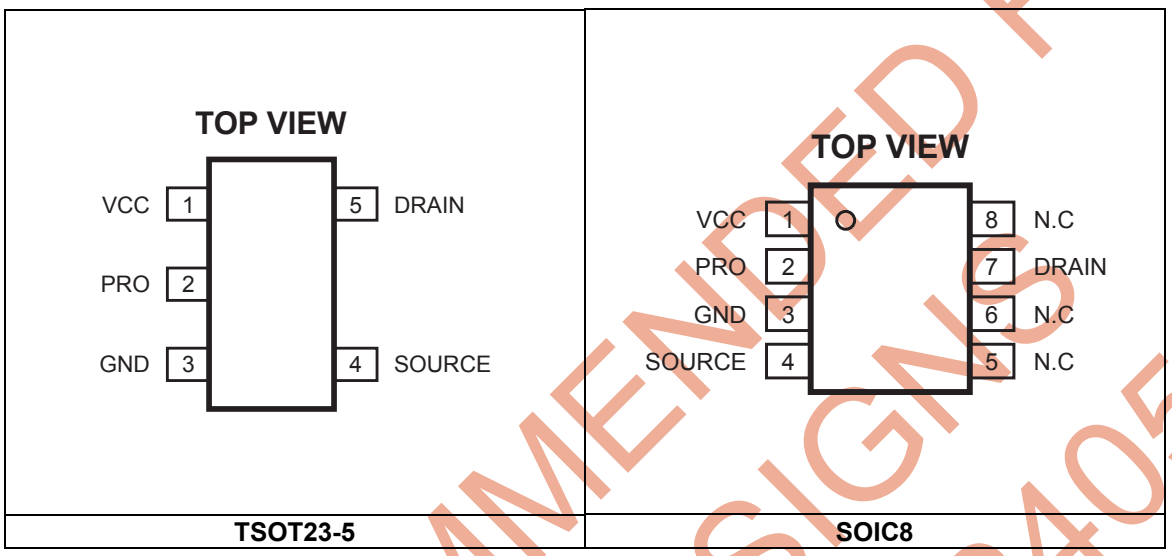
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ORDERING INFORMATION

Part Number	Package	Top Marking
MP4050GJ*	TSOT23-5	AGN
MP4050GS**	SOIC8	MP4050

*For Tape & Reel, add suffix –Z (e.g. MP4050GJ–Z);
** For Tape & Reel, add suffix –Z (e.g. MP4050GS–Z);

PACKAGE REFERENCE



TSOT23-5 | SOIC8

ABSOLUTE MAXIMUM RATINGS (1)

Drain to SOURCE ..... -0.3V to 500V
VCC, SOURCE to GND… ……..-0.3V to 6.5V
PRO to GND ..... -0.7V to 6.5V
Source Current on PRO 4mA
Continuous Power Dissipation (T_A = +25°C) (2)
--TSOT23-5, T_A=25°C 1W
--SOIC8, T_A=25°C 1W
Junction Temperature ..... 150°C
Lead Temperature ..... 260°C
Storage Temperature ..... -60°C to +150°C
ESD Capability Human Body Mode 2.0kV
ESD Capability Machine Mode 200V

Recommended Operating Conditions (3)

Operating Junction Temp. (T_J)..-40°C to +125°C
Operating VCC range ..... 4.5V to 4.7V

Thermal Resistance (4)

	θ_{JA}	θ_{JC}	
TSOT23-5	100	55	°C/W
SOIC8	96	45	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

V_{CC} = 4.7V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Start-up Current Source (Drain Pin)						
Internal regulator supply current	$I_{Regulator}$	V_{CC}=4.5V;V_{Drain}=100V	4.5	5	6	mA
Leakage Current from Pin Drain	I_{Leak}	V_{CC}=6V;V_{darin}=400V		14	20	μA
Supply Voltage Management (VCC Pin)						
VCC Increasing Level at which the internal regulator stops	VCC_{OFF}		4.45	4.65	4.85	V
VCC Decreasing Level at which the internal regulator Turns-On	VCC_{ON}		4.2	4.4	4.6	V
VCC Hysteresis between regulator ON/OFF	VCC_{OFF-ON}		0.18	0.24	0.3	V
VCC Decreasing level at which the IC stops working	VCC_{STOP}		3.17	3.27	3.37	V
VCC Hysteresis between regulator OFF to VCC stop	$VCC_{OFF-STOP}$		1.23	1.38	1.52	V
VCC Decreasing Level at which the protection Phase Ends	VCC_{PRO}		2.10	2.35	2.60	V
Internal IC Consumption	I_{CC}	V_{CC}=4.3V, Fs=33kHz, D=84%		350	400	uA
Internal IC Consumption, Latch off Phase	$I_{CCLATCH}$	V_{CC}=5V		18	21	μA
Internal MOSFET (Drain Pin)						
Break Down Voltage	V_{BRDSS}		500			V
On-State resistance	R_{ON}	I_D=10mA, Tj=25℃		7.2	10	Ω
Current Sampling Management (Source Pin)						
Peak Current Limit	V_{Limit}		0.42	0.45	0.49	V
Leading edge blanking	T_{LEB}			200		ns
Feedback Threshold to turn on the primary MOSFET	V_{FB}		0.188	0.194	0.200	V
Minimum OFF time limitation	T_{OFF_MIN}		3.5	4.7	5.9	μs
Maximum ON time limitation	T_{ON_MAX}		18	25	33	μs

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{CC} = 4.7V, T_A = 25°C, unless otherwise noted.

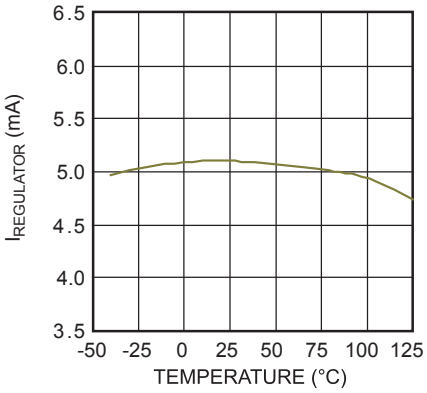
Parameter	Symbol	Condition	Min	Typ	Max	Units
Protection input (PRO Pin)						
Threshold to trigger the OVP	V_{OVP}		1.9	2.0	2.1	V
Time Constraint on the OVP Comparator	T_{OVP}			21	28	µs
Threshold to trigger the UVP	V_{UVP}		0.35	0.39	0.43	V
Thermal Shutdown						
Thermal shutdown threshold				150		ºC
Thermal shutdown recovery hysteresis				60		ºC

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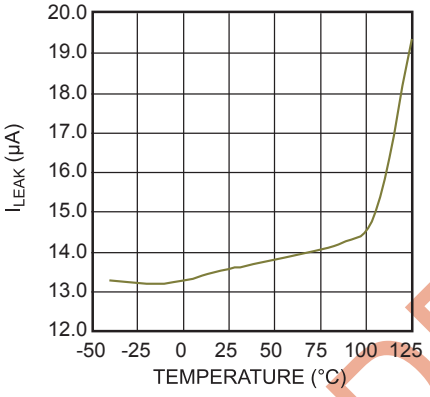
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TYPICAL CHARACTERISTICS

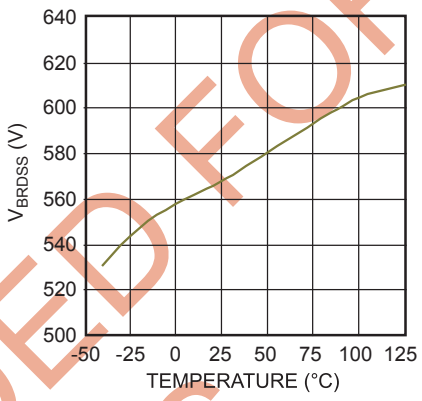
Internal Regulation Currentt vs. Junction Temperature



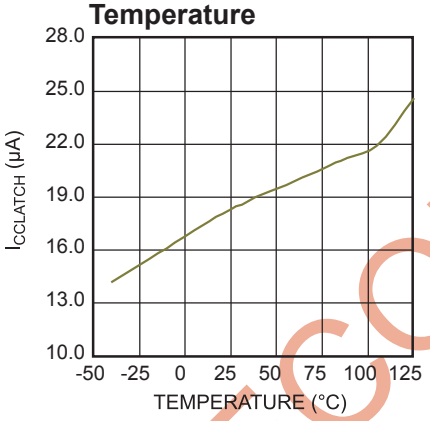
Leakage Current vs. Junction Temperature



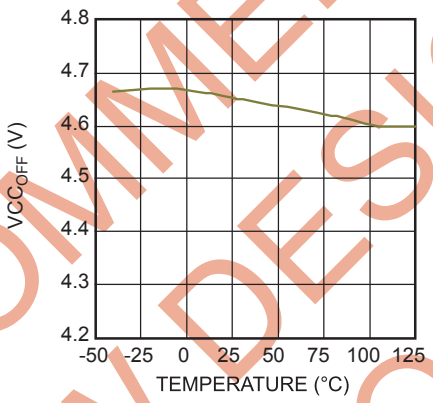
Break Down Voltage vs. Junction Temperature



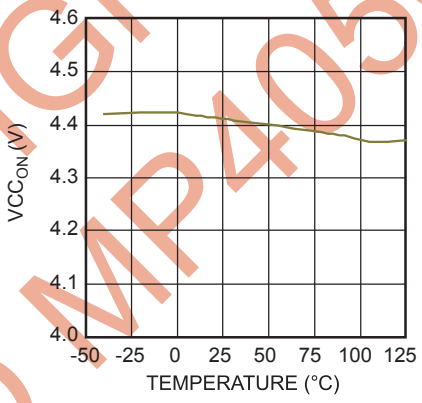
VCC Current In Latch Phase vs. Junction Temperature



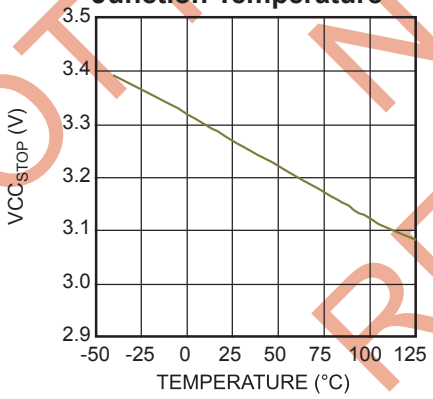
VCC OFF Threshold vs. Junction Temperature



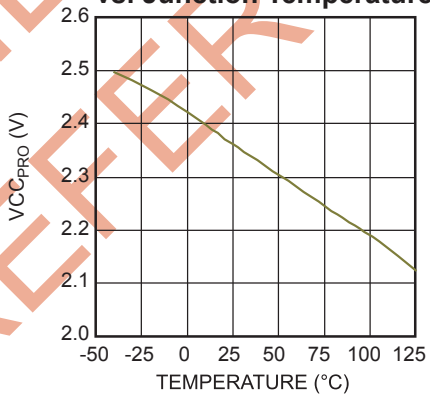
VCC ON Threshold vs. Junction Temperature



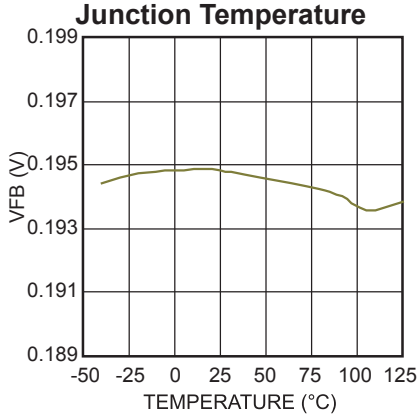
VCC Stop Threshold vs. Junction Temperature



VCC Protection Threshold vs. Junction Temperature



Feedback Reference vs. Junction Temperature

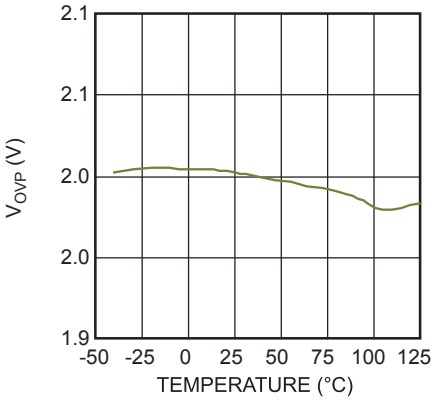


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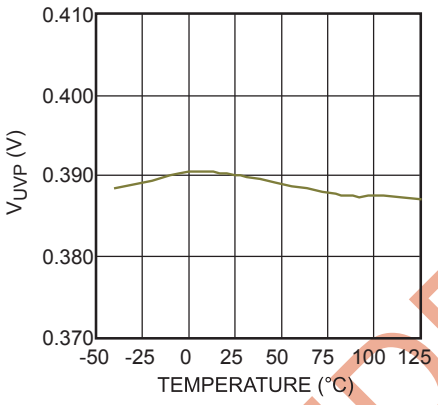
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TYPICAL CHARACTERISTICS *(continued)*

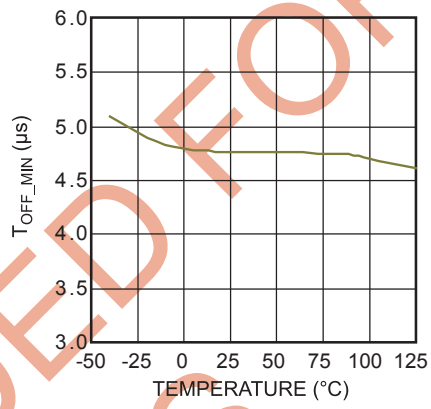
Over Voltage Protection Reference vs. Junction Temperature



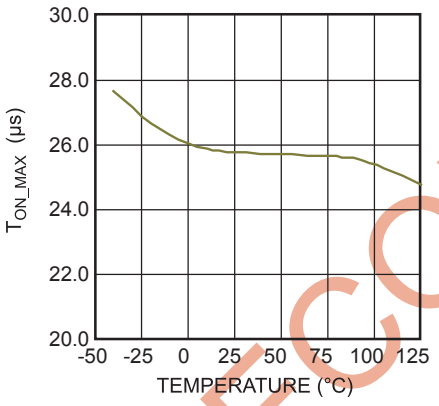
Under Voltage Protection Reference vs. Junction Temperature



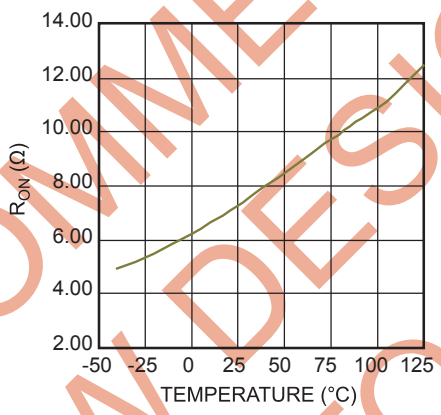
Minimum OFF Time vs. Junction Temperature



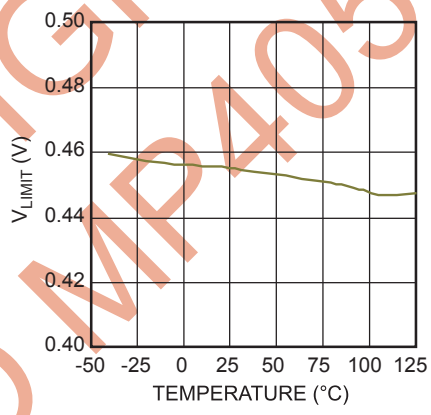
Minimum ON Time vs. Junction Temperature



On-State Resistance vs. Junction Temperature



Peak Current Limit vs. Junction Temperature



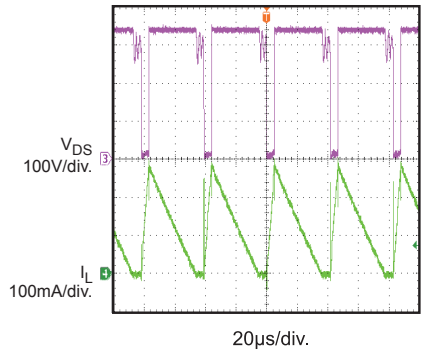
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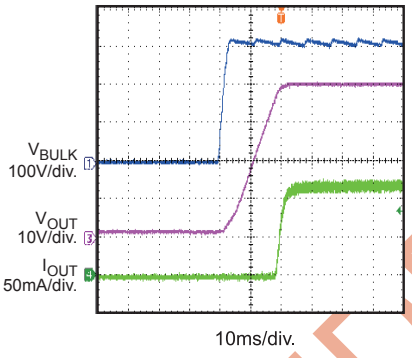
TYPICAL PERFORMANCE CHARACTERISTICS

Performance waveforms are tested on the evaluation board of the Design Example section.
V_{IN} = 230Vac, V_{OUT} = 40V, I_{OUT}=115mA, L = 4.7mH, C_{OUT}=47uF, T_A = 25°C, unless otherwise noted.

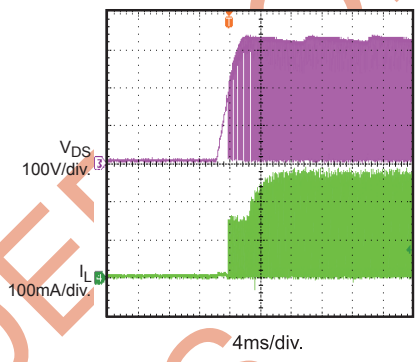
Steady State



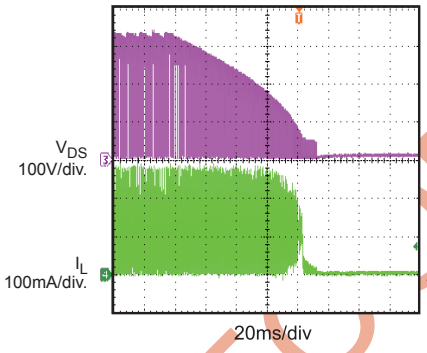
Turn On Delay



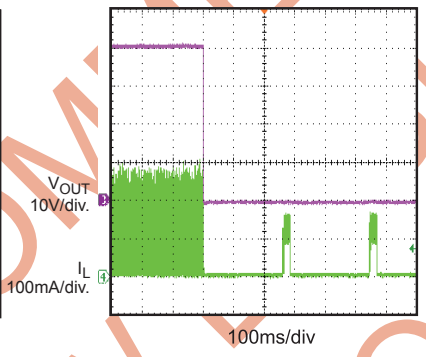
Input Power Startup



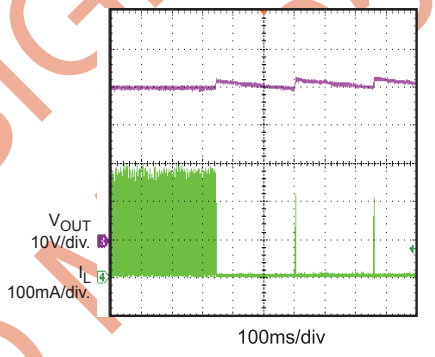
Input Power Shutdown



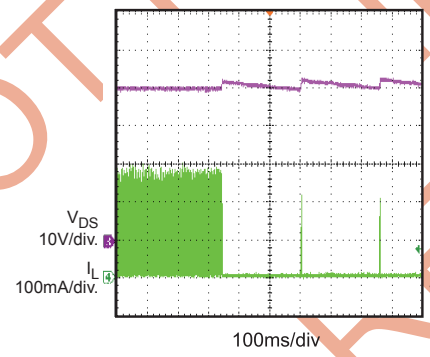
SCP Entry



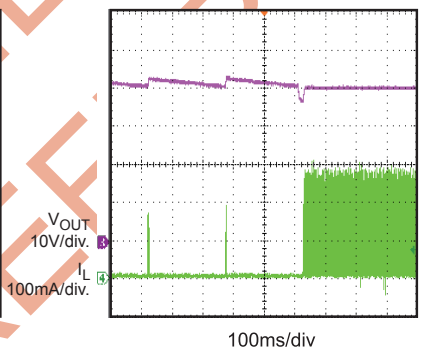
SCP Recovery



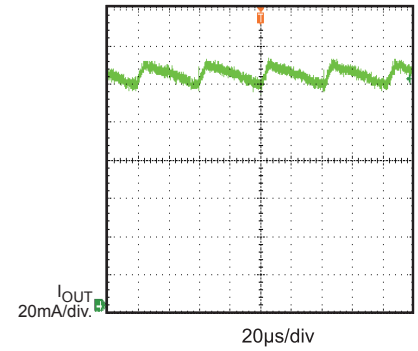
OVP Entry



OVP Recovery



Output Current Ripple



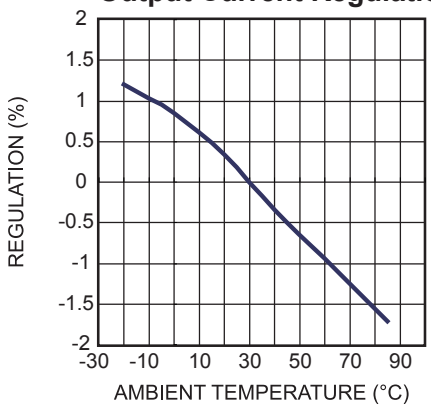
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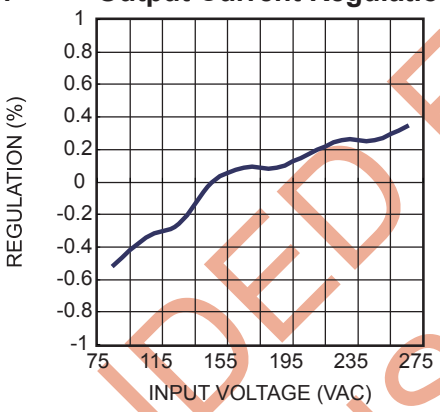
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

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V_{IN} = 230Vac, V_{OUT} = 40V, I_{OUT}=115mA, L = 4.7mH, C_{OUT}=47uF, T_A = 25°C, unless otherwise noted.

High/Low Temperature Output Current Regulation



Input Line Voltage to Output Current Regulation



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PIN FUNCTIONS

Pin # TSOT23-5	Pin # SOIC8	Name	Description
1	1	VCC	Power supply for all the control circuits.
2	2	PRO	Open lamp protection if the voltage is higher than V_{OVP}, Short Lamp protection if the voltage is lower than V_{UVP}.
3	3	GND	Ground of the IC
4	4	SOURCE	Source of internal power MOSFET. Internal peak current limit is 0.45V (typical value). Output current sample.
5	7	DRAIN	Drain of internal power MOSFET. Input of high voltage current source.
	5,6,8	N.C	Not Connected.

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FUNCTION BLOCK DIAGRAM

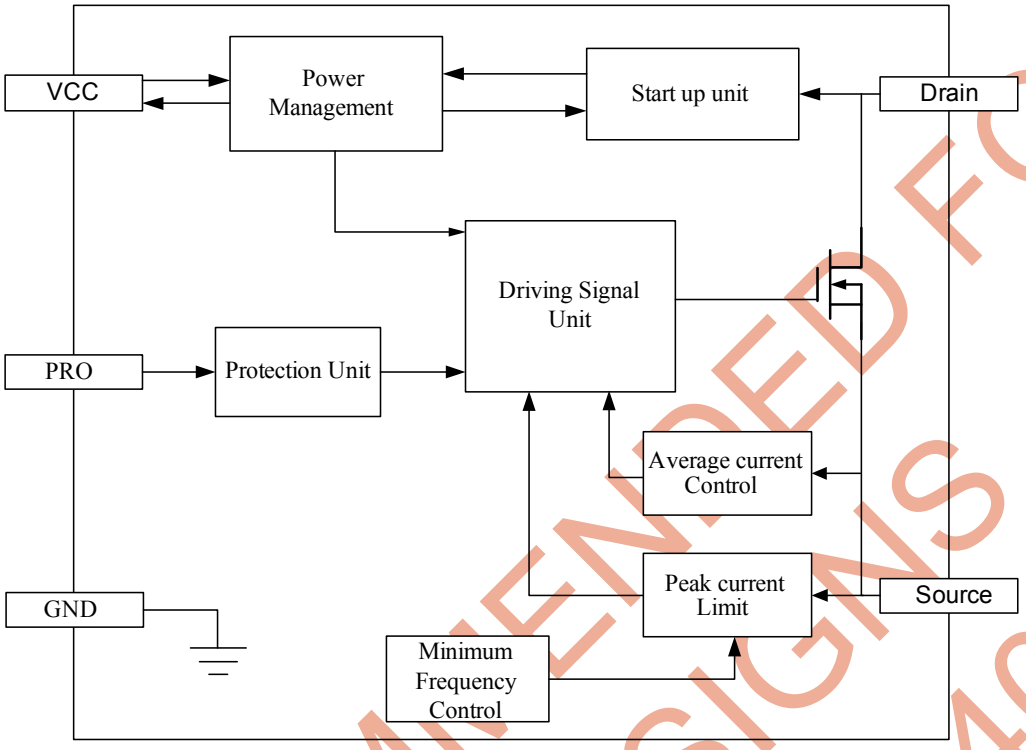


Figure 1: Functional Block Diagram

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OPERATION

MP4050 is a non-isolated, cost-effective, high efficiency converter designed to drive high-brightness light emitting diodes (LEDs) from an 85Vac to 265 Vac line, or a DC input. As shown in the typical application diagram, the regulator is designed to operate with a minimum number of external components. It incorporates the following features:

Start-up and Under Voltage Lock-out (UVLO)

The IC is self supplied by the internal high voltage regulator which is drawn from the Drain pin. The IC starts switching and the internal high voltage regulator turns off as soon as the voltage on pin V_{CC} reaches VCC_{OFF}. When the voltage on Pin VCC decreases below VCC_{ON}, the internal high voltage regulator turns on again to charge the external V_{CC} capacitor. A small capacitor such as several μF capacitor is enough to hold on the voltage of V_{CC} and a smaller capacitor also reduce component cost. When the voltage on Pin V_{CC} drops blow VCC_{STOP}, the IC stops working, the internal high voltage regulator recharges the Vcc capacitor.

When fault conditions happen, such as Short Lamp Protection, Open Lamp Protection and Over Temperature Protection (OTP), MP4050 stops working and a 18uA internal current source discharges the Vcc capacitor. After the V_{CC} drops below VCC_{PRO}, the internal high voltage regulator recharges the V_{CC} capacitor again. The restart time can be calculated by the following equation,

$$t_{restart} = C_{Vcc} \times \frac{Vcc - 2.37V}{18\mu A} + C_{Vcc} \times \frac{4.65V - 2.37V}{5mA}$$

Figure 2 shows the typical waveform with VCC under voltage lock out.

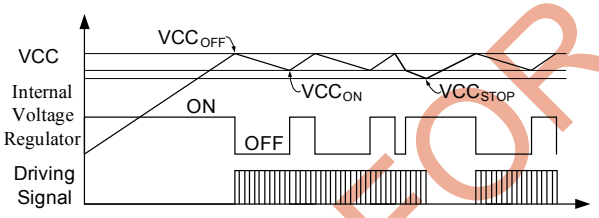


Figure 2: VCC Under-Voltage Lock Out (UVLO)

Constant Current Operation

MP4050 is a fully integrated regulator, the internal feedback logic responds to the internal sample and hold circuit to achieve constant output current regulation. The voltage of the internal sampling capacitor (V_{FB}) is compared to the internal reference 0.194V, when the sampling capacitor voltage (V_{FB}) falls below the reference voltage, which indicates insufficient output current, the integrated MOSFET is turned ON. The ON period is determined by the peak current limit. After the ON period elapses, the integrated MOSFET is turned OFF. The detail operation is shown as Figure 3.

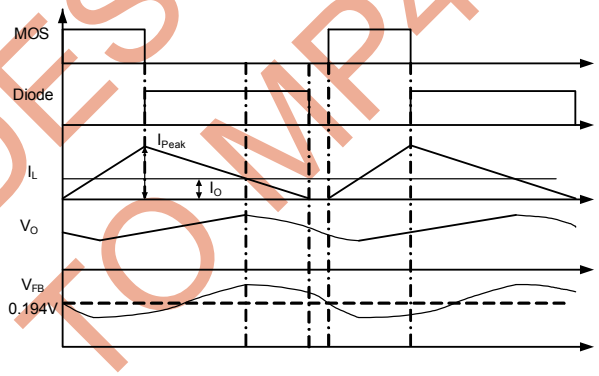


Figure 3: V_{FB} vs I_{OUT}

Thus by monitoring the internal sampling capacitor voltage, the output current can be regulated and the output current is determined by the following equation:

$$I_O = \frac{0.194V}{R1}$$

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The peak current can be obtained as follow:

$$I_{Peak} = \frac{0.45V}{R1}$$

R1 is the sense resistor.

Minimum Operating Frequency Limit

MP4050 incorporates minimum operating frequency (22kHz) to eliminate the audible noise when frequency is less than 20kHz.

When operating frequency is less than 22kHz, the internal peak current regulator will decrease the peak current value to keep the operating frequency constant about 22kHz.

If the inductance value is too large to make the operating frequency reach the minimum operating frequency, the converter will enter the CCM. And the converter works in DCM when operating frequency is larger than 22kHz.

Minimum Off Time Limit

A minimum off time limit is implemented. During the normal operation, the minimum off time limit is 4.7us, and during the start up period, the minimum off time limit is shortened gradually from 18.8μs, 9.4μs to 4.7μs (Shown as Figure 4). Each minimum off time keeps 128 switching cycle. This soft start function enables safe start-up.

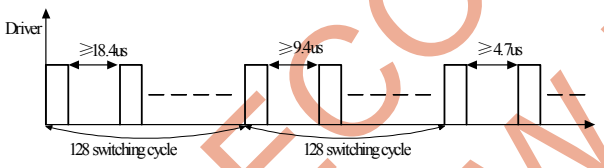


Figure 4: t_{minoff} at start-up

Thermal Shutdown (TSD)

To prevent MP4050 from any thermal damage, MP4050 shuts down switching cycle when the junction temperature exceeds 150°C. As soon as the junction temperature drops below 90°C, the power supply resumes operation. During the thermal shutdown (TSD), the V_{CC} is discharged to VCC_{PRO}, and then is re-charged by the internal high voltage regulator.

Open Lamp Protection

If the PRO pin voltage (V_{PRO}) is higher than V_{OVP} when MOSFET turns off, MP4050 stops working and a re-start cycle begins. Open lamp protection is hiccup mode. MP4050 monitors the PRO pin voltage continuously and the VCC voltage discharges and charges repeatedly. MP4050 resumes work until the fault disappears.

Short Lamp Protection

If the PRO pin voltage (V_{PRO}) is lower than V_{UVP} when MOSFET turns off, MP4050 stops working and a re-start cycle begins. Short lamp protection is hiccup mode. MP4050 monitors the PRO pin voltage continuously and the VCC voltage discharges and charges repeatedly. MP4050 resumes work until the fault disappears.

Leading Edge Blanking

There are parasitic capacitances in the circuit which can cause high current spike during the turn-on of the internal MOSFET. In order to avoid the premature termination of the switching pulse, an internal Leading Edge Blanking (LEB) unit is employed. During the blanking time, the current comparator is disabled and blocked from turning off the internal MOSFET. Figure 5 shows the leading edge blanking.

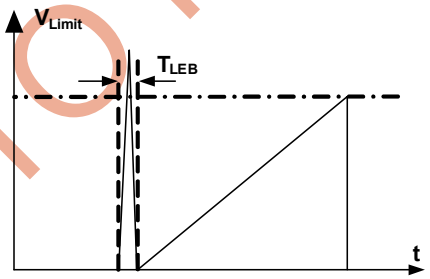


Figure 5: Leading Edge Blanking (LED)

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APPLICATION INFORMATION

Component Selection

Input Capacitor

The input capacitor is used to supply the DC input voltage for the converter. Figure 6 shows the typical DC bus voltage waveform of full bridge rectifier.

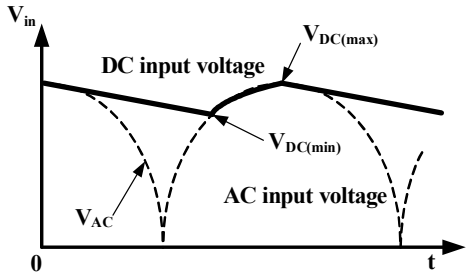


Figure 6: Input voltage waveform

When the full-bridge rectifier is used, the input capacitor is usually set as 2μF/W for the universal input condition. And when small power output, the half-bridge rectifier could also be used with a bigger capacitor.

Very low DC input voltage could cause thermal problem in LED application in Buck topology application. The minimum DC voltage is limited by the maximum duty cycle of MP4050 as following expression:

$$V_{DC(min)} > \frac{V_O \cdot (t_{ON_MAX} + t_{OFF_MIN})}{t_{ON_MAX}}$$

Inductor

MP4050 has a minimum off time limit and maximum on time limit. Both time limits affect the inductance value. The maximum inductance value and minimum inductance value can be obtained as follows:

$$L_m < L_{MAX} = \frac{(V_{DC(min)} - V_O) \cdot t_{ON_MAX}}{I_{Peak}}$$

$$L_m > L_{MIN} = \frac{V_O \cdot t_{OFF_MIN}}{I_{Peak}}$$

If the inductance value is too large, the converter enters CCM when the frequency reaches the minimum operating frequency. In such case, the reverse recovery of freewheeling diode results more power loss. Normally, it's better to make the converter operate in DCM. The following expression shows the limit of the minimum operating frequency.

$$L_m < \frac{2 \cdot I_O}{f_{SMIN} \cdot (\frac{1}{V_{DC(min)} - V_O} + \frac{1}{V_O}) \cdot I_{Peak}^2}$$

Freewheeling Diode

The diode should have a maximum reverse voltage rating which is greater than the maximum input voltage. The current rating of diode is determined by the output current which should be larger than 1.5~2 times output current.

Slow diodes cause excessive leading edge current spikes during start-up which is not acceptable. Long reverse recovery time of freewheeling diode can also affect the efficiency and the circuit operation. So ultrafast diode (Trr<75ns) such as WUGC10JH or EGC10GH are recommended.

Output Capacitor

The output capacitor is required to filter the inductance current and maintain the DC output voltage.

The output current ripple is reduced by using a bigger output capacitor. A low ESR capacitor is necessary in low temperature application.

If the output voltage ripple is limited, the ceramic, tantalum or low ESR electrolytic capacitors are recommends to use. The output voltage ripple can be estimated by:

$$V_{CCM_Ripple} = \frac{\Delta i}{8 f_S C_O} + \Delta i \cdot R_{ESR} \quad \text{CCM}$$

$$V_{DCM_Ripple} = \frac{I_O}{f_S C_O} \cdot (\frac{I_{Peak} - I_O}{I_{Peak}})^2 + I_{Peak} \cdot R_{ESR} \quad \text{DCM}$$

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Sense Resistor

The sense resistor needs to choose properly for better output current regulation. The right resistor guarantees stable output current regulation in high temperature and low temperature conditions. The sense resistor should have 1% tolerance. It is even better to parallel two 1% tolerance resistors to decrease the resistance value error further. Sense resistor with ± 400PPM/ ℃ temperature coefficient can be used for better output current regulation in high temperature and low temperature.

Feedback Resistor

Feedback resistor is used to detect the fault operation mode such as open lamp or short lamp conditions. Figure 7 shows the feedback resistors connection.

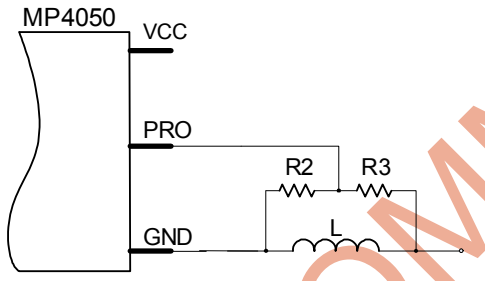


Figure 7: Feedback resistor connection

MP4050 is integrated with open lamp protection and the over voltage protection point can be designed as following function.

$$V_{OVP} = V_{PRO} \cdot (1 + \frac{R2 + R3}{R2}) - V_D$$

V_D is the freewheeling diode forward voltage drop.

The upper feedback resistor (R3) is suggested to be larger than 100kΩ to avoid the efficiency reduction in application. And the 1% tolerance type is recommended to use as feedback resistor to achieve accurate protection such over voltage protection when open lamp.

The feedback resistor R2 could be sized down to SMD 0603 package. Considering the dielectric withstanding voltage, R3 is recommended to have a minimum size of SMD 1206 package.

Dummy Load

Dummy load is recommended to regulate the output voltage low than over voltage protection point when open lamp condition. The dummy load is used to consume the power transferred to output capacitor when hiccup mode without any power consumption.

Normally less than 1mA dummy load is suggested which not deteriorate the system efficiency and also guarantees the normal open lamp protection.

PRO Decoupling Capacitor

One decoupling cap is recommended to parallel between the PRO pin and GND pin. The floating GND pin is sensitive to the voltage noise spike in high side Buck solution. One ceramic capacitor is suggested to use as decoupling capacitor to decouple the voltage noise for more stable operation.

Around 30pF PRO decoupling capacitor could be used in SOIC8 package application and as for smaller package TSOT23-5, no less than 100pF decoupling capacitor is recommended. Figure 8 shows the PRO pin decoupling capacitor connection.

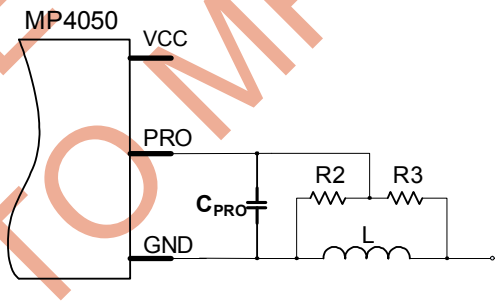


Figure 8: Decoupling capacitor

PRO Time Constant

MP4050 detects the PRO pin voltage to judge the fault condition when internal MOSEFET turns off. Long rise time of the PRO pin voltage affects MP4050 normal output voltage sample which can not judge the open lamp immediately. The PRO pin time constant (τ) should satisfy the following expression to guarantee the normal open lamp protection.

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$$\tau = C_{PRO} \cdot \frac{R2 \cdot R3}{R2 + R3} < 1\mu s$$

Output Power V-I Curve

The thermal performance limits the output power of MP4050 in very small size LED application. Different output voltage and output current specification bring about different maximum output power delivered form the MP4050 device.

Figure 9 and Figure 10 separately show the reference V-I curve in universal input voltage and high voltage input under following assumed conditions:

1. Buck topology.
2. Ambient temperature 90℃.
3. Around 30kHz working frequency.
4. No PF required where input capacitor >9uF.
5. Not trigger the thermal shutdown and leave one LED margin.

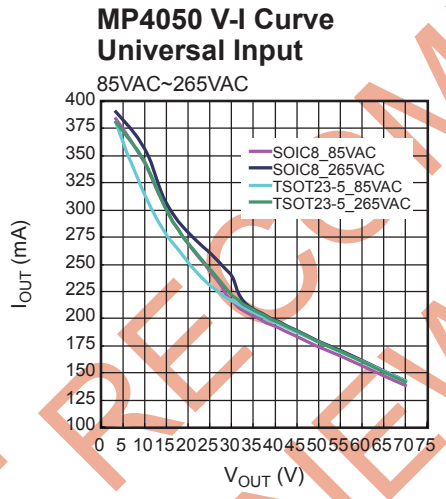


Figure 9: Universal input V-I curve

(85VAC~265VAC)

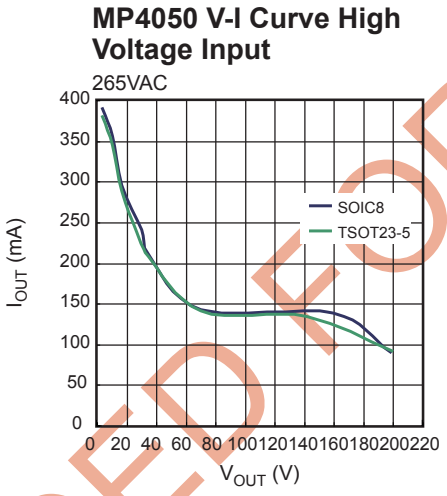


Figure 10: High voltage input V-I curve

(200VAC~265VAC)

Power Factor

MP4050 is mainly used for non-isolated, space constrained and cost sensitive LED driver solution. As for the PF>0.5 when 120VAC input required, MP4050 is also the best choose. The input capacitance is reduced to achieve the highest possible power factor as PF>0.7 when 120VAC and PF>0.5 when 230VAC if the output current regulation is not strict.

Surge

Select the appropriate input capacitance to obtain a good surge performance. With the input capacitor C2 (4.7uF) and C3 (4.7uF) as Figure 13, the board can pass 1kV differential input line 1.2/50us surge test (IEC61000-4-5). It is recommended to increase the input capacitor value to suppress above 1kV surge test. As for high PF required application with lower input capacitor value giving a greater voltage rise, a Metal Oxide Varistor (MOV) is typically required to pass the above 1kV or greater surge test.

Table 1 shows input capacitor value required for pass the differential surge test.

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Table 1: Recommended input capacitance

Surge voltage	500V	1000V	1500V	2000V
C2	3.3μF	4.7μF	4.7μF	Show in Figure11
C3	3.3μF	4.7μF	10μF	

The demo board can pass the 2000V differential surge test by adopting below circuit setup.

(1) Add a MOV RV1(TVR14431)

(2) Add a fuse F1 (SS-5-2A)

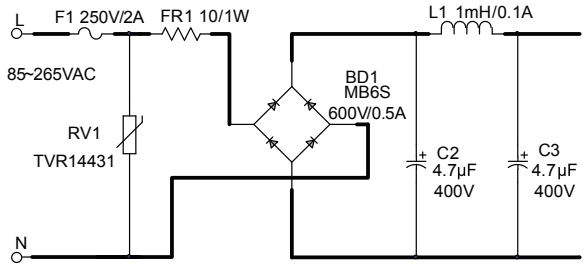


Figure11: 2kV surge solution

Layout Guide

PCB layout is very important to achieve reliable operation, good EMI and good thermal performance especially in very small size LED application. The following describe some layout recommendations.

1. The loop formed between the MP4050, inductor, freewheeling diode and output capacitor should be kept as small as possible for better EMI.
2. Put the AC input far away from the switching nodes to minimize the noise coupling that may bypass the input filter.
3. The VCC pin and PRO pin capacitor should be located physically close to the IC and GND.
4. Put the feedback resistor next to the PRO pin as possible and minimize the feedback sampling loop to minimize the noise coupling route.
5. In the buck topology, since the MP4050 SOURCE pin is switching nodes, the copper area connected to SOURCE should be minimize to minimize EMI with the thermal constraints of the design.
6. Since MP4050 DRAIN pin is static node connecting to DC input, the copper area connected to DRAIN could be maximized to improve the heat sinking.

Figure 12 shows a sample layout.

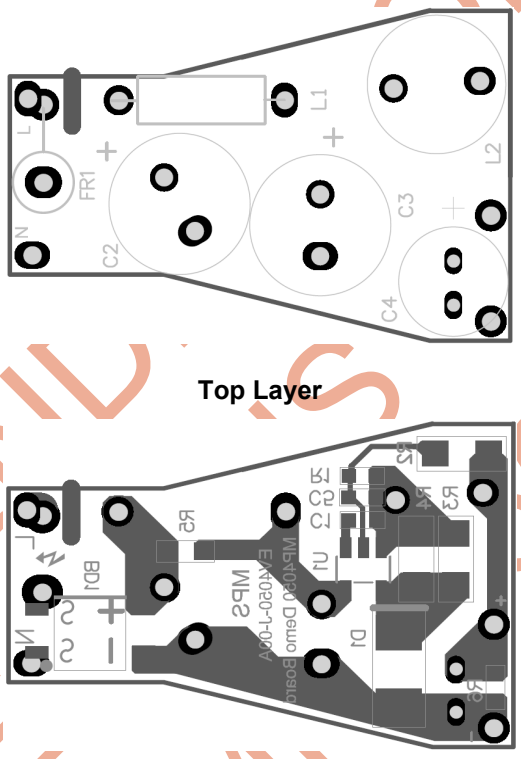


Figure 12: PCB Layout

Design Example

Below is a design example following the application guidelines based on these specifications:

Table 2: Design Example

V_{IN}	85Vac~265Vac
V_{OUT}	40V
I_{OUT}	115mA

Figure 13 shows the detailed application schematic. This circuit is used for the typical performance and circuit waveforms. For more device applications, please refer to the related evaluation board datasheets.

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TYPICAL APPLICATION CIRCUITS

Figure 13 shows a typical application example of a 40V, 115mA non-isolated buck topology power supply using MP4050.

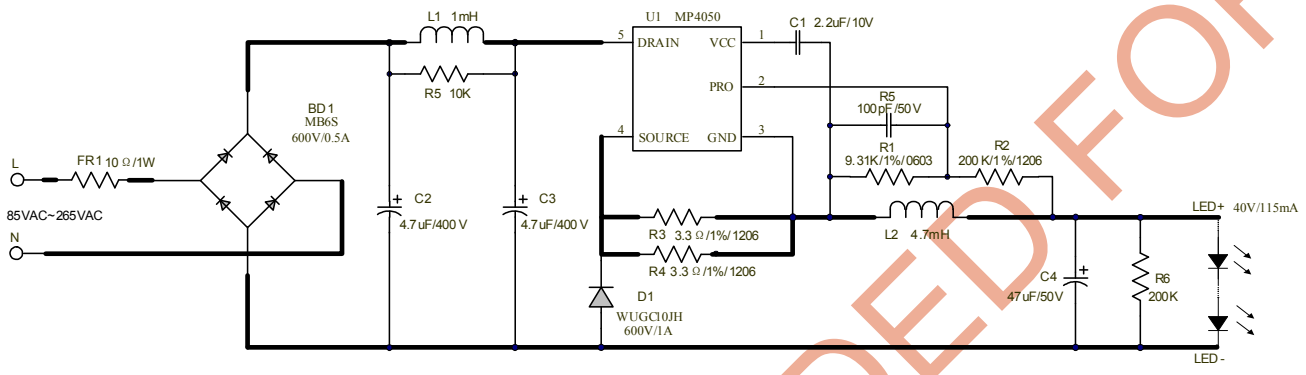
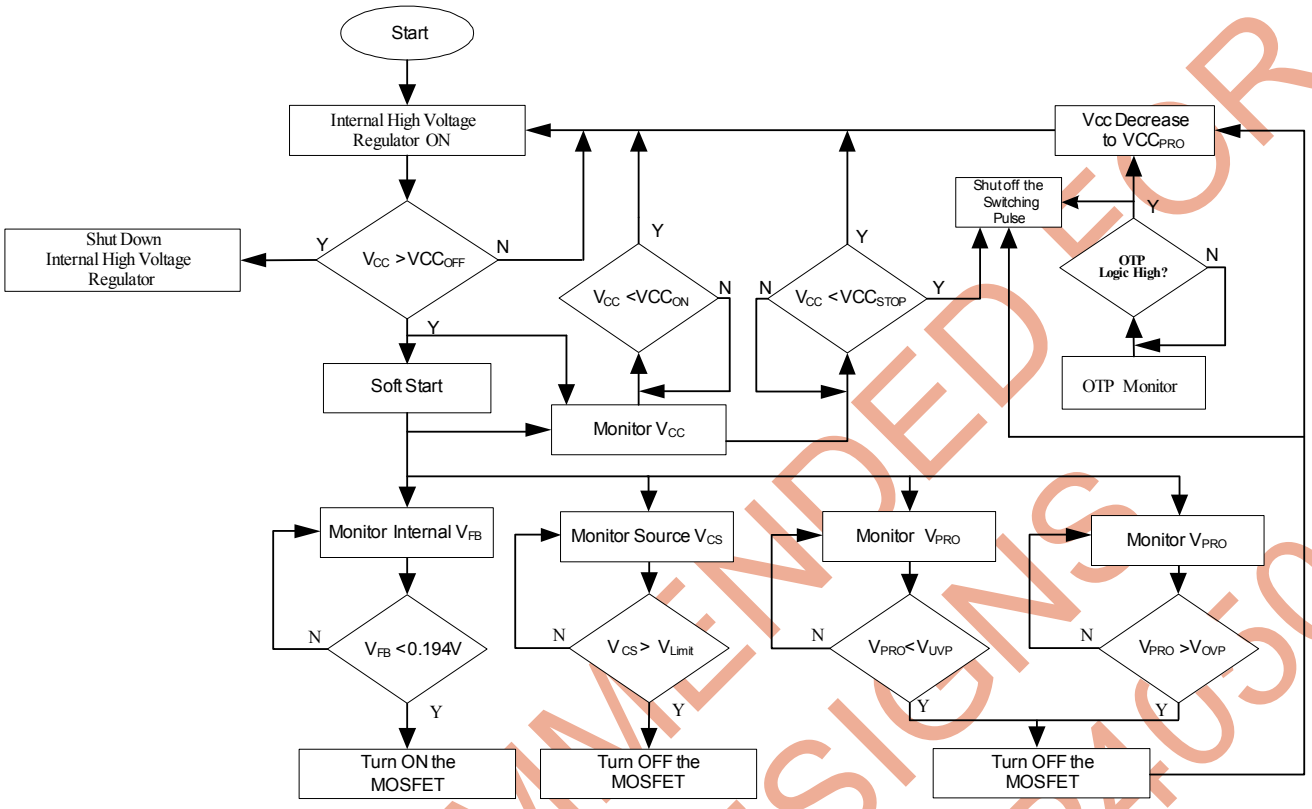


Figure 13: Typical Buck Converter Application

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FLOW CHART



UVLO, OTP, Short Lamp Protection, Open Lamp Protection
All protections are auto restart

Figure 14: Control Flow Chart

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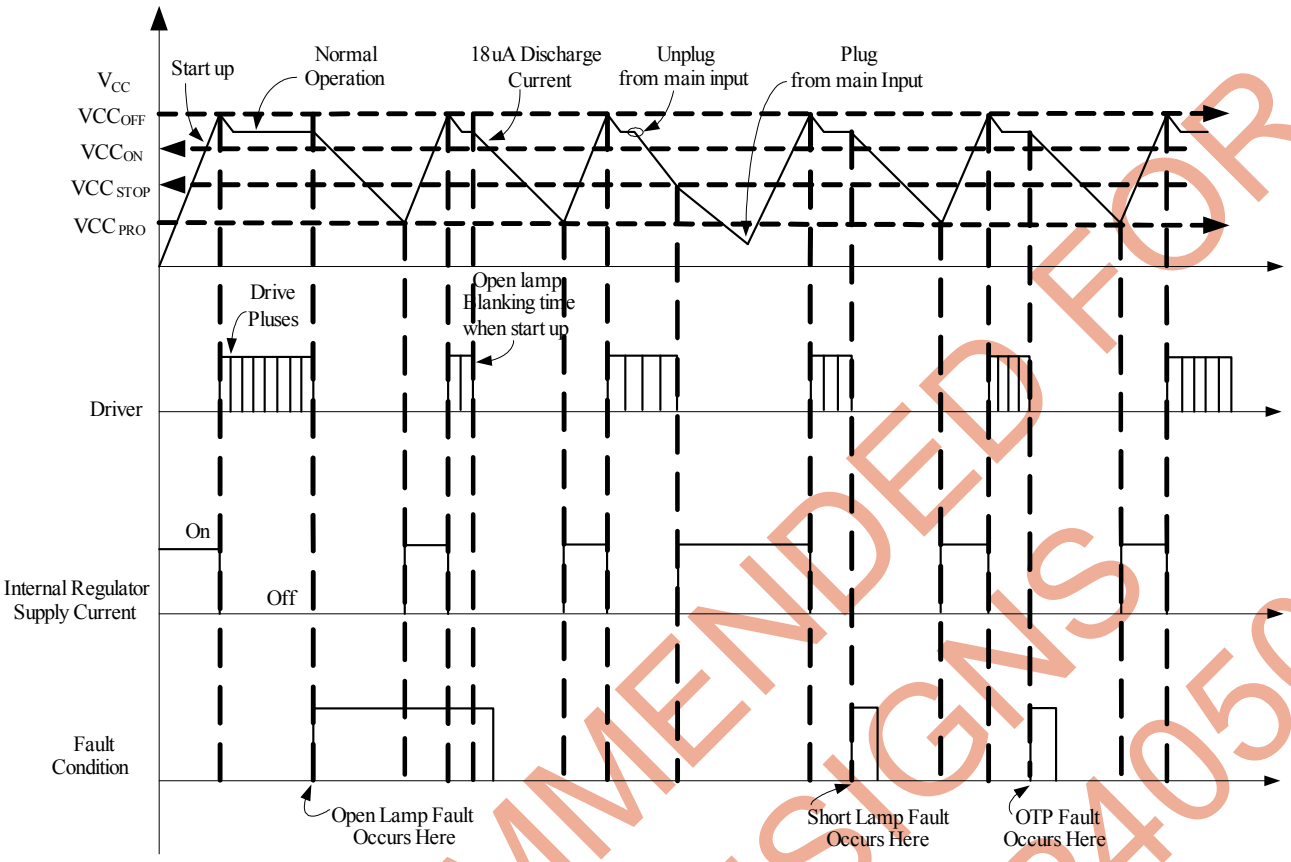


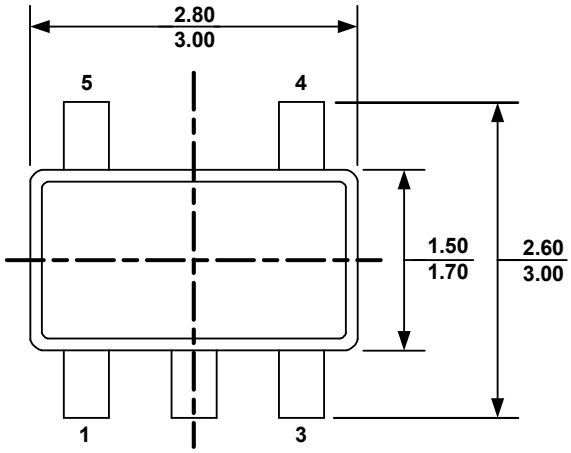
Figure 15: Evolution of the signal in presence of a Fault

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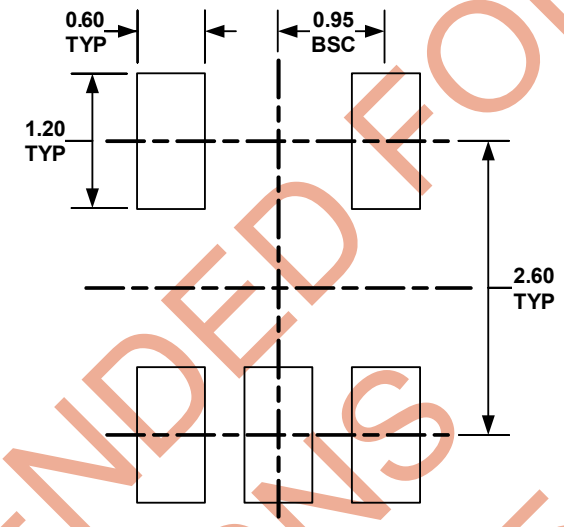
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PACKAGE INFORMATION

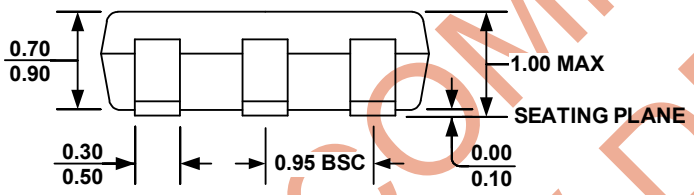
TSOT23-5



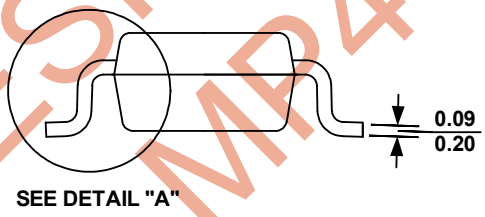
TOP VIEW



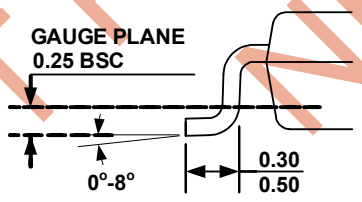
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

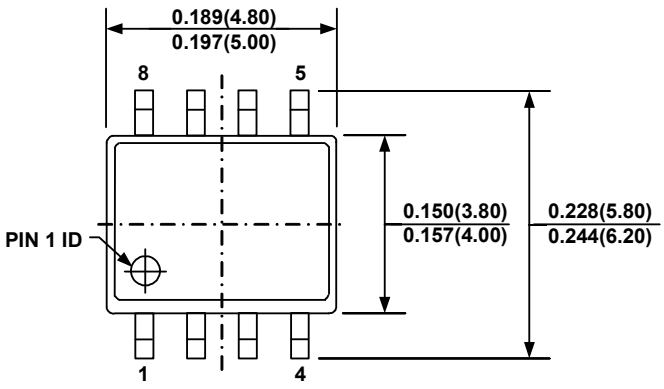
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2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY(BOTTOM OF LEADS AFTER FORMING) SHALL BE0.10 MILLIMETERS MAX.
5) DRAWING CONFORMS TO JEDEC MO-193, VARIATION AA.
6) DRAWING IS NOT TO SCALE

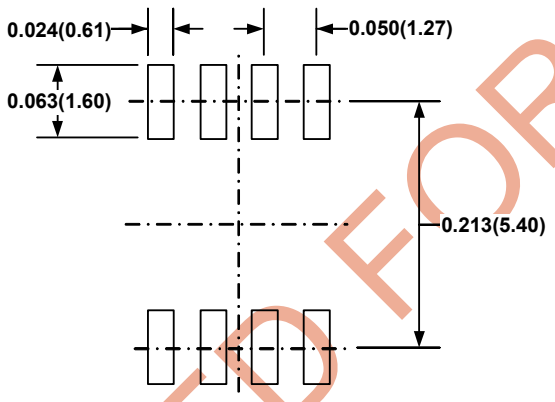
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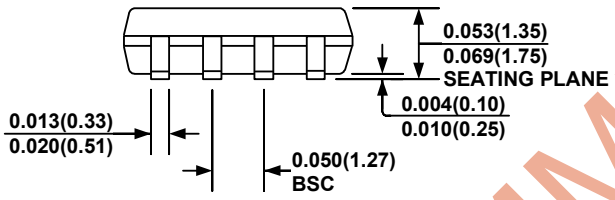
SOIC8



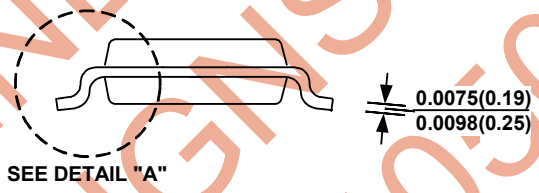
TOP VIEW



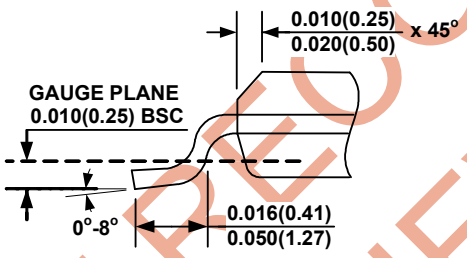
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FRONT VIEW



SIDE VIEW



DETAIL "A"

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