Freescale Semiconductor
Technical Data

Document Number: MMRF1022HS
Rev. 0, 4/2016

RF Power LDMOS Transistor

N-Channel Enhancement-Mode Lateral MOSFET

This 63 W asymmetrical Doherty RF power LDMOS transistor is optimized for instantaneous signal bandwidth capabilities covering the frequency range of 2110 to 2170 MHz. This part is ideally suited for commercial and defense communications and electronic warfare applications, such as an IED jammer.

2100 MHz

- Typical Doherty Single-Carrier W-CDMA Performance: V_{DD} = 28 Vdc, I_{DQA} = 500 mA, V_{GSB} = 0.5 Vdc, P_{out} = 63 W Avg., Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF.

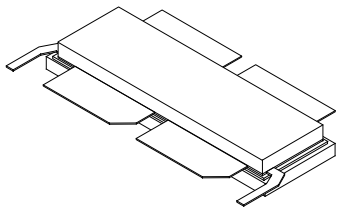
Frequency	G_{ps} (dB)	η_D (%)	Output PAR (dB)	ACPR (dBc)
2110 MHz	16.2	51.6	7.9	–28.5
2140 MHz	16.2	51.8	7.9	–28.8
2170 MHz	16.1	50.9	7.9	–29.5

Features

- Advanced high performance in-package Doherty
- Greater negative gate-source voltage range for improved Class C operation
- Designed for digital predistortion error correction systems

MMRF1022HS

2110–2170 MHz, 63 W AVG., 28 V AIRFAST RF POWER LDMOS TRANSISTOR



NI-1230S-4L2L

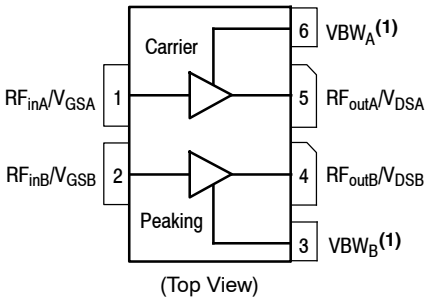


Figure 1. Pin Connections

1. Device cannot operate with the V_{DD} current supplied through pin 3 and pin 6.

© Freescale Semiconductor, Inc., 2016. All rights reserved.

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	–0.5, +65	Vdc
Gate-Source Voltage	V_{GS}	–6.0, +10	Vdc
Operating Voltage	V_{DD}	32, +0	Vdc
Storage Temperature Range	T_{stg}	–65 to +150	°C
Case Operating Temperature Range	T_C	–40 to +150	°C
Operating Junction Temperature Range (1)	T_J	–40 to +225	°C
CW Operation @ T_C = 25°C Derate above 25°C	CW	278 1.2	W W/°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value (2)	Unit
Thermal Resistance, Junction to Case Case Temperature 73°C, 63 W Avg., W-CDMA, 28 Vdc, I_{DQA} = 500 mA, V_{GSB} = 0.5 Vdc, 2140 MHz	$R_{\theta JC}$	0.33	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22-A114)	2, passes 2500 V
Machine Model (per EIA/JESD22-A115)	B, passes 200 V
Charge Device Model (per JESD22-C101)	IV, passes 1200 V

Table 4. Electrical Characteristics (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Off Characteristics (3)					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 65 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 32 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate-Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
On Characteristics - Side A (3)					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 140 μAdc)	$V_{GS(th)}$	0.8	1.2	1.6	Vdc
Gate Quiescent Voltage (V_{DD} = 28 Vdc, I_{DA} = 500 mAdc, Measured in Functional Test)	$V_{GSA(Q)}$	1.4	1.9	2.2	Vdc
Drain-Source On-Voltage (V_{GS} = 10 Vdc, I_D = 1.4 Adc)	$V_{DS(on)}$	0.1	0.2	0.3	Vdc
On Characteristics - Side B (3)					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 240 μAdc)	$V_{GS(th)}$	0.8	1.2	1.6	Vdc
Drain-Source On-Voltage (V_{GS} = 10 Vdc, I_D = 2.4 Adc)	$V_{DS(on)}$	0.1	0.2	0.3	Vdc

1. Continuous use at maximum temperature will affect MTTF.
2. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.nxp.com/RF and search for AN1955.
3. Each side of device measured separately.

(continued)

Electrical Characteristics (T_A = 25°C unless otherwise noted) **(continued)**

Characteristic	Symbol	Min	Typ	Max	Unit
Functional Tests [1,2] (In Freescale Doherty Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQA} = 500 mA, V_{GSB} = 0.5 Vdc, P_{out} = 63 W Avg., f = 2140 MHz, Single-Carrier W-CDMA, IQ Magnitude Clipping, Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ ±5 MHz Offset.					
Power Gain	G_{ps}	15.6	16.2	18.6	dB
Drain Efficiency	η_D	49.2	51.8	—	%
Output Peak-to-Average Ratio @ 0.01% Probability on CCDF	PAR	7.2	7.9	—	dB
Adjacent Channel Power Ratio	ACPR	—	–28.8	–27.2	dBc
Load Mismatch (In Freescale Test Fixture, 50 ohm system) I_{DQA} = 500 mA, f = 2140 MHz					
VSWR 10:1 at 28 Vdc, 288 W Pulse Output Power (3 dB Input Overdrive from 363 W Pulse Rated Power)	No Device Degradation				
Typical Performance [2] (In Freescale Doherty Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQA} = 500 mA, V_{GSB} = 0.5 Vdc, 2110–2170 MHz Bandwidth					
P_{out} @ 1 dB Compression Point, CW	P1dB	—	301[3]	—	W
P_{out} @ 3 dB Compression Point [4]	P3dB	—	400	—	W
AM/PM (Maximum value measured at the P3dB compression point across the 2110–2170 MHz bandwidth)	Φ	—	–27	—	°
VBW Resonance Point (IMD Third Order Intermodulation Inflection Point)	VBW_{res}	—	100	—	MHz
Gain Flatness in 60 MHz Bandwidth @ P_{out} = 63 W Avg.	G_F	—	0.2	—	dB
Gain Variation over Temperature (–30°C to +85°C)	ΔG	—	0.012	—	dB/°C
Output Power Variation over Temperature (–30°C to +85°C) [3]	ΔP1dB	—	0.002	—	dB/°C

Table 5. Ordering Information

Device	Tape and Reel Information	Package
MMRF1022HSR5	R5 Suffix = 50 Units, 56 mm Tape Width, 13-inch Reel	NI-1230S-4L2L

1. Part internally matched both on input and output.
2. Measurements made with device in an asymmetrical Doherty configuration.
3. Exceeds recommended operating conditions. See CW operation data in Maximum Ratings table.
4. P3dB = P_{avg} + 7.0 dB where P_{avg} is the average output power measured using an unclipped W-CDMA single-carrier input signal where output PAR is compressed to 7.0 dB @ 0.01% probability on CCDF.

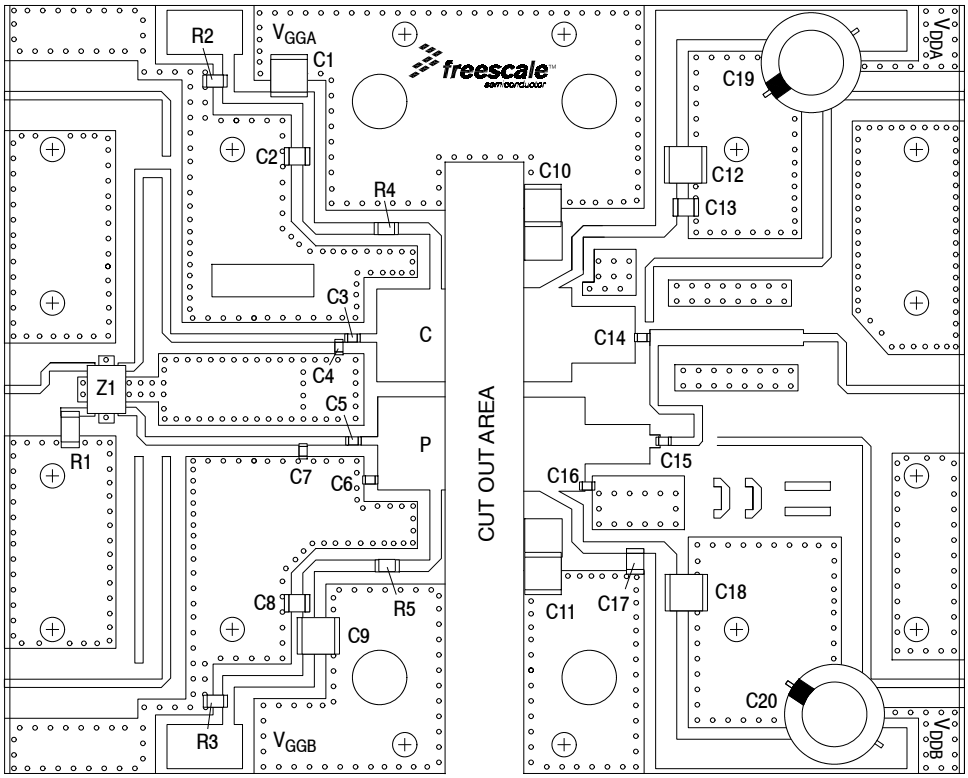


Figure 2. MMRF1022HS Test Circuit Component Layout

Table 6. MMRF1022HS Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1, C9, C10, C11, C12, C18	10 μF Chip Capacitors	C5750X7S2A106M230KB	TDK
C2, C8, C13, C17	9.1 pF Chip Capacitors	ATC100B9R1CT500XT	ATC
C3, C5, C15	9.1 pF Chip Capacitors	ATC600F9R1BT250XT	ATC
C4	0.5 pF Chip Capacitor	ATC600F0R5BT250XT	ATC
C6	0.8 pF Chip Capacitor	ATC600F0R8BT250XT	ATC
C7	1.1 pF Chip Capacitor	ATC600F1R1BT250XT	ATC
C14	4.7 pF Chip Capacitor	ATC600F4R7BT250XT	ATC
C16	0.2 pF Chip Capacitor	ATC600F0R2BT250XT	ATC
C19, C20	470 μF, 63 V Electrolytic Capacitors	MCGPR63V477M13X26-RH	Multicomp
R1	50 Ω, 20 W Chip Resistor	C20A5024	Anaren
R2, R3	5.6 KΩ, 1/4 W Chip Resistors	CRCW12065K60FKEA	Vishay
R4, R5	6.2 Ω, 1/4 W Chip Resistors	CRCW12066R20FKEA	Vishay
Z1	2000–2300 MHz Band, 90°, 5 dB Directional Coupler	X3C21P1-05S	Anaren
PCB	Rogers RO4350B, 0.020″, ε_r = 3.66	—	MTL

TYPICAL CHARACTERISTICS — 2110–2170 MHz

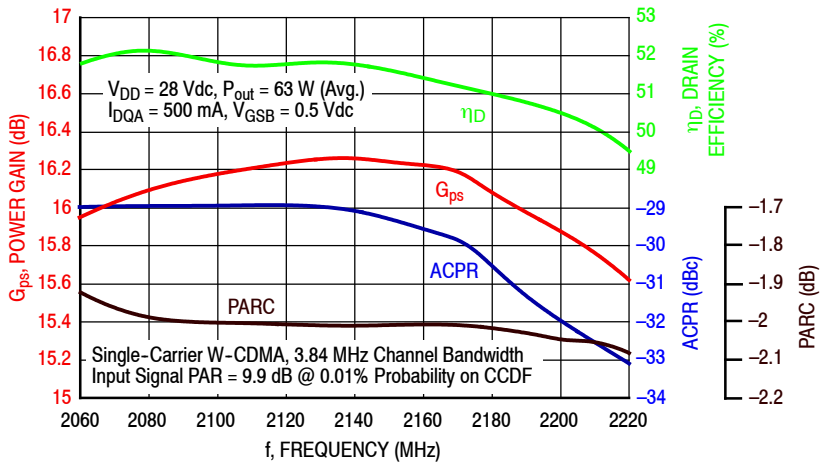


Figure 3. Single-Carrier Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ P_{out} = 63 Watts Avg.

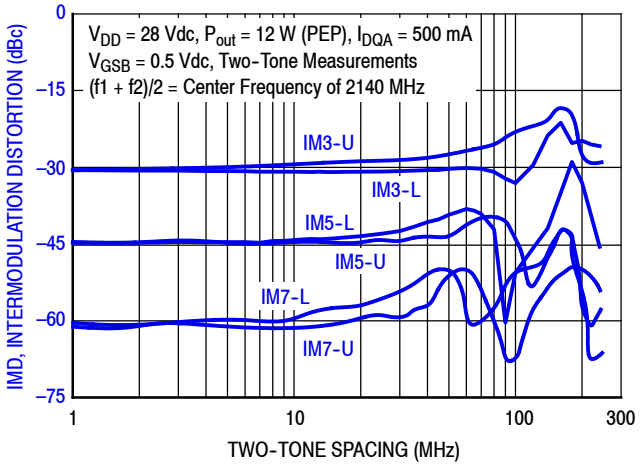


Figure 4. Intermodulation Distortion Products versus Two-Tone Spacing

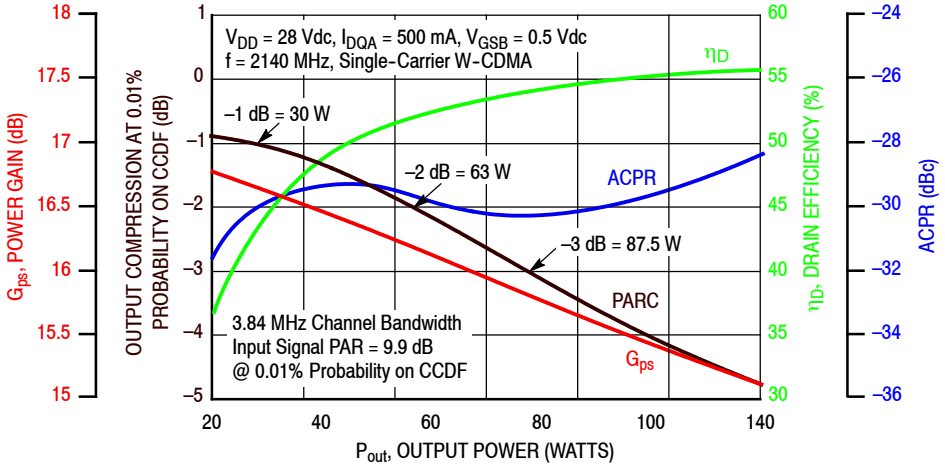


Figure 5. Output Peak-to-Average Ratio Compression (PARC) versus Output Power

TYPICAL CHARACTERISTICS — 2110–2170 MHz

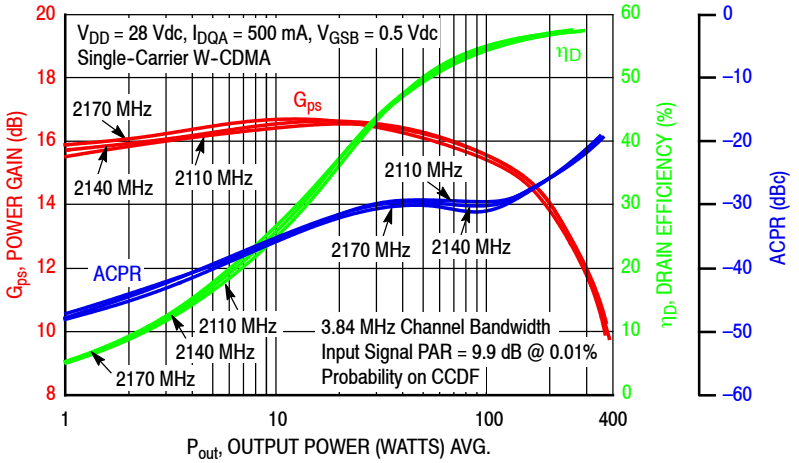


Figure 6. Single-Carrier W-CDMA Power Gain, Drain Efficiency and ACPR versus Output Power

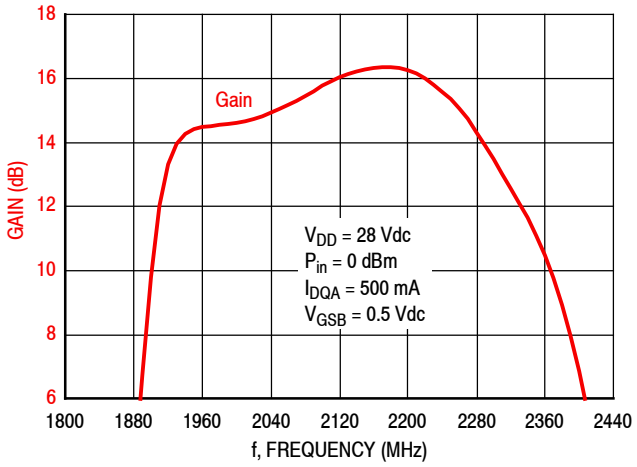


Figure 7. Broadband Frequency Response

Table 7. Carrier Side Load Pull Performance — Maximum Power Tuning

V_{DD} = 28 Vdc, I_{DQA} = 774 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

			Max Output Power					
			P1dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2110	3.58 – j6.92	3.34 + j6.51	2.02 – j4.19	19.3	51.9	155	58.6	–14
2140	4.43 – j7.58	4.13 + j7.07	2.06 – j4.27	19.3	51.9	154	58.2	–15
2170	5.91 – j8.34	5.51 + j7.60	2.07 – j4.36	19.3	51.8	153	57.2	–15

			Max Output Power					
			P3dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2110	3.58 – j6.92	3.35 + j6.99	1.95 – j4.52	16.9	52.7	184	58.7	–19
2140	4.43 – j7.58	4.25 + j7.68	2.04 – j4.59	17.0	52.6	183	58.3	–20
2170	5.91 – j8.34	5.85 + j8.37	2.03 – j4.68	17.0	52.6	181	57.4	–19

(1) Load impedance for optimum P1dB power.
(2) Load impedance for optimum P3dB power.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

Table 8. Carrier Side Load Pull Performance — Maximum Drain Efficiency Tuning

V_{DD} = 28 Vdc, I_{DQA} = 774 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

			Max Drain Efficiency					
			P1dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2110	3.58 – j6.92	3.40 + j6.96	3.99 – j2.11	22.1	49.7	93	69.3	–22
2140	4.43 – j7.58	4.27 + j7.51	3.90 – j2.21	22.0	49.7	93	68.0	–21
2170	5.91 – j8.34	5.82 + j7.92	4.04 – j2.22	22.0	49.5	88	66.1	–20

			Max Drain Efficiency					
			P3dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2110	3.58 – j6.92	3.29 + j7.28	3.58 – j2.55	19.7	50.9	122	69.6	–29
2140	4.43 – j7.58	4.19 + j8.05	3.34 – j2.43	19.7	50.7	119	67.6	–29
2170	5.91 – j8.34	5.96 + j8.77	3.33 – j2.55	19.7	50.8	119	66.4	–28

(1) Load impedance for optimum P1dB efficiency.
(2) Load impedance for optimum P3dB efficiency.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

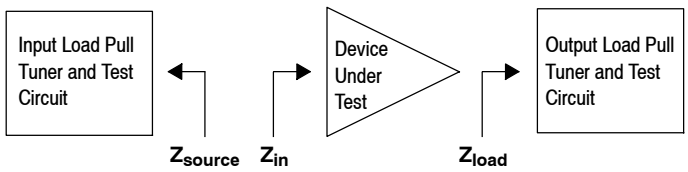


Table 9. Peaking Side Load Pull Performance — Maximum Power Tuning

V_{DD} = 28 Vdc, V_{GSB} = 0.8 Vdc, Pulsed CW, 10 μsec(on), 10% Duty Cycle

			Max Output Power					
			P1dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2110	2.40 – j5.79	2.25 + j5.71	1.80 – j4.30	14.8	54.8	300	53.8	–26
2140	2.86 – j6.24	2.71 + j6.24	1.91 – j4.27	15.2	54.8	300	54.5	–27
2170	3.85 – j6.73	3.68 + j6.78	1.96 – j4.34	15.4	54.8	302	54.3	–28

			Max Output Power					
			P3dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2110	2.40 – j5.79	2.33 + j6.08	1.77 – j4.50	12.6	55.5	353	55.2	–33
2140	2.86 – j6.24	2.94 + j6.66	1.89 – j4.66	12.9	55.4	350	54.6	–34
2170	3.85 – j6.73	4.09 + j7.25	1.95 – j4.72	13.1	55.5	351	54.6	–35

(1) Load impedance for optimum P1dB power.
(2) Load impedance for optimum P3dB power.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

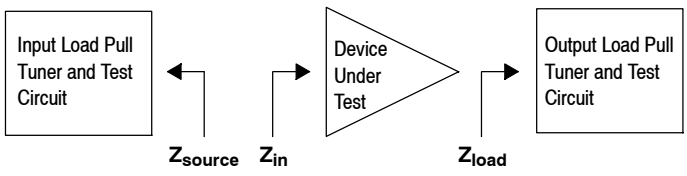
Table 10. Peaking Side Load Pull Performance — Maximum Drain Efficiency Tuning

V_{DD} = 28 Vdc, V_{GSB} = 0.8 Vdc, Pulsed CW, 10 μsec(on), 10% Duty Cycle

			Max Drain Efficiency					
			P1dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2110	2.40 – j5.79	1.97 + j5.83	4.14 – j3.31	16.4	53.3	215	64.5	–33
2140	2.86 – j6.24	2.41 + j6.35	3.90 – j2.93	16.7	53.4	218	64.4	–34
2170	3.85 – j6.73	3.27 + j6.92	3.73 – j2.68	16.9	53.3	214	64.1	–35

			Max Drain Efficiency					
			P3dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2110	2.40 – j5.79	2.14 + j6.14	4.07 – j3.91	14.1	54.1	258	64.2	–40
2140	2.86 – j6.24	2.65 + j6.74	3.90 – j3.32	14.6	54.1	257	64.4	–43
2170	3.85 – j6.73	3.74 + j7.38	3.57 – j3.27	14.7	54.3	267	64.0	–43

(1) Load impedance for optimum P1dB efficiency.
(2) Load impedance for optimum P3dB efficiency.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.



P1dB – TYPICAL CARRIER LOAD PULL CONTOURS — 2140 MHz

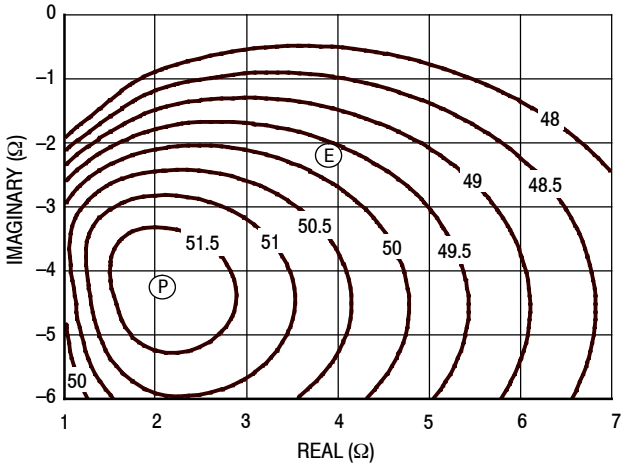


Figure 8. P1dB Load Pull Output Power Contours (dBm)

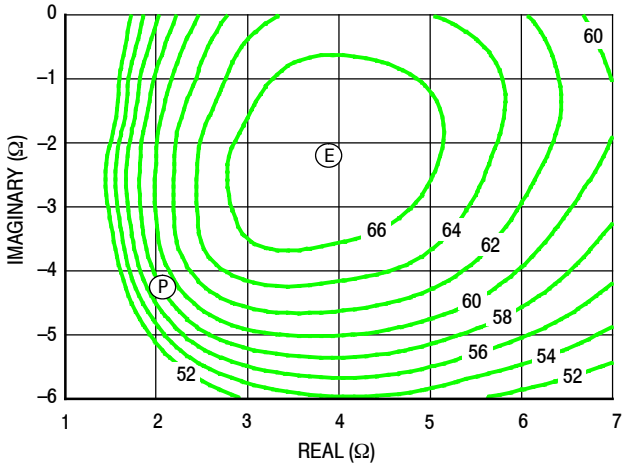


Figure 9. P1dB Load Pull Efficiency Contours (%)

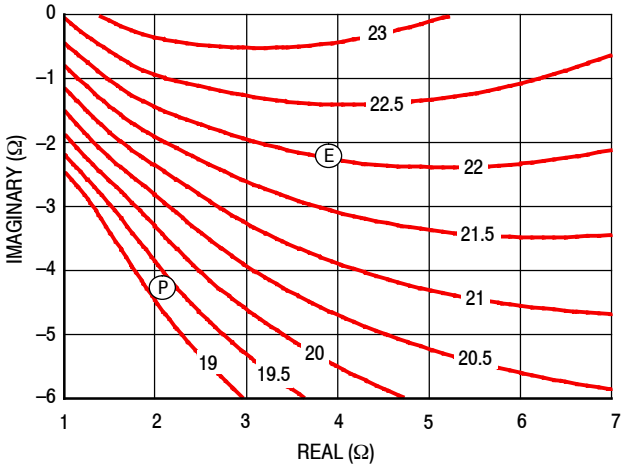


Figure 10. P1dB Load Pull Gain Contours (dB)

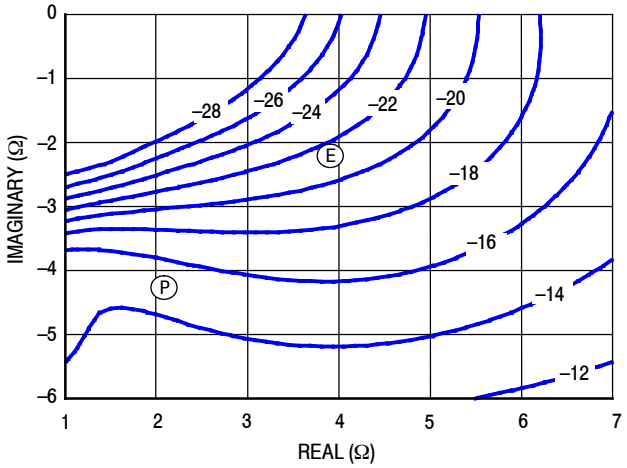


Figure 11. P1dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

Gain

Drain Efficiency

Linearity

Output Power

P3dB – TYPICAL CARRIER LOAD PULL CONTOURS — 2140 MHz

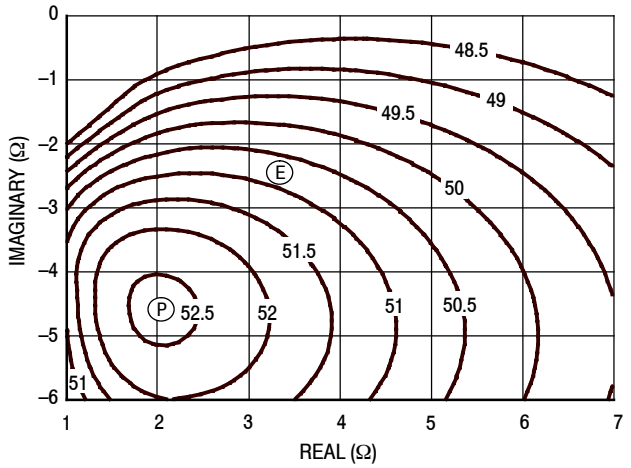


Figure 12. P3dB Load Pull Output Power Contours (dBm)

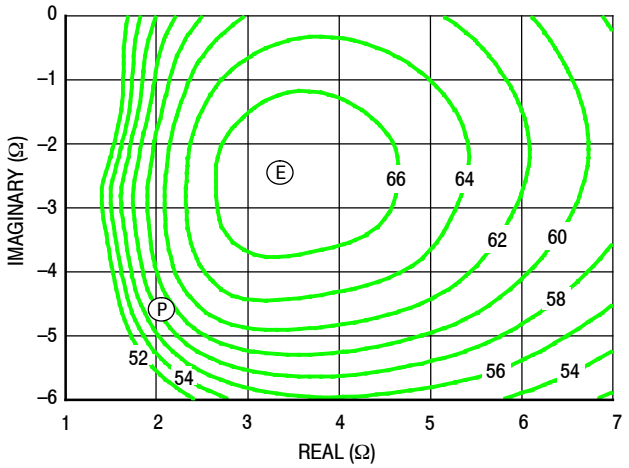


Figure 13. P3dB Load Pull Efficiency Contours (%)

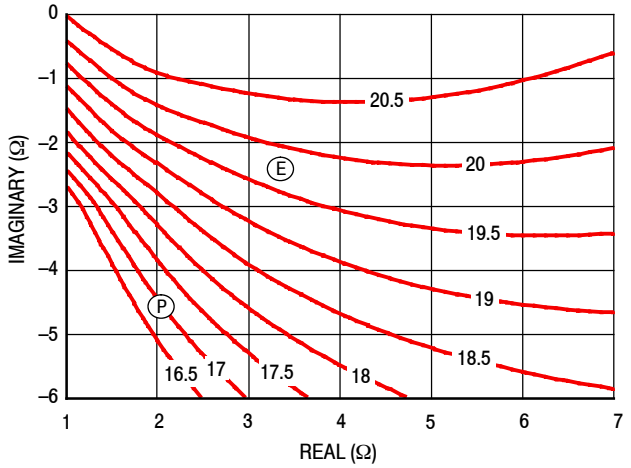


Figure 14. P3dB Load Pull Gain Contours (dB)

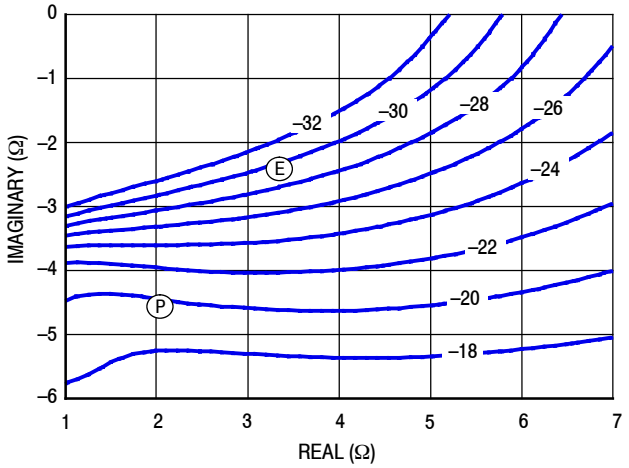


Figure 15. P3dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

Gain

Drain Efficiency

Linearity

Output Power

P1dB – TYPICAL PEAKING LOAD PULL CONTOURS — 2140 MHz

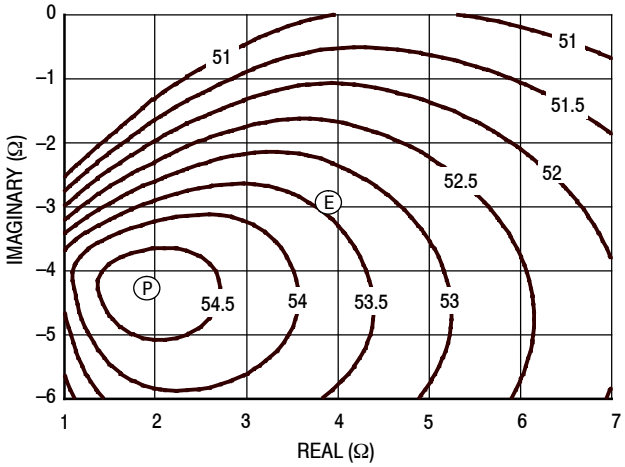


Figure 16. P1dB Load Pull Output Power Contours (dBm)

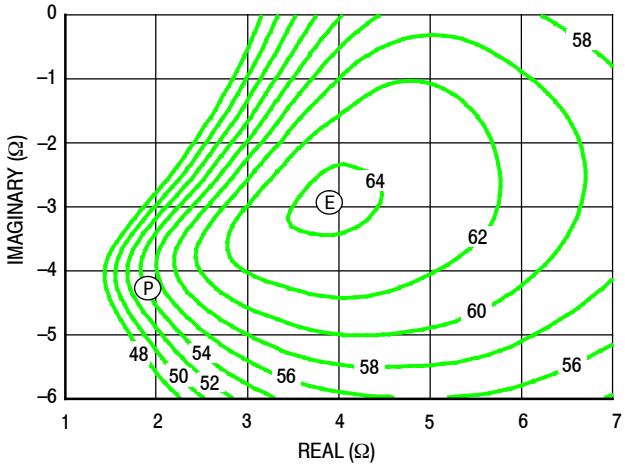


Figure 17. P1dB Load Pull Efficiency Contours (%)

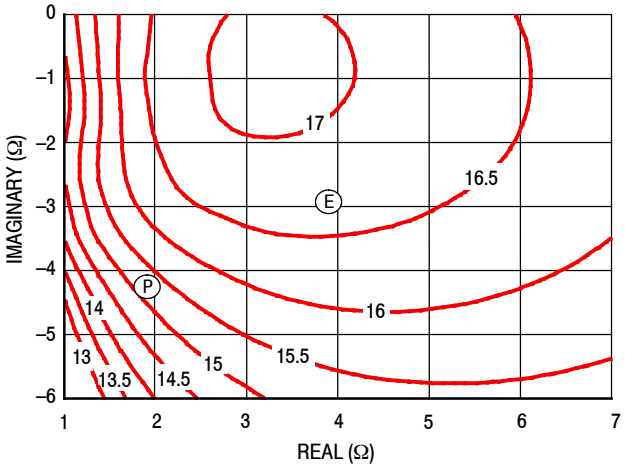


Figure 18. P1dB Load Pull Gain Contours (dB)

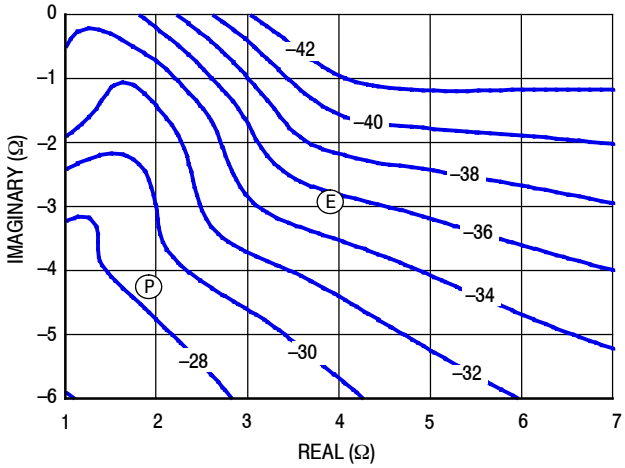


Figure 19. P1dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

Gain

Drain Efficiency

Linearity

Output Power

P3dB – TYPICAL PEAKING LOAD PULL CONTOURS — 2140 MHz

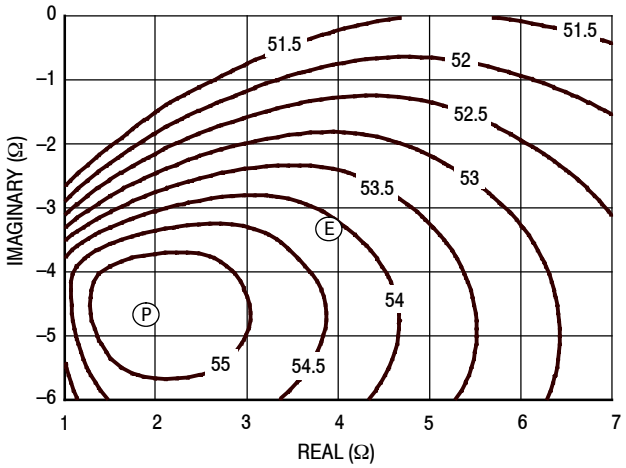


Figure 20. P3dB Load Pull Output Power Contours (dBm)

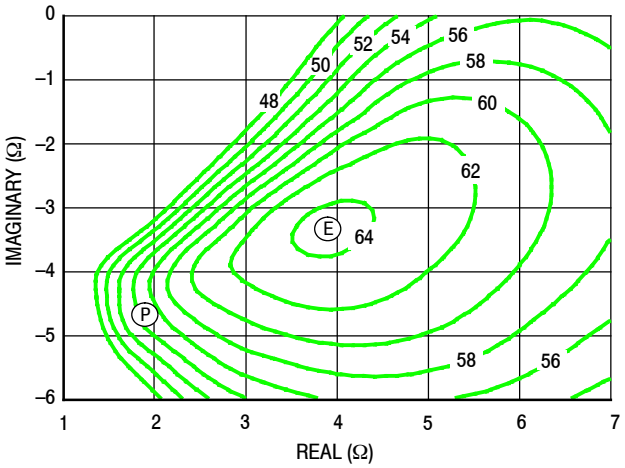


Figure 21. P3dB Load Pull Efficiency Contours (%)

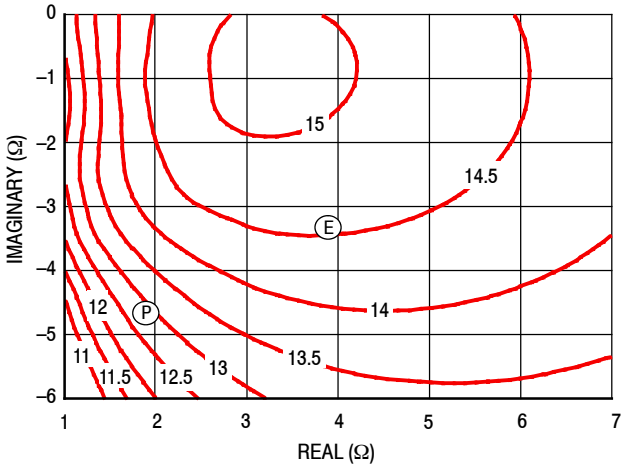


Figure 22. P3dB Load Pull Gain Contours (dB)

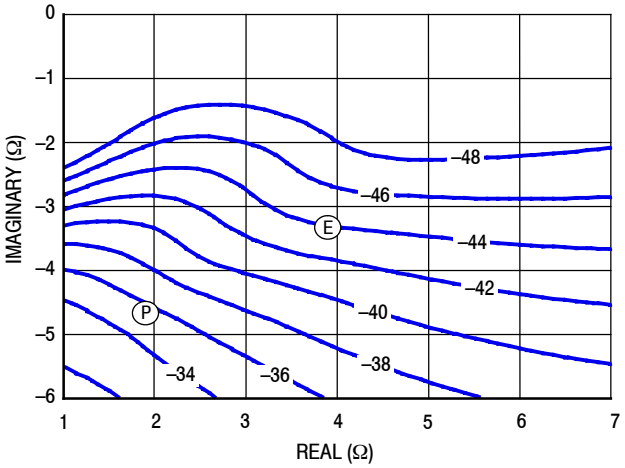


Figure 23. P3dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

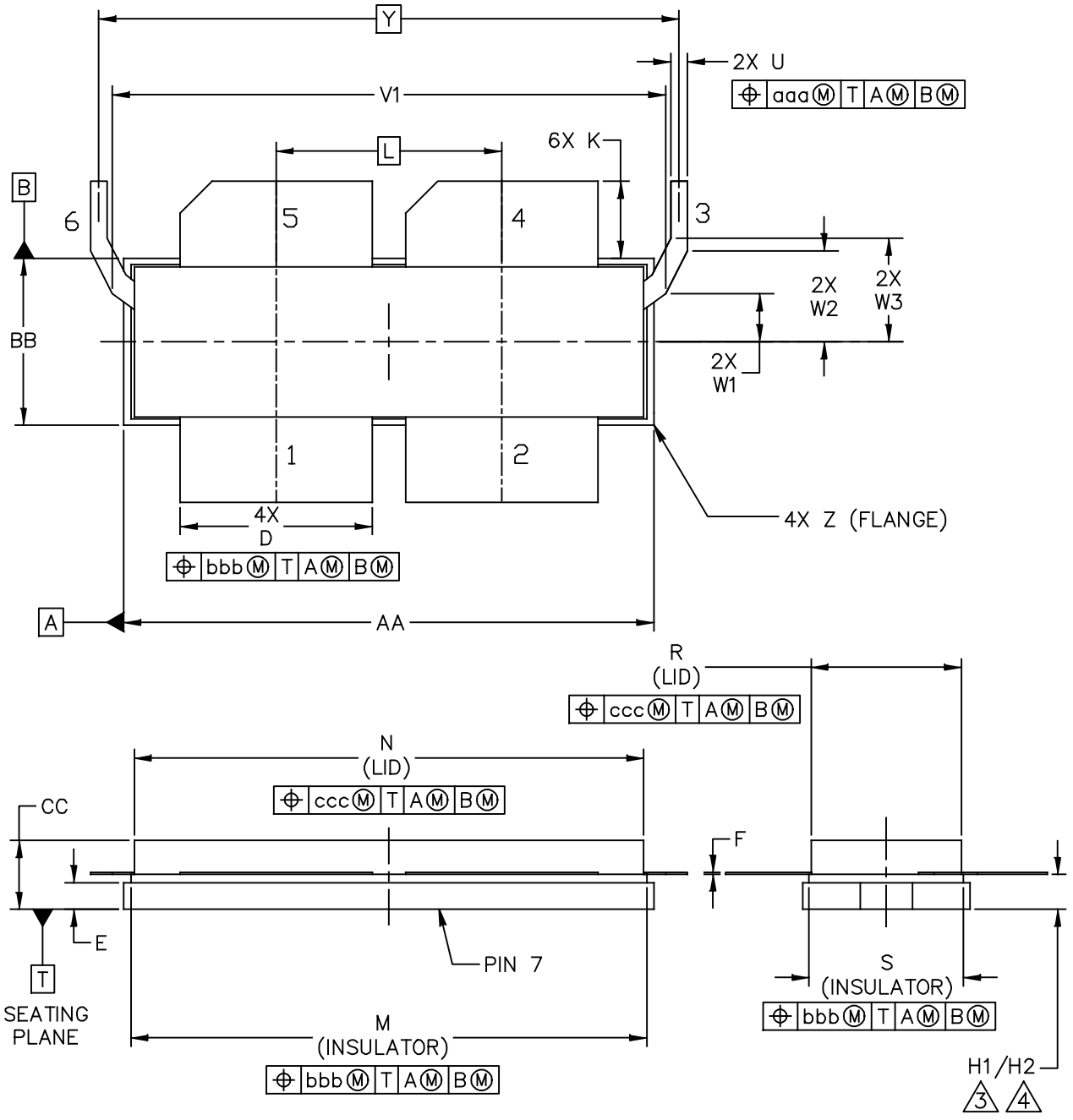
Gain

Drain Efficiency

Linearity

Output Power

PACKAGE DIMENSIONS



© NXP SEMICONDUCTORS N.V. ALL RIGHTS RESERVED	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: NI−1230−4LS2L	DOCUMENT NO: 98ASA00513D	REV: B
	STANDARD: NON−JEDEC	
	SOT1800−1	08 FEB 2016

NOTES:

1. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.

2. CONTROLLING DIMENSION: INCH

3. DIMENSIONS H1 AND H2 ARE MEASURED .030 INCH (0.762 MM) AWAY FROM FLANGE PARALLEL TO DATUM B. H1 APPLIES TO PINS 1, 2, 4 & 5. H2 APPLIES TO PINS 3 & 6.

4. TOLERANCE OF DIMENSION H2 IS TENTATIVE AND COULD CHANGE ONCE SUFFICIENT MANUFACTURING DATA IS AVAILABLE.

	INCH		MILLIMETER			INCH		MILLIMETER	
DIM	MIN	MAX	MIN	MAX	DIM	MIN	MAX	MIN	MAX
AA	1.265	1.275	32.13	32.39	N	1.218	1.242	30.94	31.55
BB	.395	.405	10.03	10.29	R	.365	.375	9.27	9.53
CC	.170	.190	4.32	4.83	S	.365	.375	9.27	9.53
D	.455	.465	11.56	11.81	U	.035	.045	0.89	1.14
E	.062	.066	1.57	1.68	V1	1.320	1.330	33.53	33.78
F	.004	.007	0.10	0.18	W1	.110	.120	2.79	3.05
H1	.082	.090	2.08	2.29	W2	.213	.223	5.41	5.66
H2	.078	.094	1.98	2.39	W3	.243	.253	6.17	6.43
K	.175	.195	4.45	4.95	Y	1.390 BSC		35.31 BSC	
L	.540 BSC		13.72 BSC		Z	R.000	R.040	R0.00	R1.02
M	1.219	1.241	30.96	31.52	aaa	.015		0.38	
					bbb	.010		0.25	
					ccc	.020		0.51	

© NXP SEMICONDUCTORS N.V.
ALL RIGHTS RESERVED

MECHANICAL OUTLINE | PRINT VERSION NOT TO SCALE

TITLE: NI–1230–4LS2L

DOCUMENT NO: 98ASA00513D REV: B

STANDARD: NON–JEDEC

SOT1800–1 08 FEB 2016

PRODUCT DOCUMENTATION

Refer to the following resources to aid your design process.

Application Notes

- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

To Download Resources Specific to a Given Part Number:

1. Go to http://www.nxp.com/RF
2. Search by part number
3. Click part number link
4. Choose the desired resource from the drop down menu

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	Apr. 2016	• Initial Release of Preliminary Data Sheet

How to Reach Us:

Home Page:
freescale.com

Web Support:
freescale.com/support

Information in this document is provided solely to enable system and software implementers to use Freescale products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits based on the information in this document.

Freescale reserves the right to make changes without further notice to any products herein. Freescale makes no warranty, representation, or guarantee regarding the suitability of its products for any particular purpose, nor does Freescale assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. “Typical” parameters that may be provided in Freescale data sheets and/or specifications can and do vary in different applications, and actual performance may vary over time. All operating parameters, including “typicals,” must be validated for each customer application by customer’s technical experts. Freescale does not convey any license under its patent rights nor the rights of others. Freescale sells products pursuant to standard terms and conditions of sale, which can be found at the following address: freescale.com/SalesTermsandConditions.

Freescale and the Freescale logo are trademarks of Freescale Semiconductor, Inc., Reg. U.S. Pat. & Tm. Off. Airfast is a trademark of Freescale Semiconductor, Inc. All other product or service names are the property of their respective owners.
© 2016 Freescale Semiconductor, Inc.

Document Number: MMRF1022HS
Rev. 0, 4/2016