MP86905

Intelli-Phase™ Solution with Integrated HS-/LS-FETs and Driver

The Future of Analog IC Technology

DESCRIPTION

The MP86905 is a monolithic half-bridge with built-in internal power MOSFETs and gate drivers. The MP86905 achieves 50A of continuous output current over a wide input supply range.

The MP86905 is a monolithic IC approach to drive up to 50A of current per-phase. The integration of drivers and MOSFETs results in high efficiency due to optimal dead time and parasitic inductance reduction. The MP86905 can operate with a range from 100kHz to 2MHz.

The MP86905 offers many features to simplify system design. The MP86905 works with controllers with tri-state PWM signal and comes with an accurate current sense to monitor the inductor current and temperature sense to report junction temperature.

The MP86905 is ideal for server applications where efficiency and small size are a premium. The MP86905 is available in a small FC-QFN (4mmx4mm) package.

FEATURES

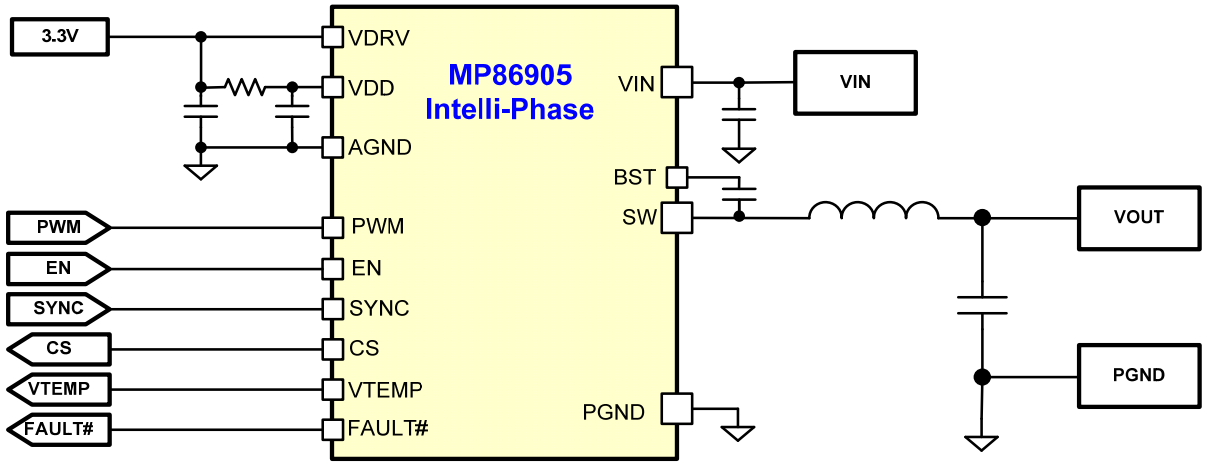
- Wide 4.5V to 16V Operating Input Range
- 50A Output Current
- Current Sense with Accu-Sense™
- Temperature Sense
- Accepts Tri-State PWM Signal
- Current-Limit Protection
- Over-Temperature Protection (OTP)
- Fault Reporting
- Available in an FC-QFN (4mmx4mm) Package

APPLICATIONS

- Server Core Voltage
- Graphic Card Core Regulators
- Power Modules

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TYPICAL APPLICATION



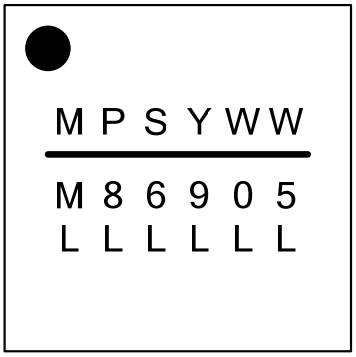
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ORDERING INFORMATION

Part Number	Package	Top Marking
MP86905GR	QFN-23 (4mmx4mm)	*See Below*

* For Tape & Reel, add suffix –Z (e.g. MP86905GR–Z)

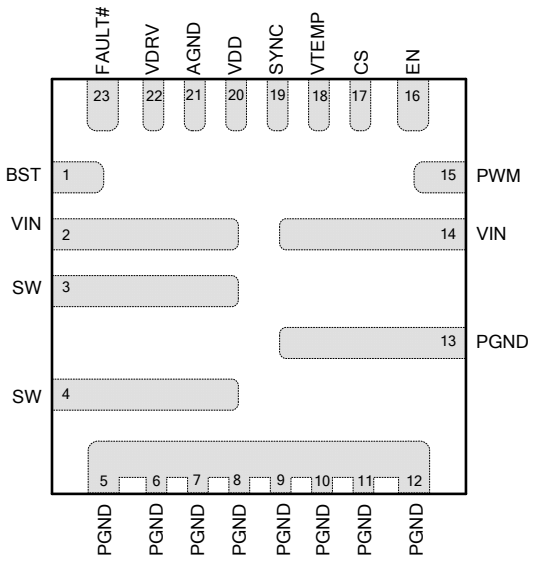
TOP MARKING



MPS: MPS prefix
Y: Year code
WW: Week code
M86905: First six digits of the part number
LLLLLL: Lot number

PACKAGE REFERENCE

TOP VIEW



QFN-23 (4mmx4mm)

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ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (VIN) 18V
V_{SW} (DC) ..... -0.3V to V_{IN} + 0.3V
V_{SW} (25ns) ..... -3V to 25V
V_{IN}-V_{SW} (10ns) ..... -5V to 32V
V_{BST}-V_{SW} (25ns) 5V
V_{BST} ..... V_{SW} + 4V
All other pins ..... -0.3V to VDD + 0.3V
Instantaneous current 90A
Junction temperature ..... 150°C
Lead temperature ..... 260°C
Storage temperature ..... -65°C to +150°C

Recommended Operating Conditions (2)

Supply voltage (VIN) ..... 4.5V to 16V
Driver voltage (VDRV) ..... 3.0V to 3.6V
Logic voltage (VDD) ..... 3.0V to 3.6V
Operating junction temp. (T_J) .... -40°C to +125°C

Thermal Resistance (3)	θ_{JB}	θ_{JC_TOP}	
QFN-23 (4mmx4mm)	2	24	°C/W

NOTES:

1) Exceeding these ratings may damage the device.
2) The device is not guaranteed to function outside of its operating conditions.
3) θ_{JB} is the thermal resistance from the junction to board around the PGND soldering point.
   θ_{JC_TOP} is the themal resistance from the junction to the top of the package.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, VDRV = VDD = EN = 3.3V, T_A = 25°C for typical value and T_J = -40°C to 125°C for max and min values, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
I_{IN} shutdown	$I_{VIN\ Off}$	EN = low			40	μA
VIN under-voltage lockout threshold rising				2.5	3.0	V
VIN under-voltage lockout threshold hysteresis			540	600	660	mV
I_{VDRV} quiescent current		EN = low			15	μA
		PWM = low			80	μA
I_{VDD} quiescent current		EN = low			45	μA
		PWM = low		4	5	mA
VDD voltage UVLO rising				2.8	2.9	V
VDD voltage UVLO hysteresis			120	250	380	mV
VDRV voltage UVLO rising				2.75	2.9	V
VDRV voltage UVLO hysteresis			360	400	440	mV
High-side current limit(4)	I_{LIM_FLT}	Cycle-by-cycle up to four cycles		75		A
Low-side current limit(4)		Negative current limit, cycle-by-cycle, no fault report		-30		A
Negative current limit low-side off time(4)				40		ns
High-side current limit shutdown counter(4)				4		times
EN input low threshold voltage			0.95	1.0	1.05	V
EN input high threshold voltage			1.15	1.2	1.25	V
Dead time rising(4)				3		ns
Dead time falling(4)		Positive inductor current		6		ns
		Negative inductor current		35		ns
SYNC internal pull-down resistor	R_{SYNC}			100		kΩ
SYNC logic high voltage			2			V
SYNC logic low voltage					0.8	V
PWM high-to-SW rising delay(4)	t_{Rising}			15		ns
PWM low-to-SW falling delay(4)	$t_{Falling}$			15		ns
PWM tri-state to SW Hi-Z delay(4)	t_{LT}			40		ns
	t_{TL}			20		ns
	t_{HT}			40		ns
	t_{TH}			20		ns

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ELECTRICAL CHARACTERISTICS *(continued)*

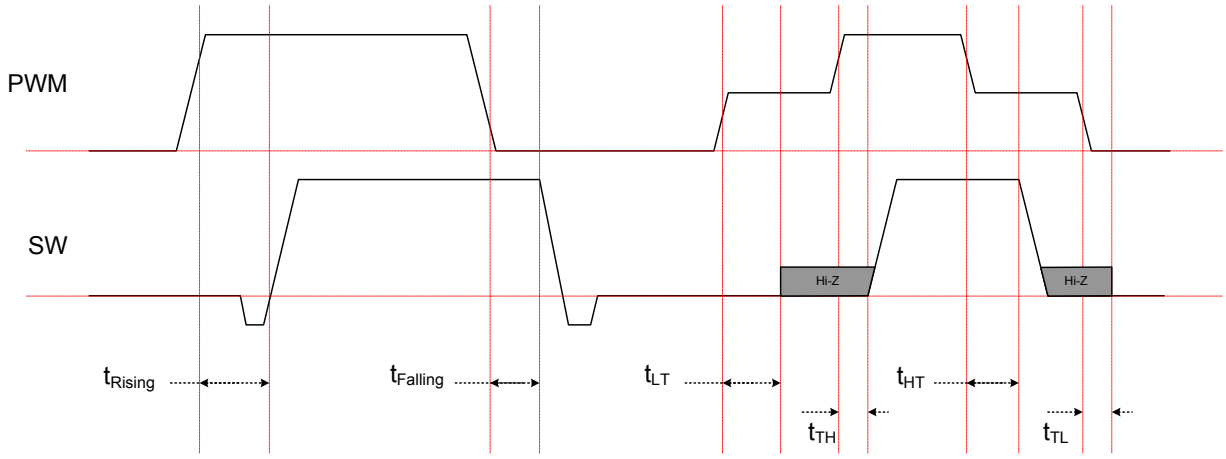
V_{IN} = 12V, VDRV = VDD = EN = 3.3V, T_A = 25°C for typical value and T_J = -40°C to 125°C for max and min values, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Minimum PWM pulse width(4)				20		ns
CS sense gain accuracy		15A ≤ I_{OUT} ≤ 50A	-2	0	2	%
CS sense gain				9.7		μA/A
CS offset		I_{OUT} = 0A	-5		5	μA
CS voltage range(4)	V_{CS}		0.7		2.1	V
VTEMP sense gain(4)				10		mV/°C
VTEMP sense offset(4)		T_J = 25°C		-100		mV
Over-temperature shutdown and fault flag(4)				160		°C
Over-temperature threshold hysteresis(4)				30		°C
PWM input current	I_{PWM}	V_{PWM} = 3.3V, V_{EN} = 3.3V		660		μA
		V_{PWM} = 0V, V_{EN} = 3.3V		-550		μA
PWM logic high voltage			2.35			V
PWM tri-state region			1.10		1.90	V
PWM logic low voltage					0.80	V
FAULT# pull-down		Sink 5mA			0.3	V

NOTE:

4) Guaranteed by design or characterization data, not tested in production.

PWM TIMING DIAGRAM



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PIN FUNCTIONS

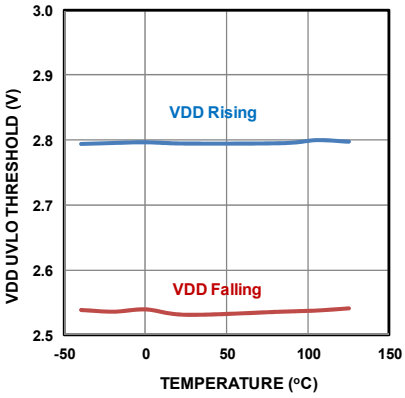
Pin #	Name	Description
1	BST	**Bootstrap.** BST requires a 0.1μF to 1μF capacitor to drive the high-side power switch's gate above the supply voltage. Connect the capacitor between BST and SW to form a floating supply across the power switch driver.
2, 14	VIN	**Supply voltage.** Place C_{IN} close to the device to support the switching current and reduce voltage spikes at input.
3, 4	SW	**Phase node.**
5 - 13	PGND	**Power ground.**
15	PWM	**Pulse width modulation input.** Leave PWM floating or drive PWM to mid-state to enter diode emulation mode.
16	EN	**Enable.** Pull EN low to disable the device and place SW in a high impedance state.
17	CS	**Current sense output.**
18	VTEMP	**Junction temperature sense output.**
19	SYNC	**Diode emulation mode.** Pull SYNC low to enable diode emulation mode.
20	VDD	**Internal circuitry voltage.** Connect VDD to VDRV through a 2.2Ω resistor and decouple with a 1μF capacitor to AGND.
21	AGND	**Analog ground.** Connect AGND to PGND on the VDD capacitor.
22	VDRV	**Driver voltage.** Connect VDRV to a 3.3V supply and decouple with a 1μF to 4.7μF ceramic capacitor close to VDRV to PGND.
23	FAULT#	**Fault report.** FAULT# is an open drain, active low. FAULT# pulls low when SW short detection, HS current limit, or over-temperature is triggered. During a cycle-by-cycle high-side current limit event, FAULT# is kept high until the fourth cycle.

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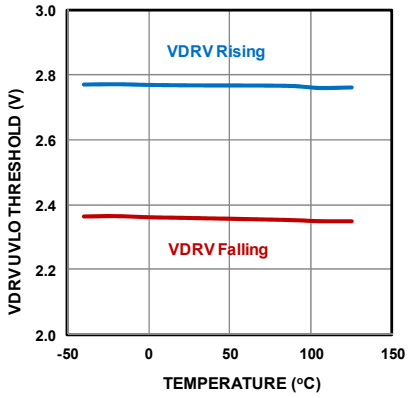
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{DD} = V_{DRV} = 3.3V, T_A = 25˚C, unless otherwise noted.

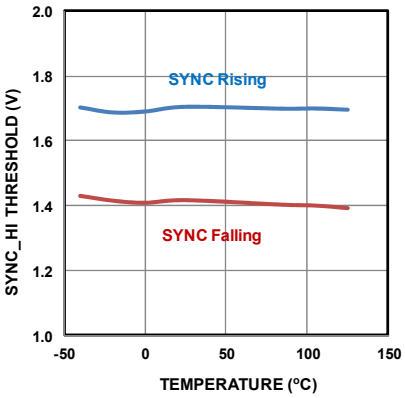
VDD UVLO



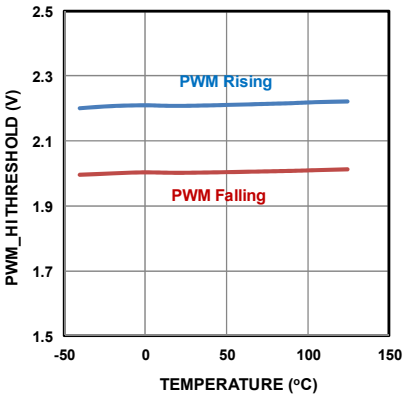
VDRV UVLO



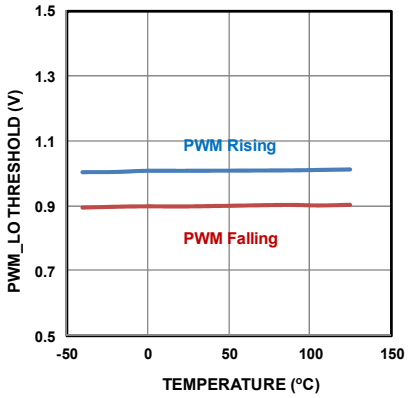
SYNC HI



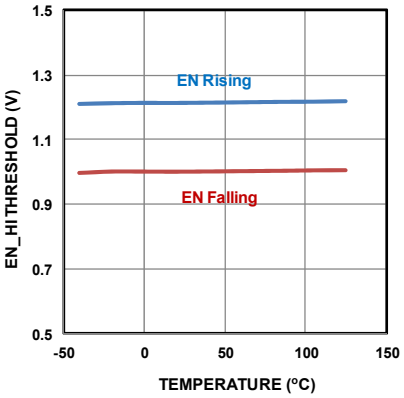
PWM HI



PWM LO

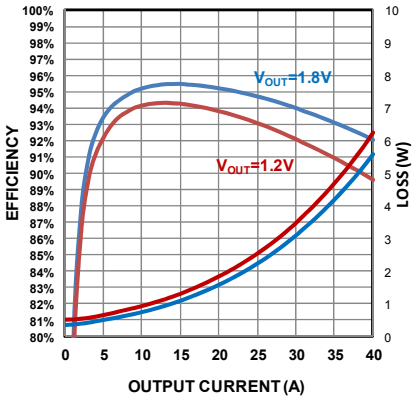


EN HI



DEVICE EFFICIENCY & LOSS

V_{IN}=12V; L=220nH; F_{SW}=500KHz



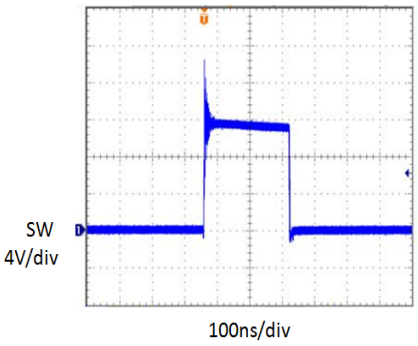
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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

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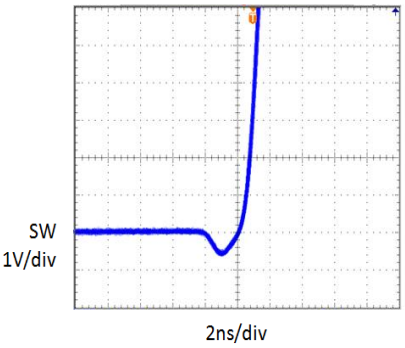
SWITCHING WAVEFORM

V_{IN}=12V; L=150nH; I_{OUT}=20A

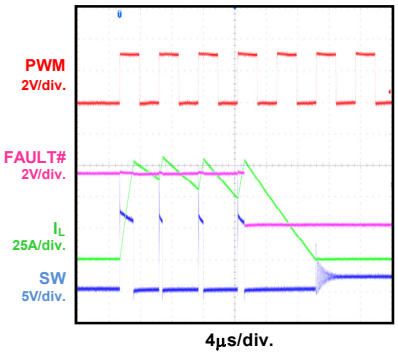


DEAD TIME@ SW RISING

I_{OUT}=20A

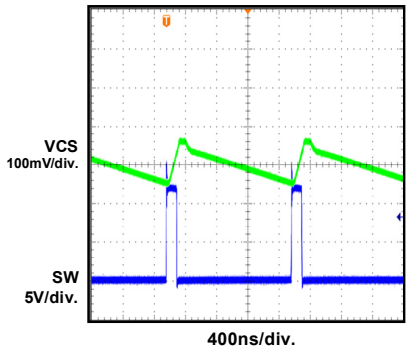


HS CURRENT LIMIT



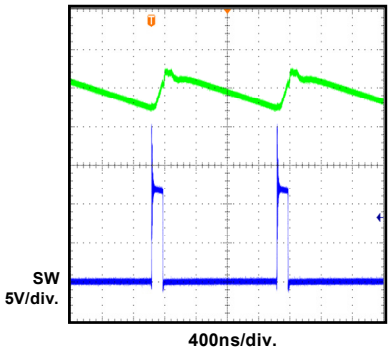
CS OUTPUT WAVEFORM

I_{OUT}=0A



CS OUTPUT WAVEFORM

I_{OUT}=20A



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BLOCK DIAGRAM

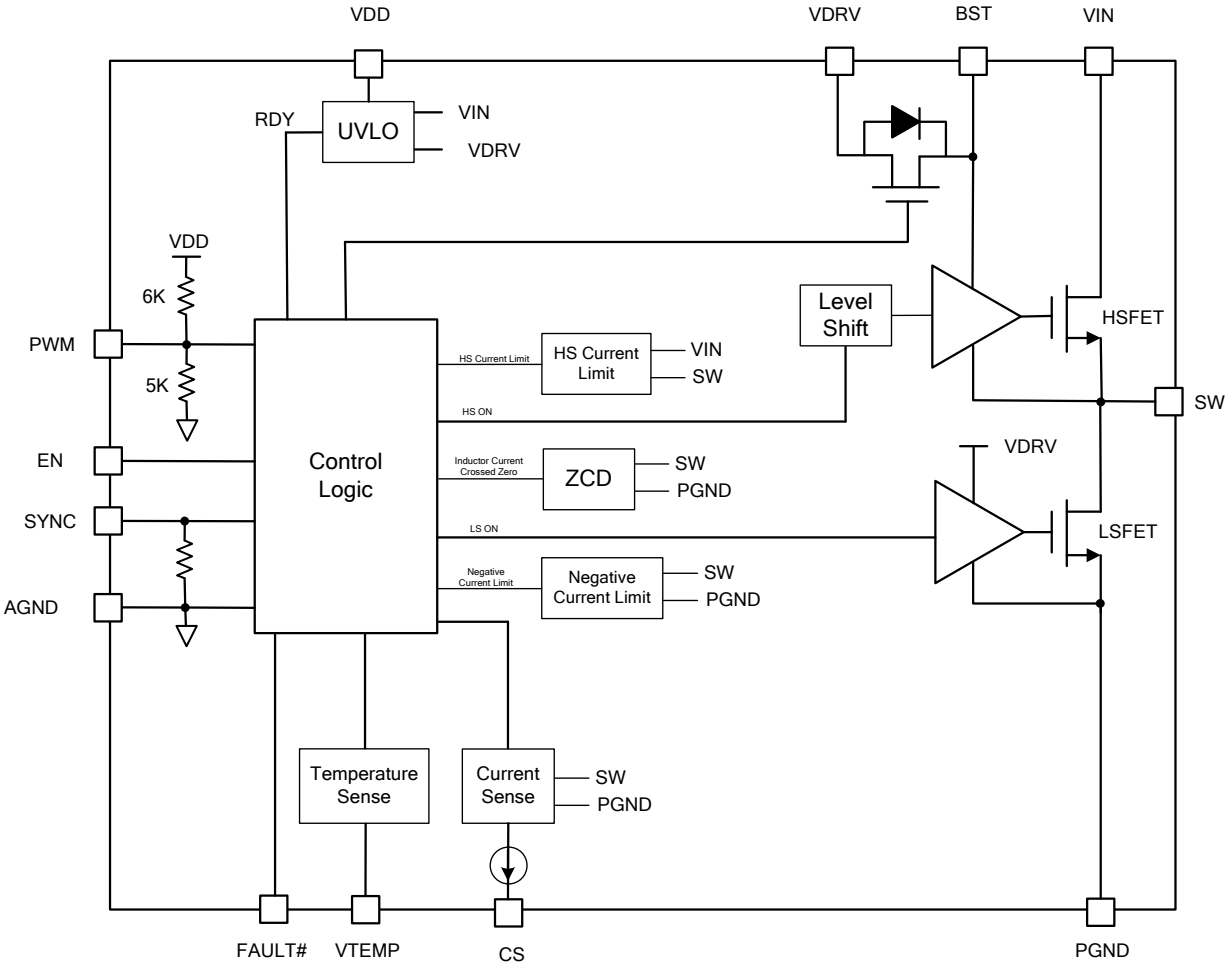


Figure 1: Functional Block Diagram

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APPLICATION INFORMATION

Operation

The MP86905 is a 50A, monolithic, half-bridge driver with integrated MOSFETs and is ideally suited for multi-phase buck regulators.

An external 3.3V supply is required to supply both VDD and VDRV. When EN transitions from low to high, and the VDD and VDRV signals are both sufficiently high, operation begins.

PWM

The PWM input is capable of a tri-state input. When the PWM input signal is within the tri-state threshold window for 50ns (t_{HT} or t_{LT}), the HS-FET is turned off immediately, and the LS-FET enters diode emulation mode, which is on until zero-current detection. The tri-state PWM input can come from a forced middle voltage PWM signal or made by floating the PWM input so the internal current source charges the signal to a middle voltage. Please refer to the PWM timing diagram on page 5 for the propagation delay definition from PWM to the SW node.

Diode Emulation Mode

In diode emulation mode, when PWM is either low or in a tri-state input, the LS-FET is turned on whenever the inductor current is positive. The LS-FET turns off if the inductor current is negative or after the inductor current crosses zero current. Diode emulation mode can be enabled by pulling SYNC low, driving PWM to middle-state, or floating PWM.

Current Sense (CS)

CS is a bi-directional current source proportional to the inductor current. The current sense gain is 9.7μA/A (G_{CS}). Generally, there is a resistor (R_{CS}) connected from CS to an external voltage which is capable of sinking small currents to provide enough of a voltage level shift to meet the CS operating voltage. The CS voltage range of 0.7V to 2.1V is required to keep CS's output current linearly proportional to the inductor current.

A proper reference voltage, V_{CM}, and R_{CS} values can be determined with Equation (1) and Equation (2):

$$0.7V < I_{CS} \times R_{CS} + V_{CM} < 2.1V \quad (1)$$

$$I_{CS} = I_L \times G_{CS} \quad (2)$$

Where V_{CM} is a reference voltage connected to R_{CS}.

Intelli-Phase's current sense output can be used by the controller to accurately monitor the output current. The cycle-by-cycle current information from CS can be used for phase-current balancing, over-current protection, and active voltage positioning (output-voltage droop).

Positive and Negative Inductor Current Limit

When HS-FET over-current is detected for four consecutive cycles, the HS-FET latches off, and FAULT# is asserted low. The LS-FET is turned on until zero-current detection, and then is turned off. Recycling VIN, VDD/VDRV, or toggling EN releases the latch and restarts the device.

When the LS-FET detects a -30A current, the MP86905 turns off the LS-FET for 40ns to limit the negative current. The LS-FET's negative current limit will not trigger a fault report.

Over-Temperature Protection (OTP)

When the junction temperature reaches the over-temperature threshold, the HS-FET is latched off, FAULT# is asserted low, and the LS-FET is turned on until zero-current detection.

Temperature Sense Output (VTEMP)

VTEMP reports the junction temperature. VTEMP is a voltage proportional to the junction temperature. The VTEMP output voltage is 10mV/°C (G_{VTEMP}) with a -100mV offset (VTEMP_Offset) and can be calculated with Equation (3):

$$V_{TEMP} = T_{JUNCTION} \times G_{VTEMP} + VTEMP_Offset \quad (3)$$

For example, if the junction temperature is 100°C, then VTEMP is 0.9V. VTEMP = 0V for junction temperatures below 10°C. In multi-phase operation, VTEMP of every Intelli-Phase can be connected to the temperature monitor pin of the controller (see Figure 2).

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Fault Report (FAULT#)

FAULT# is an open-drain, active-low signal that reports faults from the Intelli-Phase. When any fault occurs, FAULT# is pulled low.

FAULT# monitors three fault events:

1) Over-current limit: To trip the over-current fault, the current limit must be exceeded four consecutive times. Once the fault occurs, the MP86905 latches off to turn off the HS-FET. The LS-FET turns off when the inductor current reaches zero.
2) Over-temperature fault at T_J > 160°C: Once the fault occurs, the MP86905 latches off to turn off the HS-FET. The LS-FET turns off when the inductor current reaches zero.
3) SW to PGND shorted: Once the fault occurs, the part latches off to turn off the HS-FET.

The fault latch can be released by recycling VIN, VDD, or toggling EN.

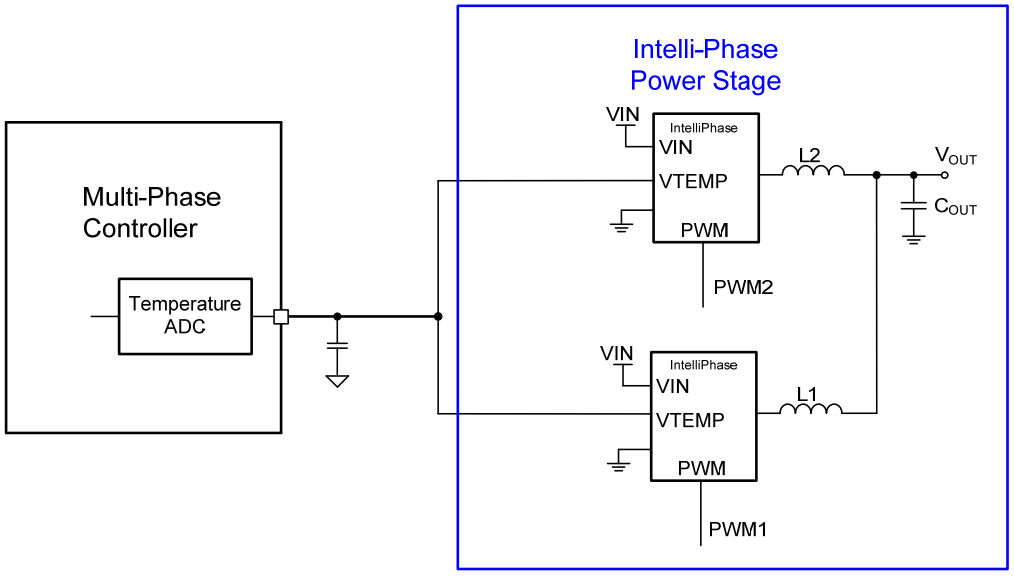


Figure 2: Multi-Phase Temperature Sense Utilization

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PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. For best results, refer to Figure 3 and follow the guidelines below.

1. Place the input MLCC capacitors as close to VIN and PGND as possible.
2. Place the major MLCC capacitors on the same layer as the MP86905.
3. Place as many VIN and PGND vias underneath the package as possible.
4. Place the vias between the VIN or PGND long pads.
5. Place a VIN copper plane on the second inner layer to form the PCB stack as VIN on top, GND on the second layer, and VIN on the third layer to reduce parasitic impedance from the input MLCC cap to the MP86905.
6. Ensure that the copper plane on the inner layer at least covers the VIN vias underneath the package and input MLCC capacitors.
7. Place more PGND vias close to the PGND pin/pad to minimize both parasitic resistance/impedance and thermal resistance.
8. Place a BST capacitor and a VDRV capacitor as close to the MP86905 pins as possible. VDRV and BST capacitors size 0402 are recommended.
9. Use a trace width 20 mils or higher to route the path.
10. Avoid the via for the BST driving path. It is recommended to use a bootstrap capacitor 0.1μF to 1μF in a size 0402 package.
11. Place the VDD decoupling capacitor (size 0402) close to the device.
12. Connect AGND and PGND at the point of the VDD capacitor's ground connection.
13. Keep the CS signal trace away from high current paths like SW and PWM.

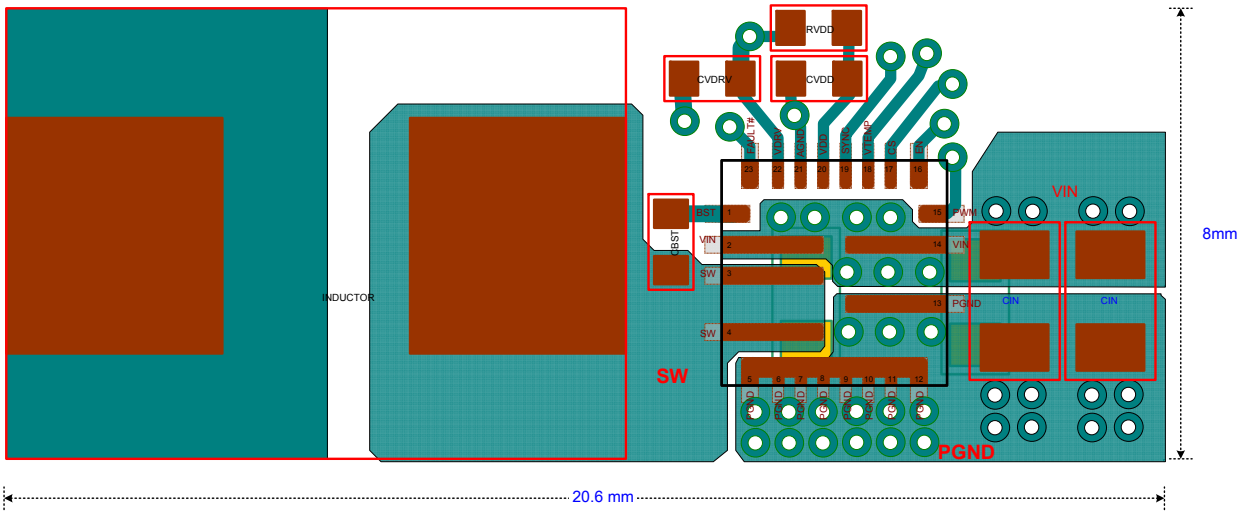


Figure 3: Example of PCB Layout (Placement & Top Layer PCB)

Input Capacitor: 1206 package (top side) and 0805 package (bottom side)

Inductor: 10x8 package

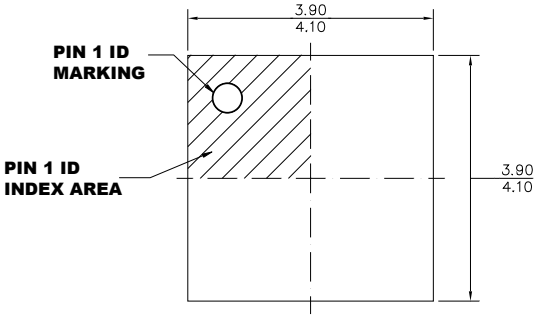
VDD/BST/VDRV capacitor: 0402 package

Via size: 20/10 mils

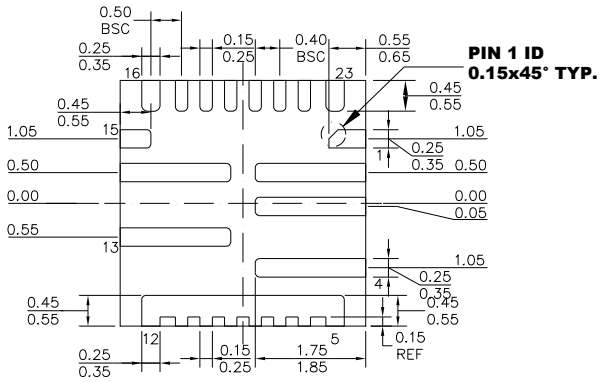
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PACKAGE INFORMATION

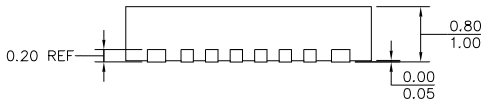
QFN-23 (4mmx4mm)



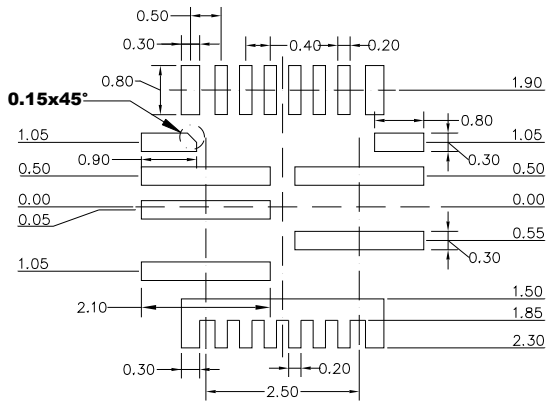
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

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Revision History

Revision #	Revision Date	Description	Pages Updated
1.1	5/21/2020	Correct/add the “Vin-Vsw (10ns) …… -5V to 32V” on absMax rating.	P3

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