ADC084S021 4-Channel, 50 Ksps to 200 Ksps, 8-Bit A/D Converter

1 Features

- Specified Over a Range of Sample Rates
- Four Input Channels
- Variable Power Management
- Single Power Supply With 2.7 V to 5.25 V Range
- DNL: ±0.04 LSB (Typical)
- INL: ±0.04 LSB (Typical)
- SNR: 49.6 dB (Typical)
- Power Consumption:
  - 3-V Supply: 1.6 mW (Typical)
  - 5-V Supply: 5.8 mW (Typical)

2 Applications

- Portable Systems
- Remote Data Acquisition
- Instrumentation and Control Systems

3 Description

The ADC084S021 is a low-power, four-channel CMOS 8-bit analog-to-digital converter with a high-speed serial interface. Unlike the conventional practice of specifying performance at a single sample rate only, the ADC084S021 is fully specified over a sample rate range of 50 ksps to 200 ksps. The converter is based upon a successive-approximation register architecture with an internal track-and-hold circuit. It can be configured to accept up to four input signals at inputs IN1 through IN4.

The output serial data is straight binary, and is compatible with several standards, such as SPI™, QSPI™, MICROWIRE, and many common DSP serial interfaces.

The ADC084S021 operates with a single supply that can range from 2.7 V to 5.25 V. Normal power consumption using a 3-V or 5-V supply is 1.6 mW and 5.8 mW (respectively). The power-down feature reduces the power consumption to just 0.12 µW using a 3-V supply or 0.35 µW using a 5-V supply.

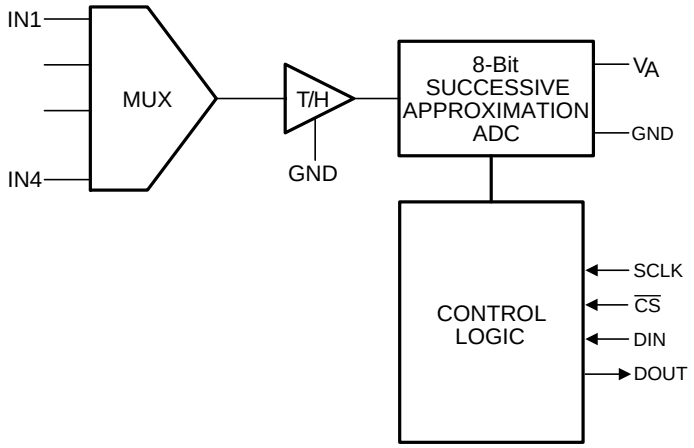
The ADC084S021 comes in a 10-pin VSSOP package. Operation over the industrial temperature range of –40°C to 85°C is ensured.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
ADC084S021	VSSOP (10)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Block Diagram



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (March 2013) to Revision F **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Added Updated values in *Thermal Information* table ... 5

Changes from Revision D (March 2013) to Revision E **Page**

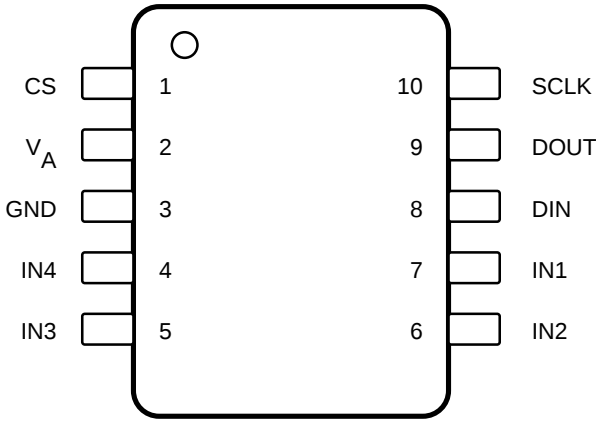
- Changed layout of National Semiconductor Data Sheet to TI format ... 1

5 Device Comparison Table

RESOLUTION	SAMPLE RATE RANGE		
	50 TO 200 KSPS	200 TO 500 KSPS	500 KSPS TO 1 MSPS
12 Bit	ADC124S021	ADC124S051	ADC124S101
10 Bit	ADC104S021	ADC104S051	ADC104S101
8 Bit	*ADC084S021*	ADC084S051	ADC084S101

6 Pin Configuration and Functions

DGK Package
10-Pin VSSOP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	$\overline{CS}$	I	Chip select. A conversion begins at the falling edge of $\overline{CS}$. Conversions continue as long as $\overline{CS}$ is held low.
2	V_A	—	Positive supply pin. This pin must be connected to a quiet 2.7-V to 5.25-V source and be bypassed to GND with a 0.1-µF monolithic capacitor located within 1 cm of the power pin and with a 1-µF capacitor.
3	GND	—	Device ground return for all signals.
4, 5, 6, 7	IN1 to IN4	I	Analog inputs. These signals can range from 0 V to V_A.
8	DIN	I	Digital data input. The ADC084S021's control register is loaded through this pin on rising edges of SCLK.
9	DOUT	O	Digital data output. The output samples are clocked out at this pin on falling edges of the SCLK pin.
10	SCLK	I	Digital clock input. This clock directly controls the conversion and readout processes.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)(3)

	MIN	MAX	UNIT
Supply voltage, V_A	–0.3	6.5	V
Voltage on any pin to GND	–0.3	V_A + 0.3	V
Input current at any pin(4)		±10	mA
Package input current(4)		±20	mA
Power consumption at T_A = 25°C	See (5)		
Junction temperature, T_J		150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are measured with respect to GND = 0 V (unless otherwise specified).
(3) If Military/Aerospace specified devices are required, contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(4) When the input voltage at any pin exceeds the power supply (that is, V_{IN} < GND or V_{IN} > V_A), the current at that pin must be limited to 10 mA. The 20-mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 10 mA to two. The *Absolute Maximum Ratings* does not apply to the V_A pin. The current into the V_A pin is limited by the analog supply voltage specification.
(5) The absolute maximum junction temperature ($T_J$max) for this device is 150°C. The maximum allowable power dissipation is dictated by $T_J$max, the junction-to-ambient thermal resistance ($R_{\theta JA}$), and the ambient temperature (T_A), and can be calculated using the formula P_DMAX = ($T_J$max − T_A) / $R_{\theta JA}$. The values for maximum power dissipation listed above is reached only when the device is operated in a severe fault condition (that is, when input or output pins are driven beyond the power supply voltages, or the power supply polarity is reversed). Such conditions must always be avoided.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)(2)	±2500	V
		Machine model (MM)(3)	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) Human-body model is 100-pF capacitor discharged through a 1.5-kΩ resistor.
(3) Machine model is 220-pF discharged through 0 Ω.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)(2)

		MIN	NOM	MAX	UNIT
V_A	Supply voltage	2.7		5.25	V
	Digital input voltage	–0.3		V_A	V
	Analog input voltage	0		V_A	V
	Clock frequency	0.8		3.2	MHz
T_A	Operating temperature	–40		85	°C

(1) *Recommended Operating Ratings* indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the *Electrical Characteristics*. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(2) All voltages are measured with respect to GND = 0 V (unless otherwise specified).

7.4 Thermal Information

THERMAL METRIC[1][2]		ADC084S021 DGK (VSSOP) 10 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	190	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	61.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	90	°C/W
ψ_{JT}	Junction-to-top characterization parameter	7.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	88.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) Reflow temperature profiles are different for lead-free and non-lead-free packages.

7.5 Electrical Characteristics

V_A = 2.7 V to 5.25 V, GND = 0 V, f_{SCLK} = 0.8 MHz to 3.2 MHz, f_{SAMPLE} = 50 ksps to 200 ksps, C_L = 50 pF, and T_A = 25°C (unless otherwise noted)[1]

PARAMETER		TEST CONDITIONS	MIN[2]	TYP	MAX[2]	UNIT
STATIC CONVERTER CHARACTERISTICS						
	Resolution with no missing codes				8	Bits
INL	Integral non-linearity			±0.04	±0.2	LSB
DNL	Differential non-linearity			±0.04	±0.2	LSB
V_{OFF}	Offset error			0.52	±0.7	LSB
OEM	Channel-to-channel offset error match			±0.01	±0.3	LSB
FSE	Full-scale error			0.51	±0.7	LSB
FSEM	Channel-to-channel full-scale error match			0.01	±0.3	LSB
DYNAMIC CONVERTER CHARACTERISTICS						
SINAD	Signal-to-noise plus distortion ratio	V_A = 2.7 V to 5.25 V f_{IN} = 39.9 kHz, –0.02 dBFS	49.1	49.6		dB
SNR	Signal-to-noise ratio	V_A = 2.7 V to 5.25 V f_{IN} = 39.9 kHz, –0.02 dBFS	49.2	49.6		dB
THD	Total harmonic distortion	V_A = 2.7 V to 5.25 V f_{IN} = 39.9 kHz, –0.02 dBFS		−76	−62	dB
SFDR	Spurious-free dynamic range	V_A = 2.7 V to 5.25 V f_{IN} = 39.9 kHz, −0.02 dBFS	63	68		dB
ENOB	Effective number of bits	V_A = 2.7 V to 5.25 V f_{IN} = 39.9 kHz, –0.02 dBFS		7.9		Bits
	Channel-to-channel crosstalk	V_A = 5.25 V f_{IN} = 39.9 kHz		−73		dB
IMD	Intermodulation distortion, second order terms	V_A = 5.25 V f_a = 40.161 kHz, f_b = 41.015 kHz		−78		dB
	Intermodulation distortion, third order terms	V_A = 5.25 V f_a = 40.161 kHz, f_b = 41.015 kHz		−73		
FPBW	Full power bandwidth, –3 dB	V_A = 5 V		11		MHz
		V_A = 3 V		8		
ANALOG INPUT CHARACTERISTICS						
V_{IN}	Input range			0 to V_A		V
I_{DCL}	DC leakage current				±1	µA
C_{INA}	Input capacitance	Track mode		33		pF
		Hold mode		3		

(1) Tested limits are specified to TI's AOQL (Average Outgoing Quality Level).
(2) Minimum and maximum specification limits are specified by design, test, or statistical analysis.

Electrical Characteristics (continued)

V_A = 2.7 V to 5.25 V, GND = 0 V, f_{SCLK} = 0.8 MHz to 3.2 MHz, f_{SAMPLE} = 50 ksps to 200 ksps, C_L = 50 pF, and T_A = 25°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN(2)	TYP	MAX(2)	UNIT
DIGITAL INPUT CHARACTERISTICS						
V_{IH}	Input high voltage	V_A = 5.25 V	2.4			V
		V_A = 3.6 V	2.1			
V_{IL}	Input low voltage				0.8	V
I_{IN}	Input current	V_{IN} = 0 V or V_A			±10	µA
C_{IND}	Digital input capacitance			2	4	pF
DIGITAL OUTPUT CHARACTERISTICS						
V_{OH}	Output high voltage	I_{SOURCE} = 200 µA	V_A – 0.5	V_A – 0.03		V
		I_{SOURCE} = 1 mA		V_A – 0.1		
V_{OL}	Output low voltage	I_{SINK} = 200 µA		0.03	0.4	V
		I_{SINK} = 1 mA		0.1		
I_{OZH}, I_{OZL}	TRI-STATE® leakage current				±1	µA
C_{OUT}	TRI-STATE® output capacitance			2	4	pF
	Output coding		Straight (natural) binary			
POWER SUPPLY CHARACTERISTICS (C_L = 10 pF)						
V_A	Supply voltage		2.7		5.25	V
I_A	Supply current, normal mode (operational, $\overline{CS}$ low)	V_A = 5.25 V, f_{SAMPLE} = 200 ksps, f_{IN} = 40 kHz		1.1	1.7	mA
		V_A = 3.6 V, f_{SAMPLE} = 200 ksps, f_{IN} = 40 kHz		0.45	0.8	
	Supply current, shutdown ($\overline{CS}$ high)	V_A = 5.25 V, f_{SAMPLE} = 0 ksps		200		nA
		V_A = 3.6 V, f_{SAMPLE} = 0 ksps		200		
P_D	Power consumption, normal mode (operational, $\overline{CS}$ low)	V_A = 5.25 V		5.8	8.9	mW
		V_A = 3.6 V		1.6	2.9	
	Power consumption, shutdown ($\overline{CS}$ high)	V_A = 5.25 V		1.05		µW
		V_A = 3.6 V		0.72		
AC ELECTRICAL CHARACTERISTICS						
f_{SCLK}	Clock frequency	(3)	0.8		3.2	MHz
f_S	Sample rate	(3)	50		200	ksps
t_{CONV}	Conversion time				13	SCLK cycles
DC	SCLK duty cycle	f_{SCLK} = 3.2 MHz	30%	50%	70%	
t_{ACQ}	Track or hold acquisition time	Full-scale step input			3	SCLK cycles
	Throughput time	Acquisition time + conversion time			16	SCLK cycles

(3) This is the frequency range over which the electrical performance is ensured. The device is functional over a wider range which is specified in *Recommended Operating Conditions*.

7.6 Timing Requirements

V_A = 2.7 V to 5.25 V, GND = 0 V, f_{SCLK} = 0.8 MHz to 3.2 MHz, f_{SAMPLE} = 50 ksps to 200 ksps, C_L = 50 pF, and T_A = 25°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		MIN	NOM	MAX	UNIT
t_{CSU}	Setup time SCLK high to $\overline{CS}$ falling edge(2)	V_A = 3 V		10			ns
		V_A = 5 V		10	–0.5		
t_{CLH}	Hold time SCLK low to $\overline{CS}$ falling edge(2)	V_A = 3 V		10	4.5		ns
		V_A = 5 V		10	1.5		
t_{EN}	Delay from $\overline{CS}$ until DOUT active	V_A = 3 V			4	30	ns
		V_A = 5 V			2	30	
t_{ACC}	Data access time after SCLK falling edge	V_A = 3 V			16.5	30	ns
		V_A = 5 V			15	30	
t_{SU}	Data setup time prior to SCLK rising edge			10	3		ns
t_H	Data valid SCLK hold time			10	3		ns
t_{CH}	SCLK high pulse width			0.3 × t_{SCLK}	0.5 × t_{SCLK}		ns
t_{CL}	SCLK low pulse width			0.3 × t_{SCLK}	0.5 × t_{SCLK}		ns
t_{DIS}	$\overline{CS}$ rising edge to DOUT high-impedance	Output falling	V_A = 3 V		1.7	20	ns
			V_A = 5 V		1.2	20	
		Output rising	V_A = 3 V		1	20	
			V_A = 5 V		1	20	

(1) Tested limits are specified to TI's AOQL (Average Outgoing Quality Level).
(2) Clock may be either high or low when $\overline{CS}$ is asserted as long as setup and hold times t_{CSU} and t_{CLH} are strictly observed.

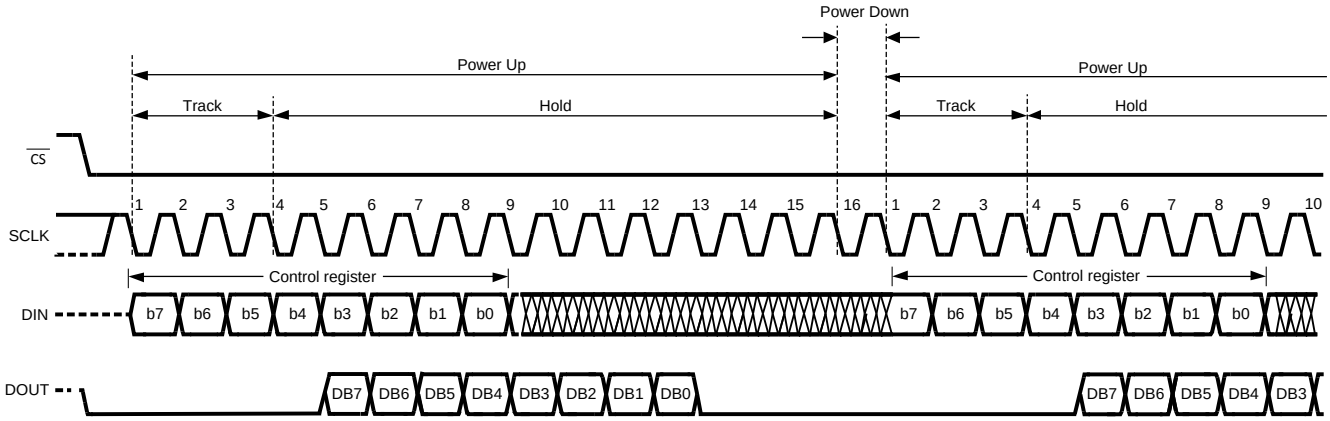


Figure 1. Operational Timing Diagram

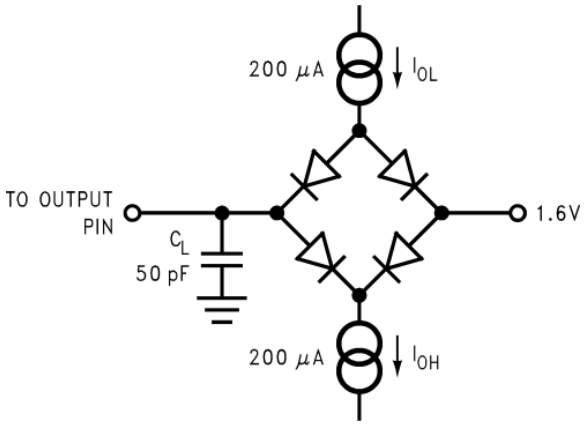


Figure 2. Timing Test Circuit

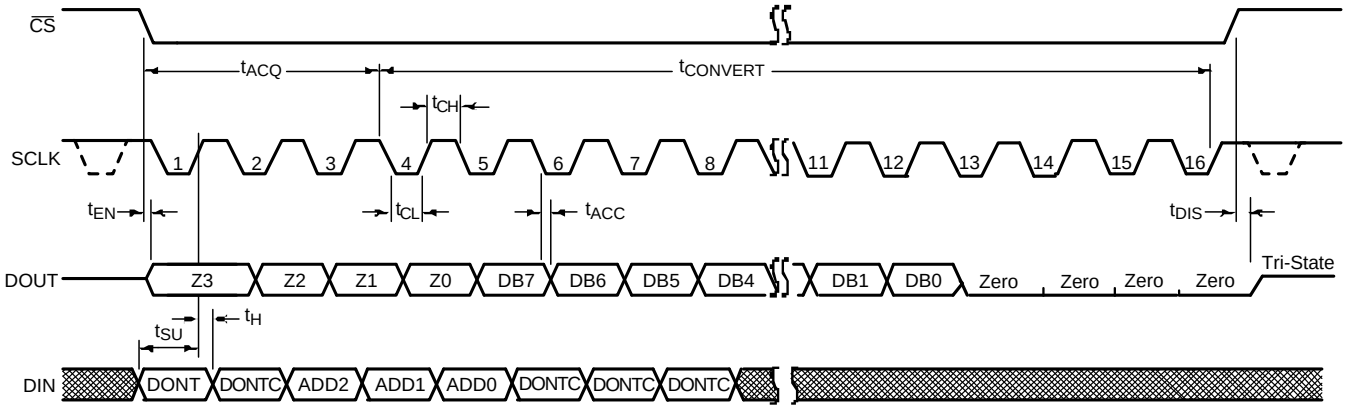


Figure 3. Serial Timing Diagram

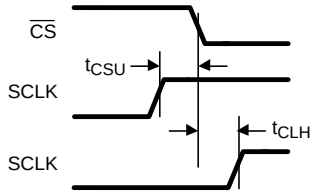


Figure 4. SCLK and $\overline{CS}$ Timing Parameters

7.7 Typical Characteristics

T_A = 25°C, f_{SAMPLE} = 50 ksps to 200 ksps, f_{SCLK} = 0.8 MHz to 3.2 MHz, and f_{IN} = 39.9 kHz (unless otherwise noted)

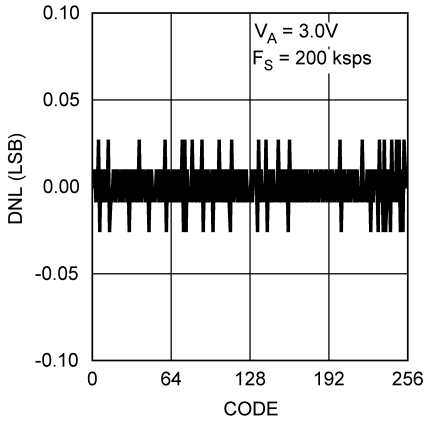


Figure 5. DNL – V_A = 3 V

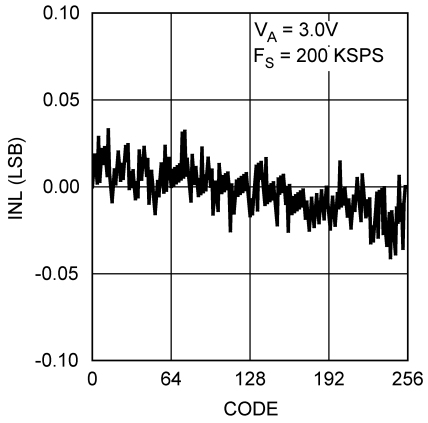


Figure 6. INL – V_A = 3 V

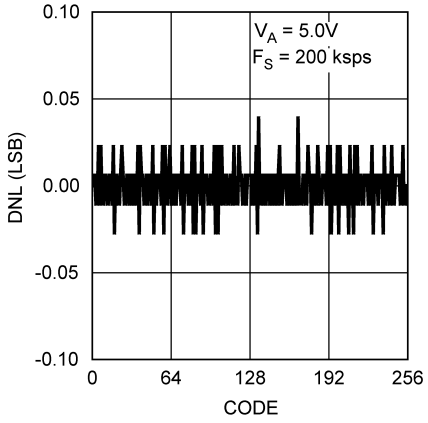


Figure 7. DNL – V_A = 5 V

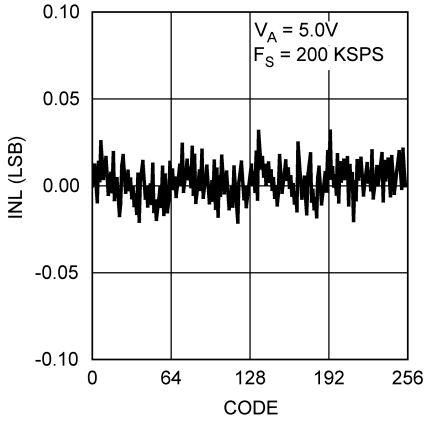


Figure 8. INL – V_A = 5 V

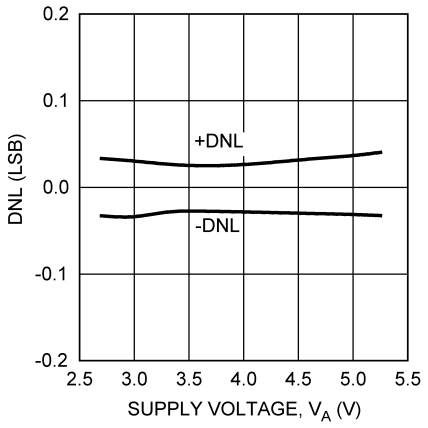


Figure 9. DNL vs Supply

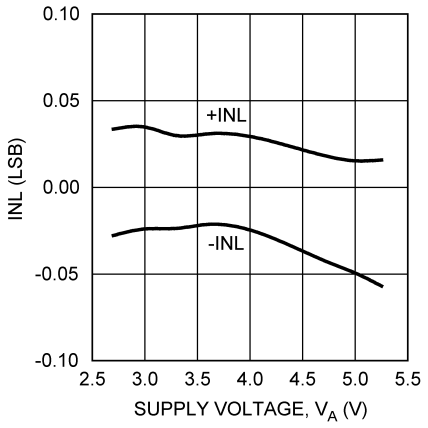


Figure 10. INL vs Supply

Typical Characteristics (continued)

T_A = 25°C, f_{SAMPLE} = 50 ksps to 200 ksps, f_{SCLK} = 0.8 MHz to 3.2 MHz, and f_{IN} = 39.9 kHz (unless otherwise noted)

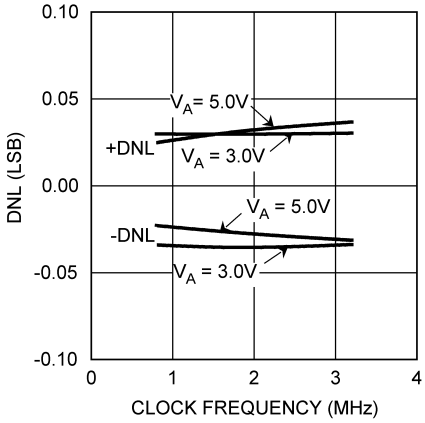


Figure 11. DNL vs Clock Frequency

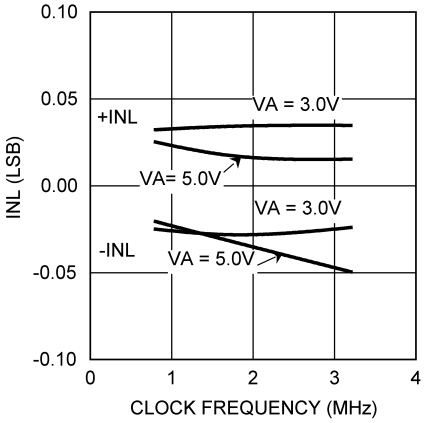


Figure 12. INL vs Clock Frequency

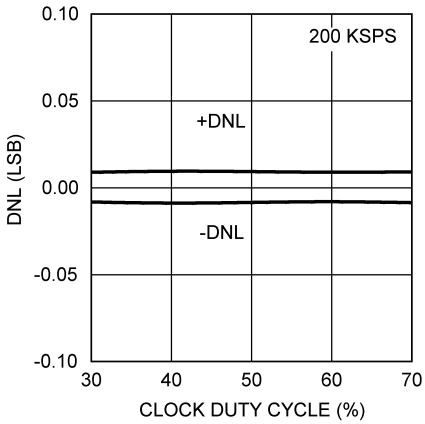


Figure 13. DNL vs Clock Duty Cycle

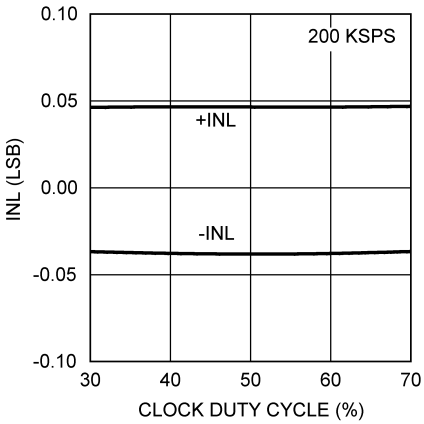


Figure 14. INL vs Clock Duty Cycle

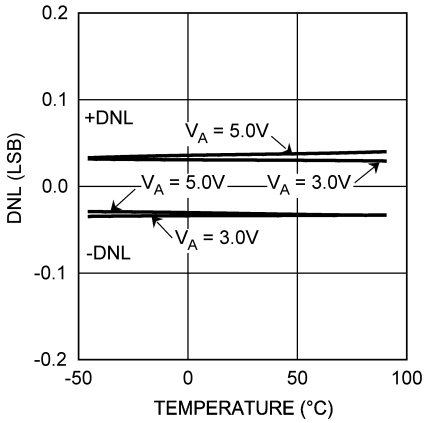


Figure 15. DNL vs Temperature

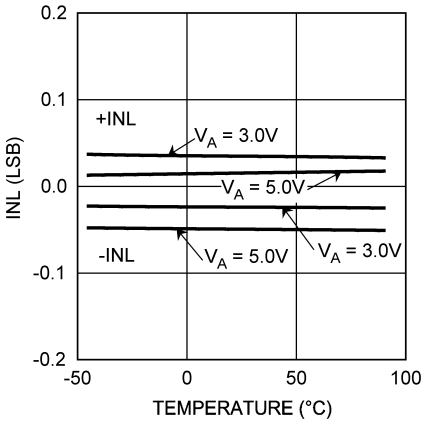


Figure 16. INL vs Temperature

Typical Characteristics (continued)

T_A = 25°C, f_{SAMPLE} = 50 ksps to 200 ksps, f_{SCLK} = 0.8 MHz to 3.2 MHz, and f_{IN} = 39.9 kHz (unless otherwise noted)

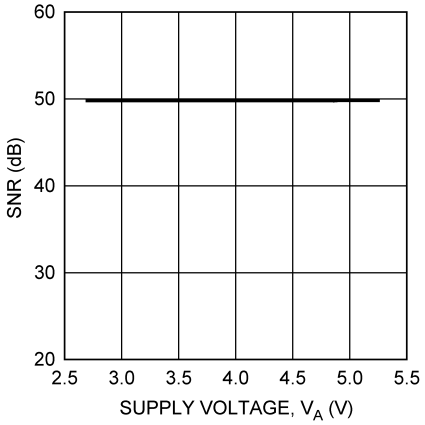


Figure 17. SNR vs Supply

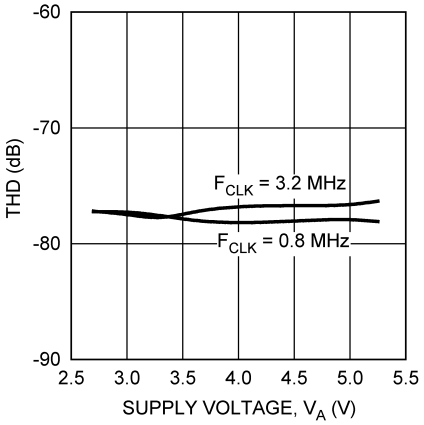


Figure 18. THD vs Supply

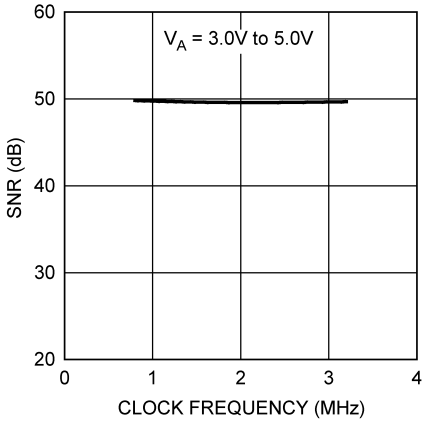


Figure 19. SNR vs Clock Frequency

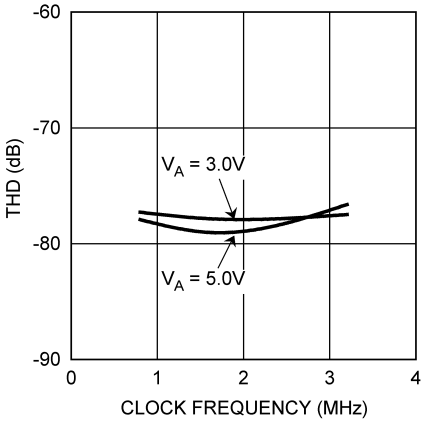


Figure 20. THD vs Clock Frequency

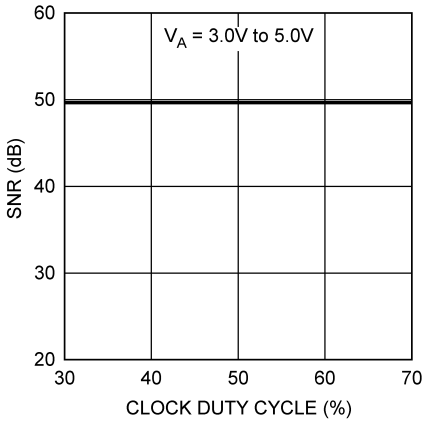


Figure 21. SNR vs Clock Duty Cycle

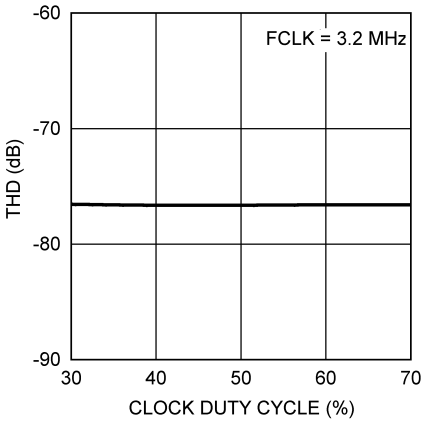


Figure 22. THD vs Clock Duty Cycle

Typical Characteristics (continued)

T_A = 25°C, f_{SAMPLE} = 50 ksps to 200 ksps, f_{SCLK} = 0.8 MHz to 3.2 MHz, and f_{IN} = 39.9 kHz (unless otherwise noted)

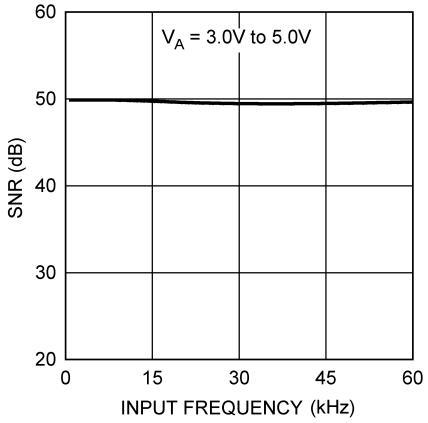


Figure 23. SNR vs Input Frequency

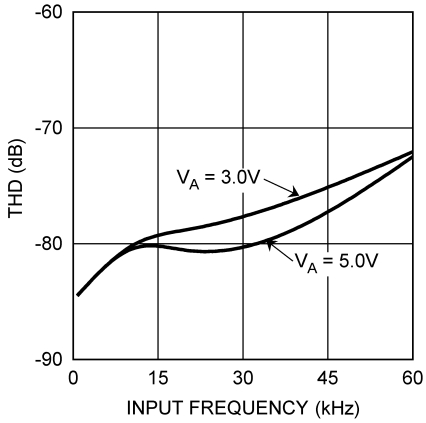


Figure 24. THD vs Input Frequency

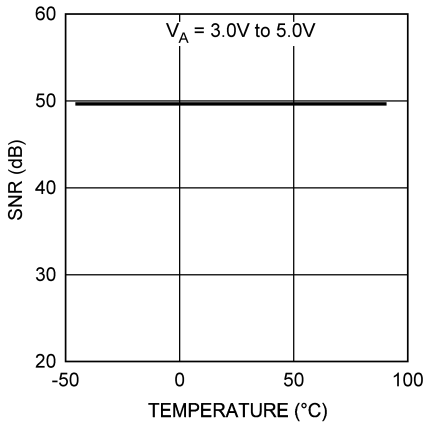


Figure 25. SNR vs Temperature

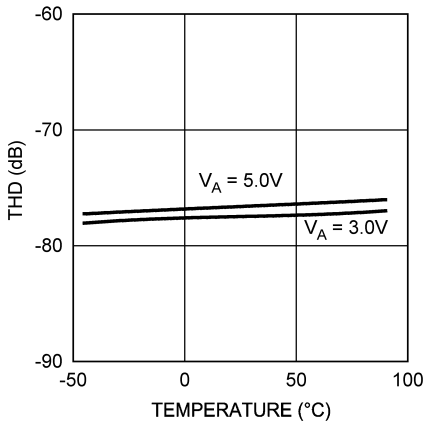


Figure 26. THD vs Temperature

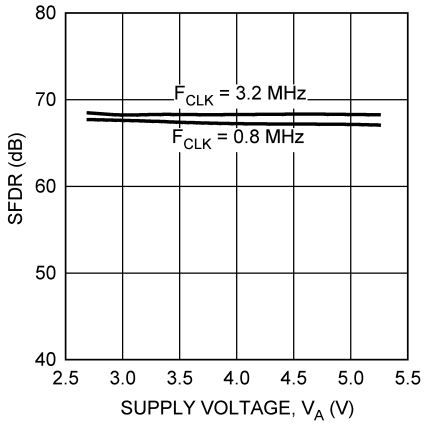


Figure 27. SFDR vs Supply

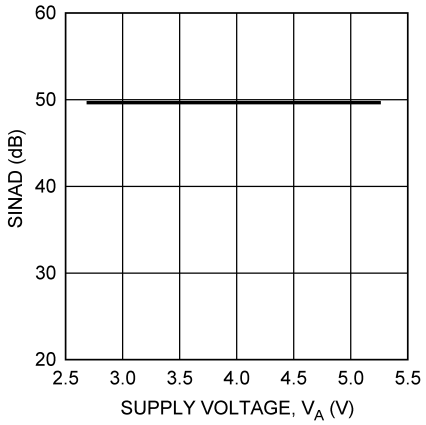


Figure 28. SINAD vs Supply

Typical Characteristics (continued)

T_A = 25°C, f_{SAMPLE} = 50 ksps to 200 ksps, f_{SCLK} = 0.8 MHz to 3.2 MHz, and f_{IN} = 39.9 kHz (unless otherwise noted)

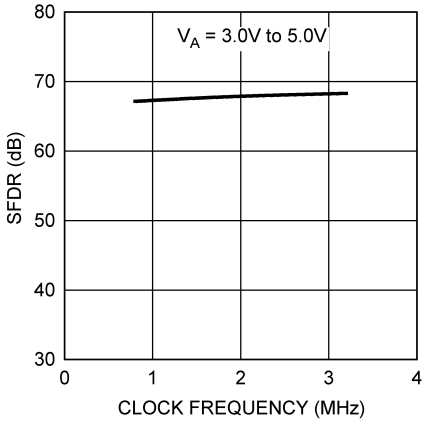


Figure 29. SFDR vs Clock Frequency

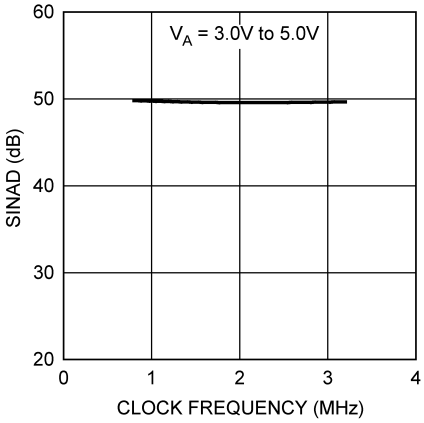


Figure 30. SINAD vs Clock Frequency

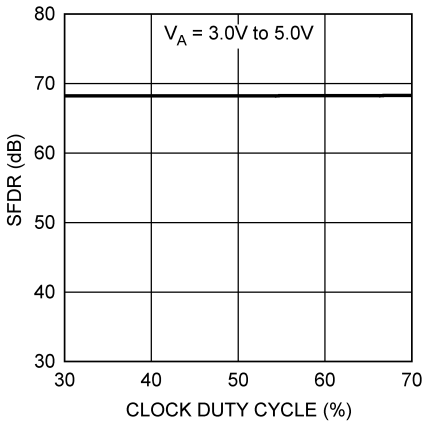


Figure 31. SFDR vs Clock Duty Cycle

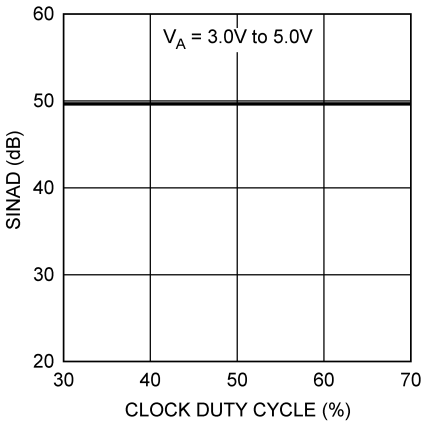


Figure 32. SINAD vs Clock Duty Cycle

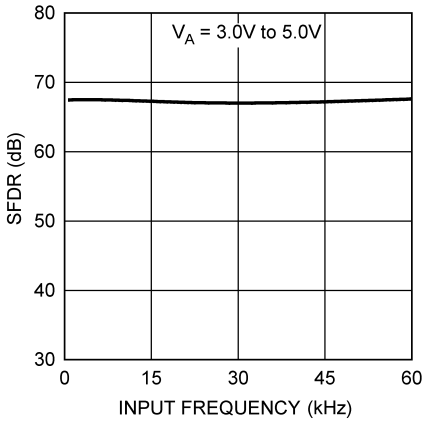


Figure 33. SFDR vs Input Frequency

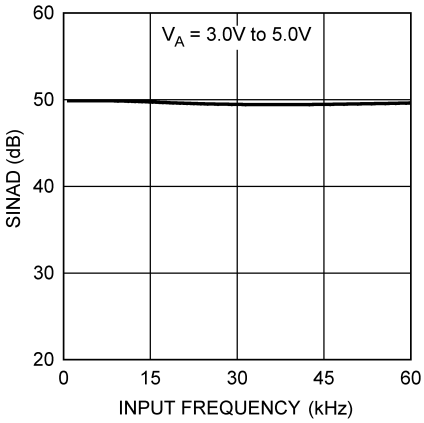


Figure 34. SINAD vs Input Frequency

Typical Characteristics (continued)

T_A = 25°C, f_{SAMPLE} = 50 ksps to 200 ksps, f_{SCLK} = 0.8 MHz to 3.2 MHz, and f_{IN} = 39.9 kHz (unless otherwise noted)

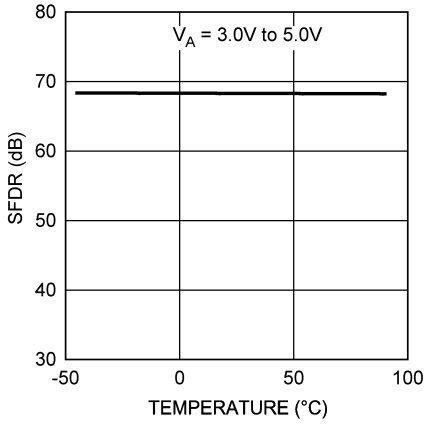


Figure 35. SFDR vs Temperature

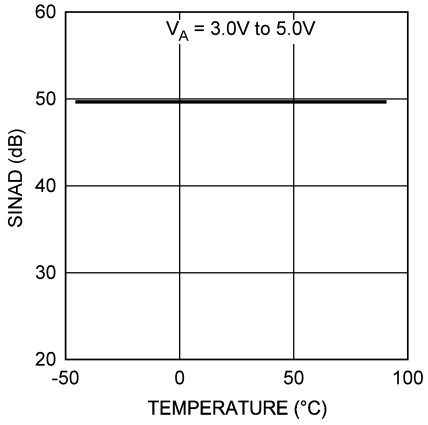


Figure 36. SINAD vs Temperature

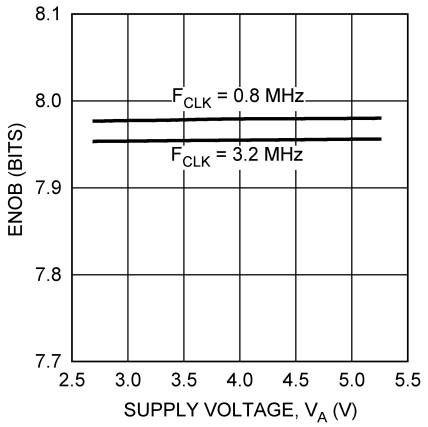


Figure 37. ENOB vs Supply

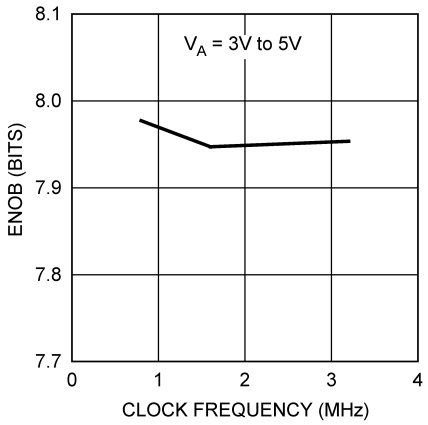


Figure 38. ENOB vs Clock Frequency

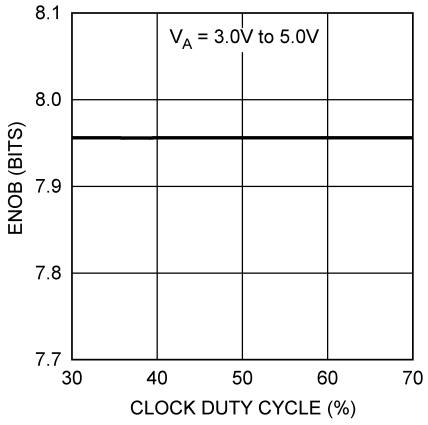


Figure 39. ENOB vs Clock Duty Cycle

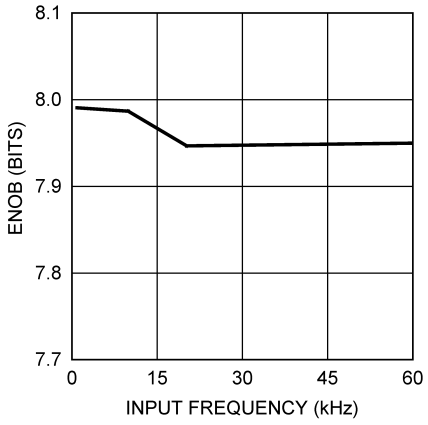


Figure 40. ENOB vs Input Frequency

Typical Characteristics (continued)

T_A = 25°C, f_{SAMPLE} = 50 ksps to 200 ksps, f_{SCLK} = 0.8 MHz to 3.2 MHz, and f_{IN} = 39.9 kHz (unless otherwise noted)

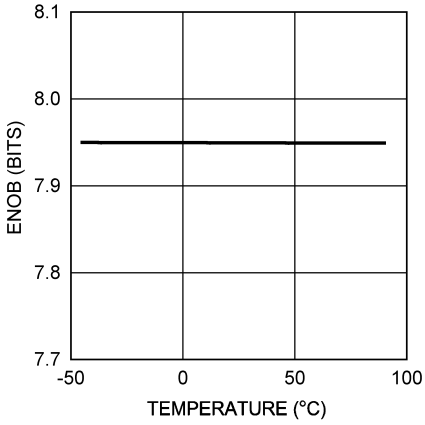


Figure 41. ENOB vs Temperature

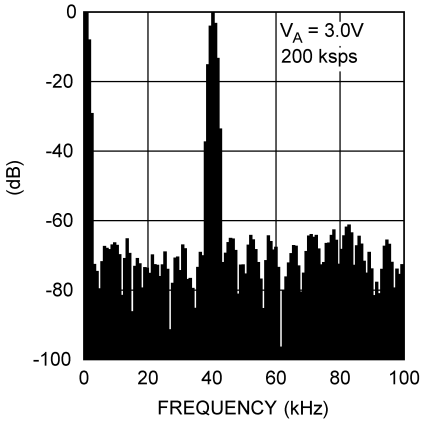


Figure 42. Spectral Response: 3 V, 200 ksps

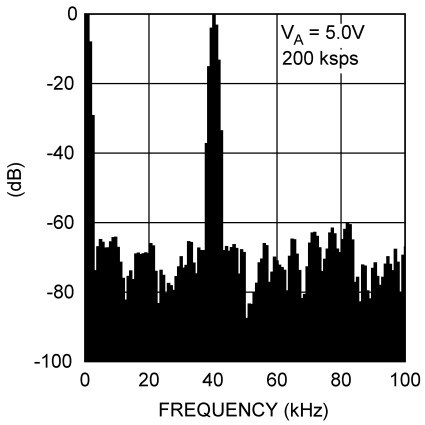


Figure 43. Spectral Response: 5 V, 200 ksps

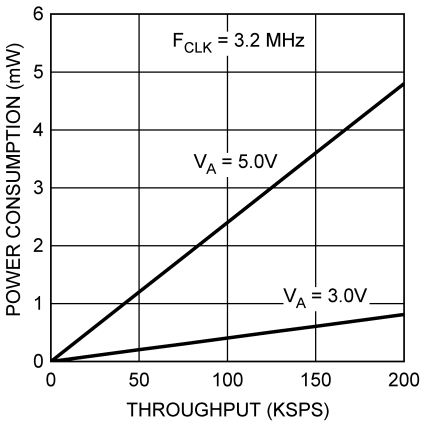


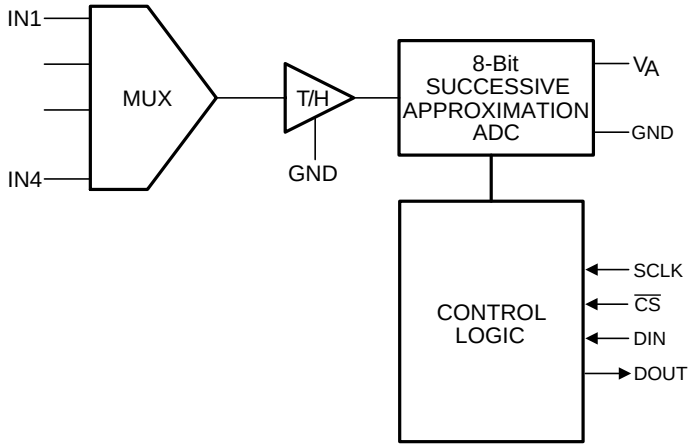
Figure 44. Power Consumption vs Throughput

8 Detailed Description

8.1 Overview

The ADC084S021 is a successive-approximation analog-to-digital converter designed around a charge-redistribution digital-to-analog converter.

8.2 Functional Block Diagram



8.3 Feature Description

Figure 1 and Figure 3 for the ADC084S021 are shown in *Timing Requirements*. $\overline{CS}$ is chip select, which initiates conversions and frames the serial data transfers. SCLK (serial clock) controls both the conversion process and the timing of serial data. DOUT is the serial data output pin, where a conversion result is sent as a serial data stream, MSB first. Data at DIN, the serial data input pin, is written to the control register of the ADC084S021. New data is written to DIN with each conversion.

A serial frame is initiated on the falling edge of $\overline{CS}$ and ends on the rising edge of $\overline{CS}$. Each frame must contain an integer multiple of 16 rising SCLK edges. The ADC output data (DOUT) is in a high impedance state when $\overline{CS}$ is high and is active when $\overline{CS}$ is low. $\overline{CS}$ thus acts as an output enable, in addition to being a start conversion input. Additionally, the device goes into a power-down state when $\overline{CS}$ is high and between continuous conversion cycles.

During the first 3 cycles of SCLK, the ADC is in the track mode, acquiring the input voltage. For the next 13 SCLK cycles the conversion is accomplished and the data is clocked out, MSB first, starting with the 5th clock. If there is more than one conversion in a frame, the ADC re-enters the track mode on the falling edge of SCLK after the N*16th rising edge of SCLK, and re-enter the hold/convert mode at the N*16+4th falling edge of SCLK, where *N* is an integer.

SCLK is internally gated off when $\overline{CS}$ is high. If SCLK is stopped in the low state while $\overline{CS}$ is high, the subsequent fall of $\overline{CS}$ generates a falling edge of the internal version of SCLK, putting the ADC into the track mode. This is seen by the ADC as the first falling edge of SCLK. If SCLK is stopped with SCLK high, the ADC enters the track mode at the first falling edge of SCLK after the falling edge of $\overline{CS}$.

During each conversion, data is clocked into the device at the DIN pin on the first 8 rising edges of SCLK after the fall of $\overline{CS}$. For each conversion, it is necessary to clock in the data indicating the input that is selected for the conversion after the current one. That is, the conversion that is started at the fall of $\overline{CS}$ is of the voltage at the channel that was selected when the last conversion was started. The first conversion after power up is of the first channel. See Table 1 and Table 3.

If $\overline{CS}$ and SCLK go low within the times defined by t_{CSU} and t_{CLH}, the rising edge of SCLK that begins clocking data in at DIN may be one clock cycle later than expected. It is, therefore, best to strictly observe the minimum t_{CSU} and t_{CLH} times given in *Timing Requirements*.

Feature Description (continued)

There are no power-up delays or dummy conversions required with the ADC084S021. The ADC is able to sample and convert an input to full conversion immediately following power up. The first conversion result after power up is that of IN1.

8.3.1 Transfer Function

The output format of the ADC084S021 is straight binary. Code transitions occur midway between successive integer LSB values. The LSB width for the ADC084S021 is V_A / 256, and Figure 45 shows the ideal transfer characteristic. The transition from an output code of 0000 0000 to a code of 0000 0001 is at 1/2 LSB, or a voltage of V_A / 512. Other code transitions occur at steps of one LSB.

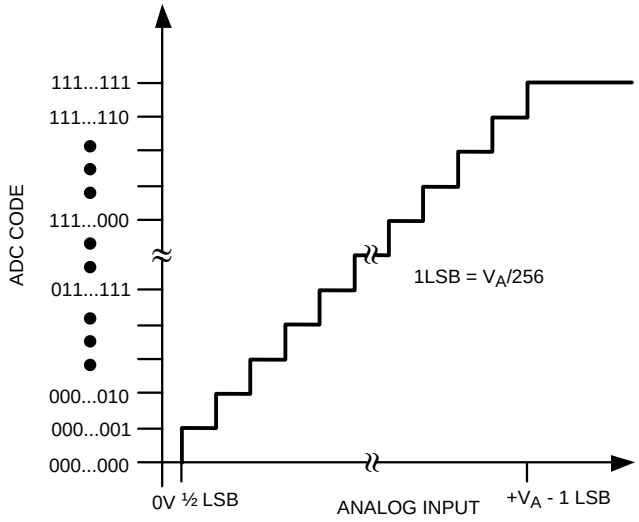


Figure 45. Ideal Transfer Characteristic

8.3.2 Analog Inputs

Figure 46 shows an equivalent circuit for one of the ADC084S021's input channels. Diodes D1 and D2 provide ESD protection for the analog inputs. At no time must any input go beyond (V_A + 300 mV) or (GND − 300 mV), as these ESD diodes begin conducting, which could result in erratic operation. For this reason, these ESD diodes must not be used to clamp the input signal.

The capacitor C1 in Figure 46 has a typical value of 3 pF, and is mainly the package pin capacitance. Resistor R1 is the on resistance of the multiplexer and track or hold switch, which is typically 500 Ω. Capacitor C2 is the ADC084S021 sampling capacitor, which is typically 30 pF. The ADC084S021 delivers the best performance when driven by a low-impedance source to eliminate distortion caused by the charging of the sampling capacitance. This is especially important when using the ADC084S021 to sample AC signals. Also important when sampling dynamic signals is a band-pass or low-pass filter to reduce harmonics and noise, improving dynamic performance.

Feature Description (continued)

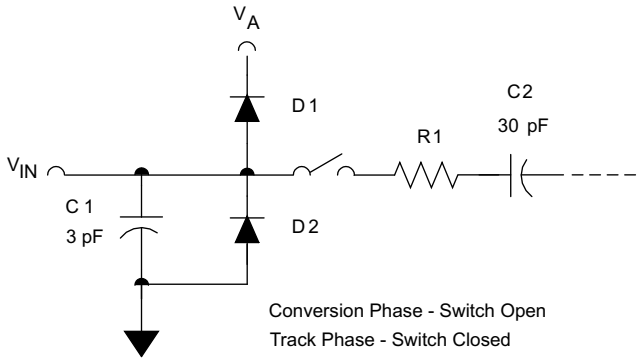


Figure 46. Equivalent Input Circuit

8.3.3 Digital Inputs and Outputs

The digital output of the ADC084S021, DOUT, is limited by and cannot exceed the supply voltage, V_A. The digital input pins are not prone to latch-up and, and although not recommended, SCLK, $\overline{CS}$, and DIN may be asserted before V_A without any latch-up risk.

8.4 Device Functional Modes

The ADC084S021 has two primary modes of operation necessary for capturing an analog signal: track mode and hold mode. Simplified schematics of the ADC084S021 in both track and hold modes are shown in Figure 47 and Figure 48, respectively.

8.4.1 Track Mode

Figure 47 shows the ADC084S021 in track mode: switch SW1 connects the sampling capacitor to one of four analog input channels through the multiplexer, and SW2 balances the comparator inputs. The ADC084S021 is in this state for the first three SCLK cycles after $\overline{CS}$ is brought low.

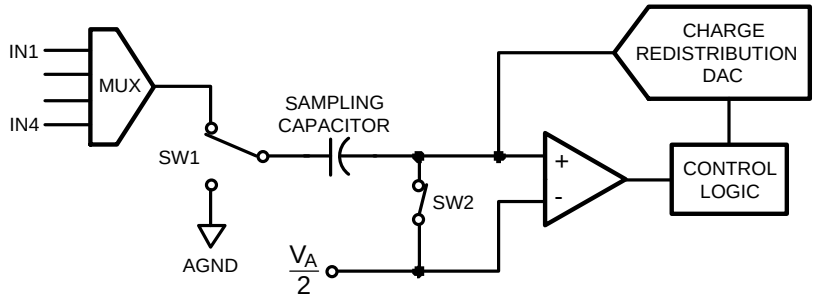


Figure 47. ADC084S021 in Track Mode

8.4.2 Hold Mode

Figure 48 shows the ADC084S021 in hold mode: switch SW1 connects the sampling capacitor to ground, maintaining the sampled voltage, and switch SW2 unbalances the comparator. The control logic then instructs the charge-redistribution DAC to add fixed amounts of charge to the sampling capacitor until the comparator is balanced. When the comparator is balanced, the digital word supplied to the DAC is the digital representation of the analog input voltage. The ADC084S021 is in this state for the fourth through sixteenth SCLK cycles after $\overline{CS}$ is brought low.

The time when $\overline{CS}$ is low is considered a serial frame. Each of these frames must contain an integer multiple of 16 SCLK cycles, during which time a conversion is performed and clocked out at the DOUT pin and data is clocked into the DIN pin to indicate the multiplexer address for the next conversion.

Device Functional Modes (continued)

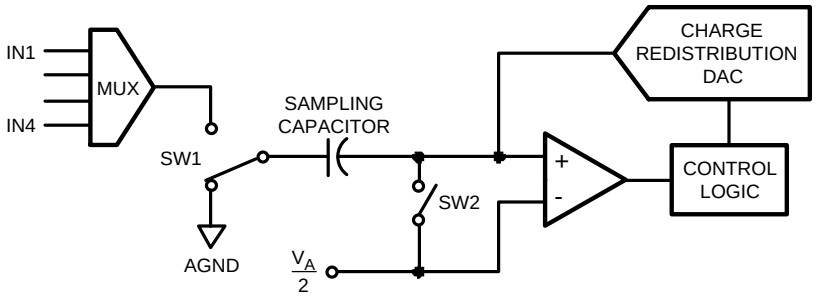


Figure 48. ADC084S021 in Hold Mode

8.5 Register Maps

Table 1 shows the control register bits for the ADC084S021.

Table 1. Control Register Bits

BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DONTC	DONTC	ADD2	ADD1	ADD0	DONTC	DONTC	DONTC

8.5.1 Register Description

Table 2 shows the register descriptions for bit 7 through bit 0.

Table 2. Control Register Bit Descriptions

BIT NO.	SYMBOL	DESCRIPTION
7 to 6, 2 to 0	DONTC	Don't care. The value of these bits do not affect device operation.
5	ADD2	These three bits determine which input channel will be sampled and converted in the next track/hold cycle. The mapping between codes and channels is shown in Table 3.
4	ADD1	
3	ADD0	

Table 3 shows the input channel selection for register bits ADD2, ADD1, and ADD0.

Table 3. Input Channel Selection

INPUT CHANNEL	ADD2	ADD1	ADD0
IN1 (Default)	×	0	0
IN2	×	0	1
IN3	×	1	0
IN4	×	1	1

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

Figure 49 shows a typical application of the ADC084S021. Power is provided, in this example, by the Texas Instruments LP2950 low-dropout voltage regulator, available in a variety of fixed and adjustable output voltages. The power supply pin is bypassed with a capacitor network located close to the ADC084S021.

Because the reference for the ADC084S021 is the supply voltage, any noise on the supply degrades device noise performance. Use a dedicated linear regulator for this device, or provide sufficient decoupling from other circuitry to keep noise off the ADC084S021 supply pin. Because of the low power requirements of the ADC084S021, it is also possible to use a precision reference as a power supply to maximize performance. The four-wire interface is also shown connected to a microprocessor or DSP.

9.2 Typical Application

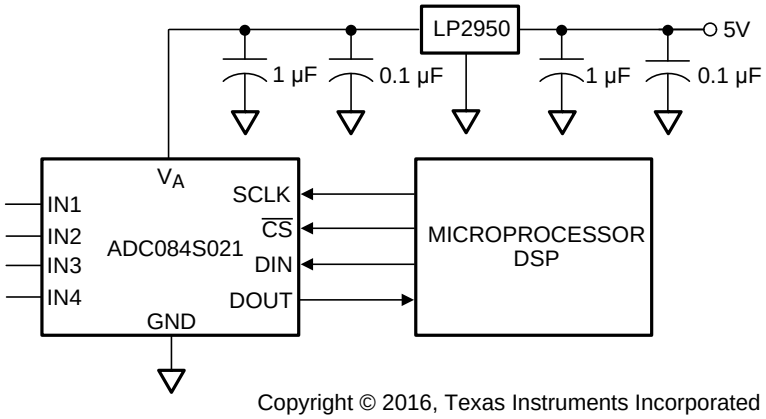


Figure 49. Typical Application Circuit

9.2.1 Design Requirements

In this application, the power consumption of the ADC084S021 must not exceed 1 mW and the throughput may range from 50 ksps to 200 ksps.

9.2.2 Detailed Design Procedure

The two largest factors that impact the power consumption of the ADC084S021 are the supply voltage and the throughput. According to Figure 50, a supply voltage of 3 V allows a throughput of up to 200 ksps at less than 1-mW power consumption. If a supply voltage of 5 V is chosen then the maximum throughput achievable is about 40 ksps, which does not meet the design requirements. Select a supply voltage of 3 V with a F_{CLK} of 3.2 MHz to meet all of the design requirements.

Typical Application (continued)

9.2.3 Application Curve

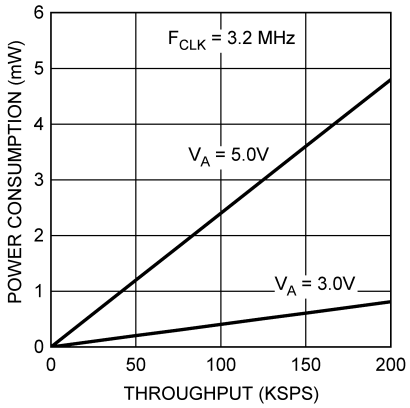


Figure 50. Power Consumption vs Throughput

10 Power Supply Recommendations

The ADC084S021 is fully powered up whenever $\overline{CS}$ is low, and fully powered down when $\overline{CS}$ is high, with one exception: the ADC084S021 automatically enters power-down mode between the 16th falling edge of a conversion and the 1st falling edge of the subsequent conversion (see *Timing Requirements*).

The ADC084S021 can perform multiple conversions back to back; each conversion requires 16 SCLK cycles. The ADC084S021 performs conversions continuously as long as $\overline{CS}$ is held low.

10.1 Power Management

When the ADC084S021 is operated continuously in normal mode, the maximum throughput is $f_{SCLK}/16$. Performance remains as stated in *Electrical Characteristics* as long as the SCLK frequency remains within the range stated at the heading of those tables. Throughput may be traded for power consumption by running f_{SCLK} at its maximum 3.2 MHz and performing fewer conversions per unit time, putting the ADC084S021 into shutdown mode between conversions. See Figure 44 in *Typical Characteristics*. To calculate the power consumption for a given throughput, multiply the fraction of time spent in the normal mode by the normal mode power consumption and add the fraction of time spent in shutdown mode multiplied by the shutdown mode power consumption. Generally, the user places the part into normal mode and then put the part back into shutdown mode. Note that the curve of Figure 44 is nearly linear. This is because the power consumption in the shutdown mode is so small that it can be ignored for all practical purposes.

10.2 Noise Considerations

The charging of any output load capacitance requires current from the power supply, V_A. The current pulses required from the supply to charge the output capacitance causes voltage variations of the supply voltage. If these variations are large enough, they could degrade SNR and SINAD performance of the ADC. Furthermore, discharging the output capacitance when the digital output goes from a logic high to a logic low dumps current into the die substrate. Load discharge currents causes *ground bounce* noise in the substrate that degrades noise performance if that current is large enough. The larger is the output capacitance, the more current flows through the die supply line and substrate, causing more noise to be coupled into the analog channel and degrading noise performance.

To keep noise out of the power supply, keep the output load capacitance as small as practical. If the load capacitance is greater than 50 pF, use a 100-Ω series resistor at the ADC output, located as close to the ADC output pin as practical. This limits the charge and discharge current of the output capacitance and improve noise performance.

11 Layout

11.1 Layout Guidelines

For optimum performance, take care with the physical layout of the ADC084S021 circuitry. The basic SAR architecture is sensitive to glitches or sudden changes on the power supply and ground connections that occur just prior to latching the output of the analog comparator. Therefore, during any single conversion for an *n-bit* SAR converter, there are n *windows* in which large external transient voltages can easily affect the conversion result. Such glitches might originate from switching power supplies, nearby digital logic, and high-power devices.

With this in mind, power to the ADC084S021 must be clean and well-bypassed. A 0.1-µF ceramic bypass capacitor must be placed as close to the device as possible. A 1-µF to 10-µF capacitor may also be needed if the impedance of the connection between VA and the power supply is high. Routing of the analog inputs must be kept short and separate from the digital lines. To keep unwanted coupling to a minimum, input traces must also be routed away from noisy components or planes that could crosstalk or interfere with the signal.

11.2 Layout Example

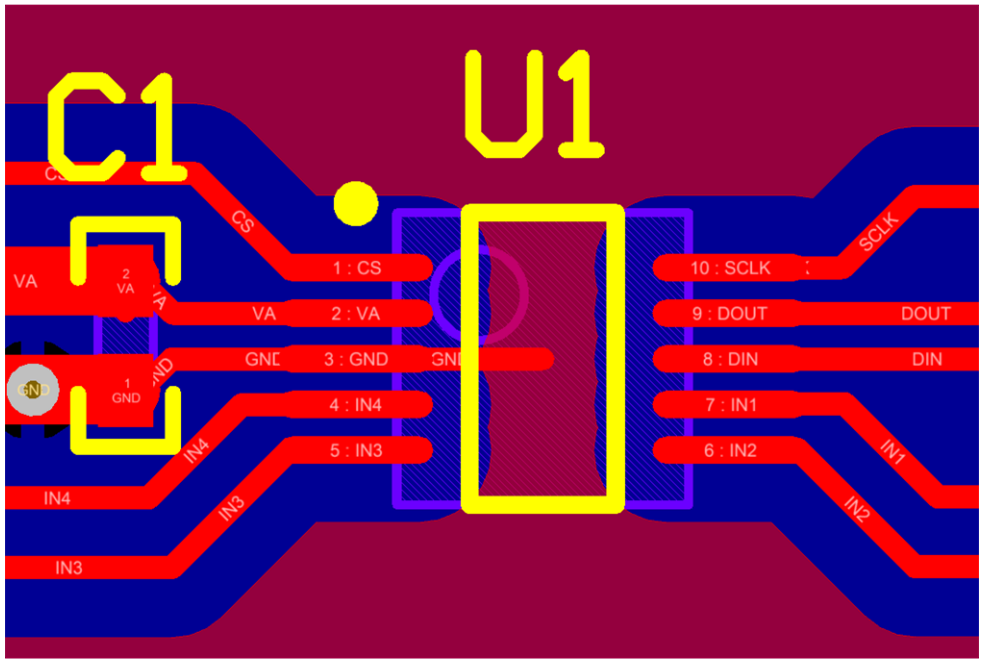


Figure 51. ADC Layout

12 Device and Documentation Support

12.1 Device Support

12.1.1 Device Nomenclature

ACQUISITION TIME is the time required to acquire the input voltage. That is, it is time required for the hold capacitor to charge up to the input voltage.

APERTURE DELAY is the time between the fourth falling SCLK edge of a conversion and the time when the input signal is acquired or held for conversion.

CONVERSION TIME is the time required, after the input voltage is acquired, for the ADC to convert the input voltage to a digital word.

CROSSTALK is the coupling of energy from one channel into the other channel, or the amount of signal energy from one analog input that appears at the measured analog input.

DIFFERENTIAL NON-LINEARITY (DNL) is the measure of the maximum deviation from the ideal step size of 1 LSB.

DUTY CYCLE is the ratio of the time that a repetitive digital waveform is high to the total time of one period. The specification here refers to the SCLK.

EFFECTIVE NUMBER OF BITS (ENOB, or EFFECTIVE BITS) is another method of specifying Signal-to-Noise and Distortion or SINAD. ENOB is defined as (SINAD − 1.76) / 6.02 and says that the converter is equivalent to a perfect ADC of this (ENOB) number of bits.

FULL POWER BANDWIDTH is a measure of the frequency at which the reconstructed output fundamental drops 3 dB below its low frequency value for a full scale input.

FULL SCALE ERROR (FSE) is a measure of how far the last code transition is from the ideal 1½ LSB below V_{REF^+} and is defined with Equation 1.

$$V_{FSE} = V_{max} + 1.5\ LSB - V_{REF^+} \quad (1)$$

where

- V_{max} is the voltage at which the transition to the maximum code occurs
- FSE can be expressed in Volts, LSB or percent of full scale range

GAIN ERROR is the deviation of the last code transition (111...110) to (111...111) from the ideal (V_{REF} − 1.5 LSB), after adjusting for offset error.

INTEGRAL NON-LINEARITY (INL) is a measure of the deviation of each individual code from a line drawn from negative full scale (½ LSB below the first code transition) through positive full scale (½ LSB above the last code transition). The deviation of any given code from this straight line is measured from the center of that code value.

INTERMODULATION DISTORTION (IMD) is the creation of additional spectral components as a result of two sinusoidal frequencies being applied to the ADC input at the same time. It is defined as the ratio of the power in the second and third order intermodulation products to the sum of the power in both of the original frequencies. IMD is usually expressed in dB.

MISSING CODES are those output codes that never appears at the ADC outputs. These codes cannot be reached with any input value. The ADC084S021 is ensured not to have any missing codes.

OFFSET ERROR is the deviation of the first code transition (000...000) to (000...001) from the ideal (that is, GND + 0.5 LSB).

SIGNAL TO NOISE RATIO (SNR) is the ratio, expressed in dB, of the rms value of the input signal at the converter output to the rms value of the sum of all other spectral components below one-half the sampling frequency, not including DC or harmonics included in the THD specification.

Device Support (continued)

SIGNAL TO NOISE PLUS DISTORTION (S/N+D or SINAD) is the ratio, expressed in dB, of the rms value of the input signal to the rms value of all of the other spectral components below half the clock frequency, including harmonics but excluding dc

SPURIOUS FREE DYNAMIC RANGE (SFDR) is the difference, expressed in dB, between the rms values of the input signal and the peak spurious signal where a spurious signal is any signal present in the output spectrum that is not present at the input, excluding dc

TOTAL HARMONIC DISTORTION (THD) is the ratio, expressed in dB or dBc, of the rms total of the first five harmonic components at the output to the rms level of the input signal frequency as seen at the output. THD is calculated with Equation 2.

$$THD = 20 \bullet \log_{10} \sqrt{\frac{Af_2^2 + \bullet\bullet\bullet + Af_6^2}{Af_1^2}} \quad (2)$$

where

- Af_1 is the RMS power of the input frequency at the output
- Af_2 through Af_6 are the RMS power in the first 5 harmonic frequencies

THROUGHPUT TIME is the minimum time required between the start of two successive conversion. It is the acquisition time plus the conversion and read out times. In the case of the ADC084S021, this is 16 SCLK periods.

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADC084S021CIMM/NOPB	ACTIVE	VSSOP	DGS	10	1000	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 85	X19C	Samples
ADC084S021CIMMX/NOPB	ACTIVE	VSSOP	DGS	10	3500	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 85	X19C	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

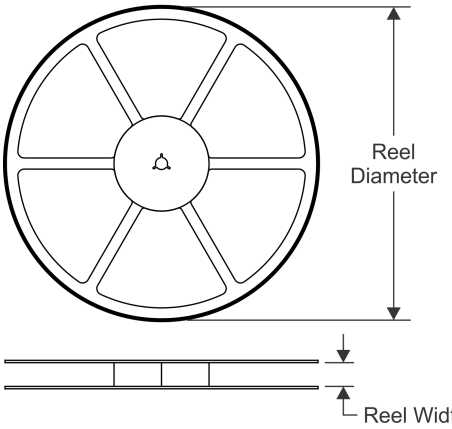
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

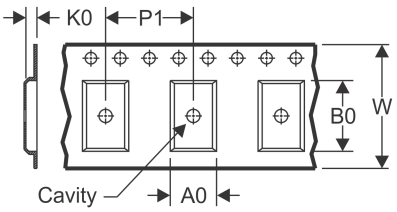
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

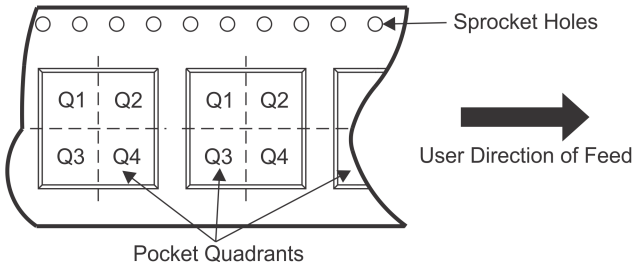


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

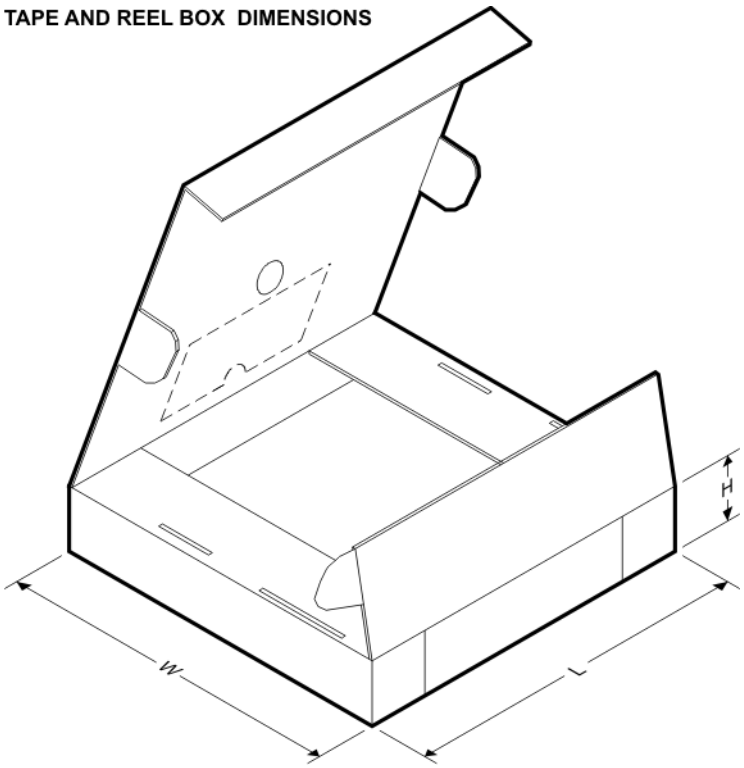
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADC084S021CIMM/NOPB	VSSOP	DGS	10	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
ADC084S021CIMMX/NOPB	VSSOP	DGS	10	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

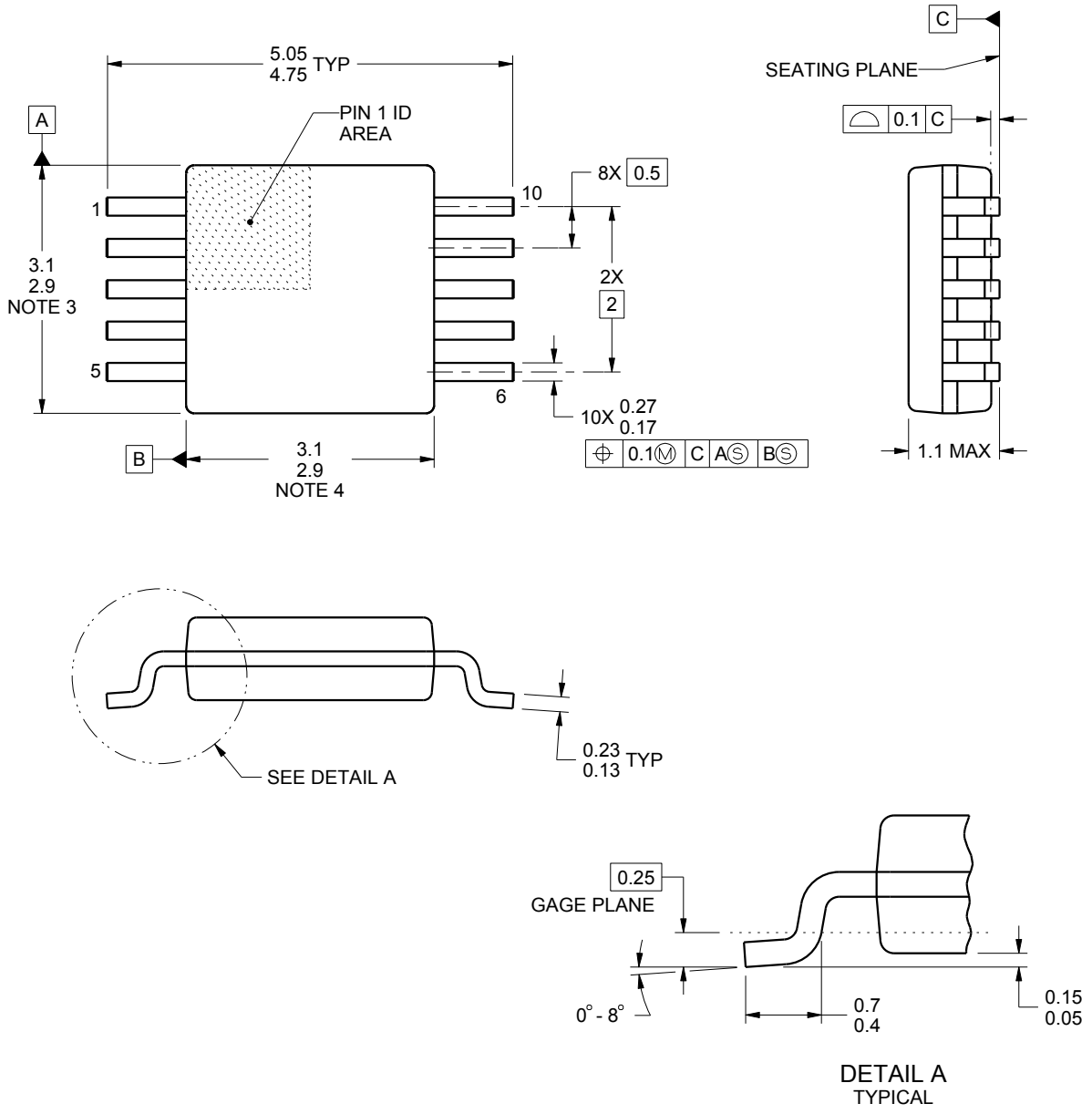
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADC084S021CIMM/NOPB	VSSOP	DGS	10	1000	210.0	185.0	35.0
ADC084S021CIMMX/NOPB	VSSOP	DGS	10	3500	367.0	367.0	35.0

PACKAGE OUTLINE

DGS0010A

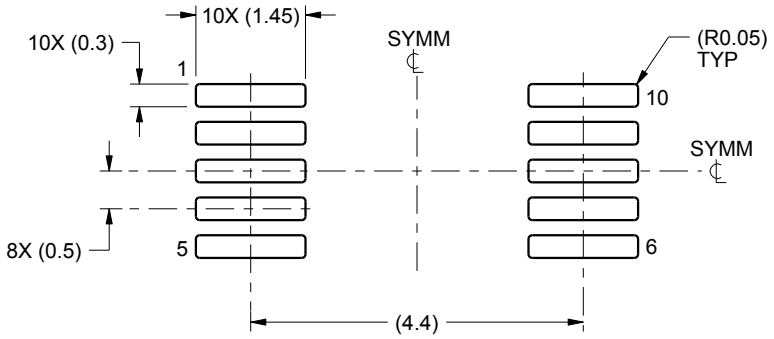
VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

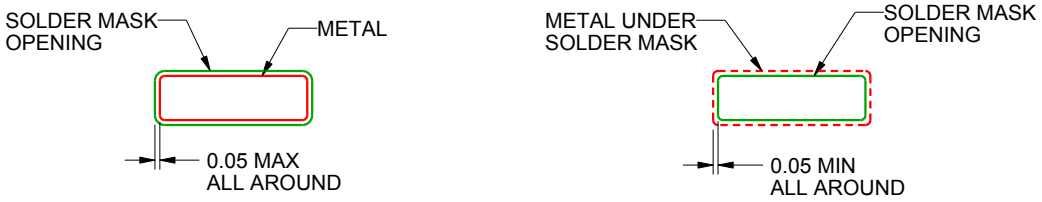


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
NOT TO SCALE

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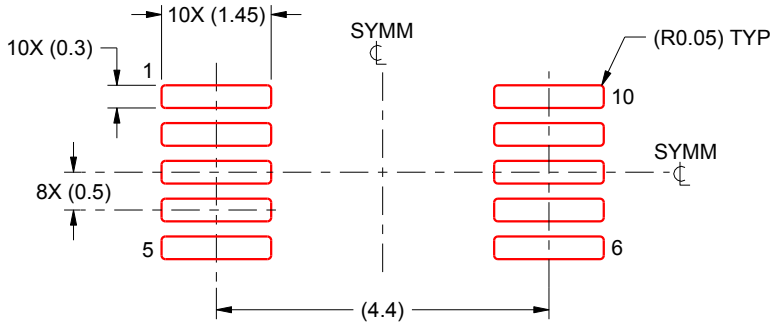
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221984/A 05/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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