bq40z80 2-Series to 7-Series Li-Ion Battery Pack Manager

1 Features

- Fully Integrated 2-Series to 7-Series Li-Ion or Li-Polymer Cell Battery Pack Manager and Protection
- Next-Generation Patented Impedance Track™ Technology Accurately Measures Available Charge in Li-Ion and Li-Polymer Batteries
- Configurable Multifunction Pins to Support a Variety of Applications
- Supports Either Elliptic Curve Cryptography (ECC) or SHA-1 Authentication
- High-Side N-CH Protection FET Drive
- Integrated Cell Balancing While Charging or at Rest
- Supports 29-Ah Batteries Natively, and Larger Capacities with Scaling
- Full Array of Programmable Protection Features
  - Voltage
  - Current
  - Temperature
  - Charge Timeout
  - CHG/DSG FETs
  - AFE
- Sophisticated Charge Algorithms
  - JEITA
  - Enhanced Charging
  - Adaptive Charging
  - Cell Balancing
- Supports TURBO Mode 2.0/Intel® Dynamic Battery Power Technology (DBPTv2)
- Diagnostic Lifetime Data Monitor and Black Box Recorder
- LED Display
- Supports Two-Wire SMBus v1.1 Interface
- IATA Support
- Compact Package: 32-Lead QFN (RSM)

2 Applications

- Industrial Appliances and Robots
- Handheld Garden and Power Tools
- Battery Powered Vacuums
- Energy Storage Systems and UPS

3 Description

The bq40z80 device, incorporating patented Impedance Track™ technology, is a fully integrated, single-chip, pack-based solution that provides a rich array of features for gas gauging, protection, and authentication for 2-series up to 7-series cell Li-Ion and Li-Polymer battery packs.

Using its integrated high-performance analog peripherals, the bq40z80 device measures and maintains an accurate record of available capacity, voltage, current, temperature, and other critical parameters in Li-Ion or Li-Polymer batteries, and reports this information to the system host controller over an SMBus v1.1 compatible interface.

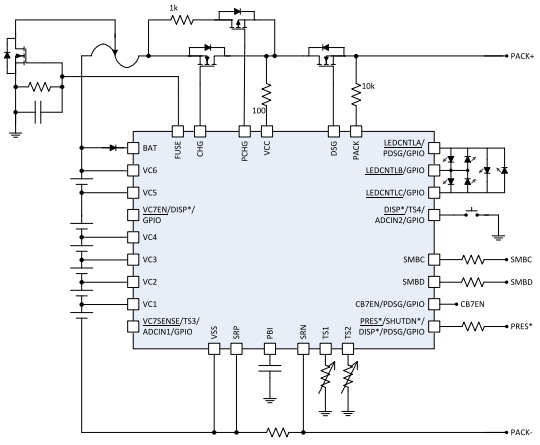
Elliptic Curve Cryptography (ECC) or SHA-1 authentication with secure memory for authentication keys enables identification of genuine battery packs.

The bq40z80 device supports TURBO Mode 2.0/Intel Dynamic Battery Power Technology (DBPTv2) by providing the available max power and max current to the host system. The device has eight multifunction pins that can be configured as thermal inputs, ADC inputs, general purpose input/output (GPIO) pins, a presence pin, LED functions, display button input, or other functions. Status and flag registers are mappable to the GPIOs and used as interrupts to the host processor.

Device Information

PART NUMBER	PACKAGE	BODY SIZE (NOM)
bq40z80	VQFN (32)	4.00 mm × 4.00 mm

Simplified Schematic



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

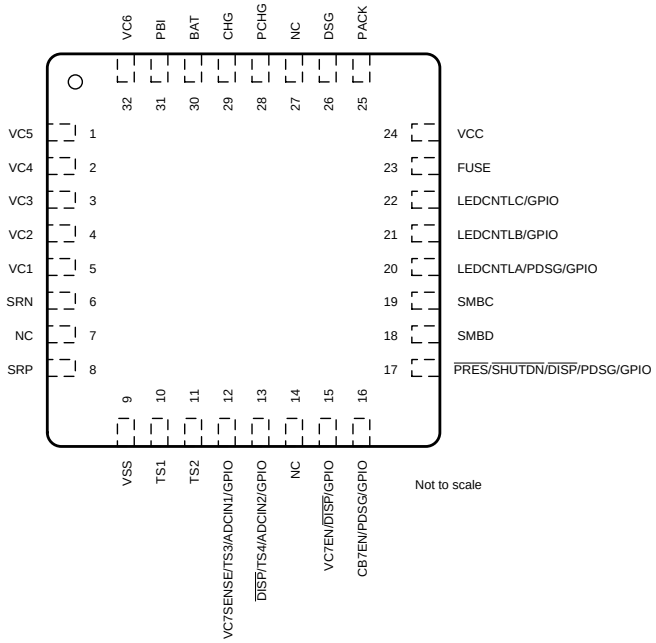
Date	Revision	Notes
November 2018	A	From Advance Information to Production Data

5 Description (continued)

The bq40z80 device provides software-based 1st- and 2nd-level safety protection against overvoltage, undervoltage, overcurrent, short-circuit current, overload, and overtemperature conditions, as well as other pack- and cell-related faults. The compact 32-lead QFN package minimizes solution cost and size for smart batteries, while providing maximum functionality and safety for battery gauging applications.

6 Pin Configuration and Functions

RSM Package
32-Pin VQFN with Exposed Thermal Pad
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NUMBER		
VC5	1	AI (1)	Sense voltage input pin for the fifth cell from the bottom of the stack, balance current input for the fifth cell from the bottom of the stack, and return balance current for the sixth cell from the bottom of the stack. Should be connected to the positive terminal of the fifth cell from the bottom of stack with a 100-Ω series resistor and a 0.1-µF capacitor to VC4. If not used, connect to VC4.
VC4	2	AI	Sense voltage input pin for the fourth cell from the bottom of the stack, balance current input for the fourth cell from the bottom of the stack, and return balance current for the fifth cell from the bottom of the stack. Should be connected to the positive terminal of the fourth cell from the bottom of stack with a 100-Ω series resistor and a 0.1-µF capacitor to VC3. If not used, connect to VC3.
VC3	3	AI	Sense voltage input pin for the third cell from the bottom of the stack, balance current input for the third cell from the bottom of the stack, and return balance current for the fourth cell from the bottom of the stack. Should be connected to the positive terminal of the third cell from the bottom of stack with a 100-Ω series resistor and a 0.1-µF capacitor to VC2. If not used, connect to VC2.
VC2	4	AI	Sense voltage input pin for the second cell from the bottom of the stack, balance current input for the second cell from the bottom of the stack, and return balance current for the third cell from the bottom of the stack. Should be connected to the positive terminal of the second cell from the bottom of stack with a 100-Ω series resistor and a 0.1-µF capacitor to VC1. If not used, connect to VC1.

(1) P = Power Connection, O = Digital Output, AI = Analog Input, I = Digital Input, I/OD = Digital Input/Output

Pin Functions (continued)

PIN		TYPE	DESCRIPTION
NAME	NUMBER		
VC1	5	AI	Sense voltage input pin for the first cell from the bottom of the stack, balance current input for the first cell from the bottom of the stack, and return balance current for the second cell from the bottom of the stack. Should be connected to the positive terminal of the first cell from the bottom of stack with a 100-Ω series resistor and a 0.1-µF capacitor to VSS.
SRN	6	I	Analog input pin connected to the internal coulomb counter peripheral for integrating a small voltage between SRP and SRN, where SRP is the top of the sense resistor and charging current flows from SRP to SRN. Should be connected through an RC filter to the sense resistor terminal connected to PACK– (not CELL–).
NC	7	—	Not internally connected
SRP	8	I	Analog input pin connected to the internal coulomb counter peripheral for integrating a small voltage between SRP and SRN, where SRP is the top of the sense resistor and charging current flows from SRP to SRN. Should be connected through an RC filter to the sense resistor positive terminal, which is connected to the least-positive cells negative terminal.
VSS	9	P	Device ground
TS1	10	AI	Temperature sensor 1 thermistor input pin. Connect to thermistor-1. If not used, connect directly to VSS and configure data flash accordingly.
TS2	11	AI	Temperature sensor 2 thermistor input pin. Connect to thermistor-2. If not used, connect directly to VSS and configure data flash accordingly.
VC7SENSE/TS3/ADCIN1/ GPIO	12	IO	Multifunction pin for VC7 Sense, TS3, ADCIN1, and GPIO. Can be configured in the control registers. If not used, connect directly to VSS and configure data flash accordingly. VC7SENSE: Connect to a resistor divider to provide the correct input for the seventh cell from the bottom of the stack. TS3: Temperature sensor 3 thermistor input pin. Connect to thermistor-3. ADCIN1: General-purpose ADCIN pin. Connect properly scaled input to this pin. GPIO: Customizable GPIO
$\overline{\text{DISP}}$/TS4/ADCIN2/GPIO	13	IO	Multifunction pin for the display button, temperature sensor input, ADC input, or GPIO. Can be configured in the control registers. If not used, connect directly to VSS and configure data flash accordingly. $\overline{\text{DISP}}$: Connect to the display button or LED. TS4: Temperature sensor 4 thermistor input pin. Connect to thermistor-4. ADCIN2: General-purpose ADCIN pin. Connect properly scaled input to this pin. GPIO: Customizable GPIO
NC	14	—	Not internally connected
VC7EN/$\overline{\text{DISP}}$/GPIO	15	I/OD	Multifunction pin for the external divider enable for the seventh cell from the bottom of the stack, display button, or GPIO. Can be configured in the control registers. If not used, connect directly to VSS and configure data flash accordingly. VC7EN: Connects to the seventh cell external divider control FET to enable voltage measurement on the seventh cell from the bottom of the stack. Only enable for measurement to reduce leakage current. $\overline{\text{DISP}}$: Connect to the display button or LED. GPIO: Customizable GPIO
CB7EN/PDSG/GPIO	16	I/OD	Multifunction pin for cell balancing enable for the seventh cell from the bottom of the stack, pre-discharge FET control, or GPIO. Can be configured in the control registers. If not used, connect directly to VSS and configure data flash accordingly. CB7EN: Connect to the N-CH FET to control external cell balancing for the seventh cell from the bottom of the stack. PDSG: Connect to the N-CH FET to control PRE-DISCHARGE mode. GPIO: Customizable GPIO
$\overline{\text{PRES}}$/$\overline{\text{SHUTDN}}$/$\overline{\text{DISP}}$/ PDSG/GPIO	17	I/OD	Multifunction pin for host system present input, emergency system shutdown, LED button control, pre-discharge control, or GPIO. Can be configured in the control registers. If not used, connect directly to VSS and configure data flash accordingly. $\overline{\text{PRES}}$: Connect to host to detect system present input for a removable battery pack. Do not pullup this pin. $\overline{\text{SHUTDN}}$: Emergency shutdown input for an embedded battery pack $\overline{\text{DISP}}$: Connect to the display button or LED. PDSG: Connect to the N-CH FET to control PRE-DISCHARGE mode. GPIO: Customizable GPIO
SMBD	18	I/OD	SMBus data pin

Pin Functions (continued)

PIN		TYPE	DESCRIPTION
NAME	NUMBER		
SMBC	19	I/OD	SMBus clock pin
LEDCNTLA/PDSG/GPIO	20	O	Multifunction pin for LED display, pre-discharge, or GPIO. If not used, connect to VSS with a 20-kΩ resistor. LEDCNTLA: LED display segment that drives the external LEDs, depending on the firmware configuration. PDSG: Connect to the N-CH FET to control PRE-DISCHARGE mode. GPIO: Customizable GPIO
LEDCNTLB/GPIO	21	O	Multifunction pin for LED display or GPIO. If not used, connect to VSS with a 20-kΩ resistor. LEDCNTLB: LED display segment that drives the external LEDs, depending on the firmware configuration. GPIO: Customizable GPIO
LEDCNTLC/GPIO	22	O	Multifunction pin for LED display or GPIO. If not used, connect to VSS with a 20-kΩ resistor. LEDCNTLC: LED display segment that drives the external LEDs, depending on the firmware configuration GPIO: Customizable GPIO
FUSE	23	O	Fuse drive output pin. Can be OR'ed together into the fuse N-CH FET gate drive with secondary protector. If not used, connect directly to VSS.
VCC	24	P	Secondary power supply input. Connect to the middle of protection FETs through the series resistor.
PACK	25	AI	Pack sense input pin. Connect through the series resistor to PACK+.
DSG	26	O	NMOS discharge FET drive output pin. Connect to the DSG FET gate.
NC	27	—	Not internally connected.
PCHG	28	O	PMOS precharge FET drive output pin. Connect to the PCHG FET gate if the precharge function is used. Leave floating if not used.
CHG	29	O	NMOS charge FET drive output pin. Connect to the CHG FET gate.
BAT	30	P	Primary power supply input pin. Connect through the diode and series resistor to the top of the cell stack.
PBI	31	P	Power supply backup input pin. Connect to the 2.2-µF capacitor to VSS.
VC6	32	AI	Sense voltage input pin for the sixth cell from the bottom of the stack, balance current input for the sixth cell from the bottom of the stack. Should be connected to the positive terminal of the sixth cell from the bottom of stack with 100-Ω series resistor and a 0.1-µF capacitor to VC5. If not used, connect to VC5.

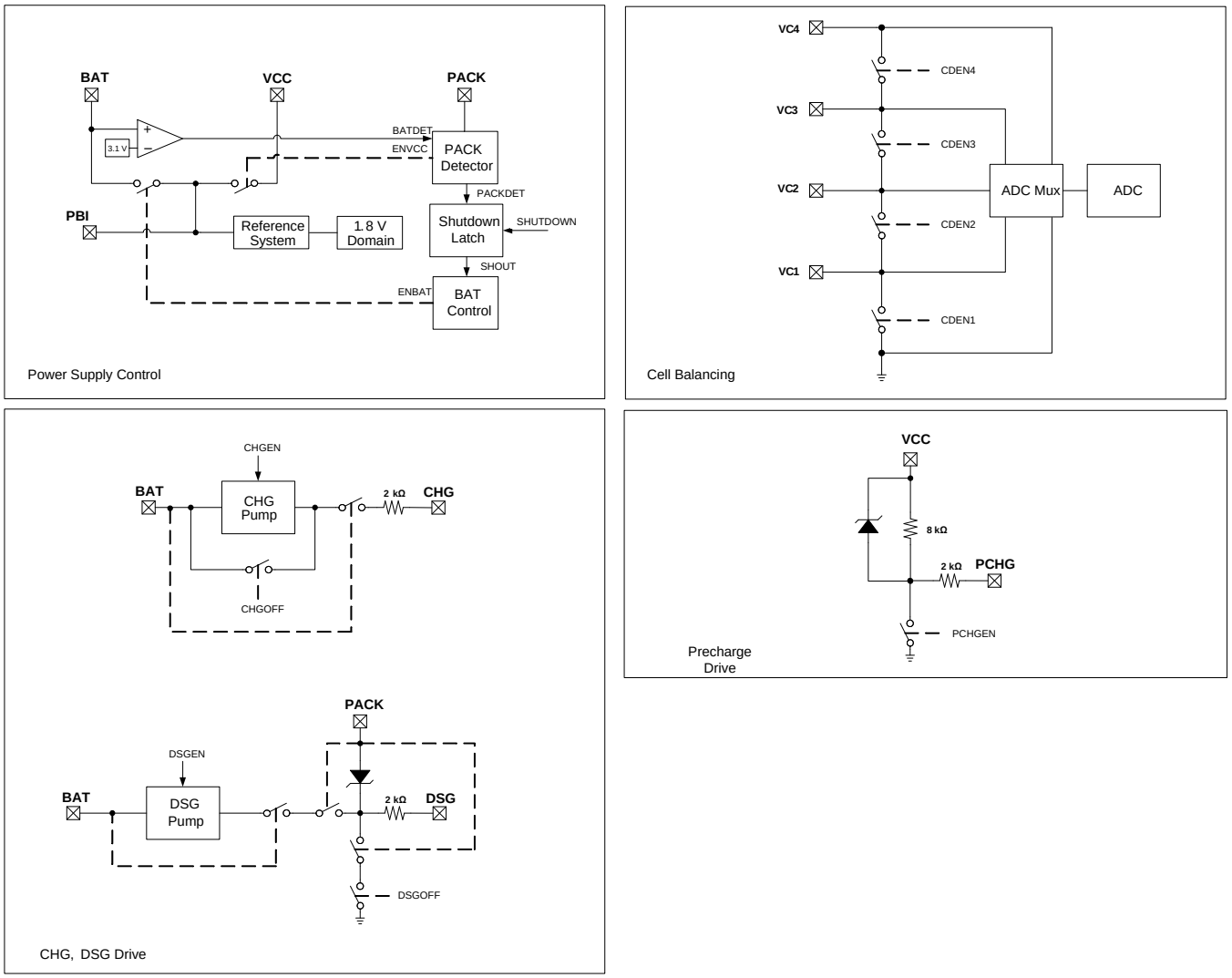


Figure 1. Pin Equivalent Diagram 1

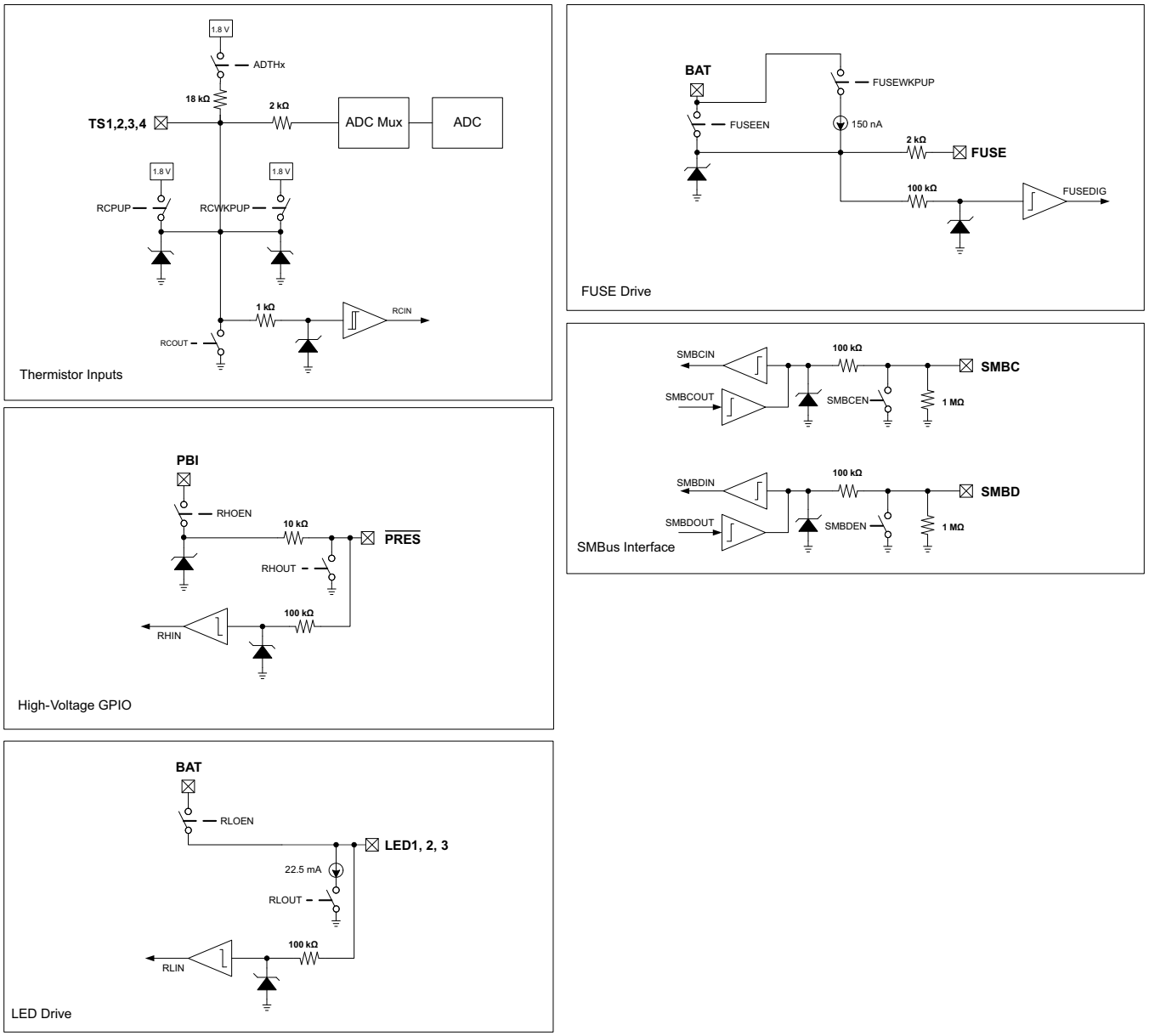


Figure 2. Pin Equivalent Diagram 2

7 Specifications

7.1 Absolute Maximum Ratings

Over-operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage range, V_{CC}	BAT(2), VCC(2), PBI(2), PACK(2)	–0.3	35	V
Input voltage range, V_{IN}	SMBC, SMBD, VC7EN/$\overline{\text{DISP}}$/GPIO, CB7EN/PDSG/GPIO, $\overline{\text{PRES}}$/SHUTDN/$\overline{\text{DISP}}$/PDSG/GPIO(2)	–0.3	35	V
	TS1, TS2, VC7SENSE/TS3/ADCIN1/GPIO, $\overline{\text{DISP}}$/TS4/ADCIN2/GPIO	–0.3	V_{REG} + 0.3	V
	LEDCNTLA/PDSG/GPIO, LEDCNTLB/GPIO, LEDCNTLC/GPIO(2)	–0.3	V_{BAT} + 0.3	V
	SRP, SRN	–0.3	V_{REG} + 0.3	V
	VC6	VC5 – 0.3	VSS + 35	V
	VC5	VC4 – 0.3	VSS + 35	V
	VC4	VC3 – 0.3	VSS + 35	V
	VC3	VC2 – 0.3	VSS + 35	V
	VC2	VC1 – 0.3	VSS + 35	V
	VC1	VSS – 0.3	VSS + 35	V
Output voltage range, V_O	CHG, DSG(2)	–0.3	43	
	PCHG, FUSE	–0.3	35	V
Maximum VSS current, I_{SS}			50	mA
Functional temperature T_{FUNC}		–40	110	
Storage temperature, T_{STG}		–65	150	°C
Lead temperature (soldering, 10 s), T_{SOLDER}			300	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) A series 50-Ω or larger resistor is needed when voltage is applied beyond 28 V.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

Typical values stated where T_A = 25°C and VCC = 25.2 V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2 V to 32 V (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	BAT(1), VCC(1), PBI(1), PACK(1)	2.2		32	V
$V_{SHUTDOWN–}$	Shutdown voltage	$V_{PACK} < V_{SHUTDOWN\ –}$	1.8	2.0	2.2	V
$V_{SHUTDOWN+}$	Start-up voltage	$V_{PACK} > V_{SHUTDOWN–} + V_{HYS}$	2.05	2.25	2.45	V
V_{HYS}	Shutdown voltage hysteresis	$V_{SHUTDOWN+} – V_{SHUTDOWN–}$		250		mV

(1) A series 50-Ω or larger resistor is needed when voltage is applied beyond 28 V.

Recommended Operating Conditions (continued)

Typical values stated where T_A = 25°C and VCC = 25.2 V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2 V to 32 V (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{IN}	Input voltage range	SMBC, SMBD, VC7EN/DISP/GPIO, CB7EN/PDSG/GPIO, PRES/SHUTDN/DISP/PDSG/GPIO (1)			32	V
		TS1, TS2, VC7SENSE/TS3/ADCIN1/GPIO, DISP/TS4/ADCIN2/GPIO			V_{REG}	
		LEDCNTLA/PDSG/GPIO, LEDCNTLB/GPIO, LEDCNTLC/GPIO (1)			V_{BAT}	
		SRP, SRN	–0.2		0.2	
		VC6	V_{VC5}		VC5 + 5	
		VC5	V_{VC4}		VC4 + 5	
		VC4	V_{VC3}		VC3 + 5	
		VC3	V_{VC2}		VC2 + 5	
		VC2	V_{VC1}		VC1 + 5	
		VC1	V_{VSS}		VSS + 5	
V_O	Output voltage range	PCHG, FUSE (1)			32	V
C_{PBI}	External PBI capacitor		2.2			µF
T_{OPR}	Operating temperature		–40		85	°C

7.4 Thermal Information

THERMAL METRIC (1)		bq40z80 RSM (QFN) 32 PINS	UNIT
$R_{\theta JA, High K}$	Junction-to-ambient thermal resistance	47.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	40.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	14.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	14.4	°C/W
$R_{\theta JC(bottom)}$	Junction-to-case(bottom) thermal resistance	3.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

Typical values stated where T_A = 25°C and VCC = 21.6 V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2 V to 32 V unless otherwise noted

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
Supply Currents						
I_{NORMAL}	NORMAL mode	CPU not active, CHG on. DSG on, High Frequency Oscillator on, Low Frequency Oscillator on, REG18 on, ADC on, ADC_Filter on, CC_Filter on, CC on, LED/Buttons/GPIOs off, SMBus not active, no Flash write		663		µA

Electrical Characteristics (continued)

Typical values stated where T_A = 25°C and VCC = 21.6 V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2 V to 32 V unless otherwise noted

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
I_{SLEEP}	SLEEP mode	CPU not active, CHG on, DSG on, High Frequency Oscillator off, Low Frequency Oscillator on, REG18 on, ADC off, ADC_Filter off, CC_Filter off, LED/Buttons/GPIOs off, SMBus not active, no Flash write		96		µA
		CPU not active, CHG off. DSG on, High Frequency Oscillator off, Low Frequency Oscillator on, REG18 on, ADC off, ADC_Filter off, CC_Filter off, LED/Buttons/GPIOs off, SMBus not active, no Flash write, BAT = 14.4 V		90		µA
$I_{SHUTDOWN}$	SHUTDOWN mode	CPU not active, CHG off. DSG off, High Frequency Oscillator off, Low Frequency Oscillator off, REG18 off, ADC off, ADC_Filter off, CC_Filter off, LED/Buttons/GPIOs off, SMBus not active, no Flash write, BAT = 14.4 V		1.4		µA
Power Supply Control						
$V_{SWITCHOVER–}$	BAT to VCC switchover voltage	$V_{BAT} < V_{SWITCHOVER–}$	1.95	2.1	2.2	V
$V_{SWITCHOVER+}$	VCC to BAT switchover voltage	$V_{BAT} > V_{SWITCHOVER–} + V_{HYS}$	2.9	3.1	3.25	V
V_{HYS}	Switchover voltage hysteresis	$V_{SWITCHOVER+} – V_{SWITCHOVER–}$		1000		mV
I_{LKG}	Input Leakage Current	BAT pin, BAT = 0 V, VCC = 32 V, PACK = 32 V			1	µA
		PACK pin, BAT = 32 V, VCC = 0 V, PACK = 0 V			1	
		BAT and PACK terminals, BAT = 0 V, VCC = 0 V, PACK = 0 V, PBI = 32 V			1	
R_{PD}	Internal pulldown resistance	PACK	30	40	50	kΩ
AFE Power-On Reset						
$V_{REGIT–}$	Negative-going voltage input	V_{REG}	1.51	1.55	1.59	V
V_{HYS}	Power-on reset hysteresis	$V_{REGIT+} – V_{REGIT–}$	70	100	130	mV
t_{RST}	Power-on reset time		200	300	400	µs
AFE Watchdog Reset and Wake Timer						
t_{WDT}	AFE watchdog timeout	t_{WDT} = 500	372	500	628	ms
		t_{WDT} = 1000	744	1000	1256	ms
		t_{WDT} = 2000	1488	2000	2512	ms
		t_{WDT} = 4000	2976	4000	5024	ms
t_{WAKE}	AFE wake timer	t_{WAKE} = 250	186	250	314	ms
		t_{WAKE} = 500	372	500	628	ms
		t_{WAKE} = 1000	744	1000	1256	ms
		t_{WAKE} = 2000	1488	2000	2512	ms
t_{FETOFF}	FET off delay after reset	t_{FETOFF} = 512	409	512	614	ms
Internal 1.8-V LDO						
V_{REG}	Regulator voltage		1.6	1.8	2	V
$\Delta V_{O(TEMP)}$	Regulator output over temperature	$\Delta V_{REG} / \Delta T_A$, I_{REG} = 10 mA		±0.25%		
$\Delta V_{O(LINE)}$	Line regulation	$\Delta V_{REG} / \Delta V_{BAT}$, I_{BAT} = 10 mA	–0.6%		0.5%	
$\Delta V_{O(LOAD)}$	Load regulation	$\Delta V_{REG} / \Delta I_{REG}$, I_{REG} = 0 mA to 10 mA	–1.5%		1.5%	

Electrical Characteristics (continued)

Typical values stated where T_A = 25°C and VCC = 21.6 V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2 V to 32 V unless otherwise noted

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
I_{REG}	Regulator output current limit	V_{REG} = 0.9 × $V_{REG(NOM)}$, V_{IN} > 2.2 V	20			mA
I_{SC}	Regulator short-circuit current limit	V_{REG} = 0 × $V_{REG(NOM)}$	25	40	55	mA
$PSRR_{REG}$	Power supply rejection ratio	ΔV_{BAT} / ΔV_{REG}, I_{REG} = 10 mA, V_{IN} > 2.5 V, f = 10 Hz		40		dB
V_{SLEW}	Slew rate enhancement voltage threshold	V_{REG}	1.58	1.65		V
Voltage Reference 1						
V_{REF1}	Internal reference voltage	T_A = 25°C, after trim	1.215	1.22	1.225	V
$V_{REF1(DRIFT)}$	Internal reference voltage drift	T_A = 0°C to 60°C, after trim		±50		PPM/°C
		T_A = –40°C to 85°C, after trim		±80		PPM/°C
Voltage Reference 2						
V_{REF2}	Internal reference voltage	T_A = 25°C, after trim	1.22	1.225	1.23	V
$V_{REF2(DRIFT)}$	Internal reference voltage drift	T_A = 0°C to 60°C, after trim		±50		PPM/°C
		T_A = –40°C to 85°C, after trim		±80		PPM/°C
VC1, VC2, VC3, VC4, VC5, VC6, BAT, PACK						
K	Scaling factor	VC1–VSS, VC2–VC1, VC3–VC2, VC4–VC3, VC5–VC4, VC6–VC5	0.198	0.2	0.202	–
		VC6–VSS	0.032	0.0333	0.034	
		BAT–VSS, PACK–VSS	0.0275	0.0286	0.0295	
		V_{REF2}	0.49	0.5	0.51	
V_{IN}	Input voltage range	VC1–VSS, VC2–VC1, VC3–VC2, VC4–VC3, VC5–VC4, VC6–VC5	–0.2		5	V
		VC6–VSS	–0.2		30	
		PACK–VSS	–0.2		32	
I_{LKG}	Input leakage current	VC1, VC2, VC3, VC4, VC5, VC6, cell balancing off, cell detach detection off, ADC multiplexer off			1	µA
Cell Balancing and Cell Detach Detection						
R_{CB}	Internal cell balance resistance	$R_{DS(ON)}$ for internal FET switch at 2 V < VDS < 4 V			200	Ω
I_{CD}	Internal cell detach check current	VCx > VSS + 0.8 V	30	50	70	µA
ADC						
V_{IN}	Input voltage range	Internal reference (V_{REF1})	–0.2		1	V
		External reference (V_{REG})	–0.2		0.8 × V_{REG}	
	Full scale range	V_{FS} = V_{REF1} or V_{REG}	$–V_{FS}$		V_{FS}	V
INL	Integral nonlinearity (1 LSB = $V_{REF1}/(10 \times 2^N)$ = 1.225/(10 × 2^{15}) = 37.41 µV)	16-bit, best fit, –0.1 V to 0.8 × V_{REF1}			±8.5	LSB
		16-bit, best fit, –0.2 V to –0.1 V			±13.1	
OE	Offset error	16-bit, post calibration, V_{FS} = V_{REF1}		±67	±157	µV
OED	Offset error drift	16-bit, post calibration, V_{FS} = V_{REF1}		0.6	3	µV/°C
GE	Gain error	16-bit, –0.1 V to 0.8 × V_{FS}		±0.2%	±0.8%	/FSR
GED	Gain error drift	16-bit, –0.1 V to 0.8 × V_{FS}			150	PPM/°C
EIR	Effective input resistance		8			MΩ
ADC Digital Filter						

Electrical Characteristics (continued)

Typical values stated where T_A = 25°C and VCC = 21.6 V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2 V to 32 V unless otherwise noted

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
t_{CONV}	Conversion time	ADCTL[SPEED1, SPEED0] = 0, 0		31.25		ms
		ADCTL[SPEED1, SPEED0] = 0, 1		15.63		
		ADCTL[SPEED1, SPEED0] = 1, 0		7.81		
		ADCTL[SPEED1, SPEED0] = 1, 1		1.95		
Res	Resolution	No missing codes, ADCTL[SPEED1, SPEED0] = 0, 0	16			Bits
Eff_Res	Effective Resolution	With sign, ADCTL[SPEED1, SPEED0] = 0, 0	14	15		Bits
		With sign, ADCTL[SPEED1, SPEED0] = 0, 1	13	14		
		With sign, ADCTL[SPEED1, SPEED0] = 1, 0	11	12		
		With sign, ADCTL[SPEED1, SPEED0] = 1, 1	9	10		
Current Wake Comparator						
V_{WAKE}	Wake voltage threshold	$V_{WAKE} = V_{SRP} – V_{SRN}$= ± 0.625 mV	±0.3	±0.625	±0.9	mV
		$V_{WAKE} = V_{SRP} – V_{SRN}$ = ± 1.25 mV	±0.6	±1.25	±1.8	
		$V_{WAKE} = V_{SRP} – V_{SRN}$ = ± 2.5 mV	±1.2	±2.5	±3.6	
		$V_{WAKE} = V_{SRP} – V_{SRN}$ = ± 5 mV	±2.4	±5.0	±7.2	
$V_{WAKE(DRIFT)}$	Temperature drift of V_{WAKE} accuracy			0.5%		/°C
t_{WAKE}	Time from application of current to wake interrupt			250	700	µs
$t_{WAKE(SU)}$	Wake comparator startup time			500	1000	µs
Coulomb Counter						
V_{INPUT}	Input voltage range		–0.1		0.1	V
V_{RANGE}	Full scale range		$–V_{REF1}$ /10		V_{REF1} /10	V
INL	Integral nonlinearity (1 LSB = $V_{REF1}/(10 \times 2^N) = 1.215/(10 \times 2^{15})$ = 3.71 µV)	16-bit, best fit over input voltage range		±5.2	±22.3	LSB
OE	Offset error	16-bit, post calibration		±5.0	±10	µV
OED	Offset error drift	15-bit + sign, post calibration		0.2	0.3	µV/°C
GE	Gain error	15-bit + sign, Over input voltage range		±0.2%	±0.8%	/FSR
GED	Gain error drift	15-bit + sign, Over input voltage range			150	PPM/°C
EIR	Effective input resistance		2.5			MΩ
t_{CONV}	Conversion Time	Single conversion		250		ms
Eff_Res	Effective Resolution	Single conversion	15			Bits
Current Protection Thresholds						
V_{OCD}	OCD detection threshold voltage range	$V_{OCD} = V_{SRP} – V_{SRN}$, PROTECTION_CONTROL[RSNS] = 1	–16.6		–100	mV
		$V_{OCD} = V_{SRP} – V_{SRN}$, PROTECTION_CONTROL[RSNS] = 0	–8.3		–50	mV

Electrical Characteristics (continued)

Typical values stated where T_A = 25°C and VCC = 21.6 V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2 V to 32 V unless otherwise noted

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
ΔV_{OCD}	OCD detection threshold voltage program step	$V_{OCD} = V_{SRP} – V_{SRN}$, PROTECTION_CONTROL[RSNS] = 1		–5.56		mV
		$V_{OCD} = V_{SRP} – V_{SRN}$, PROTECTION_CONTROL[RSNS] = 0		–2.78		mV
V_{SCC}	SCC detection threshold voltage range	$V_{SCC} = V_{SRP} – V_{SRN}$, PROTECTION_CONTROL[RSNS] = 1	44.4		200	mV
		$V_{SCC} = V_{SRP} – V_{SRN}$, PROTECTION_CONTROL[RSNS] = 0	22.2		100	mV
ΔV_{SCC}	SCC detection threshold voltage program step	$V_{SCC} = V_{SRP} – V_{SRN}$, PROTECTION_CONTROL[RSNS] = 1		22.2		mV
		$V_{SCC} = V_{SRP} – V_{SRN}$, PROTECTION_CONTROL[RSNS] = 0		11.1		mV
V_{SCD1}	SCD1 detection threshold voltage range	$V_{SCD1} = V_{SRP} – V_{SRN}$, PROTECTION_CONTROL[RSNS] = 1	–44.4		–200	mV
		$V_{SCD1} = V_{SRP} – V_{SRN}$, PROTECTION_CONTROL[RSNS] = 0	–22.2		–100	mV
ΔV_{SCD1}	SCD1 detection threshold voltage program step	$V_{SCD1} = V_{SRP} – V_{SRN}$, PROTECTION_CONTROL[RSNS] = 1		–22.2		mV
		$V_{SCD1} = V_{SRP} – V_{SRN}$, PROTECTION_CONTROL[RSNS] = 0		–11.1		mV
V_{SCD2}	SCD2 detection threshold voltage range	$V_{SCD2} = V_{SRP} – V_{SRN}$, PROTECTION_CONTROL[RSNS] = 1	–44.4		–200	mV
		$V_{SCD2} = V_{SRP} – V_{SRN}$, PROTECTION_CONTROL[RSNS] = 0	–22.2		–100	mV
ΔV_{SCD2}	SCD2 detection threshold voltage program step	$V_{SCD2} = V_{SRP} – V_{SRN}$, PROTECTION_CONTROL[RSNS] = 1		–22.2		mV
		$V_{SCD2} = V_{SRP} – V_{SRN}$, PROTECTION_CONTROL[RSNS] = 0		–11.1		mV
V_{OFFSET}	OCD, SCC, and SCDx offset error	Post-trim	–2.5		2.5	mV
V_{SCALE}	OCD, SCC, and SCDx scale error	No trim	–10%		10%	
		Post-trim	–5%		5%	
Current Protection Timing						
t_{OCD}	OCD detection delay time		1		31	ms
Δt_{OCD}	OCD detection delay time program step			2		ms
t_{SCC}	SCC detection delay time		0		915	µs
Δt_{SCC}	SCC detection delay time program step			61		µs

Electrical Characteristics (continued)

Typical values stated where T_A = 25°C and VCC = 21.6 V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2 V to 32 V unless otherwise noted

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
t_{SCD1}	SCD1 detection delay time	PROTECTION_CONTROL[SCDDx2] = 0	0		915	µs
		PROTECTION_CONTROL[SCDDx2] = 1	0		1850	µs
Δt_{SCD1}	SCD1 detection delay time program step	PROTECTION_CONTROL[SCDDx2] = 0		61		µs
		PROTECTION_CONTROL[SCDDx2] = 1		121		µs
t_{SCD2}	SCD2 detection delay time	PROTECTION_CONTROL[SCDDx2] = 0	0		458	µs
		PROTECTION_CONTROL[SCDDx2] = 1	0		915	µs
Δt_{SCD2}	SCD2 detection delay time program step	PROTECTION_CONTROL[SCDDx2] = 0		30.5		µs
		PROTECTION_CONTROL[SCDDx2] = 1		61		µs
t_{DETECT}	Current fault detect time	$V_{SRP} – V_{SRN} = V_T – 3$ mV for OCD, SCD1 and SCD2, $V_{SRP} – V_{SRN}$ = VT – 3 mV for SCC			160	µs
t_{ACC}	Current fault delay time accuracy	Max delay setting	–10%		10%	
Internal Temperature Sensor						
V_{TEMPT}	Internal temperature sensor voltage drift	V_{TEMPP}	–1.9		–2.1	mV/°C
		$V_{TEMPP} – V_{TEMPN}$, assured by design	0.177	0.178	0.179	mV/°C
NTC Thermistor Measurement Support (TS1, TS2, Pins 12 and 13 configured as TS3 and TS4)						
$R_{NTC(PU)}$	Internal pullup resistance	TS1	14.4	18	21.6	kΩ
		TS2	14.4	18	21.6	kΩ
		TS3	14.4	18	21.6	kΩ
		TS4	14.4	18	21.6	kΩ
$R_{NTC(DRIFT)}$			–360	–280	–200	PPM/°C
Low-Voltage General Purpose I/O (Multifunction Pins 12 and 13 configured as GPIO)						
V_{IH}	High-level input		0.65 × V_{REG}			V
V_{IL}	Low-level input				0.35 × V_{REG}	V
V_{OH}	Output voltage high	Output high, pullup enabled, I_{OH} = –1.0 mA	0.75 × V_{REG}			V
		Output high, pullup enabled, I_{OH} = –10 µA				
V_{OL}	Output voltage low	Output Low, I_{OL} = 1mA			0.2 × V_{REG}	V
C_{IN}	Input capacitance			5		pF
I_{LKG}	Input leakage current				1	µA
High-Voltage General Purpose I/O (multifunction pins 15, 16, 17 configured as GPIO, $\overline{PRES}$, $\overline{DISP}$, or $\overline{SHUTDN}$; Pin 15 configured as VC7EN; Pin 16 configured as PDSG)						
V_{IH}	High-level input		1.3			V
V_{IL}	Low-level input				0.55	V
V_{OH}	Output voltage high	Output enabled, V_{BAT} > 5.5 V, I_{OH} = –0 µA	3.5			V
		Output enabled, V_{BAT} > 5.5 V, I_{OH} = –10 µA	1.8			
V_{OL}	Output voltage low	Output disabled, I_{OL} = 1.5 mA			0.4	V

Electrical Characteristics (continued)

Typical values stated where T_A = 25°C and VCC = 21.6 V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2 V to 32 V unless otherwise noted

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
C_{IN}	Input capacitance			5		pF
I_{LKG}	Input leakage current				3	µA
R_O	Output reverse resistance	Between GPIO, $\overline{PRES}$, $\overline{DISP}$, SHUTDN, VC7EN, PDSG, and PBI	8			kΩ
General Purpose I/O with Constant Current Sink (Multifunction Pins 20, 21, 22 configured as LEDCNTLx)						
V_{IH}	High-level input	LEDCNTLx	1.45			V
V_{IL}	Low-level input	LEDCNTLx			0.55	V
V_{OH}	Output voltage high	LEDCNTLx, Output Enabled, V_{BAT} > 3.0 V, I_{OH} = –22.5 mA	V_{BAT} – 1.6			V
V_{OL}	Output voltage low	LEDCNTLx, Output Disabled, V_{BAT} > 3.0 V, I_{OH} = 3 mA			0.4	V
I_{SC}	High level output current protection	LEDCNTLx	–30	–45	–60	mA
I_{OL}	Low level output current	LEDCNTLx, V_{BAT} > 3.0 V, V_{OL} > 0.4 V	15.75	22.5	29.25	mA
$I_{LEDCNTLx}$	Current matching between outputs	LEDCNTLx, V_{BAT} = V_{LED} + 2.5 V		+/–1%		
C_{IN}	Input capacitance	LEDCNTLx		20		pF
I_{LKG}	Input leakage current	LEDCNTLx			1	µA
f_{LED}	Frequency of LED pattern	LEDCNTLx		124		Hz
$t_{SHUTDOWN}$	Thermal shutdown	LEDCNTLx, assured by design	120	135	150	°C
General Purpose I/O (Multifunction Pins 20, 21, 22 configured as GPIO) (Pin 20 configured as PDSG)						
V_{IH}	High-level input		1.45			V
V_{IL}	Low-level input				0.55	V
V_{OH}	Output voltage high	Output enabled, V_{BAT} > 3.0 V, I_{OH} = –22.5 mA	V_{BAT} – 1.6			V
		Output disabled, I_{OL} = 3 mA			0.4	V
I_{SC}	High level output current protection		–30	–45	–60	mA
I_{OL}	Low level output current	V_{BAT} > 3.0 V, V_{OL} > 0.4 V	15.75	22.5	29.25	mA
C_{IN}	Input capacitance			20		pF
I_{LKG}	Input leakage current				1	uA
SMBD, SMBC High Voltage I/O						
V_{IH}	Input voltage high	SMBC, SMBD, V_{REG} = 1.8 V	1.3			V
V_{IL}	Input voltage low	SMBC, SMBD, V_{REG} = 1.8 V			0.8	V
V_{OL}	Output low voltage	SMBC, SMBD, V_{REG} = 1.8 V, I_{OL} = 1.5 mA			0.4	V
C_{IN}	Input capacitance			5		pF
I_{LKG}	Input leakage current				1	µA
R_{PD}	Pulldown resistance		0.7	1	1.3	MΩ
SMBus						
f_{SMB}	SMBus operating frequency	SLAVE mode, SMBC 50% duty cycle	10		100	kHz
f_{MAS}	SMBus master clock frequency	MASTER mode, no clock low slave extend		51.2		kHz
t_{BUF}	Bus free time between start and stop		4.7			µs
$t_{HD(START)}$	Hold time after (repeated) start		4			µs
$t_{SU(START)}$	Repeated start setup time		4.7			µs
$t_{SU(STOP)}$	Stop setup time		4			µs
$t_{HD(DATA)}$	Data hold time		300			ns
$t_{SU(DATA)}$	Data setup time		250			ns

Electrical Characteristics (continued)

Typical values stated where T_A = 25°C and VCC = 21.6 V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2 V to 32 V unless otherwise noted

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
$t_{TIMEOUT}$	Error signal detect time		25		35	ms
t_{LOW}	Clock low period		4.7			µs
t_{HIGH}	Clock high period		4		50	µs
t_R	Clock rise time	10% to 90%			1000	ns
t_F	Clock fall time	90% to 10%			300	ns
$t_{LOW(SEXT)}$	Cumulative clock low slave extend time				25	ms
$t_{LOW(MEXT)}$	Cumulative clock low master extend time				10	ms
SMBus XL						
f_{SMBXL}	SMBus XL operating frequency	SLAVE mode, SMBC 50% duty cycle	40		400	kHz
t_{BUF}	Bus free time between start and stop		4.7			µs
$t_{HD(START)}$	Hold time after (repeated) start		4			µs
$t_{SU(START)}$	Repeated start setup time		4.7			µs
$t_{SU(STOP)}$	Stop setup time		4			µs
$t_{TIMEOUT}$	Error signal detect time		5		20	ms
t_{LOW}	Clock low period				20	µs
t_{HIGH}	Clock high period				20	µs
FUSE Drive (AFEFUSE)						
V_{OH}	Output voltage high	V_{BAT} ≥ 8 V, C_L = 1 nF, $I_{AFEFUSE}$ = 0 µA	6	7	8.65	V
		V_{BAT} < 8 V, C_L = 1 nF, $I_{AFEFUSE}$ = 0 µA	V_{BAT} – 0.1		V_{BAT}	V
V_{IH}	High-level input		1.5	2	2.5	V
$I_{AFEFUSE(PU)}$	Internal pullup current	V_{BAT} < 8 V, $V_{AFEFUSE}$ = VSS		150	330	nA
$R_{AFEFUSE}$	Output impedance		2	2.6	3.2	kΩ
C_{IN}	Input capacitance			5		pF
t_{DELAY}	Fuse trim detection delay		128		256	µs
t_{RISE}	Fuse output rise time			5	20	µs
N-CH FET Drive (CHG, DSG)						
	Output voltage ratio	$Ratio_{DSG}$ = (V_{DSG} – V_{BAT}) / V_{BAT}, 2.2 V < V_{BAT} < 4.92 V, 10 MΩ between PACK and DSG	2.133	2.333	2.45	—
		$Ratio_{CHG}$ = (V_{CHG} – V_{BAT}) / V_{BAT}, 2.2 V < V_{BAT} < 4.92 V, 10 MΩ between BAT and CHG	2.133	2.333	2.433	—
V_{FETON}	Output voltage, CHG and DSG on	$V_{DSG(ON)}$ = (V_{DSG} – V_{BAT}), V_{BAT} ≥ 4.92 V (up to 32 V), 10 MΩ between PACK and DSG	10.5	11.5	12.5	V
		$V_{CHG(ON)}$ = (V_{CHG} – V_{BAT}), V_{BAT} ≥ 4.92 V (up to 32 V), 10 MΩ between BAT and CHG	10.5	11.5	12.5	V
V_{FETOFF}	Output voltage, CHG and DSG off	$V_{DSG(OFF)}$ = (V_{DSG} – V_{PACK}), 10 MΩ between PACK and DSG	–0.4		0.4	V
		$V_{CHG(OFF)}$ = (V_{CHG} – V_{BAT}), 10 MΩ between BAT and CHG	–0.4		0.4	V

Electrical Characteristics (continued)

Typical values stated where T_A = 25°C and VCC = 21.6 V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2 V to 32 V unless otherwise noted

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
t_R	Rise time	V_{DSG} from 0% to 35% $V_{DSG(ON)(TYP)}$, V_{BAT} ≥ 2.2 V, C_L = 4.7 nF between DSG and PACK, 5.1 kΩ between DSG and C_L, 10 MΩ between PACK and DSG		200	500	µs
		V_{CHG} from 0% to 35% $V_{CHG(ON)(TYP)}$, V_{BAT} ≥ 2.2 V, C_L = 4.7 nF between CHG and BAT, 5.1 kΩ between CHG and C_L, 10 MΩ between BAT and CHG		200	500	µs
t_F	Fall time	V_{DSG} from $V_{DSG(ON)(TYP)}$ to 1 V, V_{BAT} ≥ 2.2 V, C_L = 4.7 nF between DSG and PACK, 5.1 kΩ between DSG and C_L, 10 MΩ between PACK and DSG		40	300	µs
		V_{CHG} from $V_{CHG(ON)(TYP)}$ to 1 V, V_{BAT} ≥ 2.2 V, C_L = 4.7 nF between CHG and BAT, 5.1 kΩ between CHG and C_L, 10 MΩ between BAT and CHG		40	200	µs
P-CH FET Drive (PCHG)						
V_{FETON}	Output voltage, PCHG on	$V_{PCHG(ON)} = V_{CC} – V_{PCHG}$, 10 MΩ between VCC and CHG, V_{BAT} ≥ 8 V	6	7	8	V
V_{FETOFF}	Output voltage, PCHG off	$V_{PCHG(OFF)} = V_{CC} – V_{PCHG}$, 10 MΩ between VCC and CHG	–0.4		0.4	V
t_R	Rise time	V_{PCHG} from 10% to 90% $V_{PCHG(ON)(TYP)}$, V_{SS} ≥ 8 V, C_L = 4.7 nF between PCHG and VCC, 5.1 kΩ between PCHG and C_L, 10 MΩ between VCC and CHG		40	200	µs
t_F	Fall time	V_{PCHG} from 90% to 10% $V_{PCHG(ON)(TYP)}$, V_{SS} ≥ 8 V, C_L = 4.7 nF between PCHG and VCC, 5.1 kΩ between PCHG and C_L, 10 MΩ between VCC and CHG		40	200	µs
High-Frequency Oscillator						
f_{HFO}	Operating frequency			16.78		MHz
$f_{HFO(ERR)}$	Frequency error	T_A = –20°C to 70°C, includes frequency drift	–2.5%	±0.25%	2.5%	
		T_A = –40°C to 85°C, includes frequency drift	–3.5%	±0.25%	3.5%	
$t_{HFO(SU)}$	Start-up time	T_A = –20°C to 85°C, ***CLKCTL[HFRAMP]*** = 1, oscillator frequency within ±3% of nominal			4	ms
		T_A = –20°C to 85°C, ***CLKCTL[HFRAMP]*** = 0, oscillator frequency within ±3% of nominal			100	µs
Low-Frequency Oscillator						
f_{LFO}	Operating frequency			262.144		kHz
$f_{LFO(ERR)}$	Frequency error	T_A = –20°C to 70°C, includes frequency drift	–1.5%	±0.25%	1.5%	
		T_A = –40°C to 85°C, includes frequency drift	–2.5%	±0.25%	2.5%	
$t_{LFO(FAIL)}$	Failure detection frequency		30	80	100	kHz
Instruction Flash						
	Data retention		10			Years
	Flash programming write cycles		1000			Cycles

Electrical Characteristics (continued)

Typical values stated where T_A = 25°C and VCC = 21.6 V, Min/Max values stated where T_A = –40°C to 85°C and VCC = 2.2 V to 32 V unless otherwise noted

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PROGWORD}$	Word programming time				40	µs
$t_{MASSERASE}$	Mass-erase time				40	ms
$t_{PAGEERASE}$	Page-erase time				40	ms
$t_{FLASHREAD}$	Flash-read current				2	mA
$t_{FLASHWRITE}$	Flash-write current				5	mA
$I_{FLASHERASE}$	Flash-erase current				15	mA
Data Flash						
	Data retention		10			Years
	Flash programming write cycles		20000			Cycles
$t_{PROGWORD}$	Word programming time				40	µs
$t_{MASSERASE}$	Mass-erase time				40	ms
$t_{PAGEERASE}$	Page-erase time				40	ms
$t_{FLASHREAD}$	Flash-read current				1	mA
$t_{FLASHWRITE}$	Flash-write current				5	mA
$I_{FLASHERASE}$	Flash-erase current				15	mA
ECC Authentication						
$I_{NORMAL+AUTH}$	NORMAL mode + Authentication	CPU active, CHG on. DSG on, High Frequency Oscillator on, Low Frequency Oscillator on, REG18 on, ADC on, ADC_Filter on, CC_Filter on, CC on, SMBus not active, Authentication Start		1350		µA
t_{SIGN}	EC-KCDSA signature signing time	3.8 V < VCC or BAT < 32 V		375		ms
	Number of Authentication operations		20000			Operations

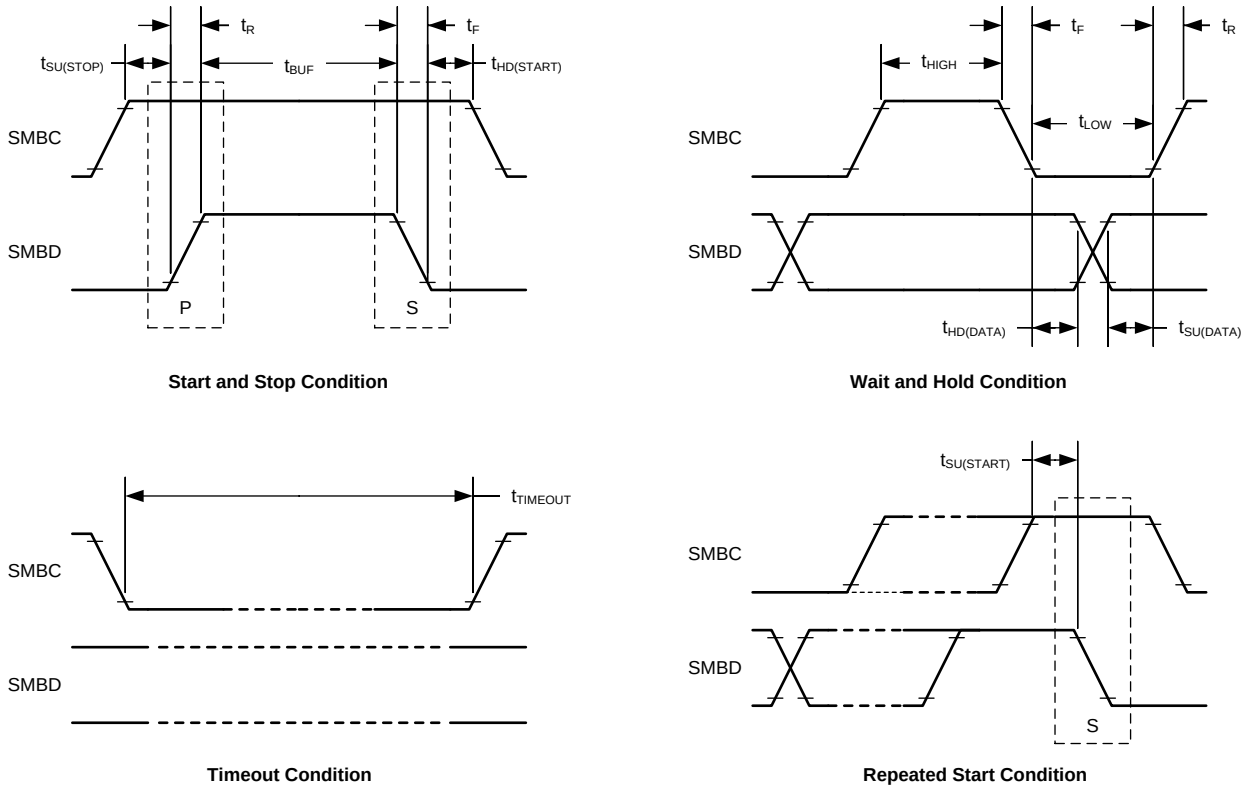


Figure 3. SMBus Timing Diagram

7.6 Typical Characteristics

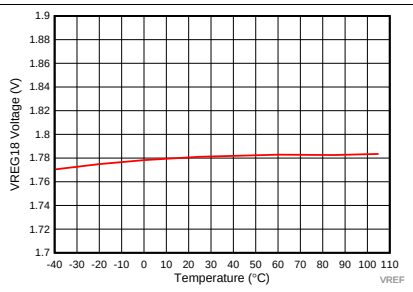


Figure 4. VREG 1.8-V Voltage vs. Temperature

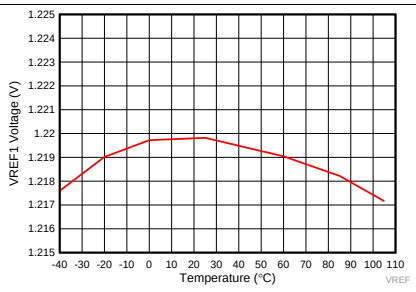


Figure 5. VREF 1 Voltage vs. Temperature

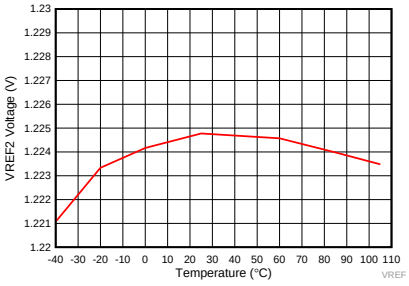


Figure 6. VREF 2 Voltage vs. Temperature

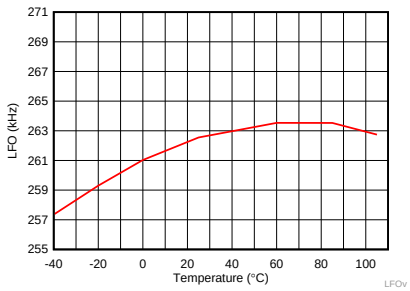


Figure 7. Low-Frequency Oscillator vs. Temperature

Typical Characteristics (continued)

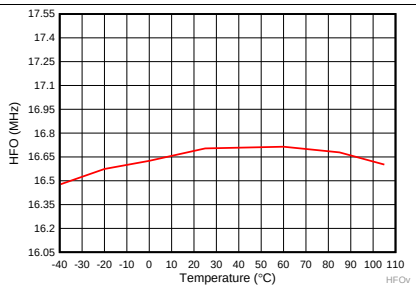


Figure 8. High-Frequency Oscillator vs. Temperature

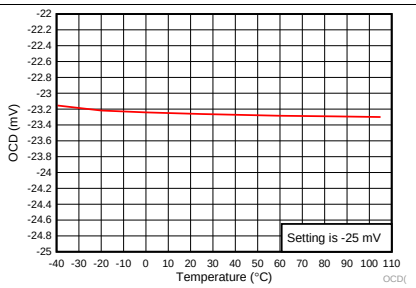


Figure 9. Overcurrent Discharge Protection Threshold vs. Temperature

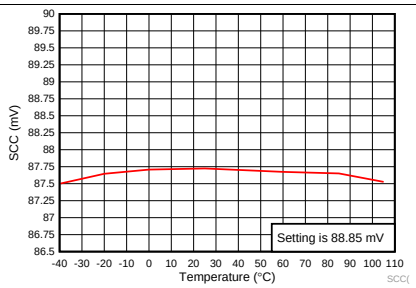


Figure 10. Short Circuit Charge Protection Threshold vs. Temperature

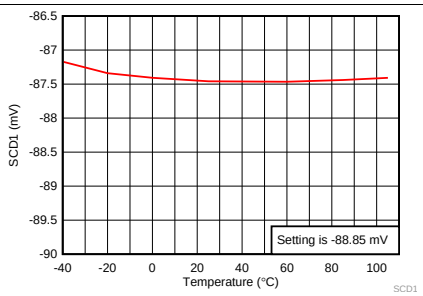
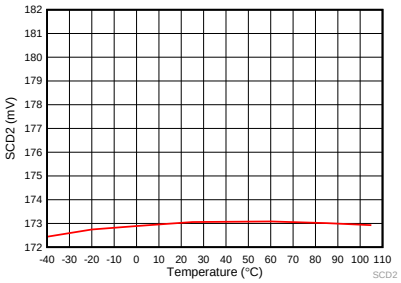


Figure 11. Short Circuit Discharge 1 Protection Threshold vs. Temperature



Threshold setting is –177.7 mV.

Figure 12. Short Circuit Discharge 2 Protection Threshold vs. Temperature

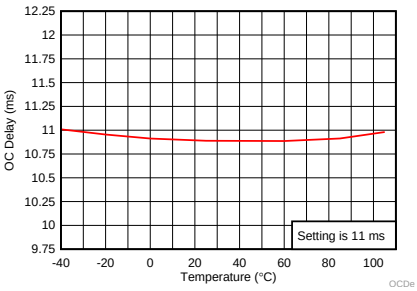


Figure 13. Overcurrent Delay Time vs. Temperature

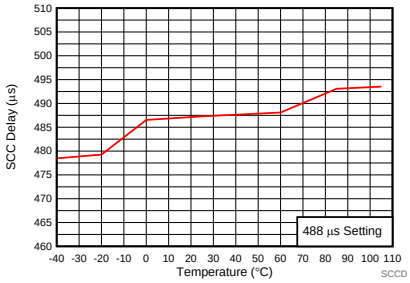


Figure 14. Short Circuit Charge Current Delay Time vs. Temperature

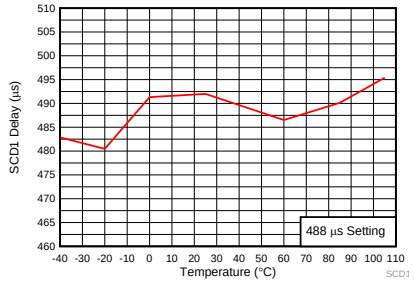


Figure 15. Short Circuit Discharge 1 Delay Time vs. Temperature

Typical Characteristics (continued)

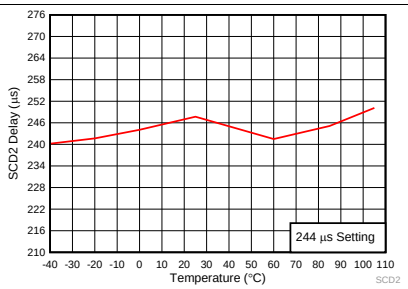


Figure 16. Short Circuit Discharge 2 Delay Time vs. Temperature

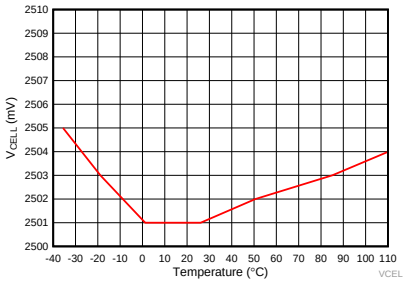
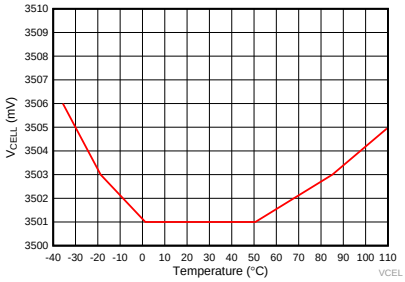
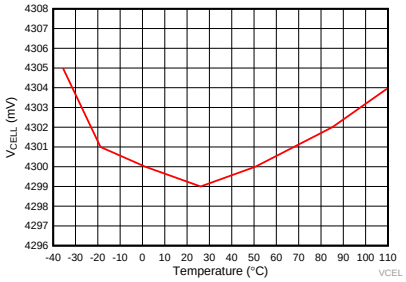


Figure 17. V_{CELL} Measurement at 2.5-V vs. Temperature



This is the V_{CELL} average for single cell.

Figure 18. V_{CELL} Measurement at 3.5 V vs. Temperature



This is the V_{CELL} average for single cell.

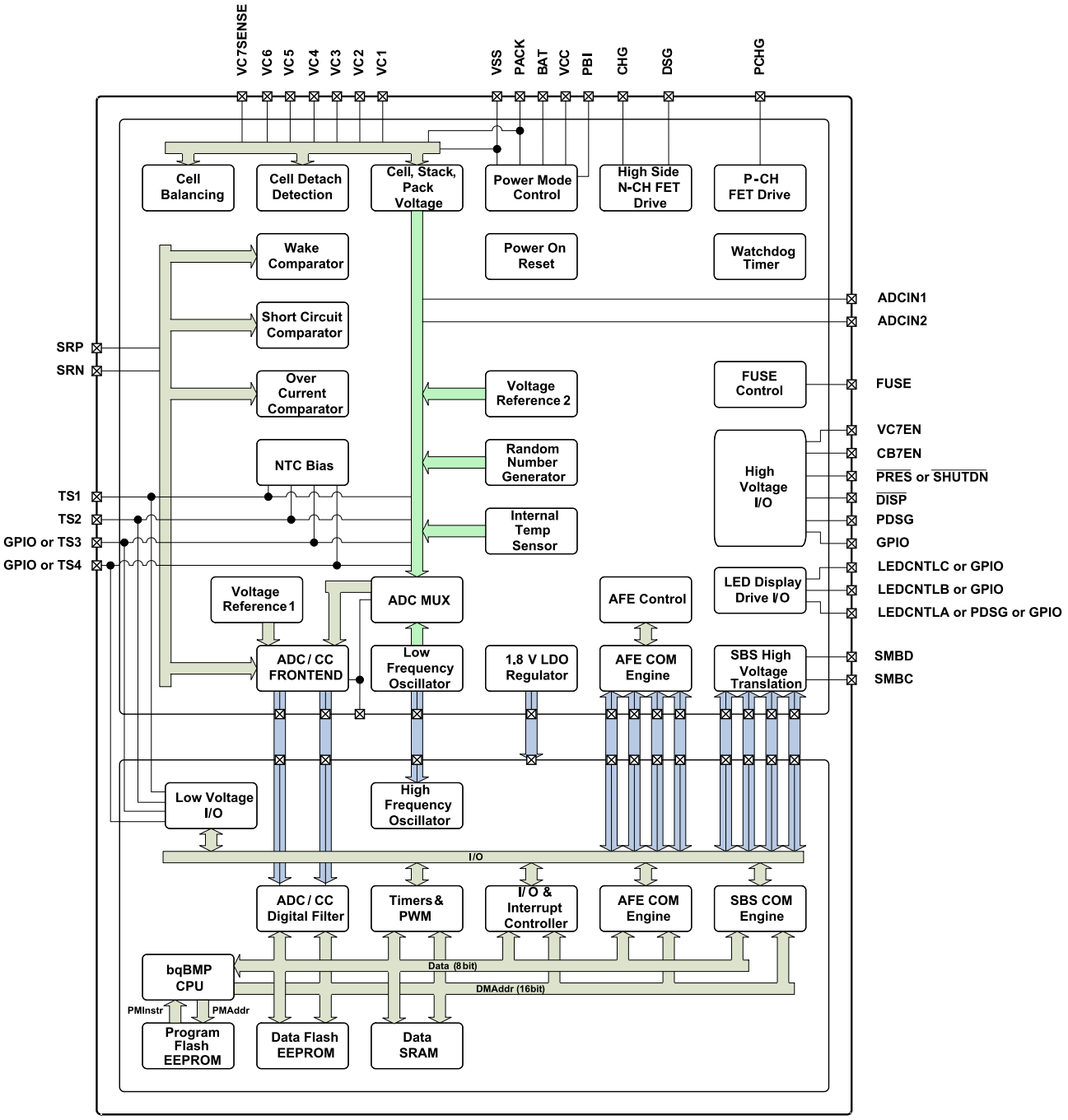
Figure 19. V_{CELL} Measurement at 4.3 V vs. Temperature

8 Detailed Description

8.1 Overview

The bq40z80 device, incorporating patented Impedance Track™ technology, provides cell balancing while charging or at rest. This fully integrated, single-chip, PACK–based solution provides a rich array of features for gas gauging, protection, and authentication for 2-series to 7-series cell Li-Ion and Li-Polymer battery packs, including a diagnostic lifetime data monitor and black box recorder.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Primary (1st Level) Safety Features

The bq40z80 supports a wide range of battery and system protection features that can easily be configured. See the *bq40z80 Technical Reference Manual* (SLUUBT5) for detailed descriptions of each protection function.

The primary safety features include:

- Cell Overvoltage Protection
- Cell Undervoltage Protection
- Cell Undervoltage Protection Compensated
- Overcurrent in Charge Protection
- Overcurrent in Discharge Protection
- Overload in Discharge Protection
- Short Circuit in Charge Protection
- Short Circuit in Discharge Protection
- Overtemperature in Charge Protection
- Overtemperature in Discharge Protection
- Undertemperature in Charge Protection
- Undertemperature in Discharge Protection
- Overtemperature FET protection
- Precharge Timeout Protection
- Host Watchdog Timeout Protection
- Fast Charge Timeout Protection
- Overcharge Protection
- Overcharging Voltage Protection
- Overcharging Current Protection
- Over Precharge Current Protection

8.3.2 Secondary (2nd Level) Safety Features

The secondary safety features of the bq40z80 can be used to indicate more serious faults via the FUSE pin. This pin can be used to blow an in-line fuse to permanently disable the battery pack from charging or discharging. See the *bq40z80 Technical Reference Manual* (SLUUBT5) for detailed descriptions of each protection function.

The secondary safety features provide protection against:

- Safety Overvoltage Permanent Failure
- Safety Undervoltage Permanent Failure
- Safety Overtemperature Permanent Failure
- Safety FET Overtemperature Permanent Failure
- Qmax Imbalance Permanent Failure
- Impedance Imbalance Permanent Failure
- Capacity Degradation Permanent Failure
- Cell Balancing Permanent Failure
- Fuse Failure Permanent Failure
- Voltage Imbalance at Rest Permanent Failure
- Voltage Imbalance Active Permanent Failure
- Charge FET Permanent Failure
- Discharge FET Permanent Failure
- AFE Register Permanent Failure
- AFE Communication Permanent Failure
- Second Level Protector Permanent Failure
- Instruction Flash Checksum Permanent Failure

Feature Description (continued)

- Open Cell Connection Permanent Failure
- Data Flash Permanent Failure
- Open Thermistor Permanent Failure

8.3.3 Charge Control Features

The bq40z80 charge control features include:

- Supports JEITA temperature ranges. Reports charging voltage and charging current according to the active temperature range
- Handles more complex charging profiles. Allows for splitting the standard temperature range into two sub-ranges and allows for varying the charging current according to the cell voltage
- Reports the appropriate charging current needed for constant current charging and the appropriate charging voltage needed for constant voltage charging to a smart charger using SMBus broadcasts
- Reduces the charge difference of the battery cells in fully charged state of the battery pack gradually using a voltage-based cell balancing algorithm during charging. A voltage threshold can be set up for cell balancing to be active. This prevents fully charged cells from overcharging and causing excessive degradation and also increases the usable pack energy by preventing premature charge termination.
- Supports charge inhibit and charge suspend if battery pack temperature is out of temperature range
- Reports charging fault and also indicates charge status via charge and discharge alarms

8.3.4 Gas Gauging

The bq40z80 uses the Impedance Track algorithm to measure and calculate the available capacity in battery cells. The bq40z80 accumulates a measure of charge and discharge currents and compensates the charge current measurement for the temperature and state-of-charge of the battery. The bq40z80 estimates self-discharge of the battery and also adjusts the self-discharge estimation based on temperature. The device also has TURBO Mode 2.0/DBPTv2 support, which enables the bq40z80 to provide the necessary data for the MCU to determine what level of peak power consumption can be applied without causing a system reset or transient battery voltage level spike to trigger termination flags. See the *bq40z80 Technical Reference Manual* (SLUUBT5) for further details.

8.3.5 Multifunction Pins

The bq40z80 includes several multifunction pins that firmware uses to implement different functions. Figure 20 is a simplified schematic of an example system implementation that uses a 7-series pack with PRECHARGE mode, six LEDs, two thermistors, and system-present functionality.

Feature Description (continued)

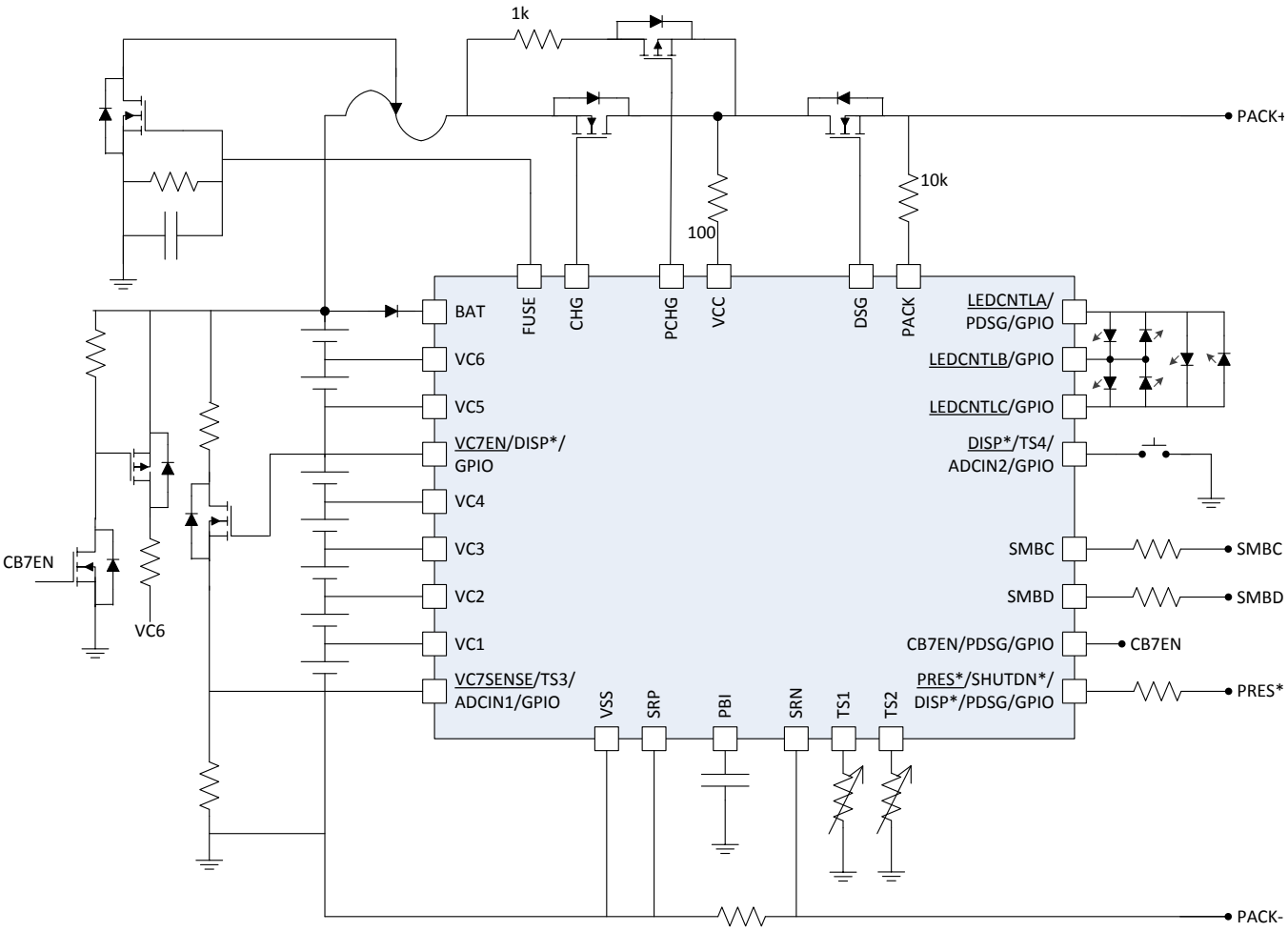


Figure 20. Simplified Schematic of a bq40z80 Configuration

Table 1 shows a summary of other common configurations.

Table 1. bq40z80 Multifunction Pin Combinations

Number of Cells (with Balancing)	Number of Thermistors	LEDs	LED Button	Pre-Discharge	SYSPRES
2S–6S	4	Yes	Yes (use VC7EN)	Yes (uses CB7EN)	Yes
7S	3	Yes	Yes (use PRES)	No	No
7S	2	Yes	Yes (use TS4)	No	Yes
7S	2	Yes	Yes (use TS4)	Yes (uses PRES)	No
7S	3	Yes	No	Yes (uses PRES)	No
7S	3	Yes	No	No	Yes
7S	3	No	No	Yes (uses LEDCNTLA)	Yes

8.3.6 Configuration

8.3.6.1 Oscillator Function

The bq40z80 fully integrates the system oscillators and does not require any external components to support this feature.

8.3.6.2 System Present Operation

The bq40z80 checks the $\overline{\text{PRES}}$ pin periodically (1 s). If $\overline{\text{PRES}}$ input is pulled to ground by the external system, the bq40z80 detects this as system present.

8.3.6.3 Emergency Shutdown

For battery maintenance, the emergency shutdown feature enables a push button action connecting the $\overline{\text{SHUTDN}}$ pin to shut down an embedded battery pack system before removing the battery. A high-to-low transition of the $\overline{\text{SHUTDN}}$ pin signals the bq40z80 to turn off both CHG and DSG FETs, disconnecting the power from the system to safely remove the battery pack. The CHG and DSG FETs can be turned on again by another high-to-low transition detected by the $\overline{\text{SHUTDN}}$ pin or when a data flash configurable timeout is reached.

8.3.6.4 2-Series, 3-Series, 4-Series, 5-Series, 6-Series, or 7-Series Cell Configuration

In a 2-series cell configuration, VC6 is shorted to VC5, VC4, VC3, and VC2. In a 3-series cell configuration, VC6 is shorted to VC5, VC4, and VC3. In a 4-series cell configuration, VC6 is shorted to VC5 and VC4. In a 5-series cell configuration, VC6 is shorted to VC5.

In a 7-series cell configuration, Pin 12 is configured as VC7SENSE and the pin is used as an ADC input to digitize the output of an external divider from the top of the stack. For best ADC performance, the voltage at this pin should be limited to between 0 V and 1.0 V. In this mode, the top of the stack can be up to 32 V, so a divider of approximately 32:1 or larger is generally needed. The external divider is enabled by an NFET switch controlled using the VC7EN signal from Pin 15 of the bq40z80 device.

8.3.6.5 Cell Balancing

For up to a 6-series cell configuration, the device supports cell balancing by bypassing the current of each cell during charging or at rest. If the device's internal bypass is used, up to 10 mA can be bypassed and multiple cells can be bypassed at the same time. A higher cell balance current can be achieved by using an external cell balancing circuit. In EXTERNAL CELL BALANCING mode, only one cell at a time can be balanced.

The cell balancing algorithm determines the amount of charge needed to be bypassed to balance the capacity of all cells.

Use multifunction Pin 16 (CB7EN/PDSG/GPIO) to enable cell balancing for the 7-series cell. When this mode is selected, this pin becomes an enable pin, causing an NFET to pull down a PFET gate. The PFET enables/disables the external cell balancing circuit for the seventh cell. This pin is driven high to turn on the NFET and PFET, and enable cell balancing. This pin is driven low to turn off the NFET and let the PFET gate be pulled high, disabling the divider. A pullup resistor from the PFET gate to BAT ensures that the PFET gate turns off when the pin is driven low and the NFET is off. A pulldown resistor from the NFET gate to VSS ensures that the NFET turns off while the gauge is in SHUTDOWN mode, and the pin is hi-Z.

8.3.7 Battery Parameter Measurements

8.3.7.1 Charge and Discharge Counting

The bq40z80 uses an integrating delta-sigma analog-to-digital converter (ADC) for current measurement, and a second delta-sigma ADC for individual cell and battery voltage and temperature measurement.

The integrating delta-sigma ADC measures the charge/discharge flow of the battery by measuring the voltage drop across a small-value sense resistor between the SRP and SRN terminals. The integrating ADC measures bipolar signals from –0.1 V to 0.1 V. The bq40z80 detects charge activity when $V_{SR} = V_{(SRP)} – V_{(SRN)}$ is positive, and discharge activity when $V_{SR} = V_{(SRP)} – V_{(SRN)}$ is negative. The bq40z80 continuously integrates the signal over time, using an internal counter. The fundamental rate of the counter is 0.26 nVh.

8.3.8 Lifetime Data Logging Features

The bq40z80 offers lifetime data logging for several critical battery parameters. The following parameters are updated every 10 hours if a difference is detected between values in RAM and data flash:

- Maximum and Minimum Cell Voltages
- Maximum Delta Cell Voltage
- Maximum Charge Current

- Maximum Discharge Current
- Maximum Average Discharge Current
- Maximum Average Discharge Power
- Maximum and Minimum Cell Temperature
- Maximum Delta Cell Temperature
- Maximum and Minimum Internal Sensor Temperature
- Maximum FET Temperature
- Number of Safety Events Occurrences and the Last Cycle of the Occurrence
- Number of Valid Charge Termination and the Last Cycle of the Valid Charge Termination
- Number of Qmax and Ra Updates and the Last Cycle of the Qmax and Ra Updates
- Number of Shutdown Events
- Cell Balancing Time for Each Cell
  (This data is updated every two hours if a difference is detected.)
- Total FW Runtime and Time Spent in Each Temperature Range
  (This data is updated every two hours if a difference is detected.)

8.3.9 Authentication

To support host authentication, the bq40z80 uses Elliptic Curve Cryptography (ECC), which requires a strong 163-bit key system for the authentication process. Additionally, the private key is required to be stored only in the bq40z80 Battery Pack Manager, which makes key management more simple and secure. See the *bq40z80 Technical Reference Manual* (SLUUBT5) for further details.

8.3.10 LED Display

The bq40z80 can drive a 3-, 4-, or 5- segment LED display for remaining capacity indication and/or a permanent fail (PF) error code indication.

8.3.11 IATA Support

The bq40z80 supports IATA with several new commands and procedures. See the *bq40z80 Technical Reference Manual* (SLUUBT5) for further details.

8.3.12 Voltage

The bq40z80 updates the individual series cell voltages at TBD-second intervals. The internal ADC of the bq40z80 measures the voltage, and scales and calibrates it appropriately. This data is also used to calculate the impedance of the cell for the Impedance Track gas gauging.

8.3.13 Current

The bq40z80 uses the SRP and SRN inputs to measure and calculate the battery charge and discharge current using a 1-mΩ to 3-mΩ typ. sense resistor.

8.3.14 Temperature

The bq40z80 has an internal temperature sensor and inputs for up to four external temperature sensors. All five temperature sensor options can be individually enabled and configured for cell or FET temperature usage. Two configurable thermistor models are provided to allow the monitoring of cell temperature in addition to FET temperature, which use a different thermistor profile.

8.3.15 Communications

The bq40z80 uses SMBus v1.1 with MASTER mode and packet error checking (PEC) options per the SBS specification.

8.3.15.1 SMBus On and Off State

The bq40z80 detects an SMBus off state when SMBC and SMBD are low for two or more seconds. Clearing this state requires that either SMBC or SMBD transition high. The communication bus will resume activity within 1 ms.

8.3.15.2 SBS Commands

See the *bq40z80 Technical Reference Manual* (SLUUBT5) for further details.

8.4 Device Functional Modes

The bq40z80 supports three power modes to reduce power consumption:

- In NORMAL mode, the bq40z80 performs measurements, calculations, protection decisions, and data updates in 250-ms intervals. Between these intervals, the bq40z80 is in a reduced power stage.
- In SLEEP mode, the bq40z80 performs measurements, calculations, protection decisions, and data updates in adjustable time intervals. Between these intervals, the bq40z80 is in a reduced power stage. The bq40z80 has a wake function that enables exit from SLEEP mode when current flow or failure is detected.
- In SHUTDOWN mode, the bq40z80 is completely disabled.

9 Applications and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The bq40z80 is a gas gauge with primary protection support, and can be used with a 2-series to 7-series Li-Ion/Li-Polymer battery pack. To implement and design a comprehensive set of parameters for a specific battery pack, the Battery Management Studio (bqStudio) graphical user-interface tool must be installed on a PC during development.

9.2 Typical Applications

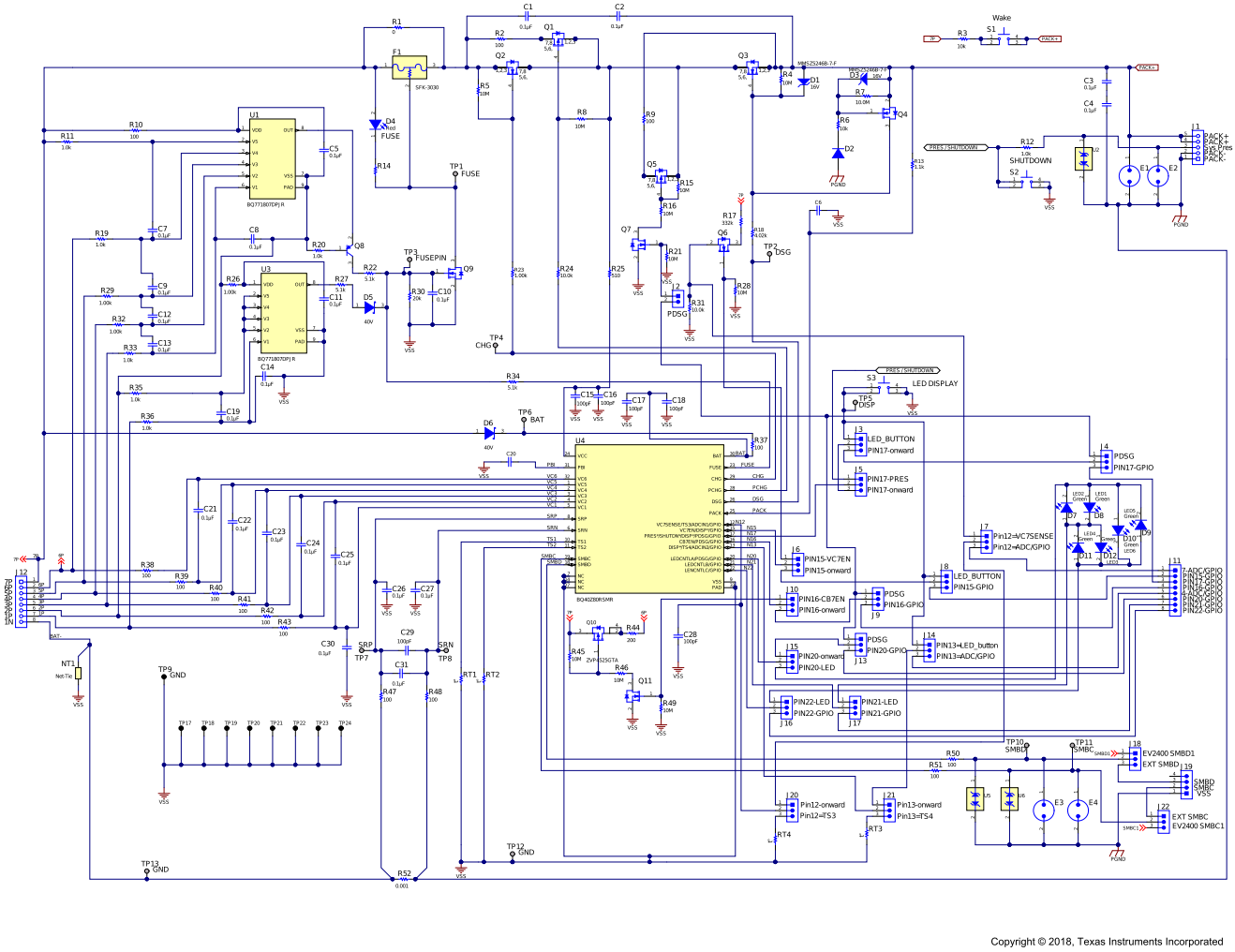


Figure 21. bq40z80EVM Gauge and Protector Schematic

Typical Applications (continued)

9.2.1 Design Requirements

Table 2 shows the default settings for the main parameters. Use the bqStudio tool to update the settings to meet the specific application or battery pack configuration requirements.

The device should be calibrated before any gauging test. Follow the bqStudio **Calibration** page to calibrate the device, and use the bqStudio **Chemistry** page to update the match chemistry profile to the device. *Design Parameters* shows all of the settings that are configurable in bqStudio and in the bq40z80 firmware.

Table 2. Design Parameters

DESIGN PARAMETER	EXAMPLE
Cell Configuration	7s (7-series)(1)
Design Capacity	6000 mAh
Device Chemistry	1210 ($LiCoO_2$/graphitized carbon)
Cell Overvoltage at Standard Temperature	4300 mV
Cell Undervoltage	2500 mV
Shutdown Voltage	2300 mV
Overcurrent in CHARGE Mode	6000 mA
Overcurrent in DISCHARGE Mode	–6000 mA
Short Circuit in CHARGE Mode	0.1 V/Rsense across SRP, SRN
Short Circuit in DISCHARGE Mode	0.1 V/Rsense across SRP, SRN
Safety Overvoltage	4500 mV
Cell Balancing	Disabled
Internal and External Temperature Sensor	External Temperature Sensor is used.
Undertemperature Charging	0°C
Undertemperature Discharging	0°C
BROADCAST Mode	Disabled

(1) When using the device the first time, if the a 1-s or 2-s battery pack is used, then a charger or power supply should be connected to the PACK+ terminal to prevent device shutdown. Then update the cell configuration (see the *bq40z80 Technical Reference Manual* [SLUUBT5] for details) before removing the charger connection.

9.2.2 Detailed Design Procedure

This application section uses the bq40z80 evaluation module (EVM) and jumper configurations to allow the user to evaluate many of the bq40z80 features.

9.2.2.1 Using the bq40z80EVM with bqStudio

The firmware installed on the bqStudio tool has bq40z80 default values, which are summarized in the *bq40z80 Technical Reference Manual* (SLUUBT5). Using the bqStudio tool, these default values can be changed to cater to specific application requirements during development once the system parameters, such as fault trigger thresholds for protection, enable/disable of certain features for operation, configuration of cells, chemistry that best matches the cell used, and more, are known.

9.2.2.2 High-Current Path

The high-current path begins at the PACK+ terminal of the battery pack. As charge current travels through the pack, it finds its way through protection FETs, a chemical fuse, the lithium-ion cells and cell connections, and the sense resistor, and then returns to the PACK– terminal. In addition, some components are placed across the PACK+ and PACK– terminals to reduce effects from electrostatic discharge.

9.2.2.2.1 Protection FETs

Select the N-CH charge and discharge FETs for a given application. For a 7-series cell application, the charge FET must be rated above the max voltage, and for this reason the TI CSD18504Q5A is used. The TI CSD18504Q5A is a 50-A, 40-V device with Rds(on) of 5.3 mΩ when the gate drive voltage is 10 V. For the discharge FET, it may see a higher voltage, and so the TI CSD18540Q5B is used. The TI CSD18540Q5B is a 100-A, 60-V device with Rds(on) of 1.8 mΩ when the gate drive voltage is 10 V.

If a precharge FET is used, R2 is calculated to limit the precharge current to the desired rate. Be sure to account for the power dissipation of the series resistor. The precharge current is limited to $(V_{CHARGER} - V_{BAT})/R2$ and maximum power dissipation is $(V_{CHARGER} - V_{BAT})^2/R2$.

The gates of all protection FETs are pulled to the source with a high-value resistor between the gate and source to ensure they are turned off if the gate drive is open.

Capacitors C1 and C2 help protect the FETs during an ESD event. Using two devices ensures normal operation if one becomes shorted. To have good ESD protection, the copper trace inductance of the capacitor leads must be designed to be as short and wide as possible. Ensure that the voltage rating of both C1 and C2 are adequate to hold off the applied voltage if one of the capacitors becomes shorted.

9.2.2.2.2 Chemical Fuse

The chemical fuse (Dexerials, Uchihashi, and so on) is ignited under command from either the bq771800 secondary voltage protection IC or from the FUSE pin of the gas gauge. Either of these events applies a positive voltage to the gate of Q9, which then sinks current from the third terminal of the fuse, causing it to ignite and open permanently.

It is important to carefully review the fuse specifications and match the required ignition current to that available from the N-CH FET. Ensure that the proper voltage, current, and Rds(on) ratings are used for this device. The fuse control circuit is discussed in detail in *FUSE Circuitry*.

9.2.2.2.3 Lithium-Ion Cell Connections

The important part about the cell connections is that high current flows through the top and bottom connections; therefore, the voltage sense leads at these points must be made with a Kelvin connection to avoid any errors due to a drop in the high-current copper trace. The location marked 6P indicates the Kelvin connection of the most positive directly measured battery node. The 7P terminal is connected by a voltage divider and the measurement of the most positive voltage in the stack is enabled using the VC7EN pin. The single-point connection at 1N to the low-current ground is needed to avoid an undesired voltage drop through long traces while the gas gauge is measuring the bottom cell voltage.

Figure 22 shows the connections for VC7SENSE, VC7EN, and CB7EN to implement the 7th cell.

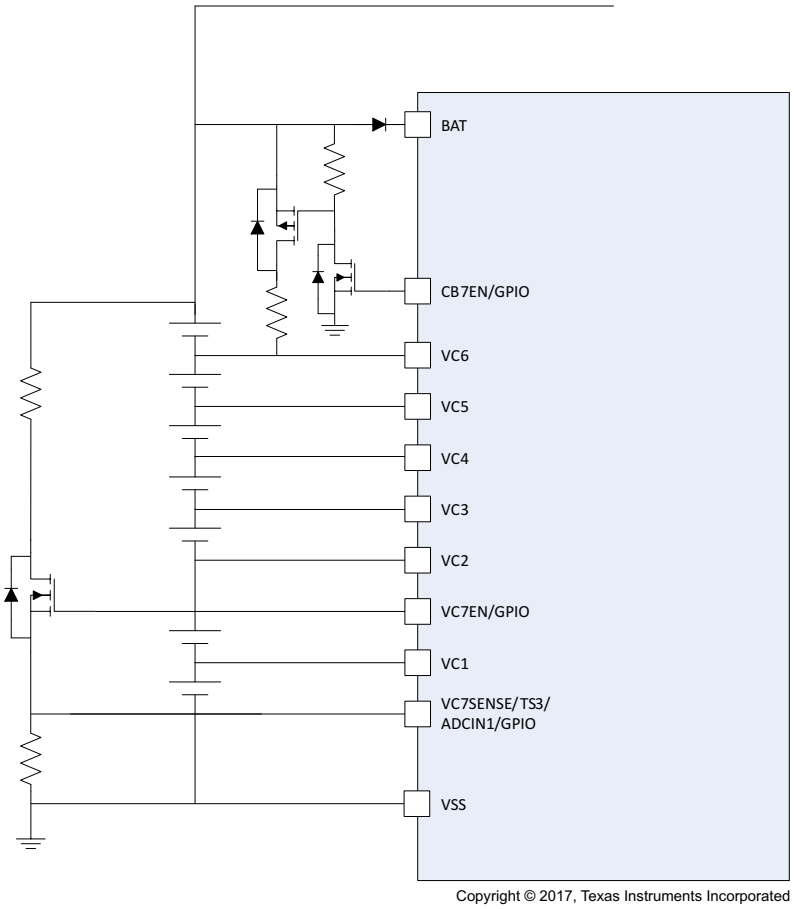


Figure 22. 7th-Cell Sense, Enable, and Cell Balancing

9.2.2.2.4 Sense Resistor

As with the cell connections, the quality of the Kelvin connections at the sense resistor is critical. The sense resistor must have a temperature coefficient no greater than 50 ppm to minimize current measurement drift with temperature. Choose the value of the sense resistor to correspond to the available overcurrent and short-circuit ranges of the bq40z80. Select the smallest value possible to minimize the negative voltage generated on the bq40z80 V_{SS} node(s) during a short circuit. This pin has an absolute minimum of –0.3 V. Parallel resistors can be used as long as good Kelvin sensing is ensured. The device is designed to support a 1-mΩ to 3-mΩ sense resistor, and a 1-mΩ sense resistor is used, shown as R52. When using 1-mΩ, large currents during a short circuit event can cause the voltage across the sense resistor to exceed the abs max of the pin. Therefore, it is required to place 100-Ω series resistors R47 and R48 as shown in the schematic.

9.2.2.2.5 ESD Mitigation

A pair of series 0.1-µF ceramic capacitors is placed across the PACK+ and PACK– terminals to help mitigate external electrostatic discharges. The two devices in series ensure continued operation of the pack if one of the capacitors becomes shorted.

Optionally, a transorb such as the SMBJ2A can be placed across the terminals to further improve ESD immunity.

9.2.2.3 Gas Gauge Circuit

The gas gauge circuit includes the bq40z80 and its peripheral components. These components are divided into the following groups: differential low-pass filter, PBI, system present, SMBus communication, FUSE circuit, and LED.

9.2.2.3.1 Coulomb-Counting Interface

The bq40z80 uses an integrating delta-sigma ADC for current measurements. Add a 100-Ω resistor from the sense resistor to the SRP and SRN inputs of the device. Place a 100-pF (C29) filter capacitor across the SRP and SRN inputs. Optional 0.1-µF filter capacitors (C26 and C27) can be added for additional noise filtering, if required for your circuit.

9.2.2.3.2 Power Supply Decoupling and PBI

The bq40z80 has an internal LDO that is internally compensated and does not require an external decoupling capacitor.

The PBI pin is used as a power supply backup input pin providing power during brief transient power outages. A standard 2.2-µF ceramic capacitor is connected from the PBI pin to ground.

9.2.2.3.3 System Present

The System Present signal is used to inform the gas gauge whether the pack is installed into or removed from the system. In the host system, this pin is grounded. The $\overline{\text{PRES}}$ pin of the bq40z80 is used if J5[1, 2] jumper is installed, and is occasionally sampled to test for system present. To save power, an internal pullup is provided by the gas gauge during a brief 4-µs sampling pulse once per second. A resistor can be used to pull the signal low and the resistance must be 20 kΩ or lower to ensure that the test pulse is lower than the VIL limit. The pullup current source is typically 10 µA to 20 µA.

Because the System Present signal is part of the pack connector interface to the outside world, it must be protected from external electrostatic discharge events. An integrated ESD protection on the $\overline{\text{PRES}}$ device pin reduces the external protection requirement to just R12 for an 8-kV ESD contact rating. However, if it is possible that the System Present signal may short to PACK+, then an E2 spark gap must be included for high-voltage protection.

9.2.2.3.4 SMBus Communication

The SMBus clock and data pins have integrated high-voltage ESD protection circuits; however, adding a ESD protection device, TPD1E10B06D (U5 and U6) and series resistor (R50 and R51), provides more robust ESD performance.

The SMBus clock and data lines have an internal pulldown. When the gas gauge senses that both lines are low (such as during removal of the pack), the device performs auto-offset calibration and then goes into SLEEP mode to conserve power.

9.2.2.3.5 FUSE Circuitry

The FUSE pin of the bq40z80 is designed to ignite the chemical fuse if one of the various safety criteria is violated. The FUSE pin also monitors the state of the secondary-voltage protection IC. Q9 ignites the chemical fuse when its gate is high. The output of the bq7718xx is divided by R22 and R30, which provides adequate gate drive for Q9 while guarding against excessive back current into the bq7718xx if the FUSE signal is high.

Using C8 is generally a good practice, especially for RFI immunity. C8 may be removed, if desired, because the chemical fuse is a comparatively slow device and is not affected by any sub-microsecond glitches that come from the FUSE output during the cell connection process.

If the AFEFUSE output is not used, it should be connected to VSS.

When the bq40z80 is commanded to ignite the chemical fuse, the FUSE pin activates to give a typical 8-V output.

9.2.2.4 Secondary-Current Protection

The bq40z80 provides secondary overcurrent and short-circuit protection, cell balancing, cell voltage multiplexing, and voltage translation. The following discussion examines cell and battery inputs, pack and FET control, temperature output, and cell balancing.

9.2.2.4.1 Cell and Battery Inputs

Each cell input is conditioned with a simple RC filter, which provides ESD protection during cell connect and acts to filter unwanted voltage transients. The resistor value allows some trade-off for cell balancing versus safety protection.

The bq40z80 has integrated cell balancing FETs for cells 1 through 6, and external cell balancing for cell 7. The internal cell balancing FETs allow the AFE to bypass cell current around a given cell or numerous cells. External series resistors placed between the cell connections and the VCx I/O pins set the balancing current magnitude. The internal FETs provide a 200-Ω resistance (2 V < VDS < 4 V). Series input resistors between 100 Ω and 1 kΩ are recommended for effective cell balancing. To use the external cell balancing for the 7th cell, configure Pin 16 as CB7EN.

The BAT input uses a diode (D6) to isolate and decouple it from the cells in the event of a transient dip in voltage caused by a short-circuit event.

9.2.2.4.2 External Cell Balancing

Internal cell balancing for cells 1 through 6 can only support up to 10 mA. External cell balancing provides another option for faster cell balancing. For details, refer to the application note, *Fast Cell Balancing Using External MOSFET* (SLUA420).

9.2.2.4.3 PACK and FET Control

The PACK and V_{CC} inputs provide power to the bq40z80 from the charger. The PACK input also provides a method to measure and detect the presence of a charger. The PACK input uses a 100-Ω resistor; whereas, the V_{CC} input uses a diode to guard against input transients and prevents misoperation of the date driver during short-circuit events.

The N-CH charge and discharge FETs are controlled with 10-kΩ series gate resistors, which provide a switching time constant of a few microseconds. The 10-MΩ resistors ensure that the FETs are off in the event of an open connection to the FET drivers. Q4 is provided to protect the discharge FET (Q3) in the event of a reverse-connected charger. Without Q4, Q3 can be driven into its linear region and suffer severe damage if the PACK+ input becomes slightly negative. Q4 turns on in that case to protect Q3 by shorting its gate to source. To use the simple ground gate circuit, the FET must have a low gate turn-on threshold. If it is desired to use a more standard device, such as the 2N7002, as the reference schematic, the gate should be biased up to 3.3 V with a high-value resistor. The bq40z80 device has the capability to provide a current-limited charging path typically used for low battery voltage or low temperature charging. The bq40z80 device uses an external P-CH, precharge FET controlled by PCHG.

9.2.2.4.4 Pre-Discharge Control

Some applications have a large capacitive load that requires a pre-discharge feature that can slowly charge the cap and avoid a large current that may trip the OC protection. The bq40z80 device can be configured to use the PDSG output of Pins 16, 17, or 20 to drive the N-CH FET Q7 to turn on the pre-discharge P-CH FET Q5. The precharge rate can be set by adjusting the resistor R9.

9.2.2.4.5 Temperature Output

For the bq40z80 device, up to four thermistor inputs can be configured. TS1, TS2, TS3, and TS4 provide thermistor drive-under program control. Each pin can be enabled with an integrated 18-kΩ (typical) linearization pullup resistor to support the use of a 10-kΩ at 25°C (103) NTC external thermistor, such as a Mitsubishi BN35-3H103. The reference design includes four 10-kΩ thermistors: RT1, RT2, RT3, and RT4.

9.2.2.4.6 LEDs

Multifunction Pins 20, 21, and 22 can be configured as three LED control outputs that provide constant current sinks for driving external LEDs. These outputs are configured to provide voltage and control for up to six LEDs. No external bias voltage is required. Unused LEDCNTL pins can remain open or they can be connected to V_{SS}. The $\overline{DISP}$ pin should be connected to V_{SS} if the LED feature is not used.

9.2.3 Application Curve

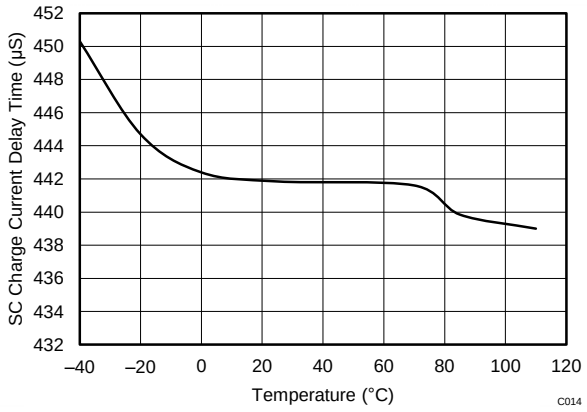


Figure 23. Short Circuit Charge Current Delay Time vs. Temperature

10 Power Supply Recommendations

The device manages its supply voltage dynamically according to the operation conditions. Normally, the BAT input is the primary power source to the device. The BAT pin should be connected to the positive termination of the battery stack. The input voltage for the BAT pin ranges from 2.2 V to 32 V.

The VCC pin is the secondary power input, which activates when the BAT voltage falls below minimum V_{CC}. This enables the device to source power from a charger (if present) connected to the PACK pin. The VCC pin should be connected to the common drain of the CHG and DSG FETs. The charger input should be connected to the PACK pin.

11 Layout

11.1 Layout Guidelines

A battery fuel gauge circuit board is a challenging environment due to the fundamental incompatibility of high-current traces and ultra-low current semiconductor devices. The best way to protect against unwanted trace-to-trace coupling is with a component placement, such as that shown in Figure 24, where the high-current section is on the opposite side of the board from the electronic devices. This may not possible in many situations due to mechanical constraints. Still, every attempt should be made to route high-current traces away from signal traces, which enter the bq40z80 directly. IC references and registers can be disturbed and in rare cases damaged due to magnetic and capacitive coupling from the high-current path.

NOTE

During surge current and ESD events, the high-current traces appear inductive and can couple unwanted noise into sensitive nodes of the gas gauge electronics, as illustrated in Figure 25.

Layout Guidelines (continued)

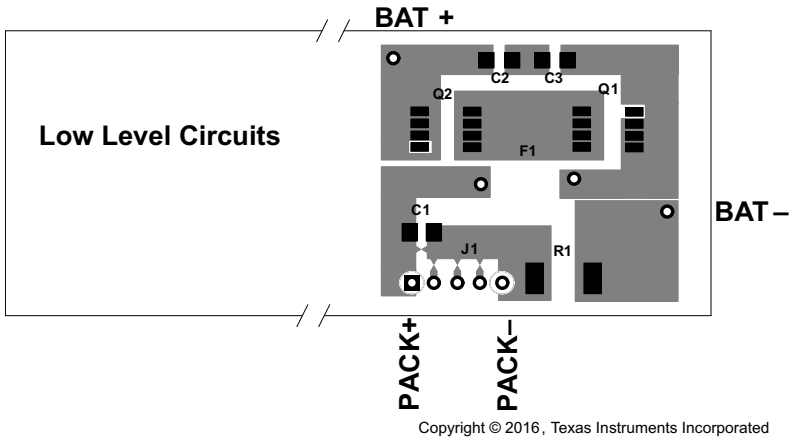


Figure 24. Separating High- and Low-Current Sections Provides an Advantage in Noise Immunity

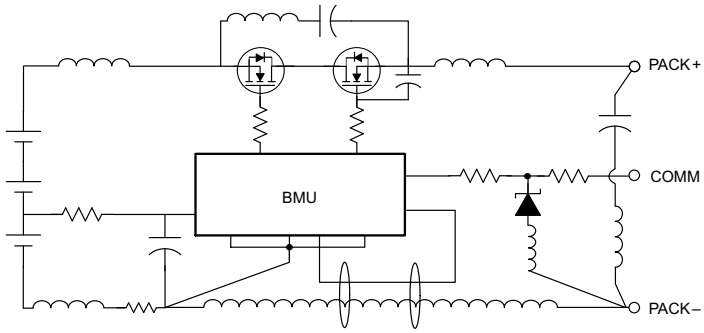


Figure 25. Avoid Close Spacing Between High-Current and Low-Level Signal Lines

Kelvin voltage sensing is extremely important in order to accurately measure current and top and bottom cell voltages. Place all filter components as close as possible to the device. Route the traces from the sense resistor in parallel to the filter circuit. Adding a ground plane around the filter network can add additional noise immunity. Figure 26 and Figure 27 demonstrate correct kelvin current sensing.

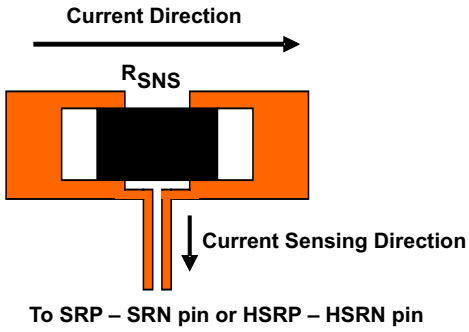


Figure 26. Sensing Resistor PCB Layout

Layout Guidelines (continued)

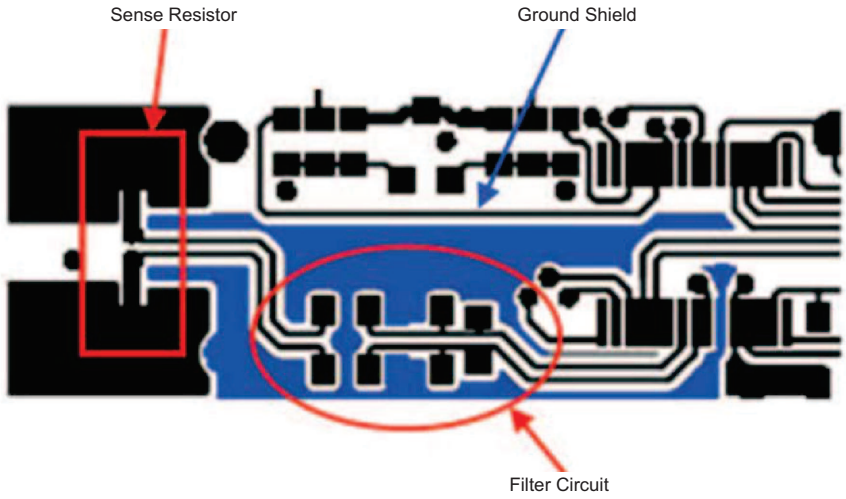


Figure 27. Sense Resistor, Ground Shield, and Filter Circuit Layout

11.1.1 Protector FET Bypass and Pack Terminal Bypass Capacitors

Use wide copper traces to lower the inductance of the bypass capacitor circuit. In Figure 28, an example layout demonstrates this technique. Note that in the *bq40z80EVM-Rev A Schematic*, these capacitors are C1, C2, C3, and C4.

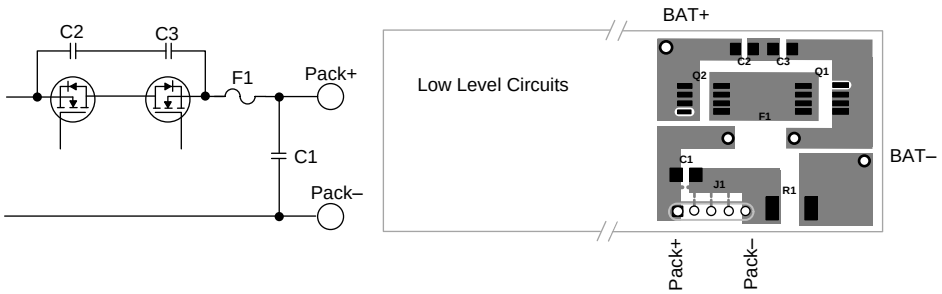


Figure 28. Wide Copper Traces Lower the Inductance of Bypass Capacitors C1, C2, and C3

11.1.2 ESD Spark Gap

Protect the SMBus clock, data, and other communication lines from ESD with a spark gap at the connector. The pattern in Figure 29 is recommended, with 0.2-mm spacing between the points.

Figure 29. Recommended Spark-Gap Pattern Helps Protect Communication Lines from ESD

11.2 Layout Examples

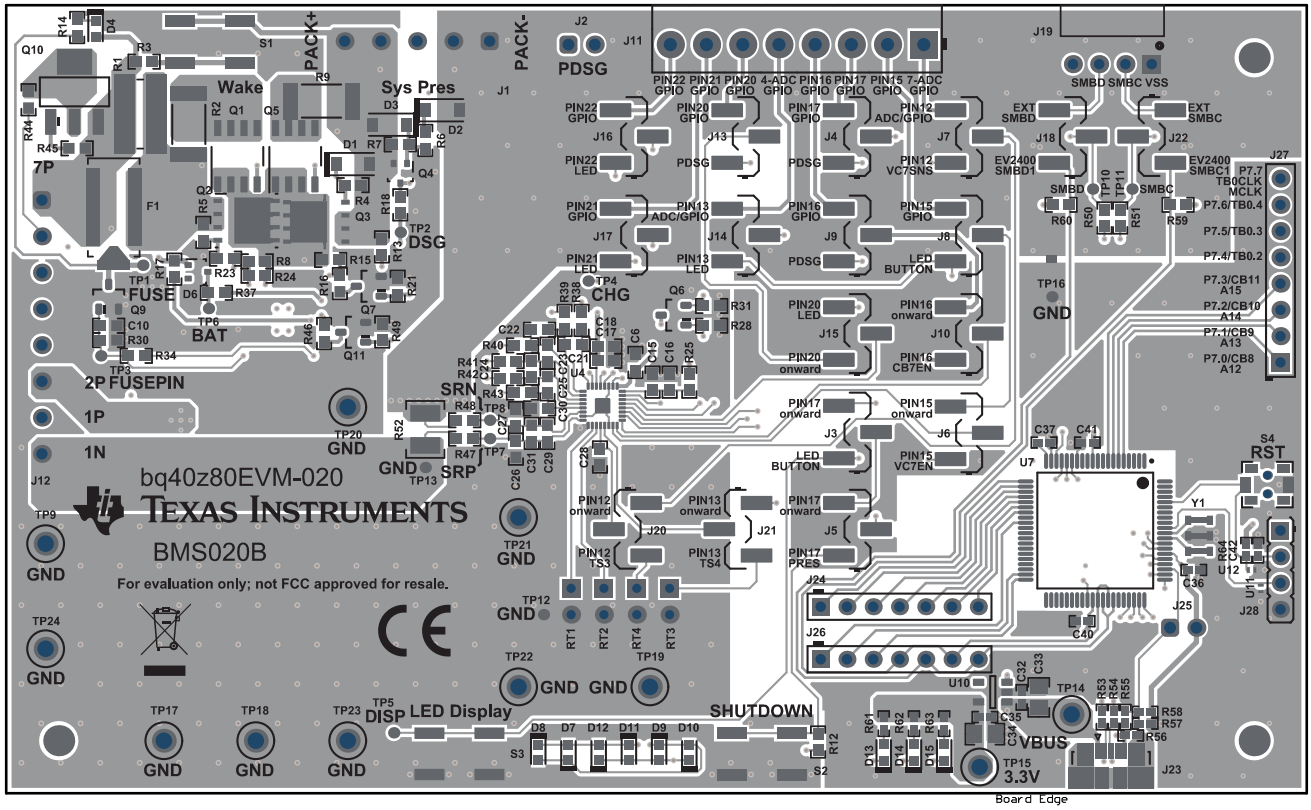


Figure 30. bq40z80EVM RevB Top Composite

Layout Examples (continued)

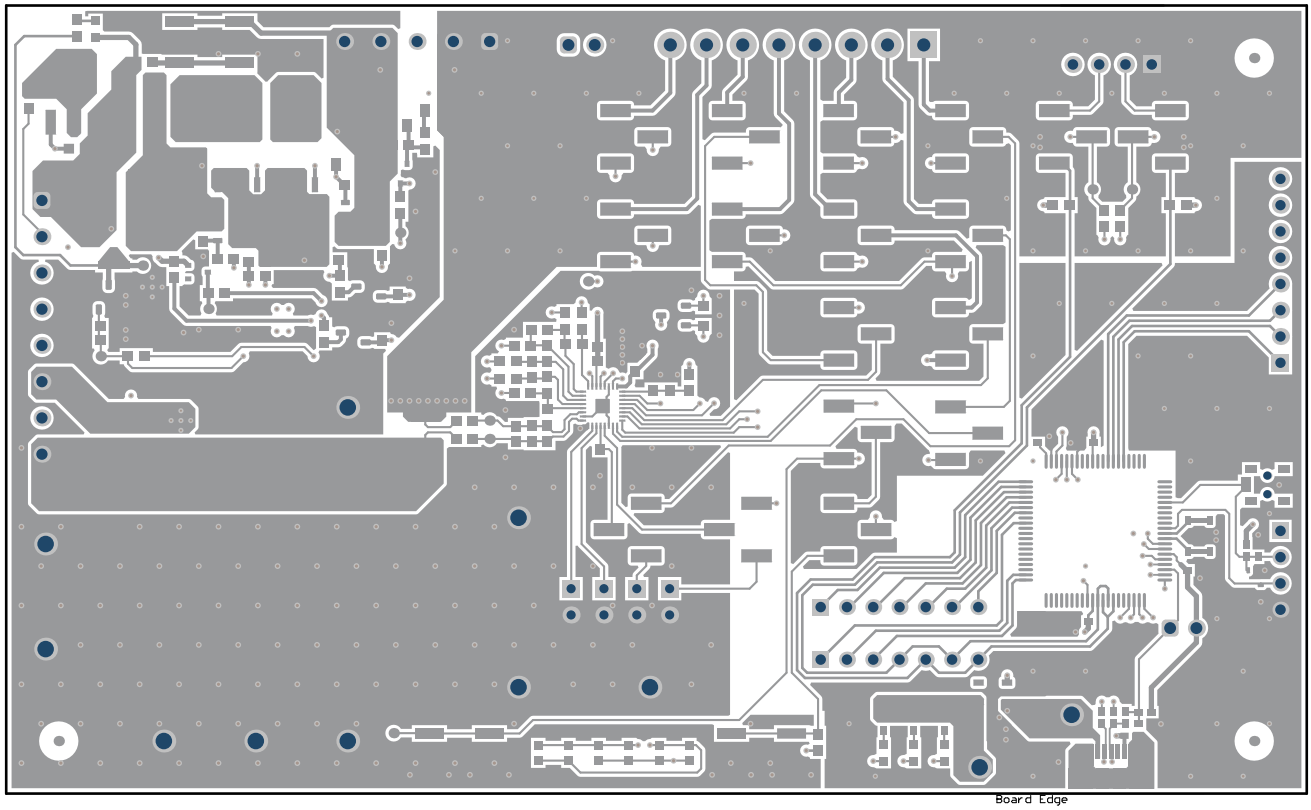


Figure 31. bq40z80EVM RevB Top Layer

Layout Examples (continued)

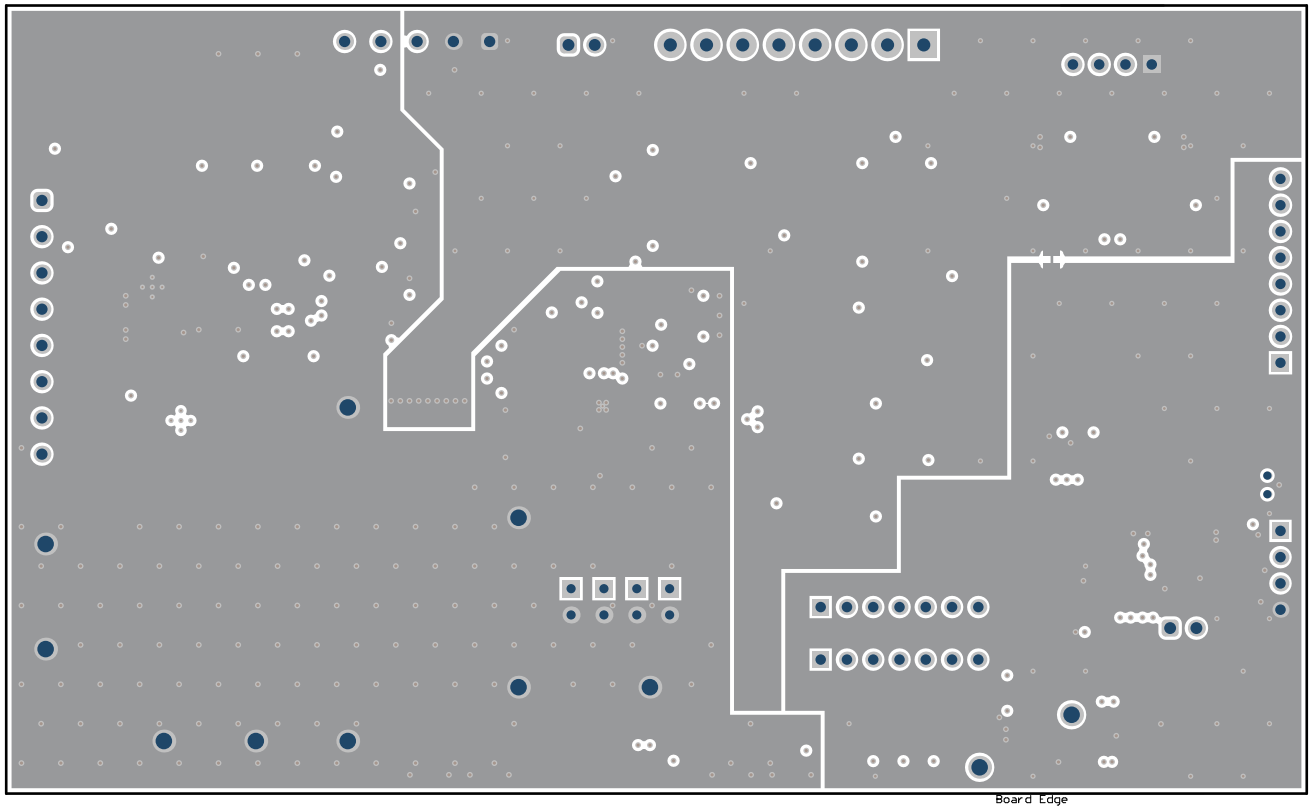


Figure 32. bq40z80EVM RevB GND Layer

Layout Examples (continued)

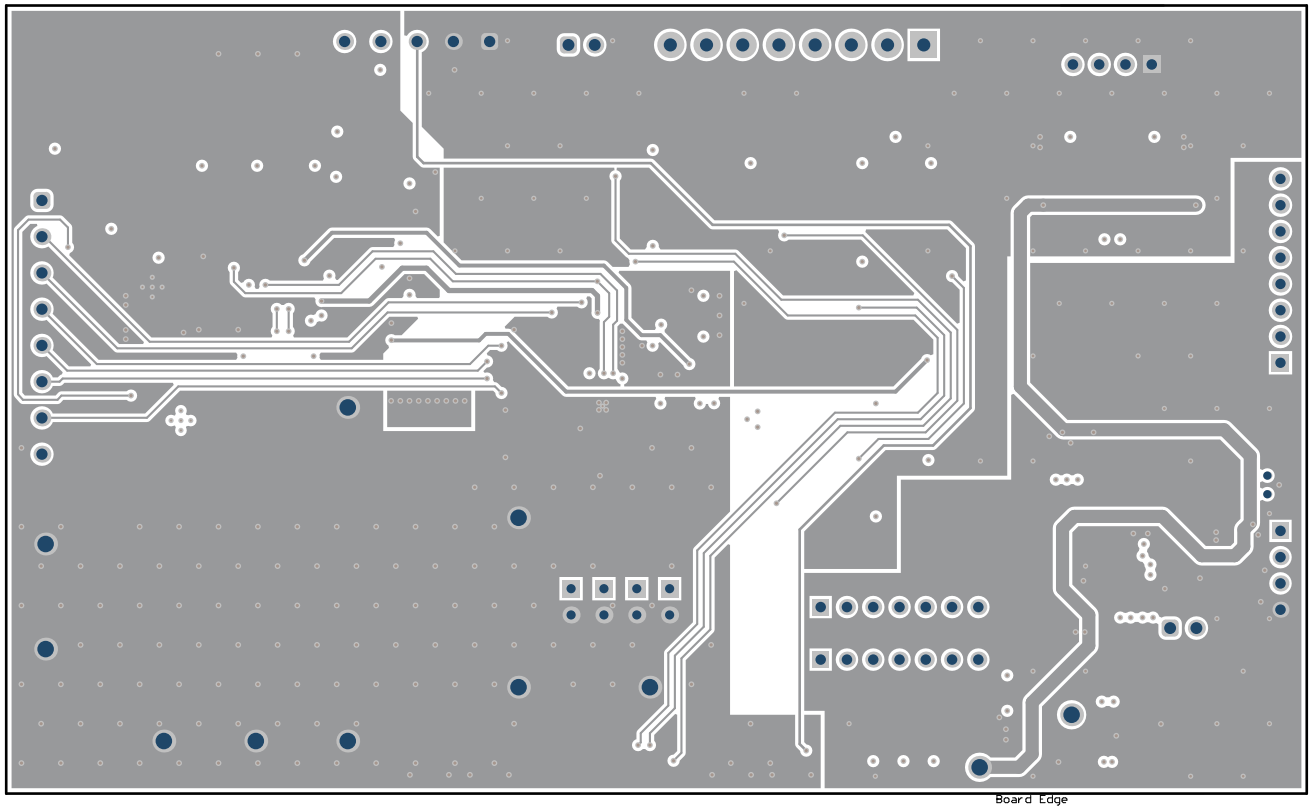


Figure 33. bq40z80EVM RevB Signal Layer

Layout Examples (continued)

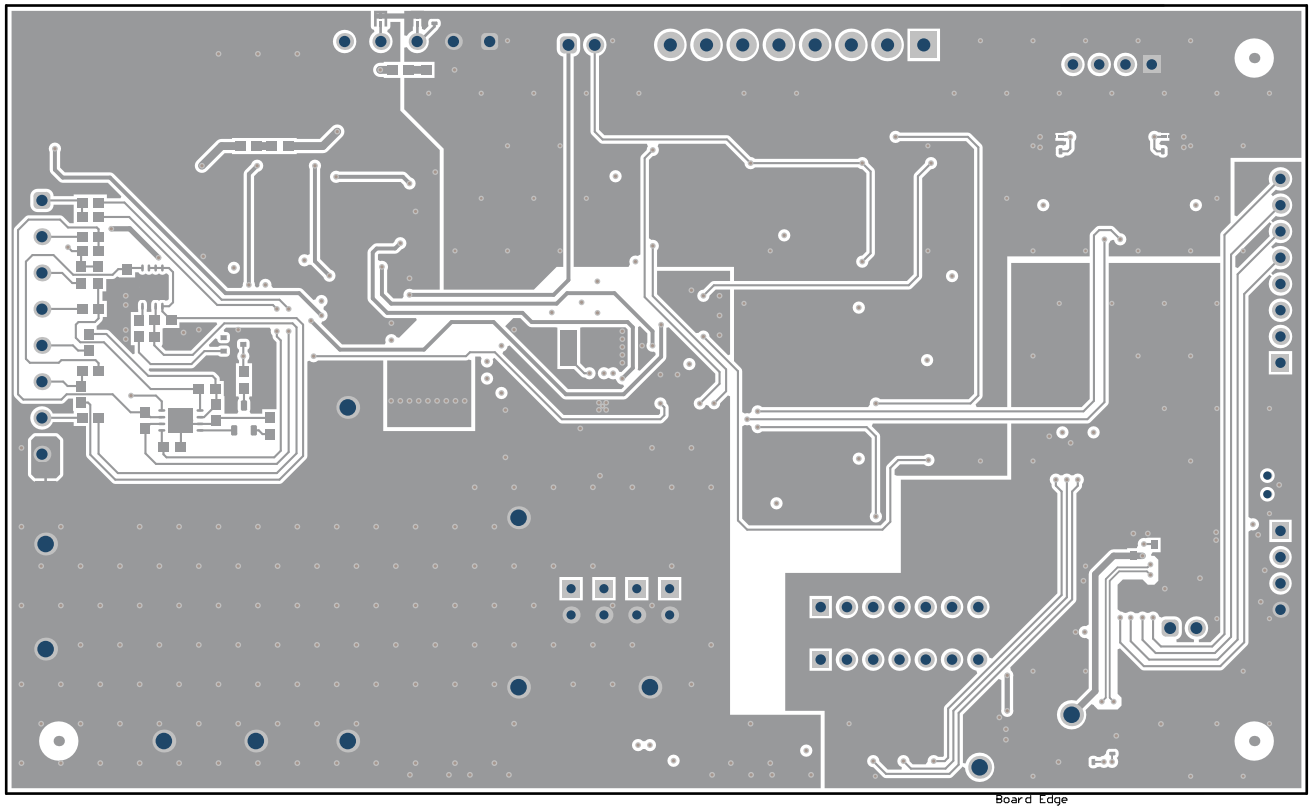


Figure 34. bq40z80EVM RevB Bottom Layer

Layout Examples (continued)

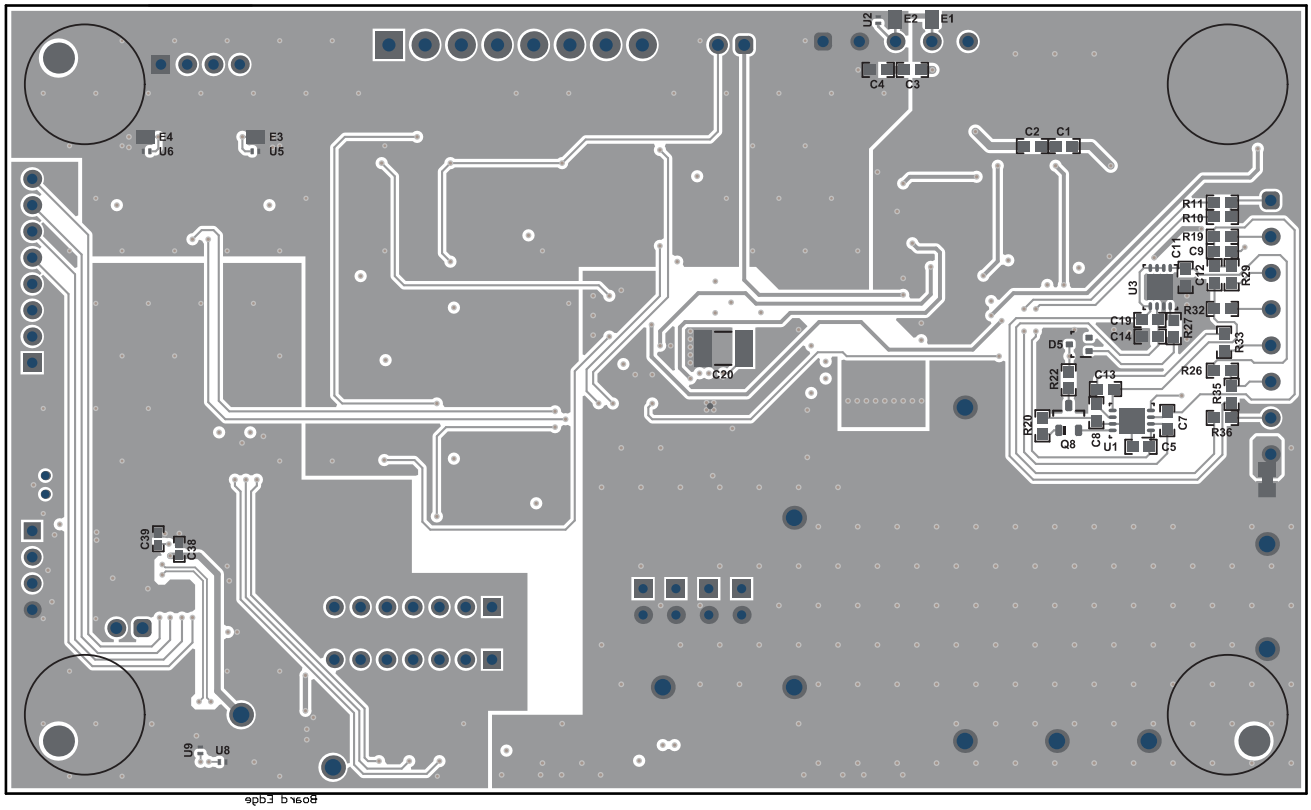


Figure 35. bq40z80EVM RevB Bottom Layer Composite

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation, see the following:

- *bq40z80 Technical Reference Manual* (SLUUBT5)
- *bq40z80 Manufacture, Production, and Calibration Application Note* (SLUA868)
- *bq40z80EVM Li-Ion Battery Pack Manager Evaluation Module User's Guide* (SLUUBZ5)
- *How to Complete a Successful Learning Cycle for the bq40z80 Application Note* (SLUA848)
- *TI Fuel Gauge Authentication Key Packager and Programmer Tools User's Guide* (SLUUBU3)

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, package, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ40Z80RSMR	ACTIVE	VQFN	RSM	32	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ40Z80	Samples
BQ40Z80RSMT	ACTIVE	VQFN	RSM	32	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ40Z80	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

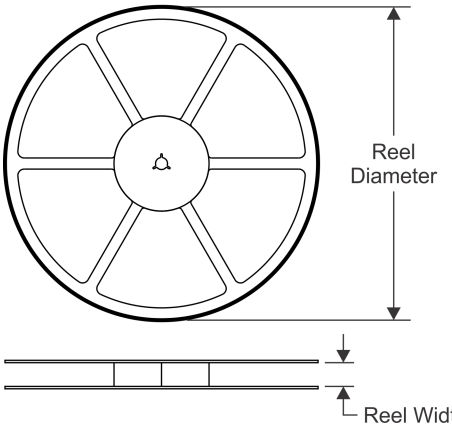
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

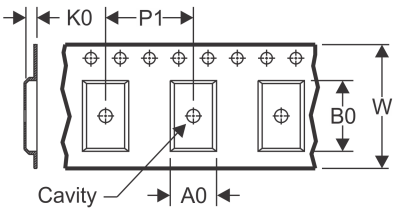
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

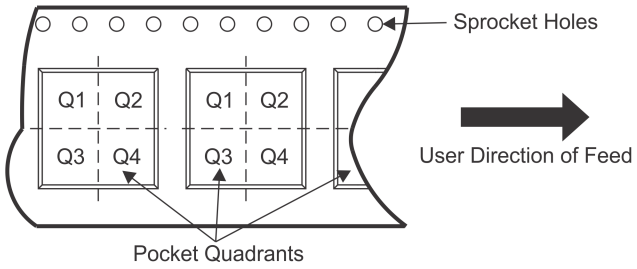


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

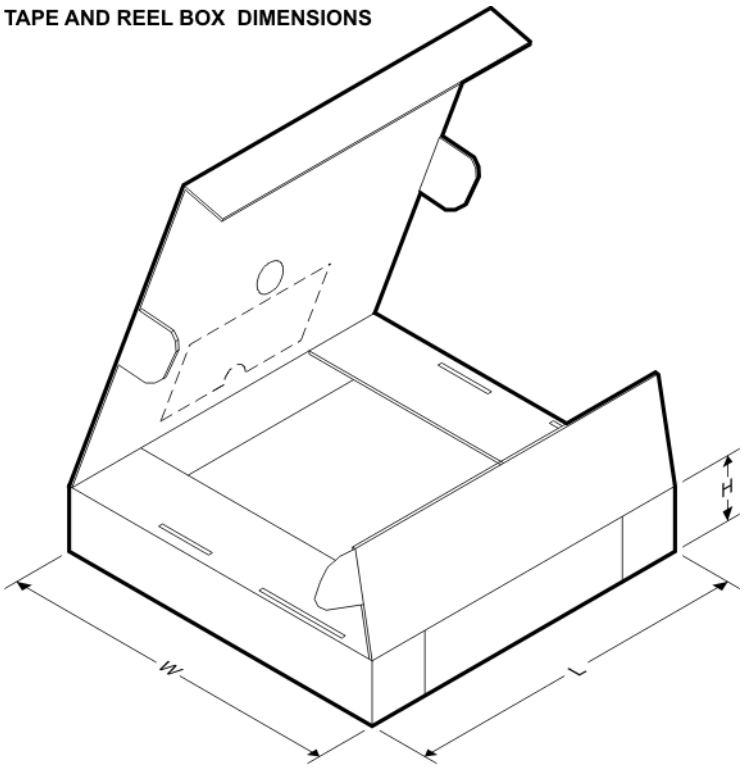
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ40Z80RSMR	VQFN	RSM	32	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
BQ40Z80RSMT	VQFN	RSM	32	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ40Z80RSMR	VQFN	RSM	32	3000	367.0	367.0	35.0
BQ40Z80RSMT	VQFN	RSM	32	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

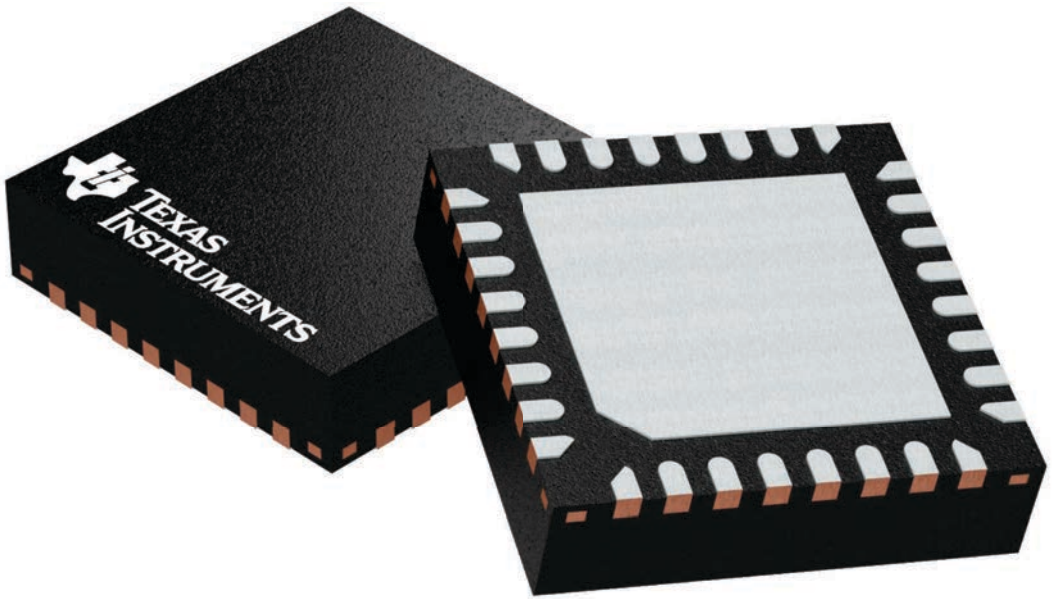
RSM 32

VQFN - 1 mm max height

4 x 4, 0.4 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



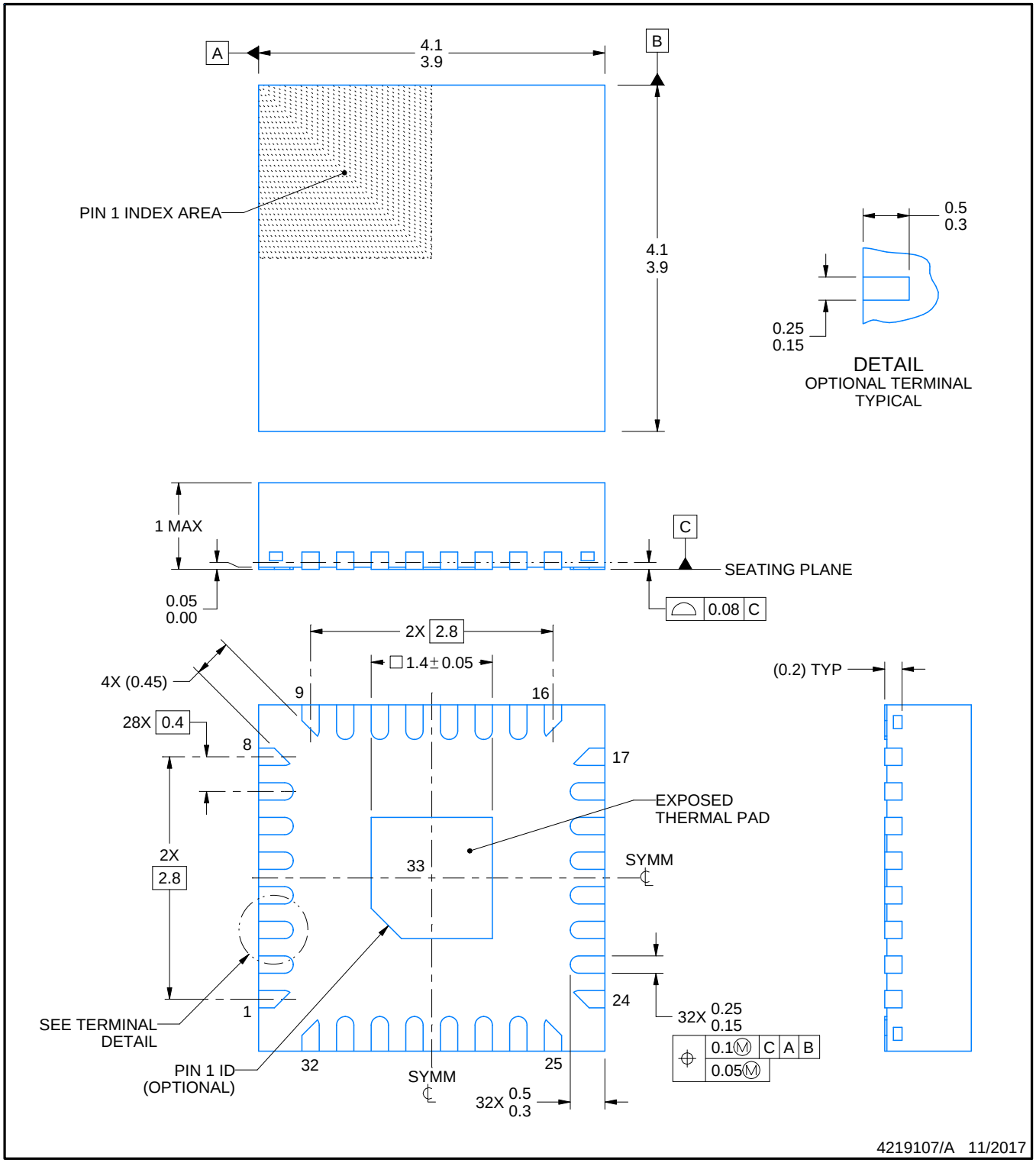
4224982/A

PACKAGE OUTLINE

RSM0032A

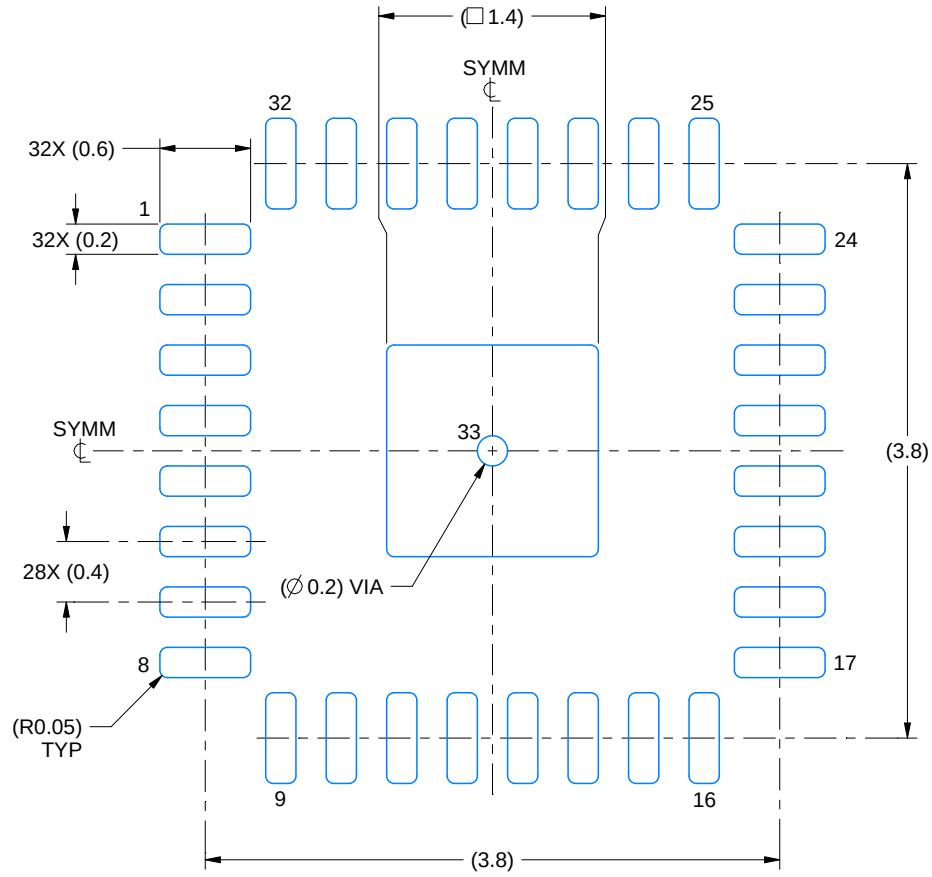
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

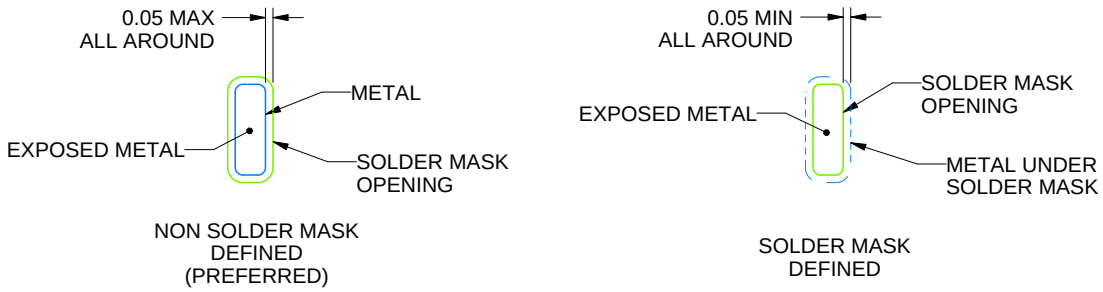


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

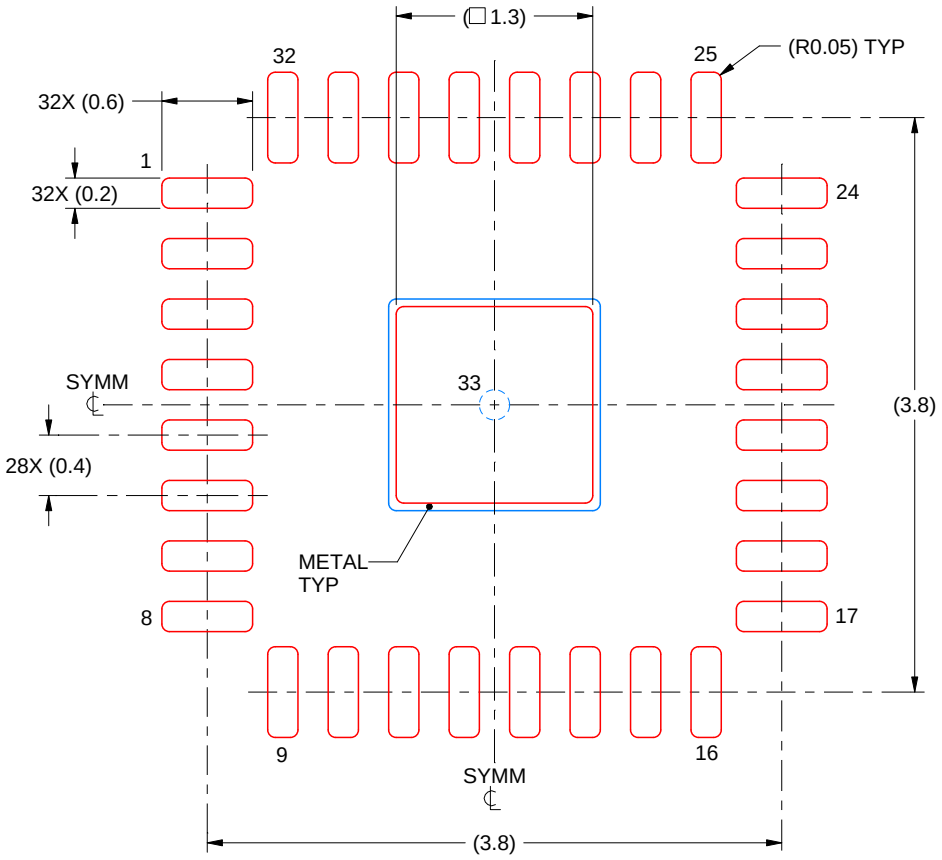


SOLDER MASK DETAILS

4219107/A 11/2017

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 33:
86% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4219107/A 11/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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