# STL75NH3LL

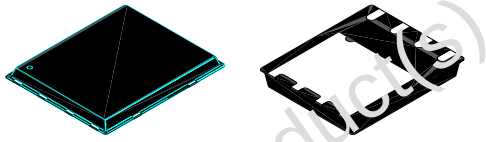
## N-channel 30 V, 0.004 Ω, 20 A, PowerFLAT™ (6x5) ultra low gate charge STripFET™ Power MOSFET

## Features

| Type | $V_{DSS}$ | $R_{DS(on)}$ max | $I_D$ |
|---|---|---|---|
| STL75NH3LL | 30V | < 0.0057 Ω | 20 A (1) |

1. This value is according $R_{thj\text{-}pcb}$

- Improved die-to-footprint ratio
- Very low profile package (1mm max)
- Very low thermal resistance
- Very low gate charge
- Low threshold device



PowerFLAT™(6x5)

## Application

- Switching applications

## Description

This application specific Power MOSFET is the latest generation of STMicroelectronics unique "STripFET™" technology. The resulting transistor is optimized for low on-resistance and minimal gate charge. The chip-scaled PowerFLAT™ package allows a significant board space saving, still boosting the performance.

**Figure 1. Internal schematic diagram**

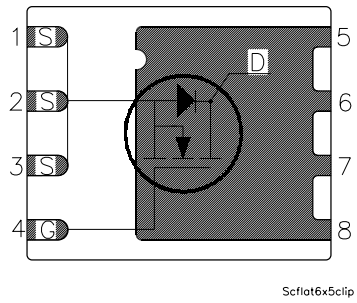



**Table 1. Device summary**

| Order code | Marking | Package | Packaging |
|---|---|---|---|
| STL75NH3LL | L75NH3LL | PowerFLAT™ (6 x 5) | Tape and reel |

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# Contents

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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DS}$ | Drain-source voltage ($V_{GS}$ = 0) | 30 | V |
| $V_{GS}$ | Gate-source voltage | ± 16 | V |
| $I_D$ (1) | Drain current (continuous) at $T_C$ = 25 °C | 75 | A |
| $I_D$ (1) | Drain current (continuous) at $T_C$ = 100 °C | 47 | A |
| $I_D$(2) | Drain current (continuous) at $T_C$ = 25 °C | 20 | A |
| $I_D$ (2) | Drain current (continuous) at $T_C$ = 100 °C | 12.5 | A |
| $I_{DM}$ (3) | Drain current (pulsed) | 80 | A |
| $P_{TOT}$(1) | Total dissipation at $T_C$ = 25 °C | 60 | W |
| $P_{TOT}$(2) | Total dissipation at $T_C$ = 25 °C | 4 | W |
| | Derating factor | 0.03 | W/°C |
| $T_j$<br>$T_{stg}$ | Operating junction temperature<br>Storage temperature | -55 to 150 | °C |

1. The value is rated according $R_{thj\text{-}C}$
2. This value is according $R_{thj\text{-}pcb}$
3. Pulse width limited by safe operating area

**Table 3. Thermal resistance**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $R_{thj\text{-}case}$ | Thermal resistance junction-case (drain) max | 2.08 | °C/W |
| $R_{thj\text{-}pcb}$ (1) | Thermal resistance junction-pcb max | 31.3 | °C/W |

1. When mounted on FR-4 board of 1inch$^2$, 2 oz Cu, t < 10 sec

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# 2 Electrical characteristics

($T_{CASE}$=25°C unless otherwise specified)

**Table 4. On/off states**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage | $I_D$ = 250 µA, $V_{GS}$= 0 | 30 | | | V |
| $I_{DSS}$ | Zero gate voltage drain current ($V_{GS}$ = 0) | $V_{DS}$ = Max rating,<br>$V_{DS}$ = Max rating, @125 °C | | | 1<br>10 | µA<br>µA |
| $I_{GSS}$ | Gate body leakage current ($V_{DS}$ = 0) | $V_{DS}$ = ± 16 V | | | ± 100 | nA |
| $V_{GS(th)}$ | Gate threshold voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = 250 µA | 1 | | | V |
| $R_{DS(on)}$ | Static drain-source on resistance | $V_{GS}$= 10 V, $I_D$= 10 A<br>$V_{GS}$= 4.5 V, $I_D$= 10 A | | 0.004<br>0.005 | 0.0057<br>0.0075 | Ω<br>Ω |

**Table 5. Dynamic**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $C_{iss}$<br>$C_{oss}$<br>$C_{rss}$ | Input capacitance<br>Output capacitance<br>Reverse transfer capacitance | $V_{DS}$ = 25 V, f = 1 MHz, $V_{GS}$=0 | | 1810<br>565<br>41 | | pF<br>pF<br>pF |
| $Q_g$<br>$Q_{gs}$<br>$Q_{gd}$ | Total gate charge<br>Gate-source charge<br>Gate-drain charge | $V_{DD}$ = 15 V, $I_D$ = 20 A,<br>$V_{GS}$ = 4.5 V<br>*(see Figure 14)* | | 18<br>4.8<br>5.3 | 24 | nC<br>nC<br>nC |
| $R_G$ | Gate input resistance | f=1 MHz Gate DC Bias = 0<br>Test signal level = 20 mV<br>open drain | 0.5 | 1.5 | 3 | Ω |

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**Table 6. Switching times**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $t_{d(on)}$<br>$t_r$ | Turn-on delay time<br>Rise time | $V_{DD}$ = 15 V, $I_D$ = 10 A<br>$R_G$= 4.7 Ω, $V_{GS}$= 10 V<br>*(see Figure 16)* | | 8<br>65 | | ns<br>ns |
| $t_{d(off)}$<br>$t_f$ | Turn-off delay time<br>Fall time | $V_{DD}$ = 15 V, $I_D$ = 10 A<br>$R_G$= 4.7 Ω, $V_{GS}$= 10 V<br>*(see Figure 16)* | | 30<br>20 | | ns<br>ns |

**Table 7. Source drain diode**

| Symbol | Parameter | Test conditions | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{SD}$<br>$I_{SDM}$ | Source-drain current<br>Source-drain current (pulsed) | | | | 20<br>80 | A<br>A |
| $V_{SD}$ (1) | Forward on voltage | $I_{SD}$ = 20 A, $V_{GS}$ = 0 | | | 1.3 | V |
| $t_{rr}$<br>$Q_{rr}$<br>$I_{RRM}$ | Reverse recovery time<br>Reverse recovery charge<br>Reverse recovery current | $I_{SD}$ = 20 A,<br>di/dt = 100 A/µs<br>$V_{DD}$ = 20 V<br>*(see Figure 15)* | | 22<br>32<br>1.9 | | ns<br>nC<br>A |

1. Pulsed: Pulse duration = 300µs, duty cycle 1.5%

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## 2.1 Electrical characteristics (curves)

**Figure 2. Safe operating area**

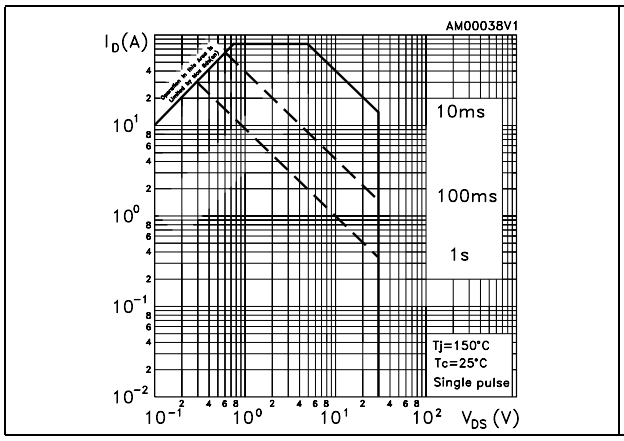



**Figure 3. Thermal impedance**

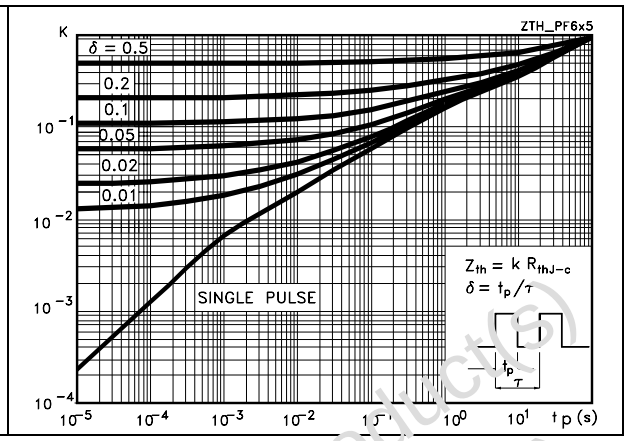



**Figure 4. Output characteristics**

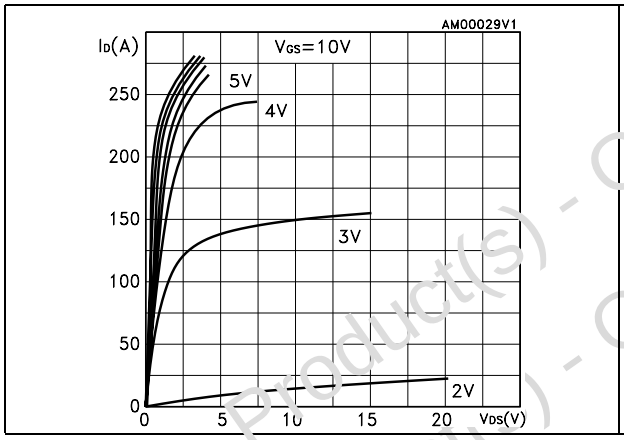



**Figure 5. Transfer characteristics**

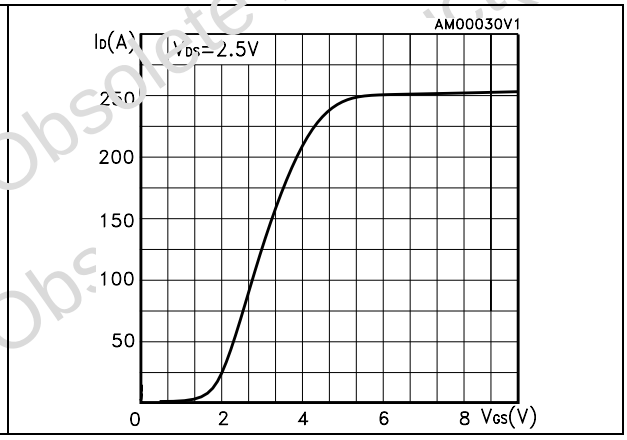



**Figure 6. Normalized $B_{VDSS}$ vs temperature**

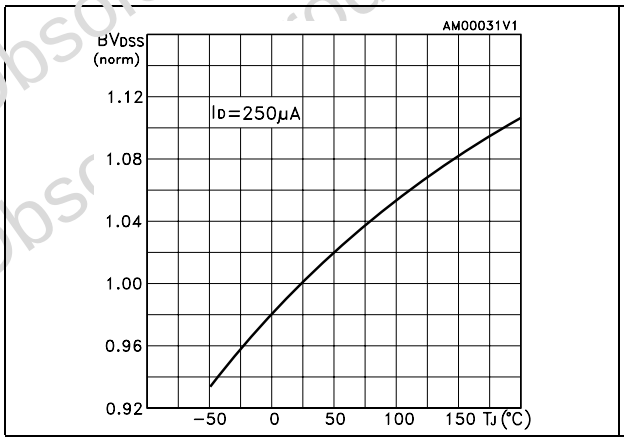
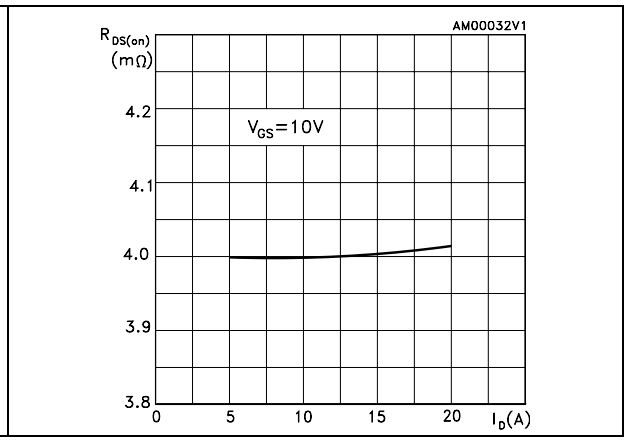



**Figure 7. Static drain-source on resistance**




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**Figure 8. Gate charge vs gate-source voltage**

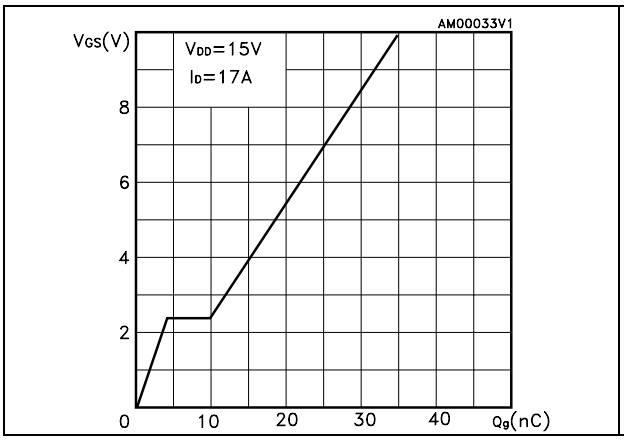



**Figure 9. Capacitance variations**

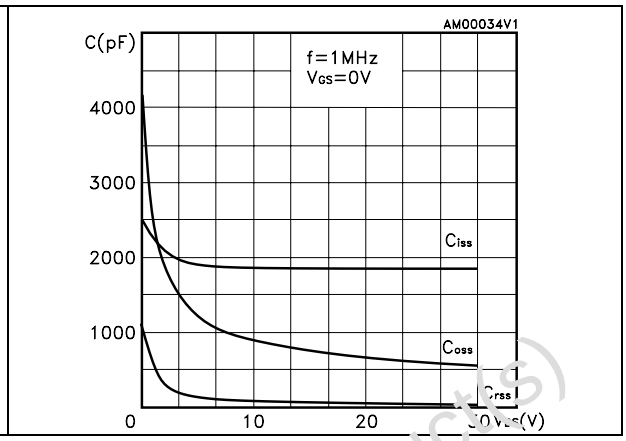



**Figure 10. Normalized gate threshold voltage vs temperature**

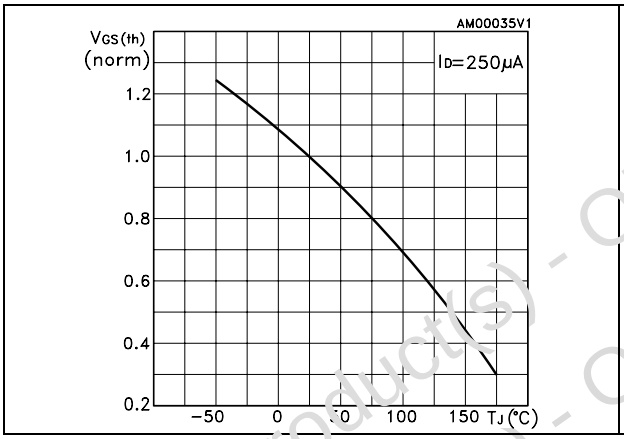



**Figure 11. Normalized on resistance vs temperature**

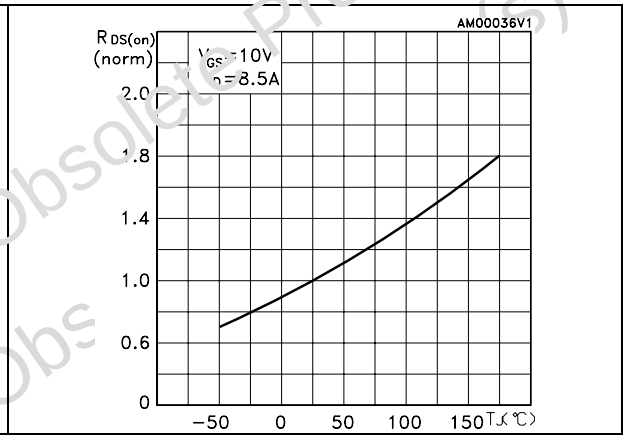
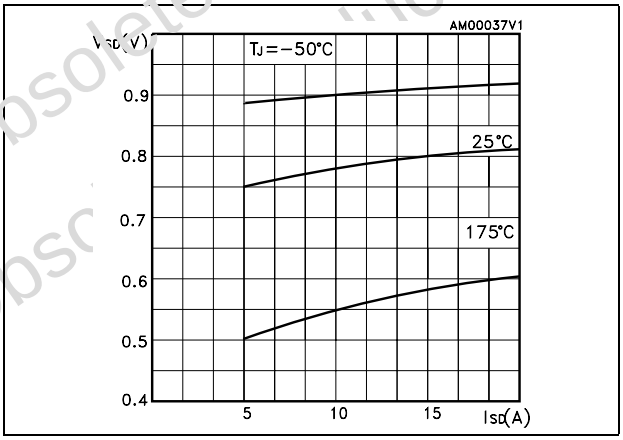



**Figure 12. Source-drain diode forward characteristics**




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# 3 Test circuits

**Figure 13. Switching times test circuit for resistive load**

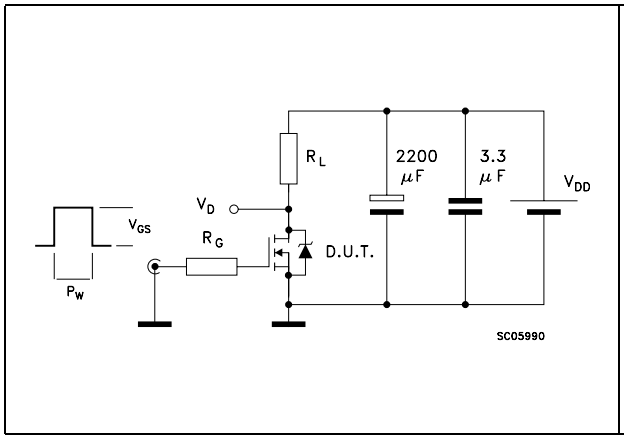



**Figure 14. Gate charge test circuit**

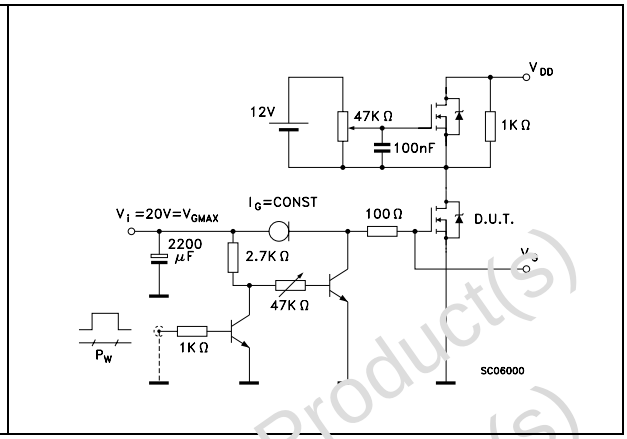



**Figure 15. Test circuit for inductive load switching and diode recovery times**

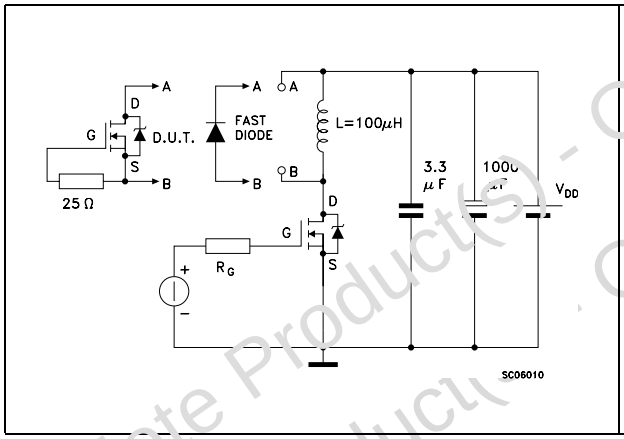



**Figure 16. Unclamped inductive load test circuit**

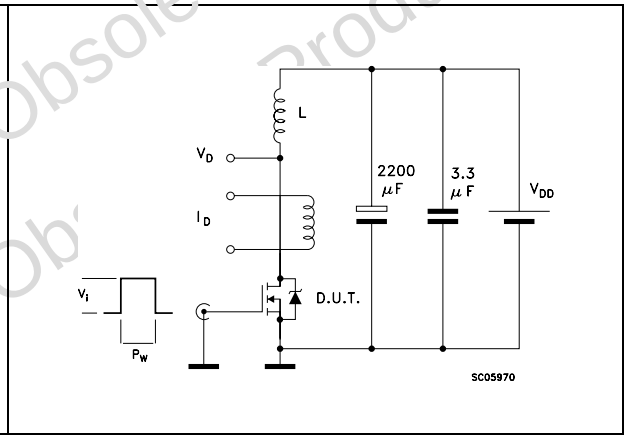



**Figure 17. Unclamped inductive waveform**

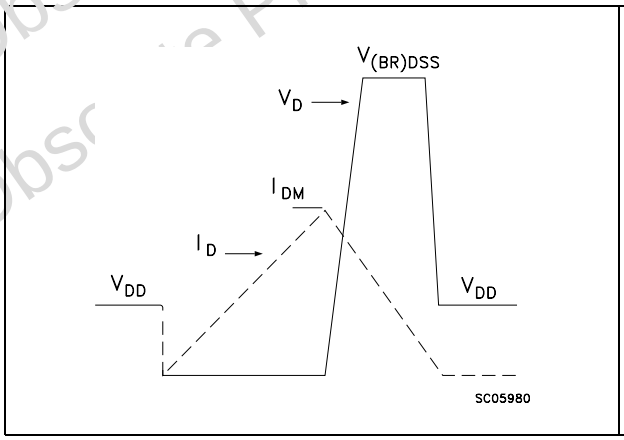
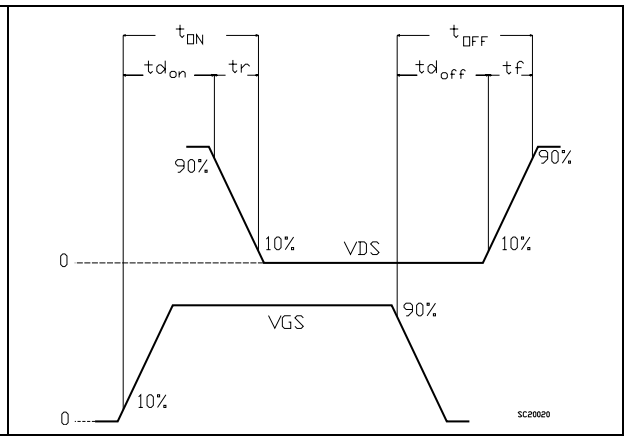



**Figure 18. Switching time waveform**




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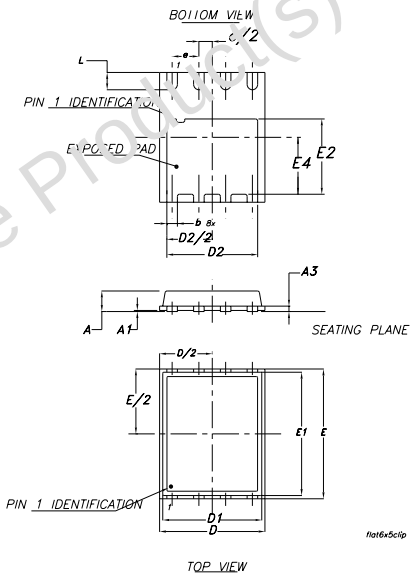
# 4 Package mechanical data

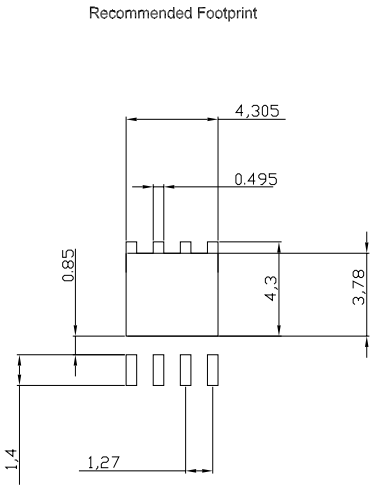
In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: *www.st.com*

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## PowerFLAT™ (6x5) MECHANICAL DATA

| DIM. | mm. | | | inch | | |
|---|---|---|---|---|---|---|
| | MIN. | TYP | MAX. | MIN. | TYP. | MAX. |
| A | 0.80 | 0.83 | 0.93 | 0.031 | 0.032 | 0.036 |
| A1 | | 0.02 | 0.05 | | 0.0007 | 0.0019 |
| A3 | | 0.20 | | | 0.007 | |
| b | 0.35 | 0.40 | 0.47 | 0.013 | 0.015 | 0.018 |
| D | | 5.00 | | | 0.196 | |
| D1 | | 4.75 | | | 0.187 | |
| D2 | 4.15 | 4.20 | 4.25 | 0.163 | 0.165 | 0.167 |
| E | | 6.00 | | | 0.236 | |
| E1 | | 5.75 | | | 0.226 | |
| E2 | 3.43 | 3.48 | 3.53 | 0.135 | 0.137 | 0.139 |
| E4 | 2.58 | 2.63 | 2.68 | | 0.103 | 0.105 |
| e | | 1.27 | | | 0.050 | |
| L | 0.70 | 0.80 | 0.90 | 0.027 | 0.031 | 0.035 |




Note: all dimentions are in mm.

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# 5 Revision history

Table 8. Document revision history

| Date | Revision | Changes |
|---|---|---|
| 12-Jun-2008 | 1 | First release |

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